CERN FDI (Fast Digital Integrator)

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Abstract

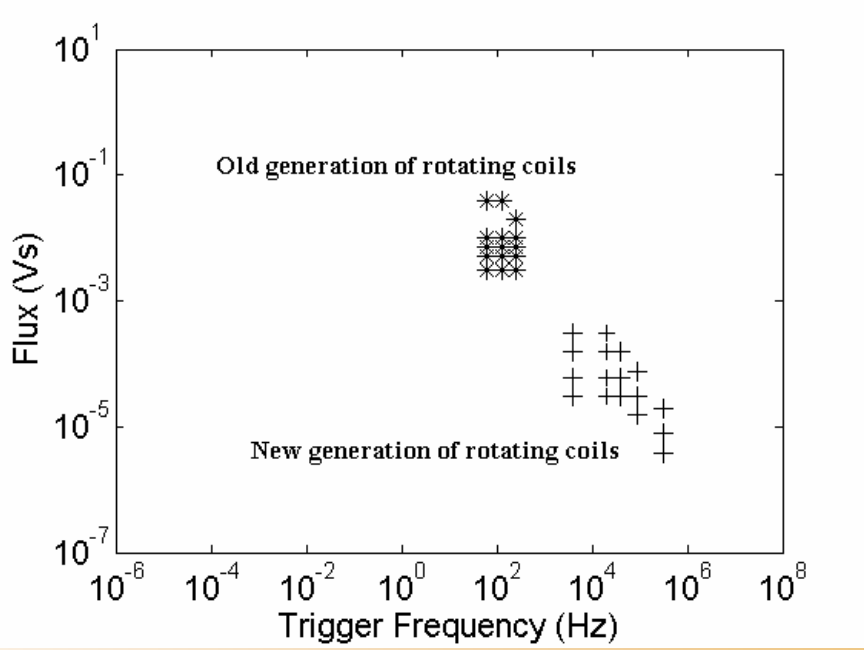
- New requirements
- Basic idea of FDI
- Numerical metrological analysis
- Implementation
- Experimental results
- Future work
- Conclusions

New Generation of Rotating Coils

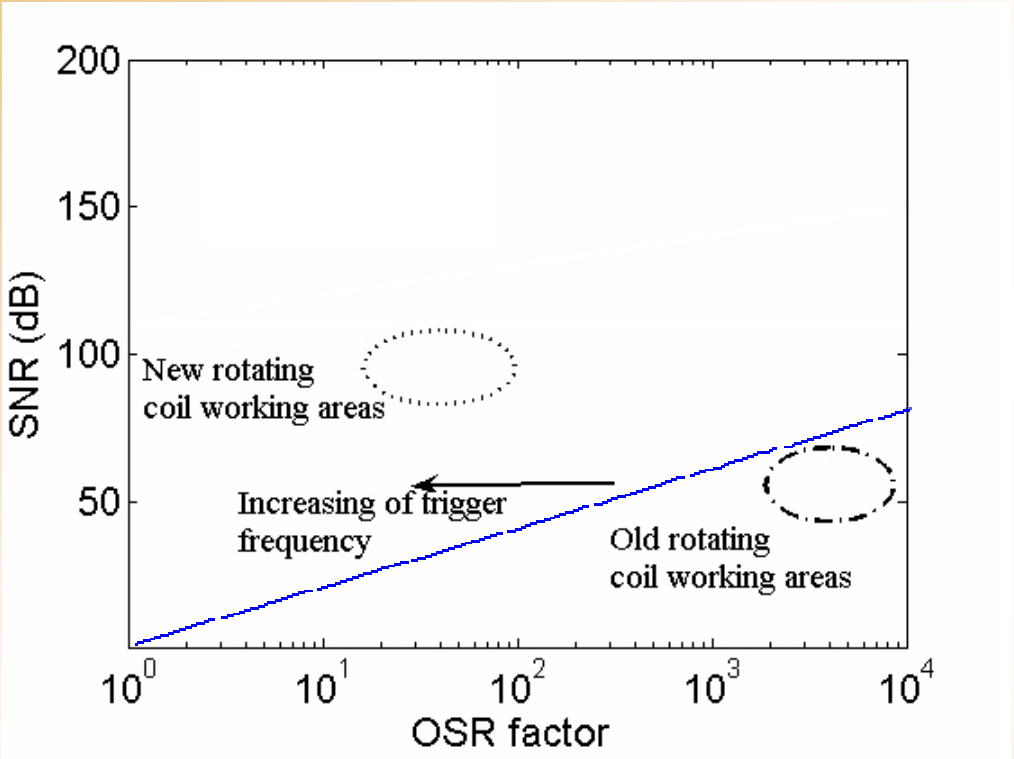
New specifications

- Increase in coil speed up to 8 Hz and more + continuous rotation
- Measurements on magnets in dynamic conditions with a ramp slope up to 1000 A/s
- Field harmonics measurements in real time in a fraction of second for on-line monitoring reference magnets

- **Flux bandwidth: up to 100 kHz**
- **Measurement time: 5 s (typical)**
- **Time resolution: 50 ns**
- **Gain linearity: 10 ppm**
- **Gain stability : 100 ppm (1 day), 10 ppm (1 hour)**
- **Uncertainty: 1 ppm at 10 kHz**



CERN State of the Art: PDI



• Designed and developed at CERN on a VFC basis (by P. Galbraith)

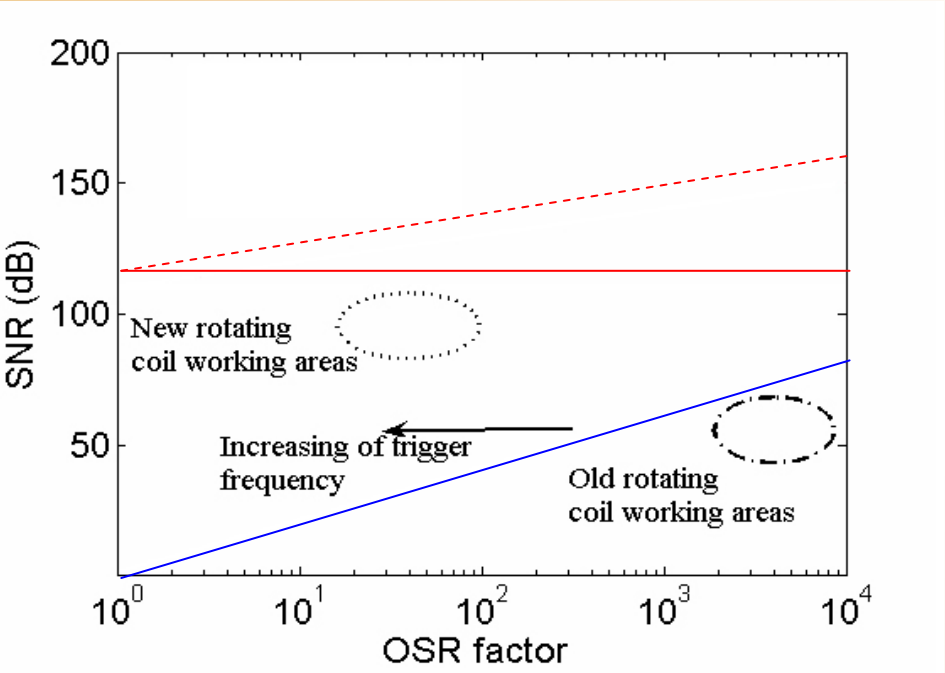
•Used for 20 years and put on the market by METRO*LAB* Instruments SA

•It goes in crisis with the new generation of rotating coils

•Its dynamic metrological performance is directly related to OSR, thus, an increase in the trigger frequency, giving rise to an OSR decrease, causes a performance loss

• OSR is the ratio between sampling rate and trigger frequency

Basic Idea and Key Design Concepts



- High oversampling + resolution digitalization
- On-line integration for enlarging bandwidth (up to 800 kHz)
- Possibility of use as dynamic signal analyzer, dynamic flux analyzer, and fluxmeter
- Differential measurement analog chain
- Dichotomic algorithm of self-calibration of offset and gain
- Real-time correction of deterministic errors

FDI: Measurement Technique

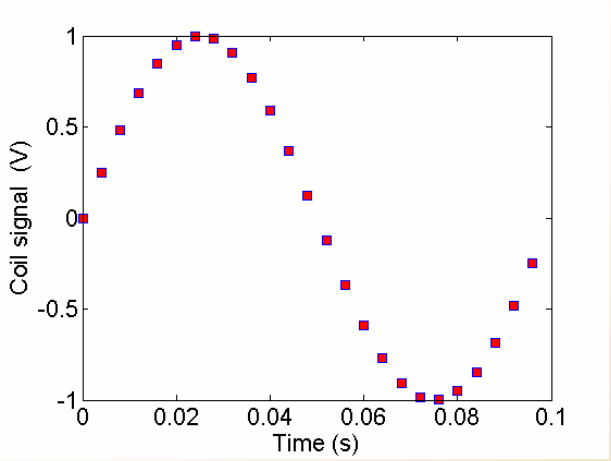
Encoder Pulses

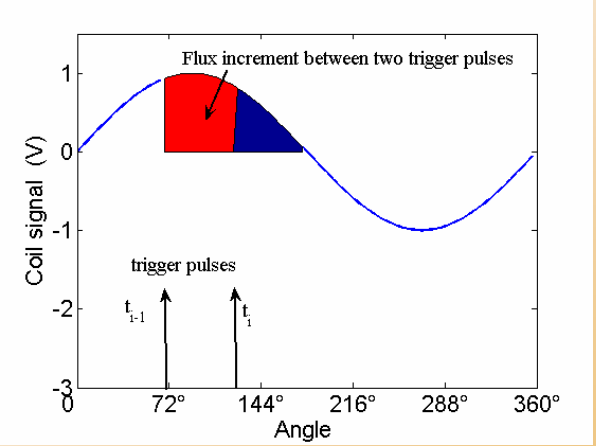
Rotating Coil

$$V = -\frac{\partial \varphi}{\partial t}$$

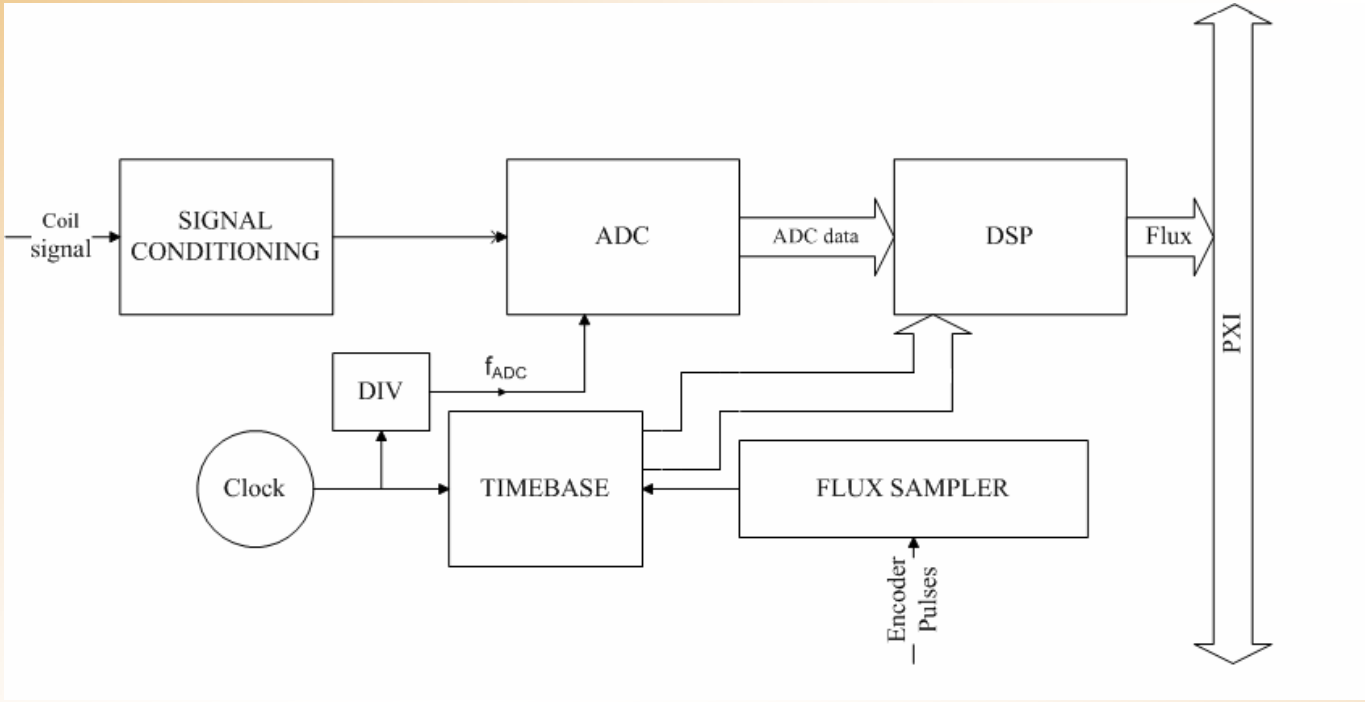
Conditioning and Digitizing (Time domain)

Digital Integration (Angular domain)



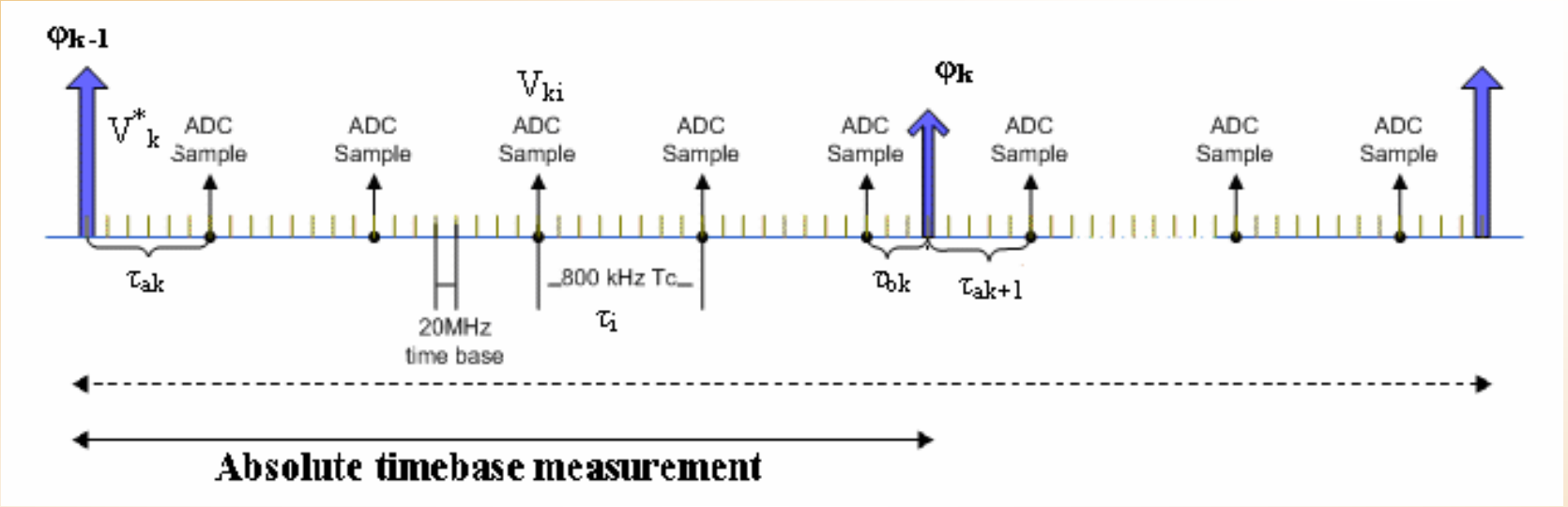


FDI: Architecture



- The input signal is conditioned by a programmable gain amplifier (PGA), with offset and gain self-calibration
- The conditioned signal is sampled and quantized by an ADC
- A DSP carries out the integration algorithm on-line
- Trigger events are provided by a flux sampler and measured by a time base
- Flux samples are sent to a host PC via PXI bus

FDI: Time Domain



Flux computation:

- $f_{timebase}$ 20 MHz
- f_w 1024 Hz
- V_{max} 5 V
- f_{ADC} 800 kS/s

$$\varphi_k = V_k^* \tau_{a_k} + \sum_{i=1}^{i=n-1} V_{k_i} \tau_i + V_{k_n} \tau_{b_k} = \varphi_{k_0} + \varphi_{k_{1..(n-1)}} + \varphi_{k_n}$$

- V_k^* is obtained by interpolation among the values before and after the trigger

- τ_{ak} and τ_{bk} are obtained from the trigger instant (known the ADC rate) and τ_{a0} measured by the absolute time base

Numerical Metrological Analysis

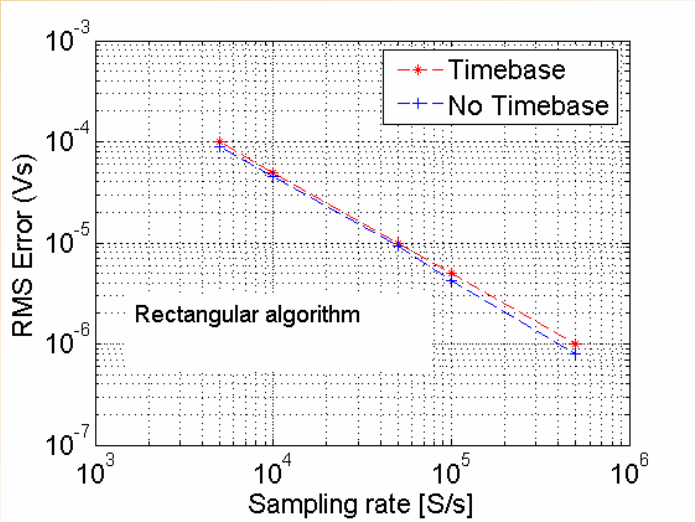
Error as difference between numerical and analytical integrals at varying:

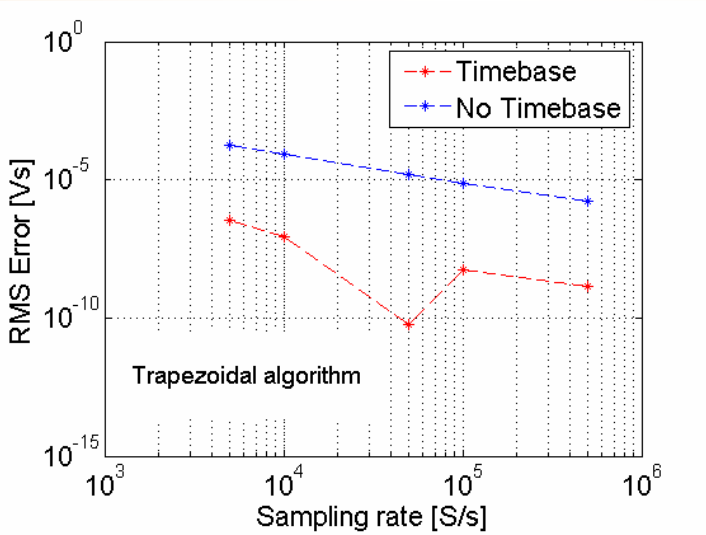
- Numerical algorithm
- Sampling rate
- Trigger frequency
- Timebase presence
- Timebase jitter

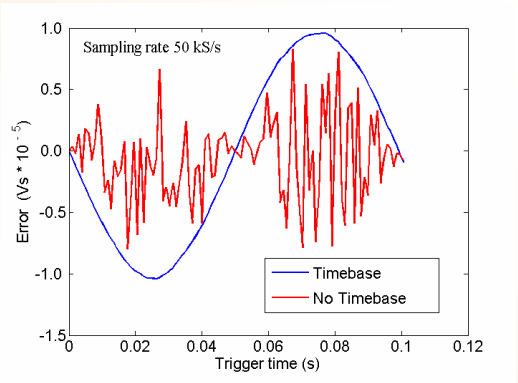
Input signal: sine wave , 2 Vpp, 10 Hz.

Deterministic error = RMS [E (Error (t))].
Random error = E [std (Error (t))].

Algorithm Error : Timebase Influence



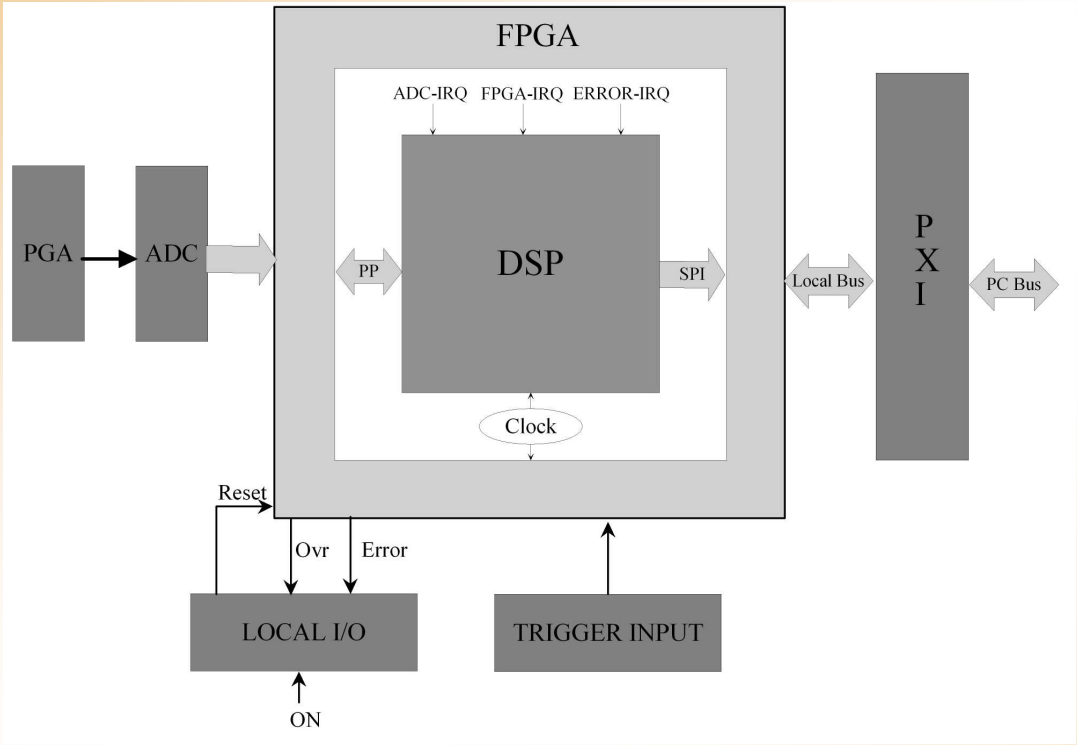




The advantages of an absolute 50-ns time base are evident for a trapezoidal algorithm. By using the rectangular algorithm, the error is increased…

→ without time base, the correlation between error and input signal is lost.

Hardware Implementation

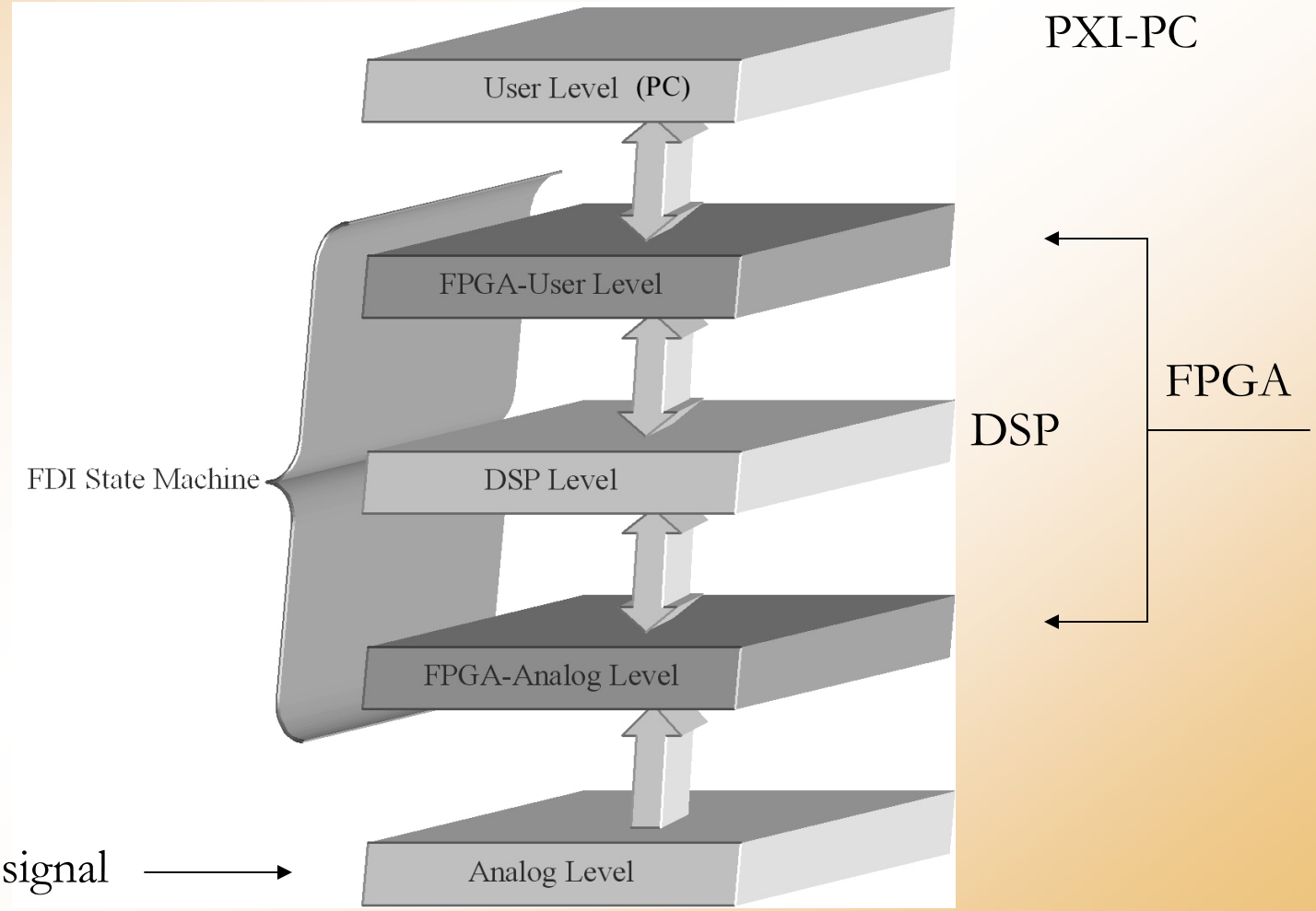


- PGA & ADC: analog front-end
- Trigger board: manages the pulses arising from an encoder
- FPGA: I/O processor
- DSP: processor for digital integration and board management
- PXI: data communication for board remote control

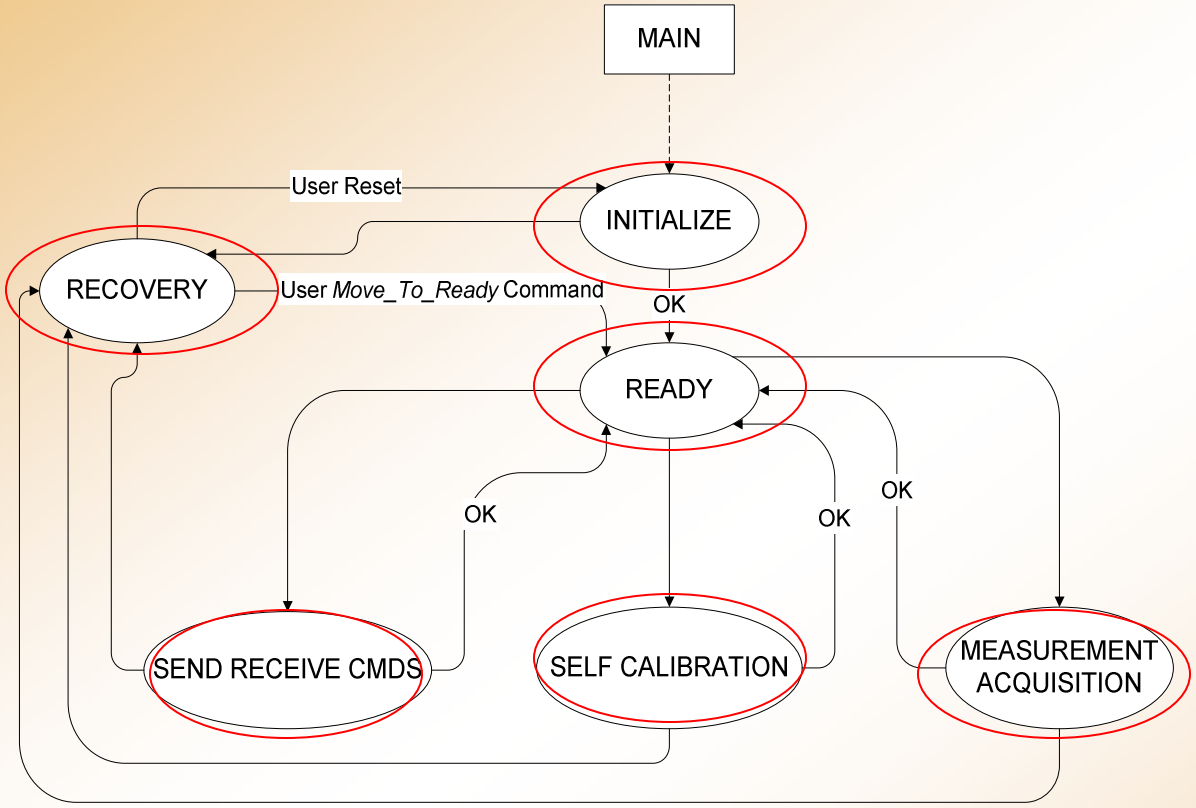
Analog Front-End

- ***Differential measurement chain***: the input section of the programmable gain amplifier (PGA) and the ADC input are fully differential in order to increase the CMRR;
- ***Digital Kelvin resistive divider***: the gain variation is obtained trough a programmable Kelvin resistor, by assuring high accuracy;
- ***FPGA control***: at low-level, a FPGA supervises PGA operations, self-calibration of the data acquisition chain, and the interface with the board bus;
- ***Dichotomic algorithm of self-calibration***: the calibration of the analog front-end is carried out in real-time automatically, by means of a dichotomic algorithm running on the FPGA;
- ***Real-time correction of systematic errors***: by processing the samples out of the ADC converter, the FPGA establishes the correction of the input gain and of the voltage offset, autonomously.

Firmware Architecture and Design: FDI Conceptual Levels



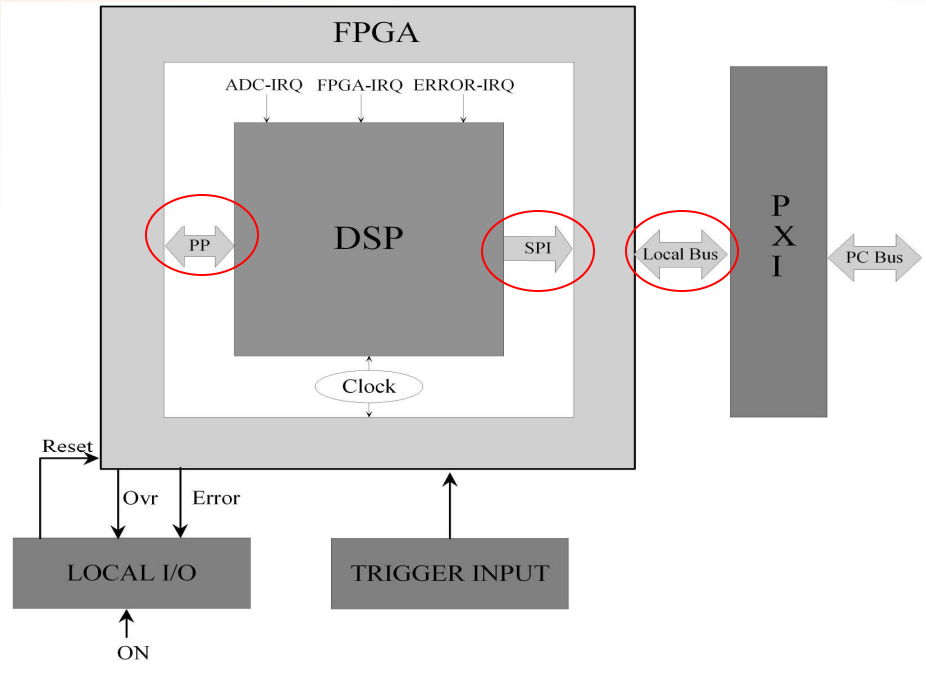
Firmware Architecture and Design: FDI State Machine



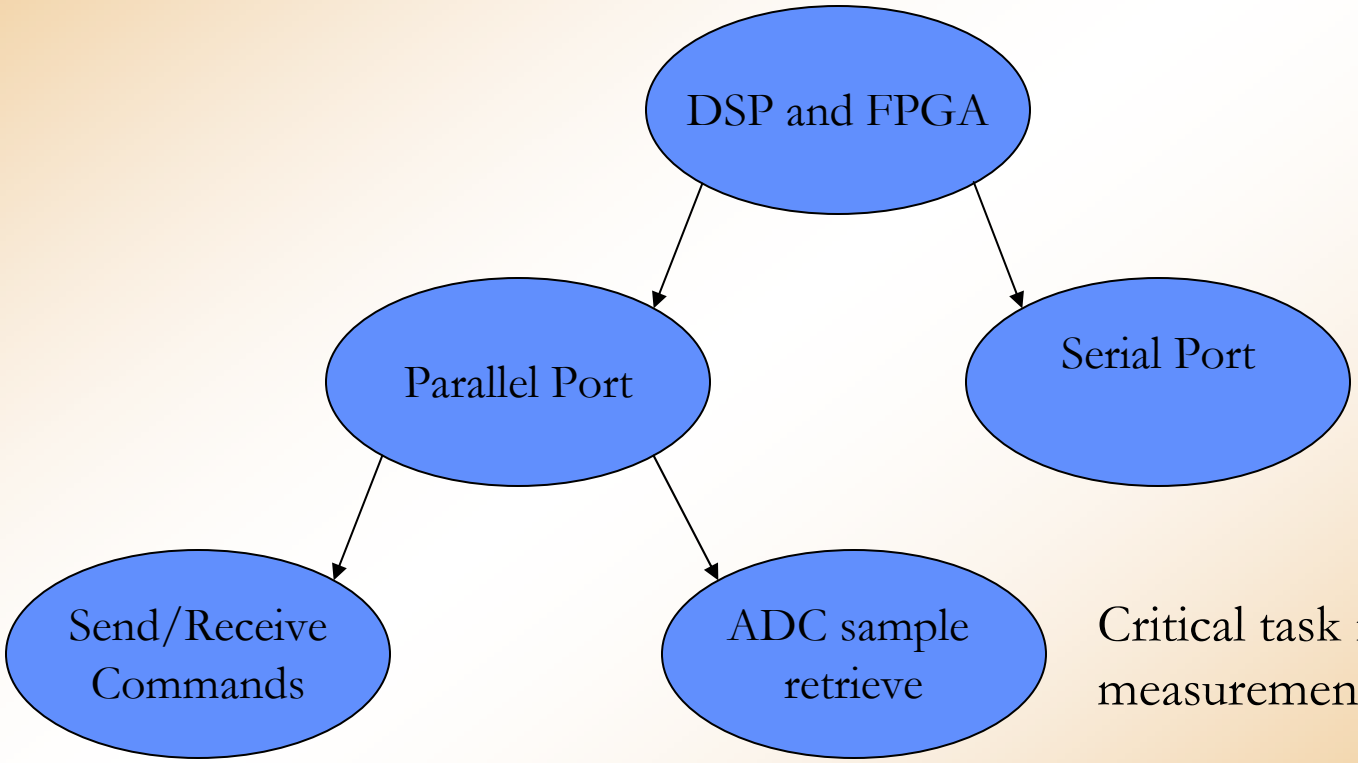
- INITIALIZE
- READY
- SELF CALIBRATION
- SEND/RECEIVE COMMANDS
- MEASUREMENT ACQUISITION
- RECOVERY

Board Communications

- FPGA acts as I/O interface for DSP by
  - Parallel Port (to ADC)
  - and Serial Port (SPI to PXI)
- FDI interfaces PC via PXI bus

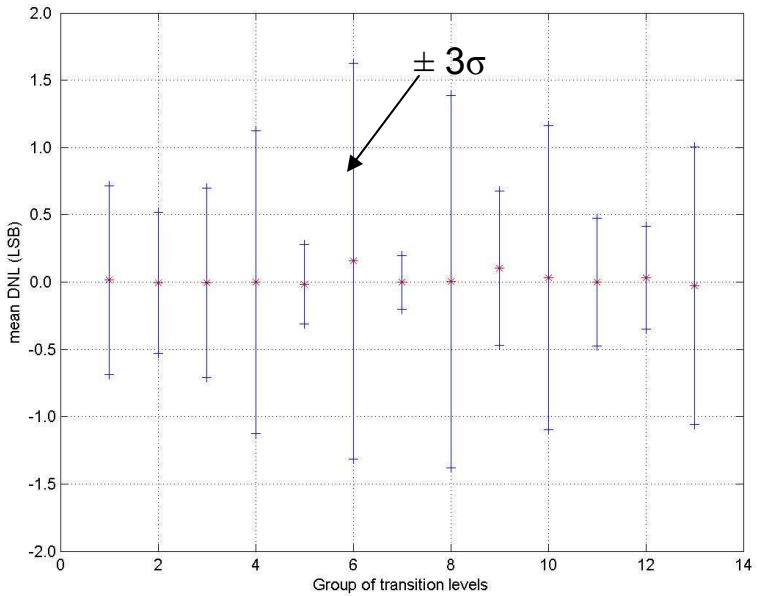


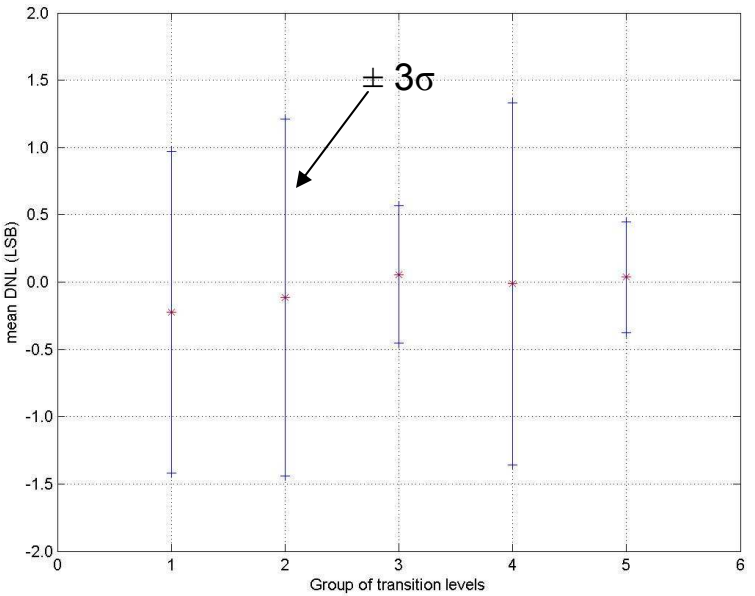
FPGA-DSP Communications



Critical task for the measurement algorithm

Results of Static Tests on prototype (I)

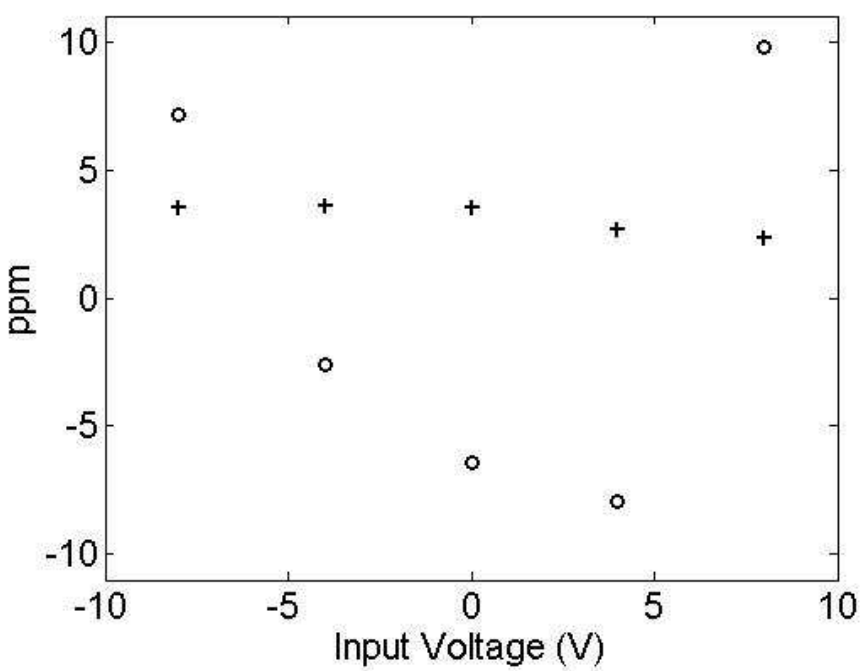


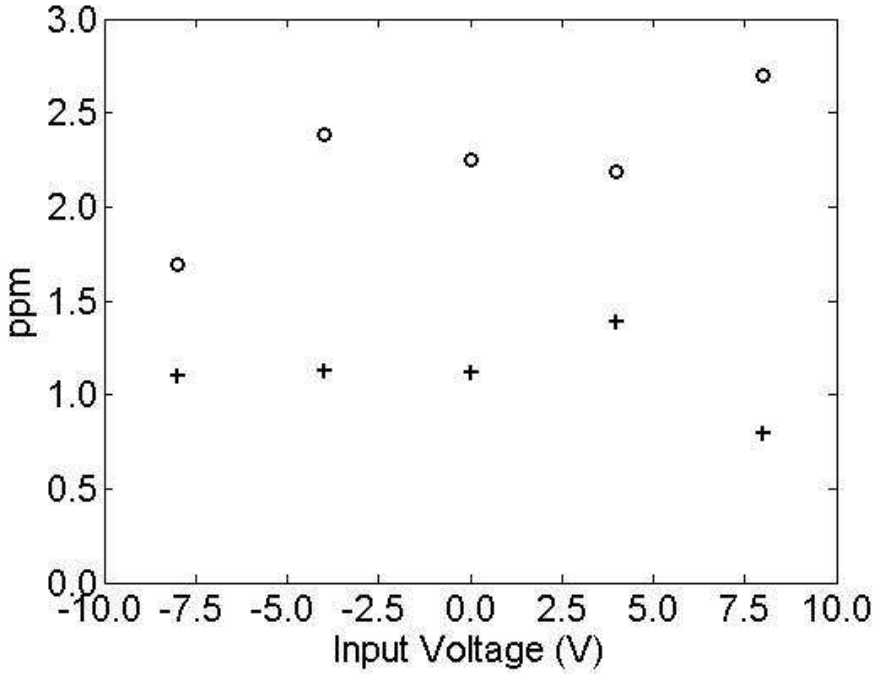


- **PDI**
  - Trigger frequency: 512 Hz
  - LSB: 10.240 mV

- **FDI**
  - Sampling rate: 625 kS/s
  - LSB: 38 µV

Results of Static Tests on prototype (II)

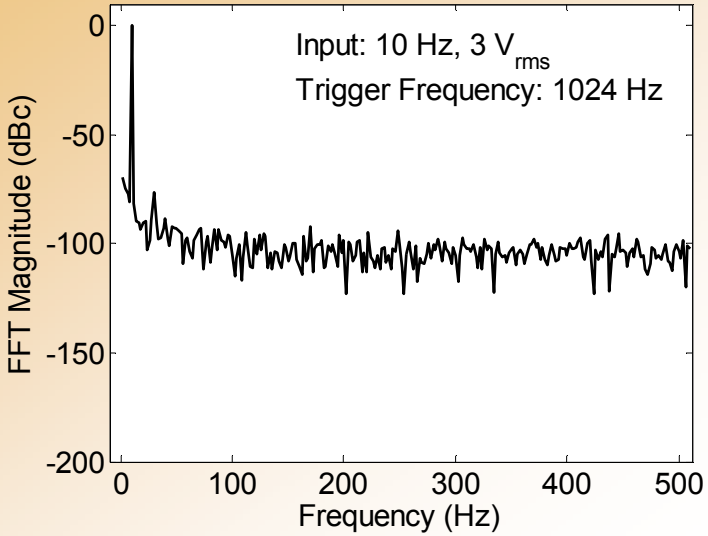




Nonlinearity error (o) and 2 **s** uncertainty Bands (+) relative to full scale

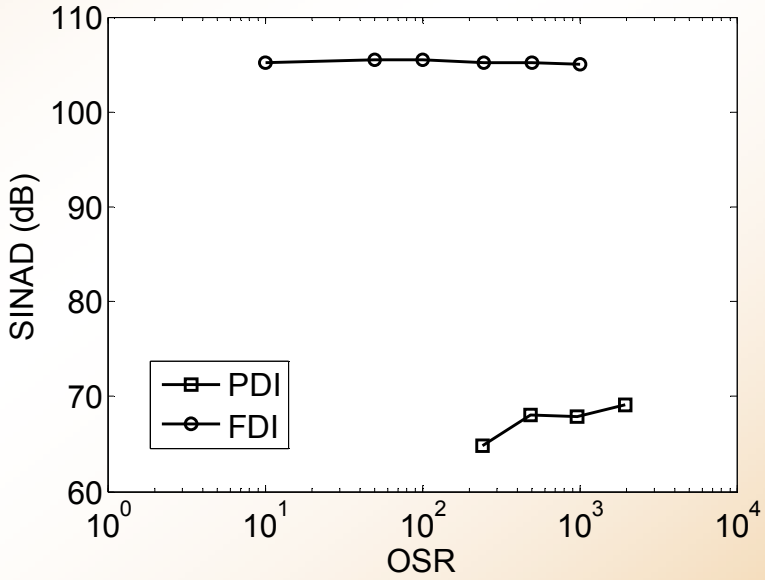
24-hours 2**s** stability bands (o) and 2**s** repeatability bands (+) (over 30 min relative to full scale

FFT Dynamic Tests Results

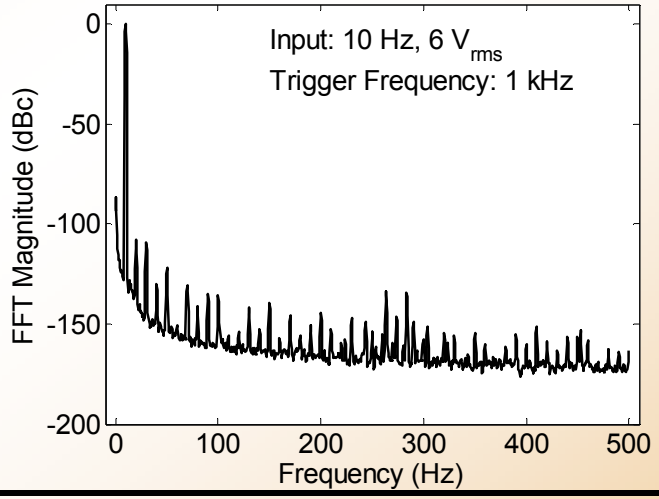


PDI

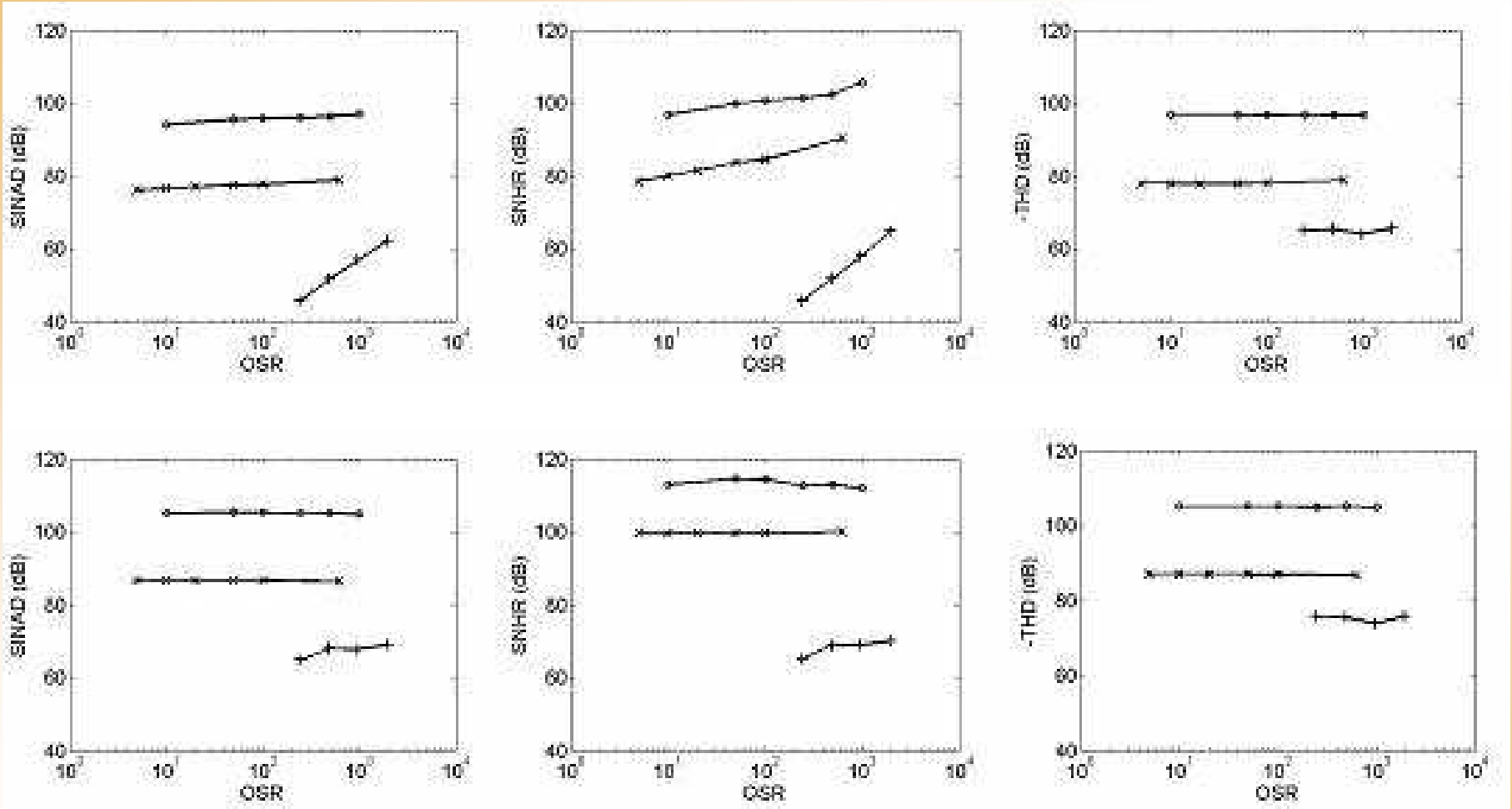
FDI



FDI – PDI comparison



Results of Dynamic tests of PDI vs. FDI



New FDI (o), previous FDI (x) and PDI (+) dynamic performance vs. oversampling ratio, as digitizers (up) and as integrators (down)

FFT Dynamic Test

	OSR	Trigger Frequency (Hz)	SINAD(dB)	SNHR(dB)	THD(dB)
PDI	1953	256	69.11	70.12	-75.95
PDI	244	2048	64.85	65.22	-75.75
FDI	1000	500	105.0	111.91	-104.94
FDI	10	50000	105.18	113.04	-105.15

- SINAD: **Signal to Noise And Distorsion Ratio**
- SNHR: **only Non Harmonic noise**
- THD: **Total Harmonic Distortion**

Future Developments

- Higher-order integrating filters will be tested in order to reduce noise
- Noise signature of rotating coils will be analyzed
- The metrological characterization will be completed
- Study interesting applications that could need modifications of this prototype

Conclusions

- FDI over performs PDI
- FDI can be easily reconfigured (firmware)
- Absolute time base improves FDI performance
- 12 FDI prototype units are being mounted to do test on SM18 this autumn on real magnets with new shafts