DUNE FD2 PDS Cold Box #1 as built Grounding, Shielding, and Cabling

Introduction

This document is the *as built* description for the DUNE Far Detector 2 (FD2) Photon Detector System (PDS) Cold Box #1 prototype. This document also defines the plans and methods for implementing grounding and shielding to ensure that the safety requirements are met, and to ensure that the noise performance of the detector and instrumentation meet experimental goals. The broad strategy is to optically isolate the cathode, have all conductive paths between components insulated and shielded, and for there to be no conductive components left floating without a reference voltage.

Here are the definitions of key terms in this document:

1. *Ground* is a general term that refers to a reference conductor that serves as a common potential for a specific circuit, subsystem, or facility. As there can be different kinds of grounds or ground references in an experiment, this document aims to be verbose when describing a reference.

2. *Shielding* refers to the application of metallic surfaces that interrupt the flow of electromagnetic energy, either radiated or conducted, to isolate sensitive circuits or conductors from the effects of interference. Generally, shields do not carry any signal current, although they may in certain circumstances.

3. *Common* is a term that is used to describe the local electrical reference node or net or plane for a circuit or set of circuits. It is often called “ground” or “ground plane” in a schematic or electronics design, although there may or may not be a direct connection to ground or Earth in the system. It is also often taken to be the “0 Volt Reference” for a circuit or system. When multiple power supplies are used in a circuit or system, often the power returns of the supplies are connected to this common node or plane.

4. *Safety Ground* refers to the system of conductors and equipment ground connections that provide a connection to the Earth Ground or the Grounding Electrode for the purpose of ensuring that hazardous electrical energy has a shunt path to Earth and away from personnel in the case of a fault.

5. D*etector Ground* refers to the system of conductors and connections that provide a reference or common for the sensitive instrumentation of the experiment. There are often certain noise requirements for this network that require special treatment. It is often distinguished from *Safety Ground* in HEP detector instrumentation systems, although the NEC places requirements on how this is connected and configured. In DUNE, warm detector components, including racks

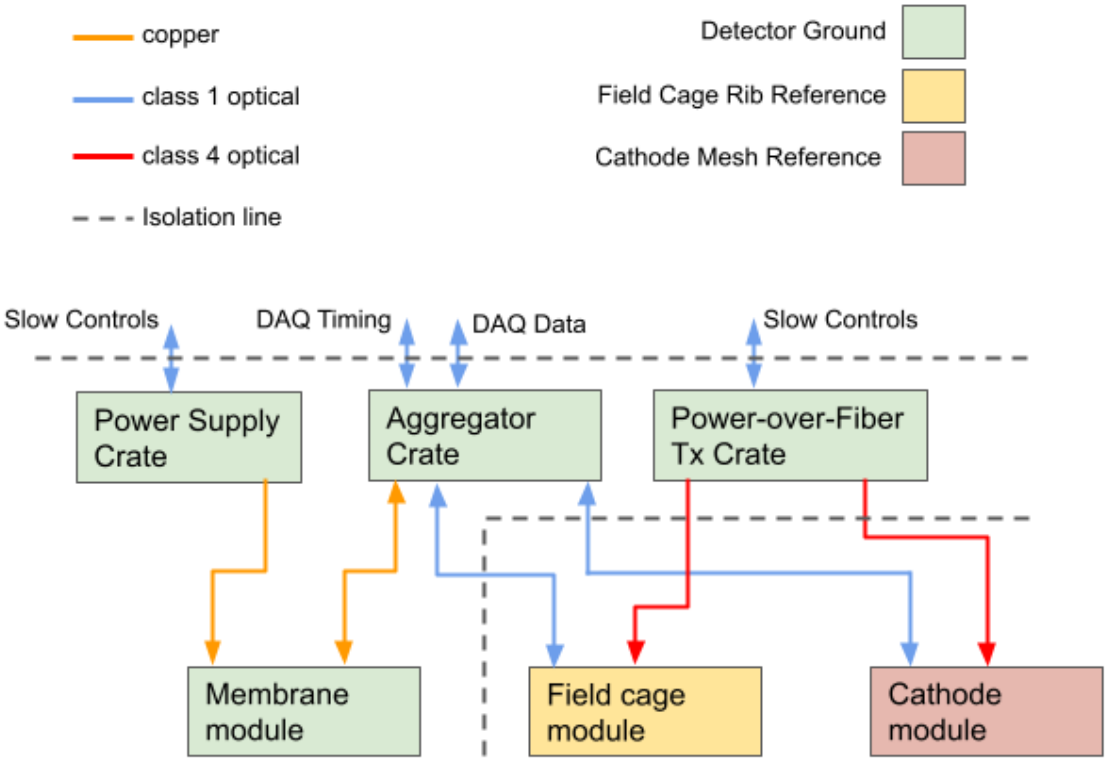
and crates, are generally referenced to *Detector Ground*. The cryostat itself is also *Detector Ground*.

6. *Cathode Mesh Reference* refers to the connection to a conductive portion of the cathode mesh. In cathode cells where the FD2 PDS modules are installed, the mesh covering the top and bottom of the cathode FRP structure is anticipated to be conductive (i.e., not resistive) for the 74cm x 65cm region of a cathode cell. A cage is formed between the top and bottom conductive mesh coverings and the M4 conductive screws securing the mesh around the perimeter of each cell. When the cathode HV is active, the cathode mesh charges up to -30kV at the Cold Box tests and -300kV at DUNE relative to the *Cryostat Reference*.

7. *Field Cage Rib Reference* refers to the connection to a rib of the field cage. The field cage is constructed of ribs, which are large conductive rings, isolated from each other and stacked between the anode and cathode and then again to the other anode. Each rib steps the cathode voltage in a controlled gradient up to the anode voltage (e.g., steps of 15kV).

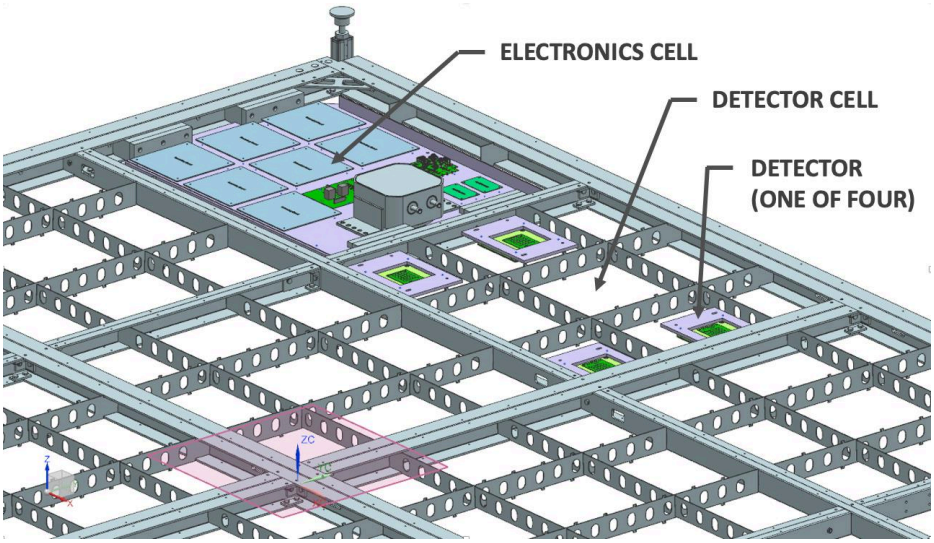
FD2 PDS System Diagram

The diagram below shows the system level view of the connection types and references in the FD2 PDS. All copper cables are shielded with the shield connected to the landing location on one or both sides.

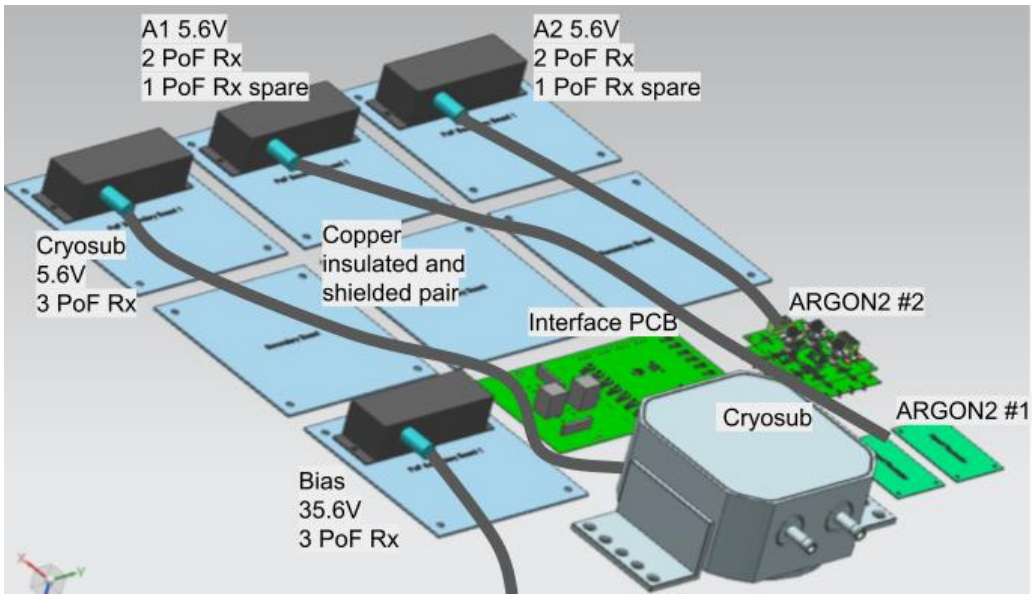


FD2 PDS Cold Box Cathode Module

The installation plan for a cathode-style module electronics cell and detector cell for the FD2 PDS at Cold Box 1 is shown in the capture below. There are two cathode module instances installed for Cold Box 1.

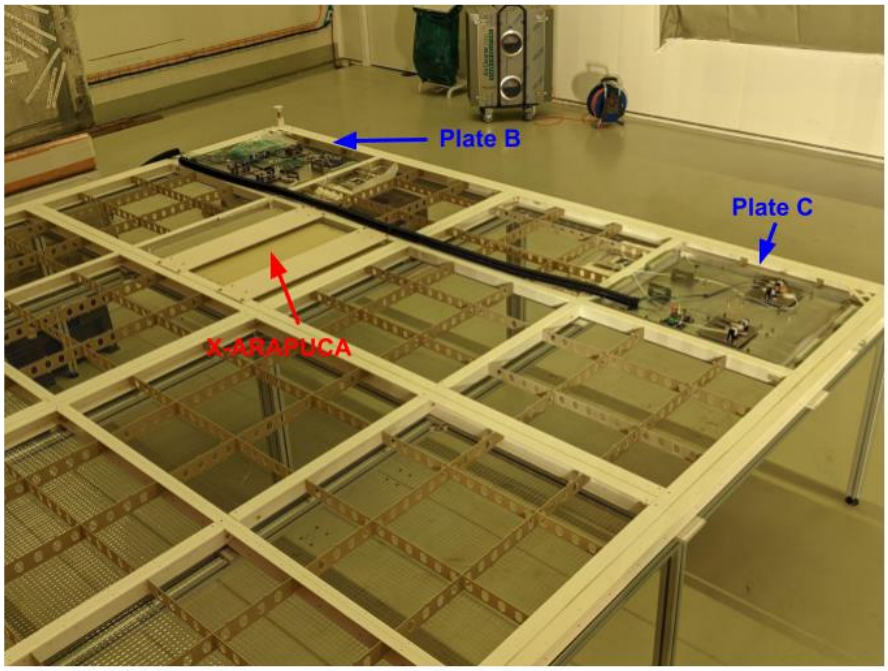


The electronics cell is comprised of an aluminum plate installed in the cathode by interfacing mounting blocks made of G10. The aluminum plate is isolated from the mesh by G10 ribs supporting the mesh. The layout of the Cold Box Test 1 FD2 PDS electronics plate is shown in the capture below:

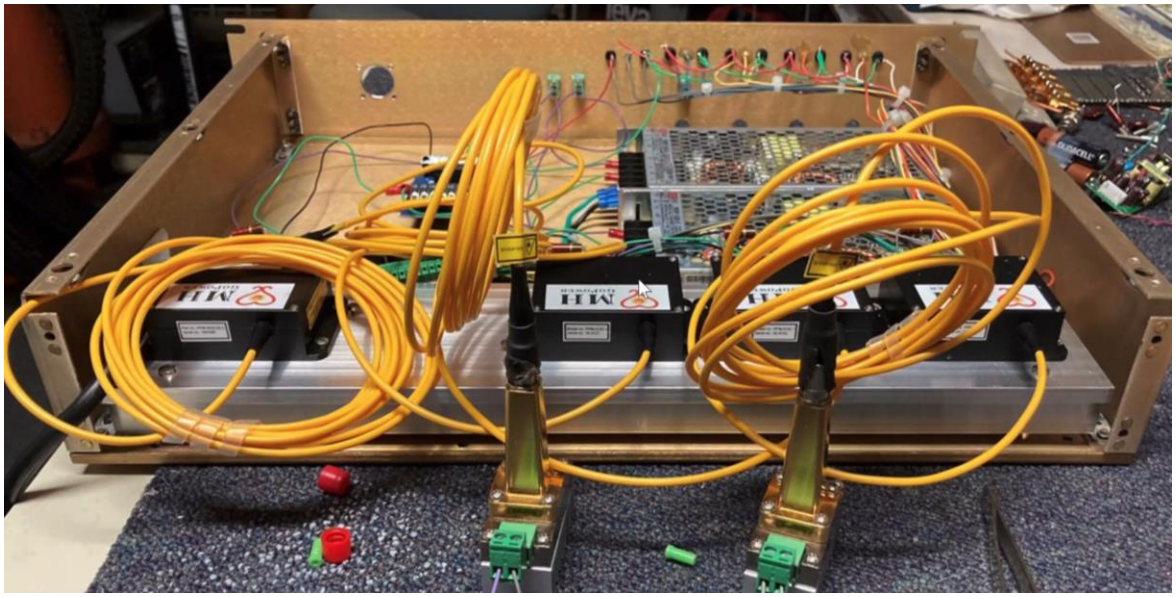


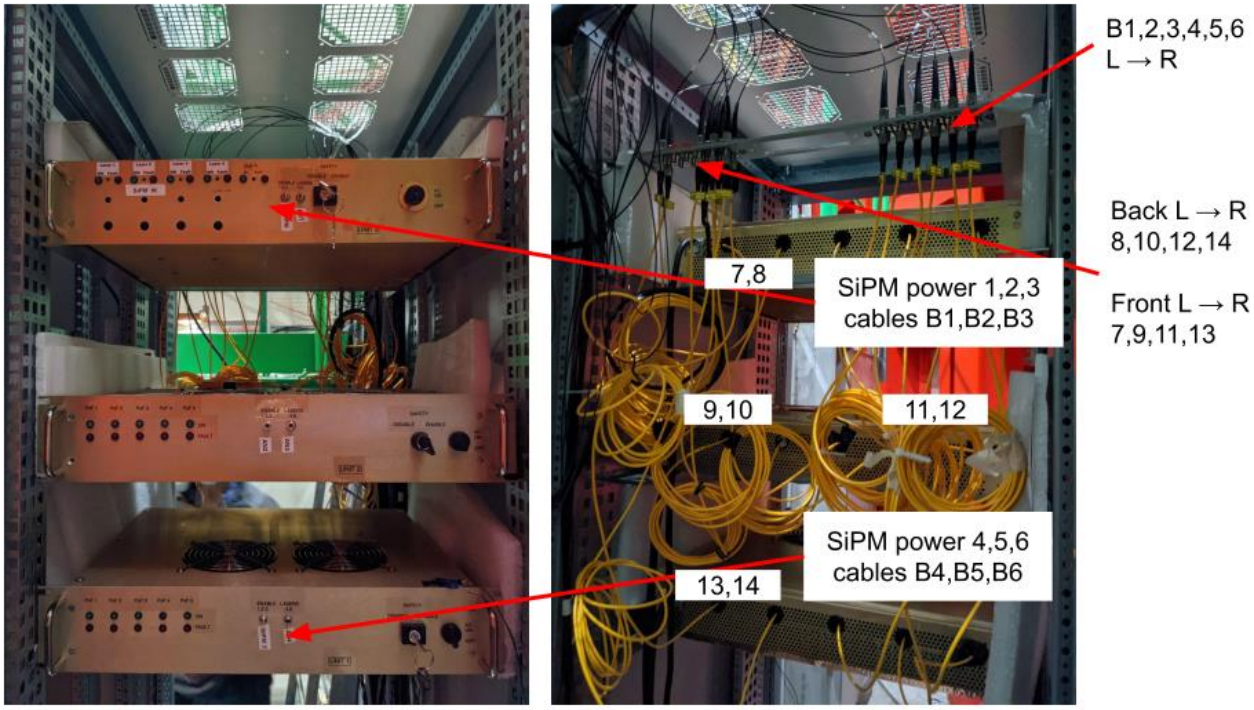
In the above capture, the four power-over-fiber modules are shown with their destination copper leads. Three class 4 fiber arrive at each power-over-fiber module to deliver the optical power for conversion.

The optical fibers for power and output signal result in the PDS cathode installation being completely isolated from Detector ground. The cathode-style modules are instead referenced to the cathode mesh.

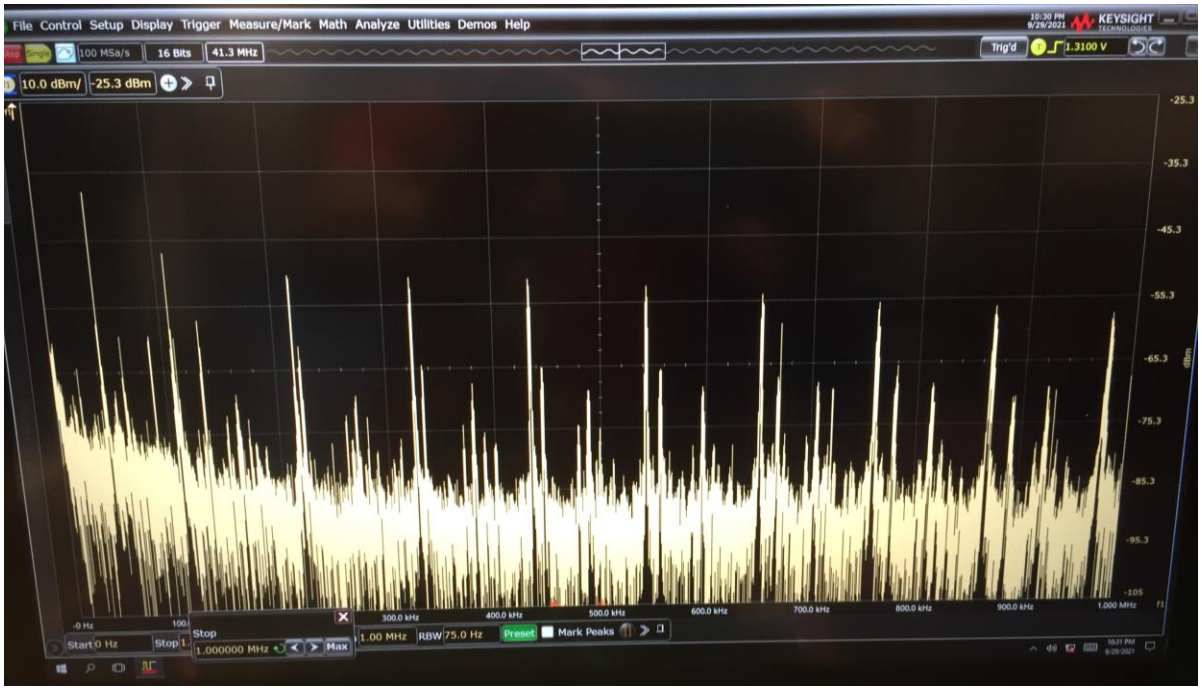


To assess any potential for noise contamination in the warm racks, a spectral analysis was conducted of the custom power-over-fiber laser transmitter unit for Cold Box 1. Shown below is the custom unit:

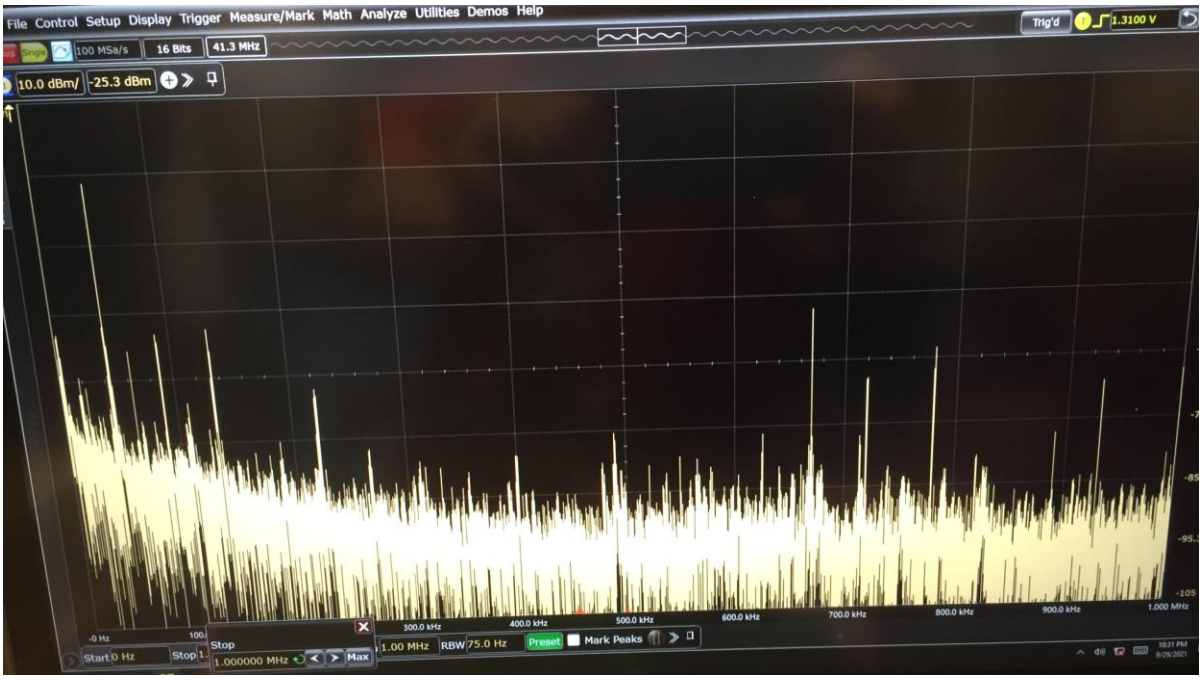




Shown below is the measurement taken at 1 foot with the unit on. A Keysight MXR404A Mixed Signal Oscilloscope was used for this measurement.



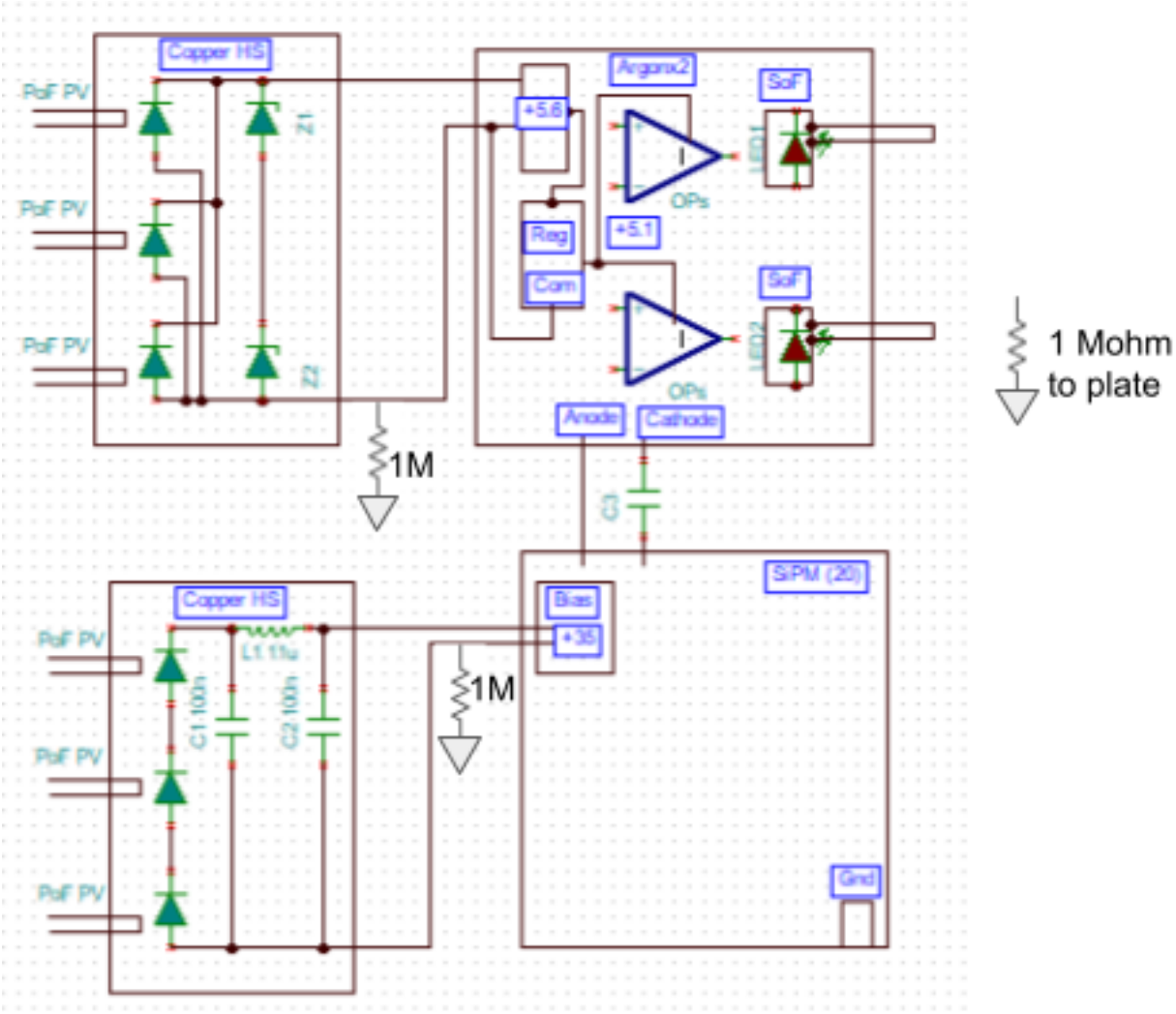
The following image is the measurement taken at 1 foot with the unit off.



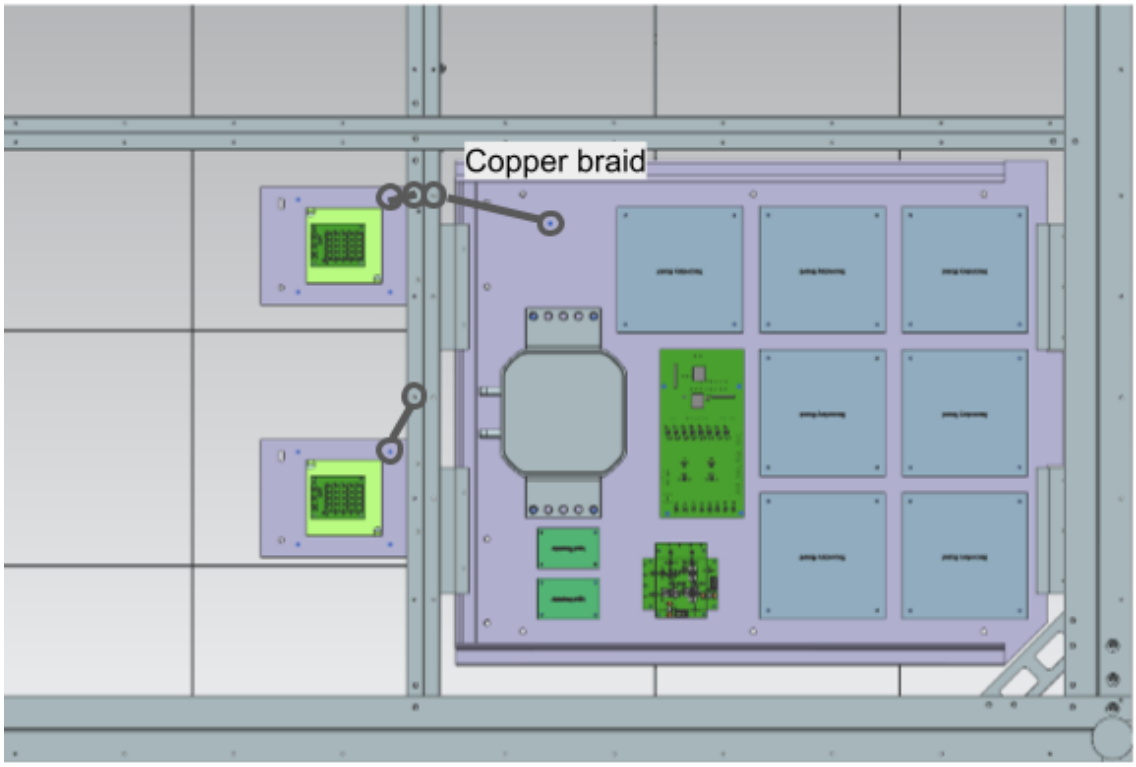
The noise from the custom power-over-fiber laser transmitter unit for Cold Box 1 is primarily observed to be the 100kHz switching noise. The custom box consists of two power supplies, five lasers, and

supporting hardware. The switching power supplies in the unit generate harmonics at that switching frequency. The results match expectations.

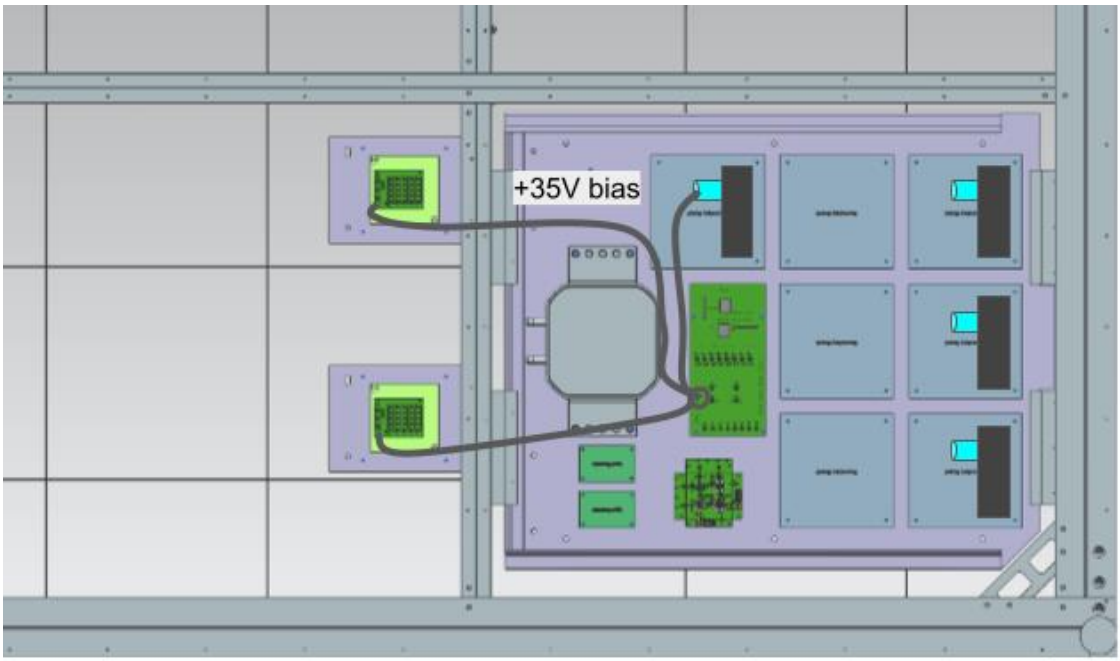
The schematic below shows the plan to tie the return leads to the aluminum plate reference through a 1 megaohm resistor to prevent the power-over-fiber module copper leads from floating:



The aluminum plate is connected to the Cathode Mesh Reference at one location as shown in the capture below:



The +35V bias power-over-fiber module will fanout the bias to the mini-ARAPUCAs and, potentially, xARAPUCA through the Interface PCB as shown in the capture below:



The schematics for the ARGON2 analog readout and the Interface PCB are attached at the end of this document.

PLATE C

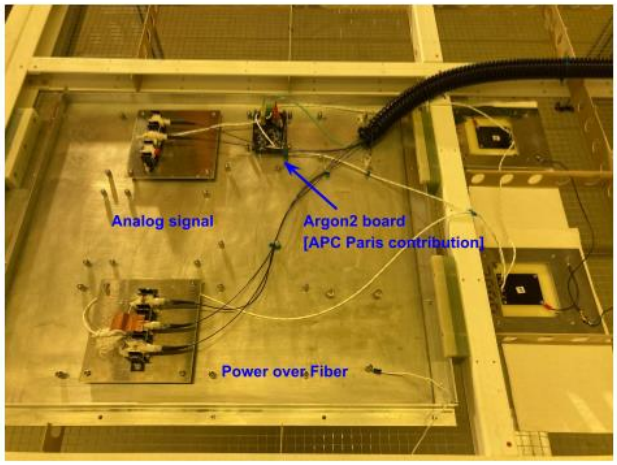
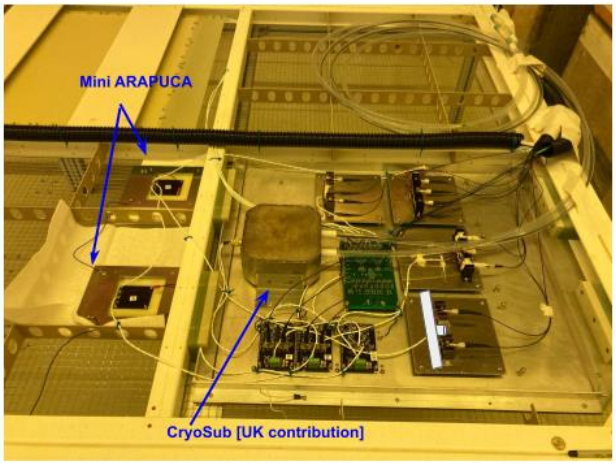
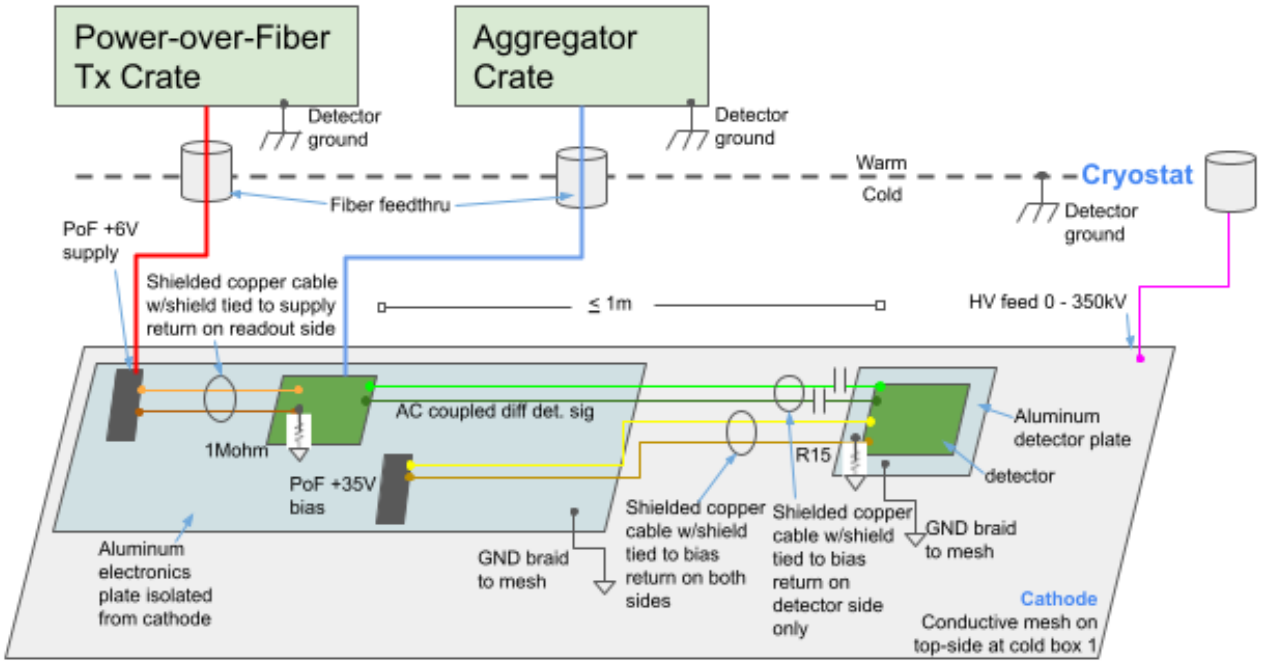


PLATE B

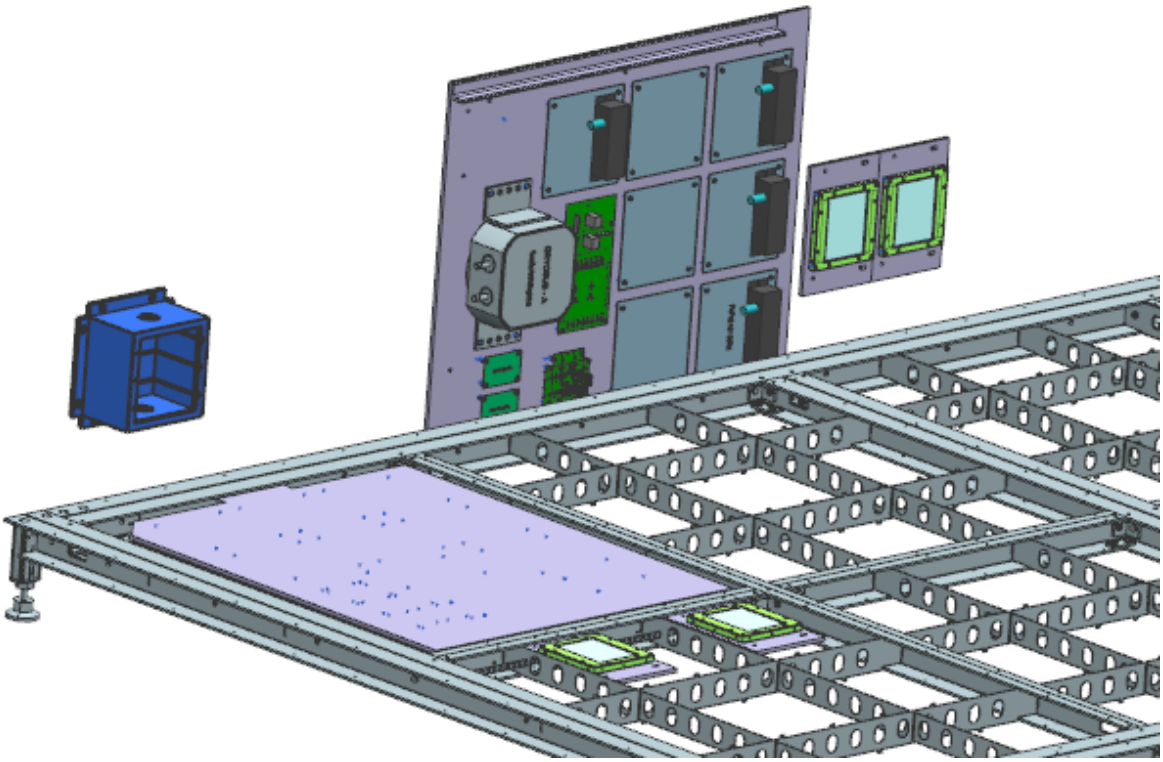


A grounding and shielding block diagram for one cathode readout channel is given in the image below:

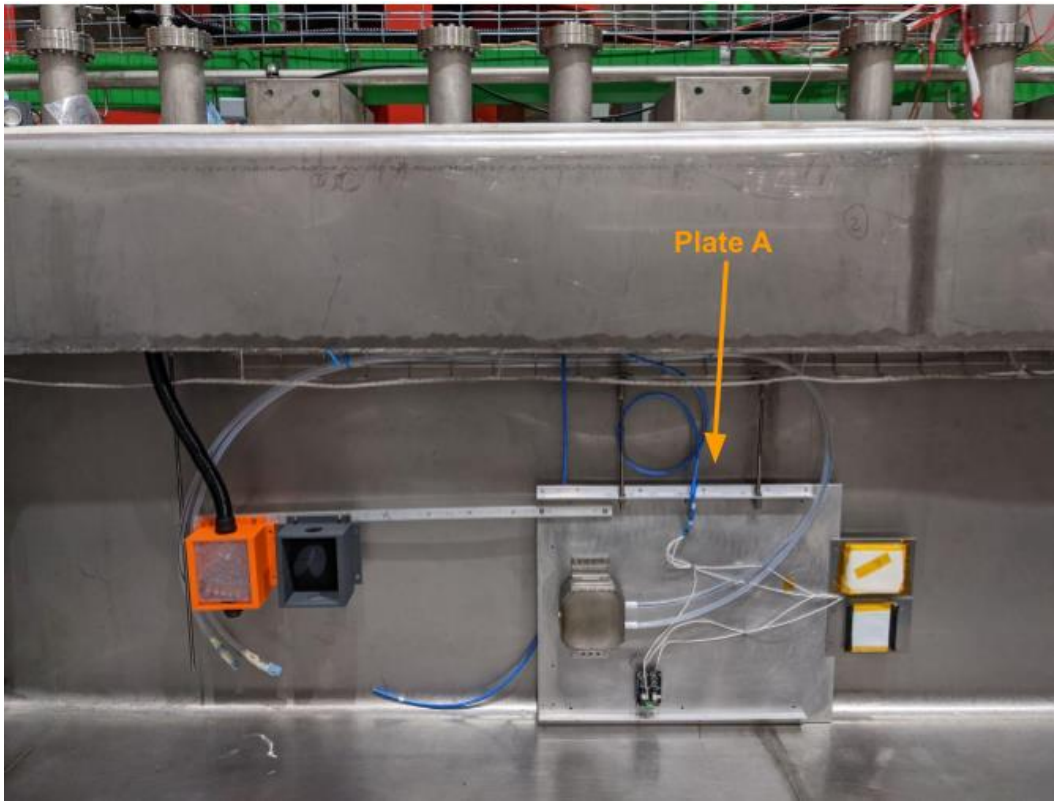


FD2 PDS Cold Box Membrane Module

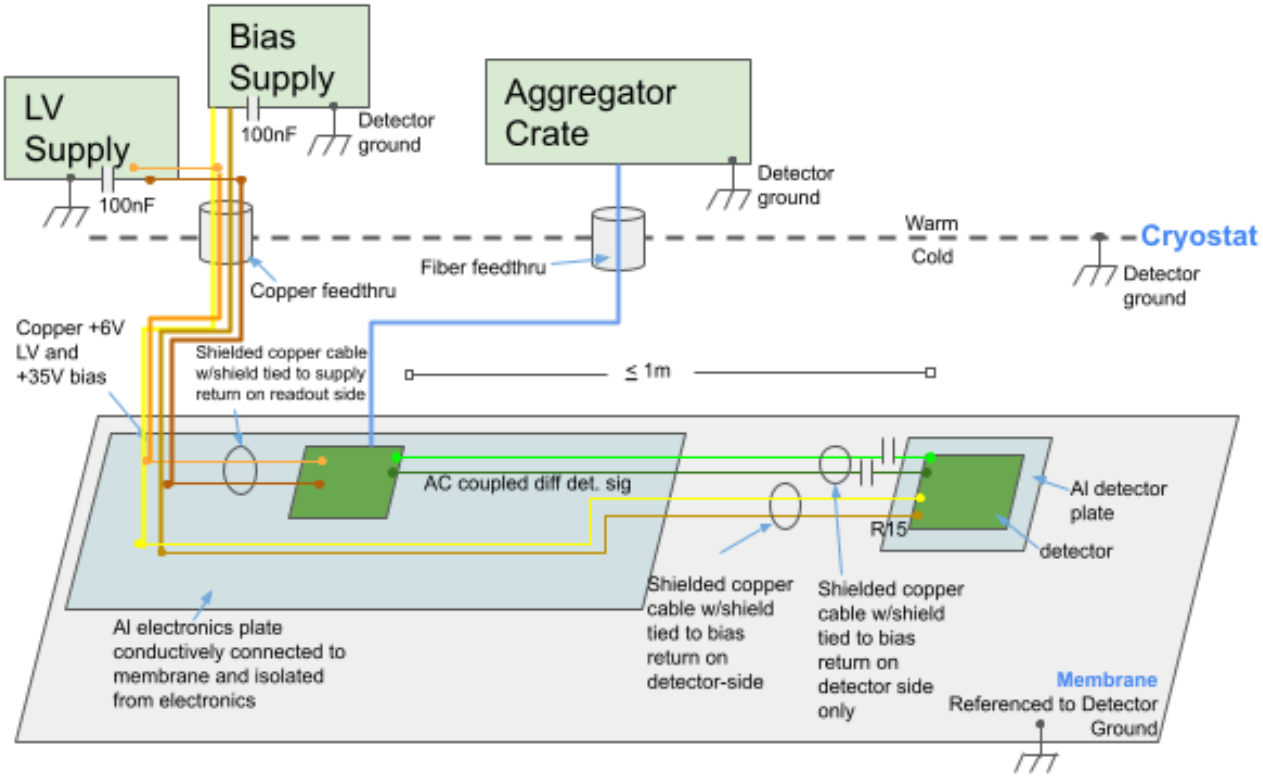
The installation plan for a membrane-style module electronics cell and detector cell for the FD2 PDS at Cold Box 1 is shown in the capture below. There is one membrane module instances planned for Cold Box 1.



The membrane-style module has the same components as the cathode-style module except for power is delivered over copper, rather than fiber.

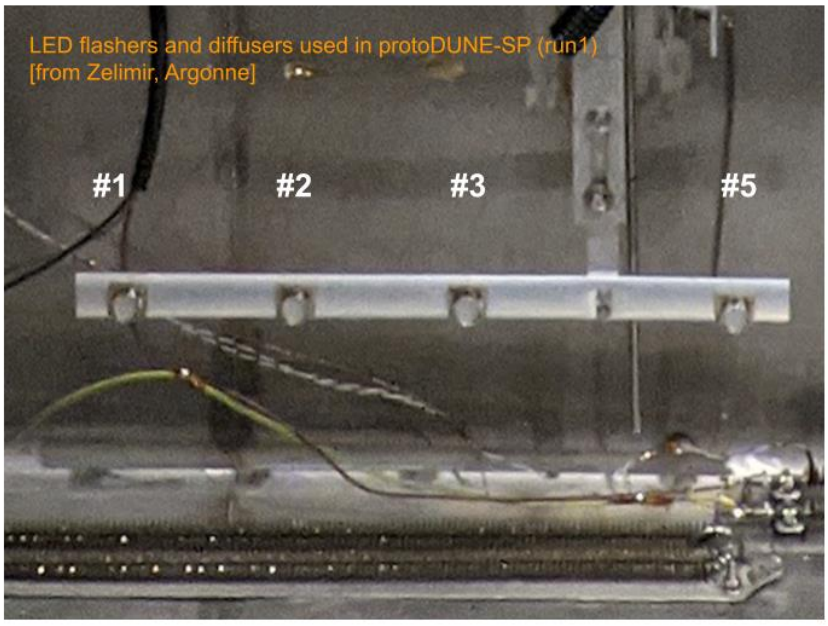


Below is a grounding and shielding block diagram representing the membrane Cold Box 1 installation:



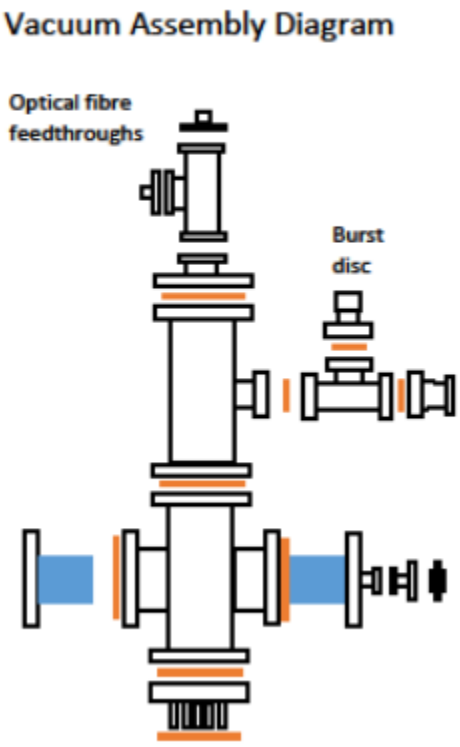
FD2 PDS Additional Components

A passive LED flasher system was installed from ProtoDUNE-SP run 1:



The Cryosub vacuum housing mounts on top of the cryostat to a dedicated flange, which is on detector ground and a vacuum pump is required to be connected to the flange for steady-state operation. If the Cryosub pump connection is conductive then care should be taken to plug it into detector ground, to avoid creating an inadvertent path to detector ground. For example, if the vacuum pump power is referenced to building/safety ground, then a conductive path is created to detector ground through conductive vacuum connector; in this case, the nonconductive connector should be installed. The cathode fiber disconnects will occur at FC couplers at the power-over-fiber coupler box and at a secondary plate on the membrane installation.

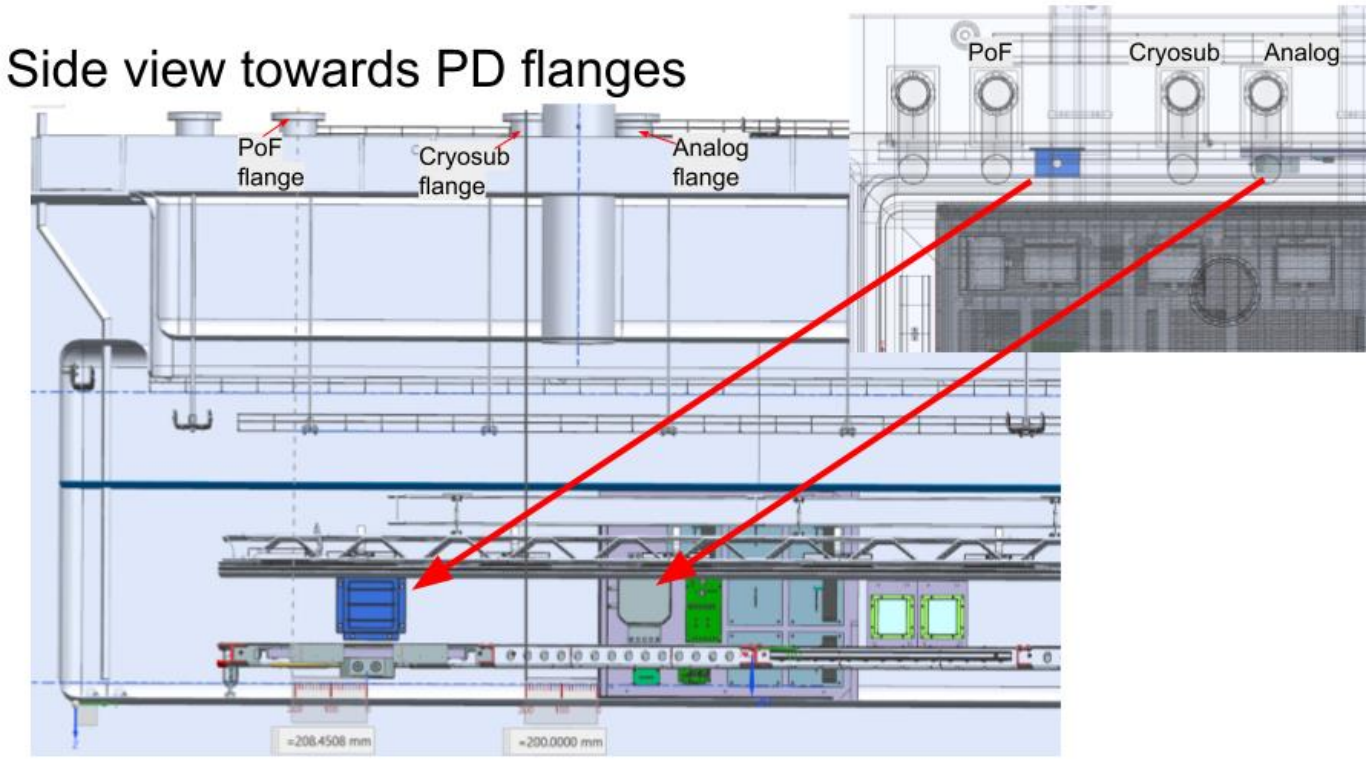
Below is the Cryosub vacuum housing assembly diagram. The Burst disc is a critical safety feature for overpressure events. Please contact the Croysub technical leads before modifying the Cryosub vacuum assembly.



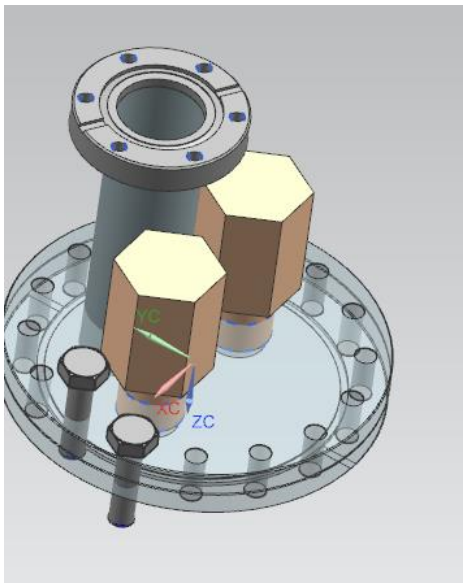
The power-over-fiber coupler box and FC-FC optical fiber coupler are shown below:

https://www.fs.com/products/17537.html

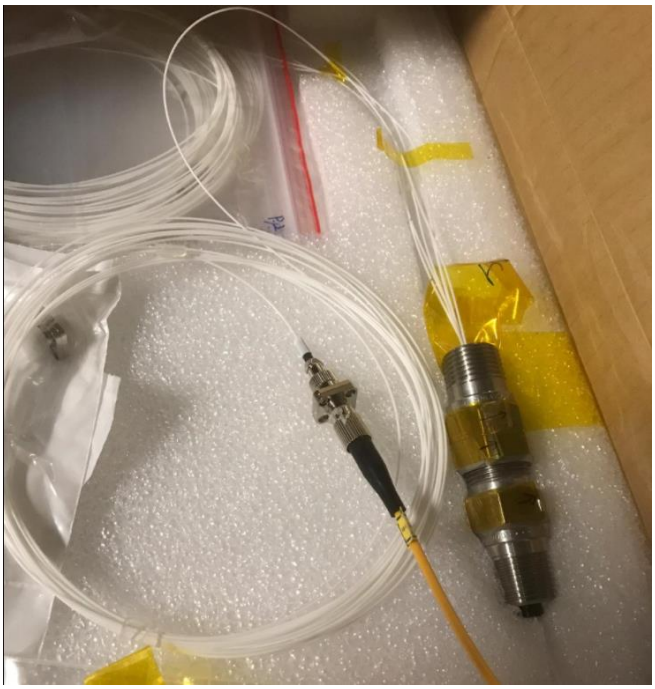
The copper power cable arrives through the Analog flange copper feedthrough. Analog flange relative position to the membrane-style module can be seen in the capture below.



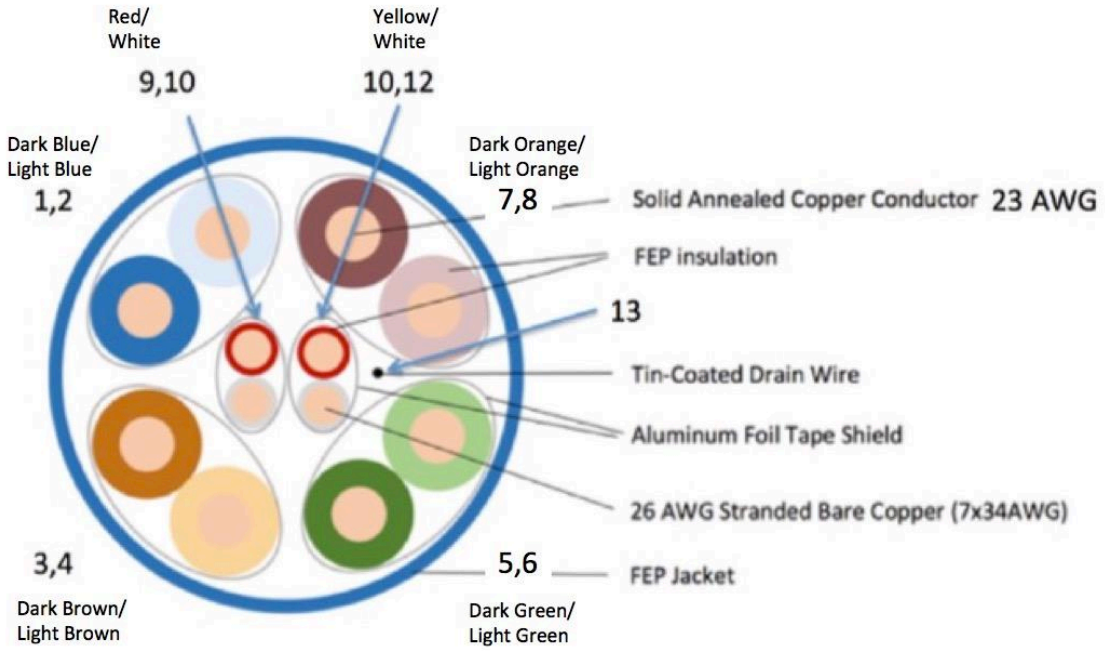
The analog flange is shown below with copper feedthrough's elevated chimney and two fiber feedthrough positions:



The optical feedthrough is shown in the image below – it is a ¾” feedthrough with either 8 signal fibers or 14 power-over-fiber fibers:



The copper cable used is the FD1 PDS Superior-Essex custom CAT-6 cable shown below. This cable is shielded with a drain wire, which will be connected at both ends to form a faraday cage penetration.



For the cold box installation, we will use the four 23 AWG pairs only as this simple passive feedthrough does not connect the internal 26 AWG pairs. The feedthrough is a passive pass through of the 8 outer conductors and the drain wire. We will have two feedthroughs on the flange for a total of 8 pairs and drain wire as shown in the image below.

Three separate low-voltage supplies of 100mA @ 5.5V will be over Dark Blue/Light Blue (1,2), Dark Brown/Light Brown (3,4), and Dark Green/Light Green (5,6) of the first feedthrough. Two bias supplies of

100nA @ 35V will be over Dark Blue/Light Blue (1,2) and Dark Brown/Light Brown (3,4) of the second feedthrough.

This simple passive test feedthrough was already used at CERN for test of ARAPUCAs with xenon at Horizontal Drift ProtoDUNE1.

The copper cable will have a male cable end plug as shown below:

HR10A-10P-12PC(73) Datasheet

Digi-Key Part Number	HR1674-ND
Manufacturer	Hirose Electric Co Ltd
Manufacturer Part Number	HR10A-10P-12PC(73)
Description	CONN PLUG HSG MALE 12POS INLINE
Manufacturer Standard Lead Time	12 Weeks
Detailed Description	12 Position Circular Connector Plug Housing Free Hanging (In-Line) Backshell, Cable Clamp, Strain Relief

The flange has a female PCB mount receptacle as shown below:

HR10A-10R-12SB(71) Datasheet

Digi-Key Part Number	HR1647-ND
Manufacturer	Hirose Electric Co Ltd
Manufacturer Part Number	HR10A-10R-12SB(71)
Description	CONN RCPT FMALE 12POS SOLDER
Manufacturer Standard Lead Time	12 Weeks
Detailed Description	12 Position Circular Connector Receptacle, Female Sockets Solder

Here is the male crimp pin for Hirose connectors:

HR10-PC-112

Datasheet

Digi-Key Part Number	HR451-ND
Manufacturer	Hirose Electric Co Ltd
Manufacturer Part Number	HR10-PC-112
Description	CONTACT PIN 26-30AWG CRIMP SLVR
Manufacturer Standard Lead Time	12 Weeks
Detailed Description	Pin Contact 26-30 AWG Size 1.0mm Crimp Silver

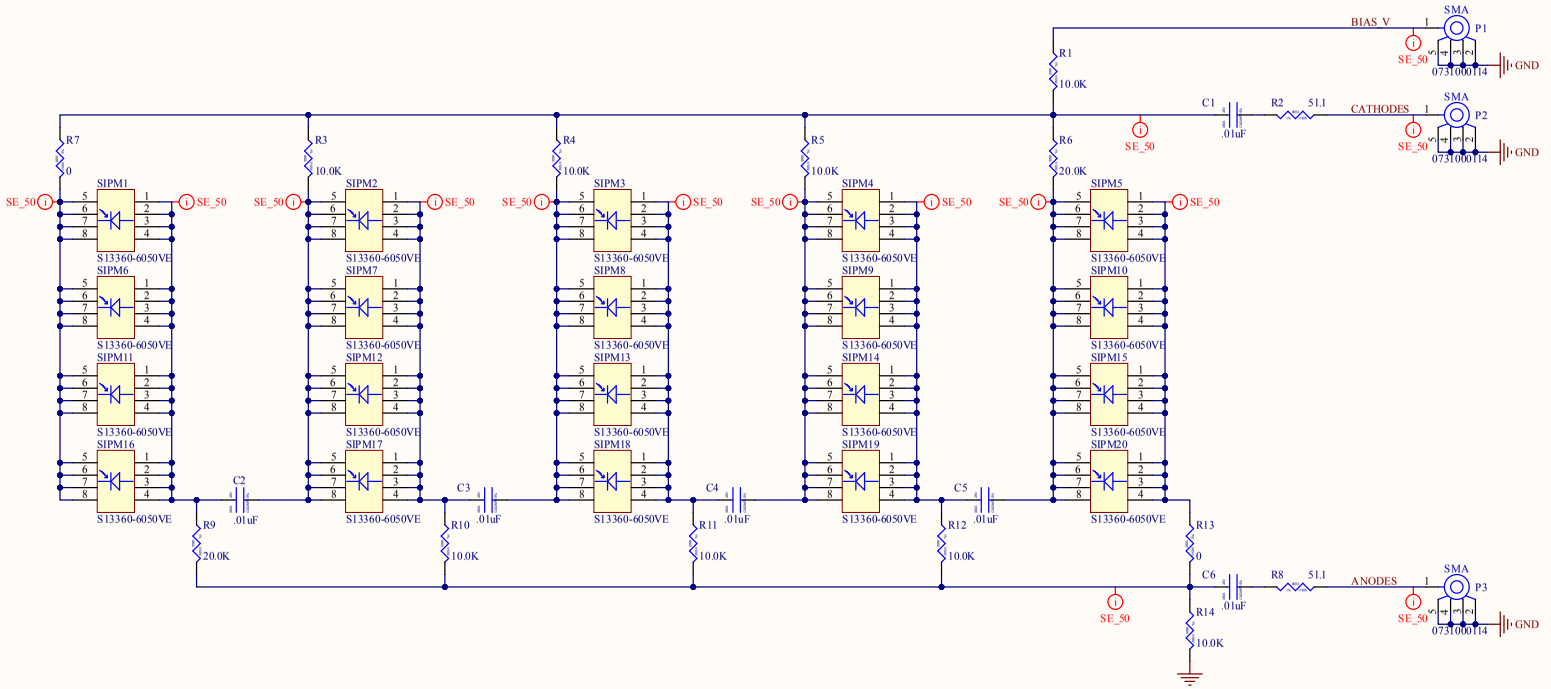
Here is the female crimp pin for Hirose connectors:

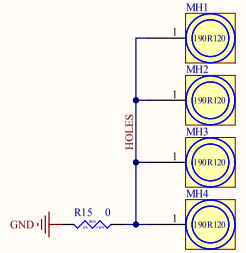
HR12-SC-112

Datasheet

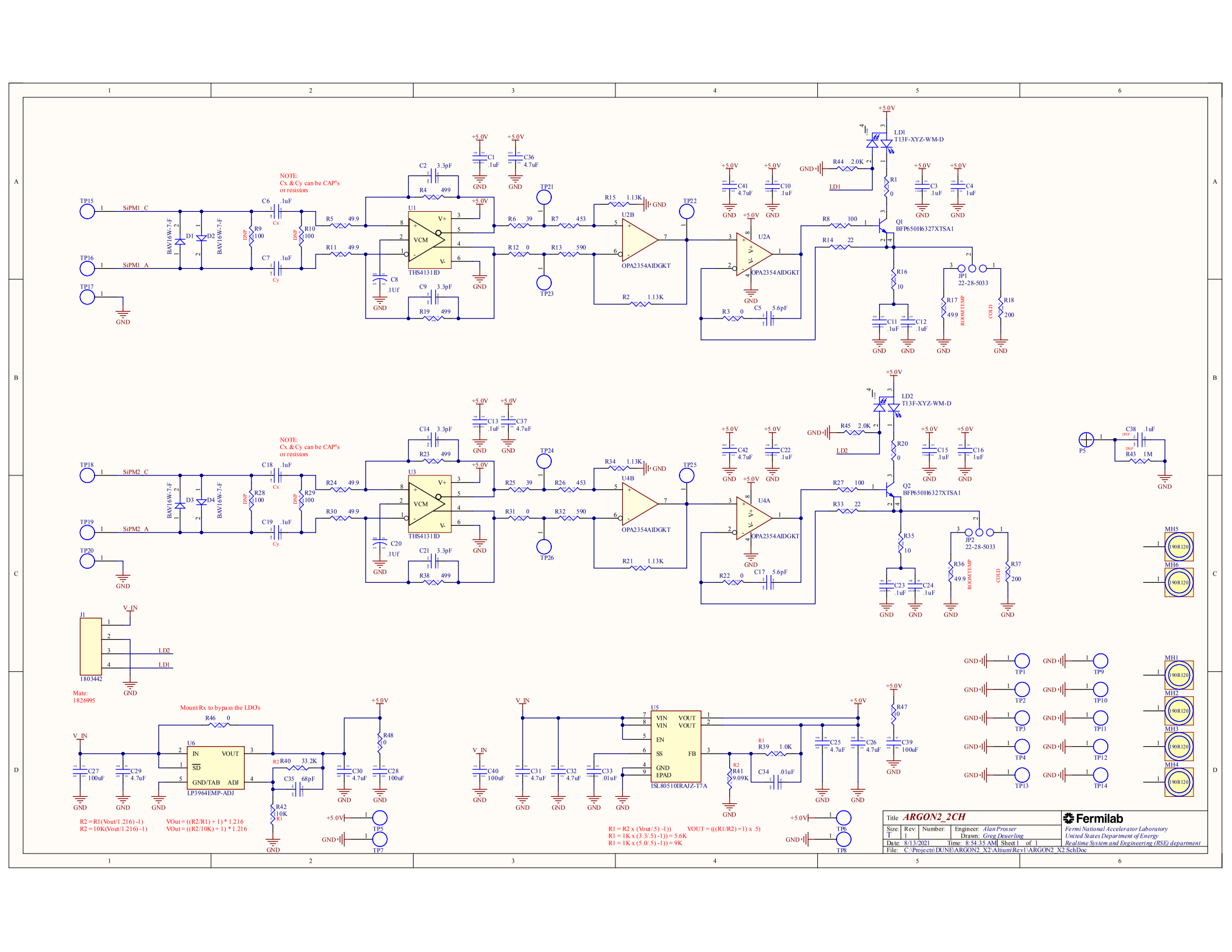
Digi-Key Part Number	HR453-ND
Manufacturer	Hirose Electric Co Ltd
Manufacturer Part Number	HR12-SC-112
Description	CONTACT SOCKET 26-30AWG CRIMP
Manufacturer Standard Lead Time	12 Weeks
Detailed Description	Socket Contact 26-30 AWG Size 1.0mm Crimp Silver

The schematics for the ARGON2 analog readout and the Interface PCB are attached at the end of this document.



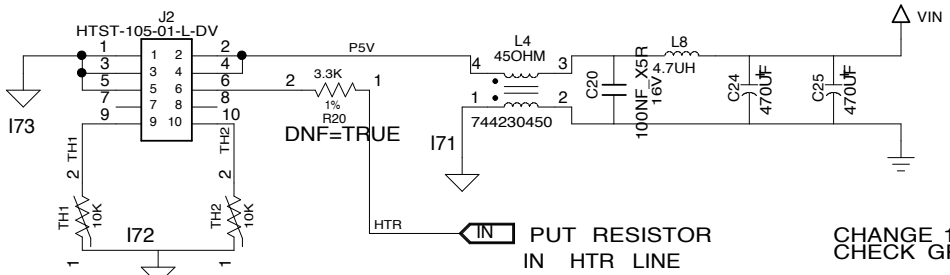


Title	DUNE-VD Test		Fermilab
Size: T	Rev: 1.0	Number:	Engineer: Greg Deuerling Drawn: Greg Deuerling
Date: 5/3/2021	Time: 10:31:34 AM	Sheet 1 of 1	Fermi National Accelerator Laboratory United States Department of Energy Realtime System and Engineering (RSE) department
File: C:\Projects\DUNE\DUNE_VD_Test\Altium\Rev1\DUNE_VD_Test.SchDoc			


NOTE:
Cx & Cy can be CAP"s
or resistors
THS4131ID
OPA2354AIDGKT
BFP650H6327XTSA1
T13F-XYZ-WM-D
22-28-5033
1803442
Mate:
1826695
Mount Rx to bypass the LDO's
LP3964EMP-ADJ
ISL80510IRAJZ-T7A
R2 = R1(Vout/1.216) -1)
R2 = 10K(Vout/1.216) -1)
VOut = ((R2/R1) + 1) * 1.216
VOut = ((R2/10K) + 1) * 1.216
R1 = R2 x (Vout/.5) -1))
R1 = 1K x (3.3/.5) -1)) = 5.6K
R1 = 1K x (5.0/.5) -1)) = 9K
VOUT = (((R1/R2) +1) x .5)
ROOM TEMP
COLD
Title ARGON2_2CH
Size: T
Rev: 1
Number:
Engineer: Alan Prosser
Drawn: Greg Deuerling
Date: 8/13/2021
Time: 8:54:35 AM
Sheet 1 of 1
File: C:\Projects\DUNE\ARGON2_X2\Altium\Rev1\ARGON2_X2.SchDoc
Fermilab
Fermi National Accelerator Laboratory
United States Department of Energy
Realtime System and Engineering (RSE) department

N.B. CAREFUL LAYOUT!
NEED TO REDUCE EMI LEAKAGE
AS MUCH AS POSSIBLE

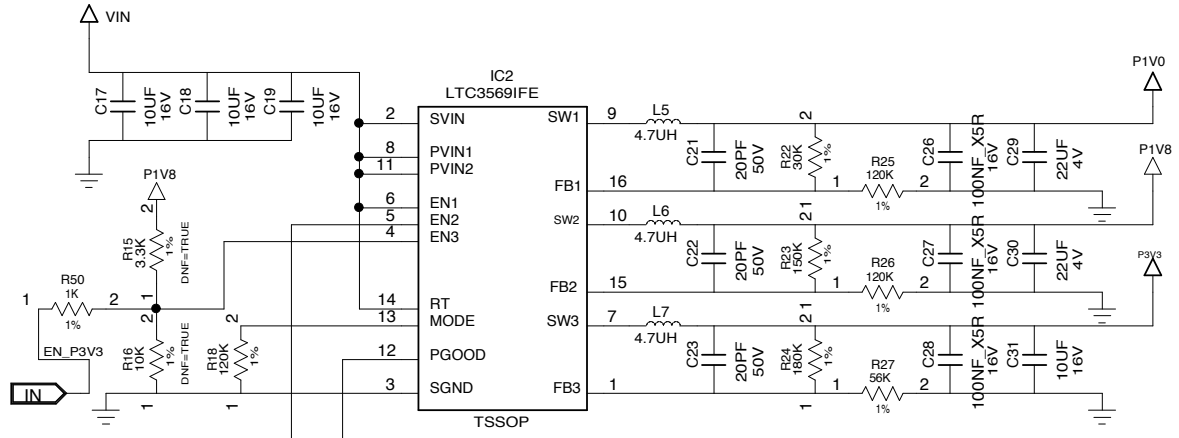
TANTALUM CAPS
ACT AS ENERGY RESERVOIR WHILE
FPGA IS CONFIGURING

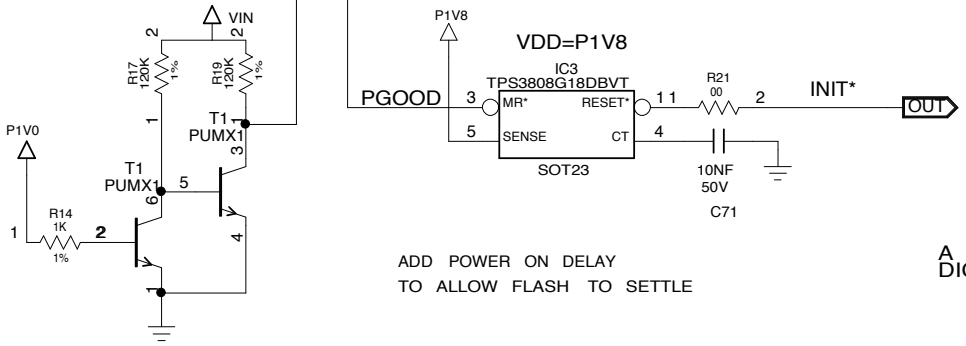


THERMISTORS FOR
POWER CONTROL

IN PUT RESISTOR
IN HTR LINE
ON DRAWBRIDGE
OF DC-DC MOAT
OMIT UNLESS NEEDED

CHANGE 180K/56K F/B RESISTORS
CHECK GROUND/POWER CONNECTIONS



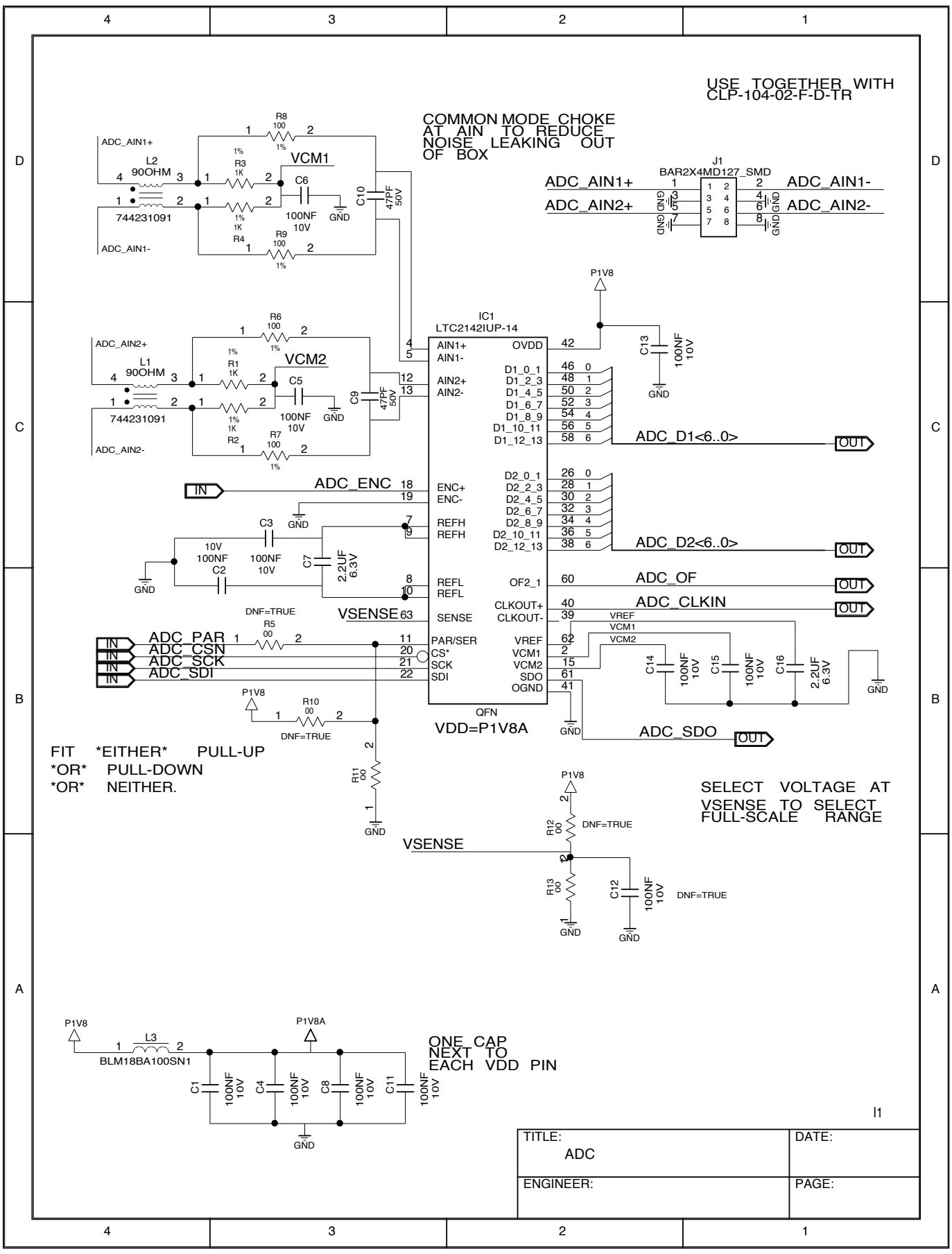


ADD POWER ON DELAY
TO ALLOW FLASH TO SETTLE

A DUMB COPY OF
DIGILENT S7 POWER

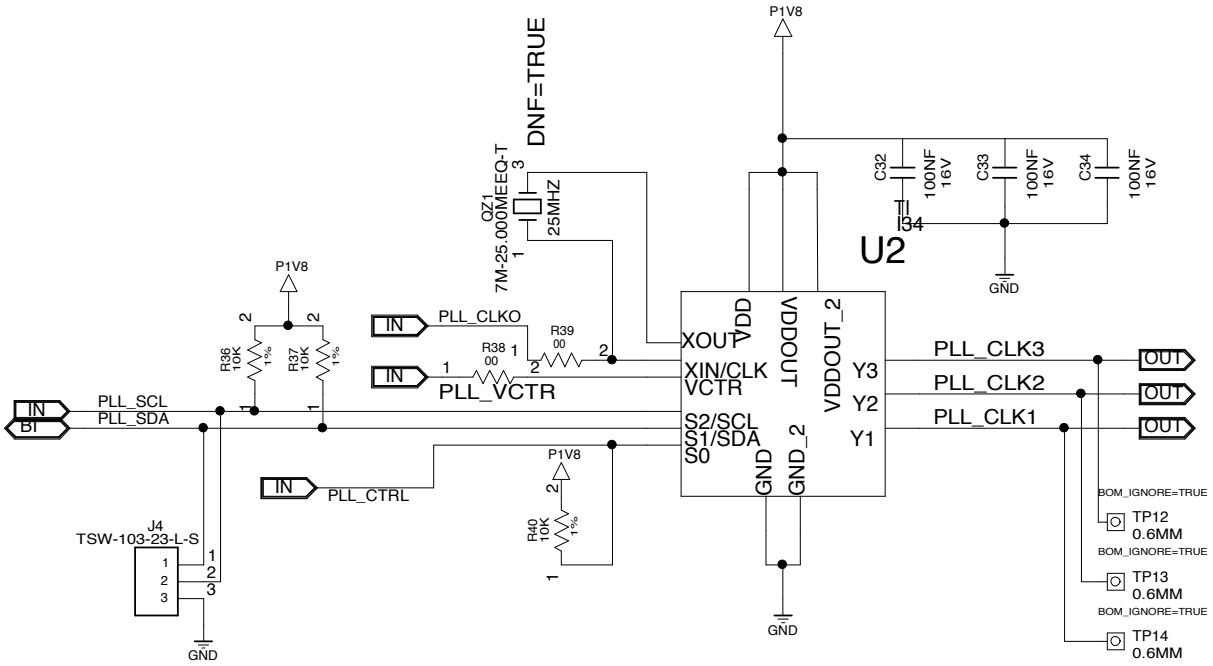
I1

TITLE: POWER SUPPLY	DATE: JUNE 21
ENGINEER: D.CUSSANS	PAGE:


USE TOGETHER WITH CLP-104-02-F-D-TR
COMMON MODE CHOKE AT AIN TO REDUCE NOISE LEAKING OUT OF BOX
J1
BAR2X4MD127_SMD
ADC_AIN1+
ADC_AIN2+
ADC_AIN1-
ADC_AIN2-
VCM1
VCM2
L1
L2
90OHM
744231091
R1
R2
R3
R4
R6
R7
R8
R9
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
100NF 10V
47PF 50V
2.2UF 6.3V
GND
IC1
LTC2142IUP-14
AIN1+
AIN1-
AIN2+
AIN2-
OVDD
P1V8
D1_0_1
D1_2_3
D1_4_5
D1_6_7
D1_8_9
D1_10_11
D1_12_13
ADC_D1<6..0>
D2_0_1
D2_2_3
D2_4_5
D2_6_7
D2_8_9
D2_10_11
D2_12_13
ADC_D2<6..0>
ADC_ENC
ENC+
ENC-
REFH
REFL
OF2_1
ADC_OF
CLKOUT+
CLKOUT-
ADC_CLKIN
VREF
VCM1
VCM2
SENSE
VSENSE
PAR/SER
CS*
SCK
SDI
SDO
OGND
ADC_SDO
ADC_PAR
ADC_CSN
ADC_SCK
ADC_SDI
IN
OUT
DNF=TRUE
R5
R10
R11
R12
R13
QFN
VDD=P1V8A
FIT *EITHER* PULL-UP *OR* PULL-DOWN *OR* NEITHER.
SELECT VOLTAGE AT VSENSE TO SELECT FULL-SCALE RANGE
P1V8A
L3
BLM18BA100SN1
ONE CAP NEXT TO EACH VDD PIN
I1
TITLE:
ADC
DATE:
ENGINEER:
PAGE:

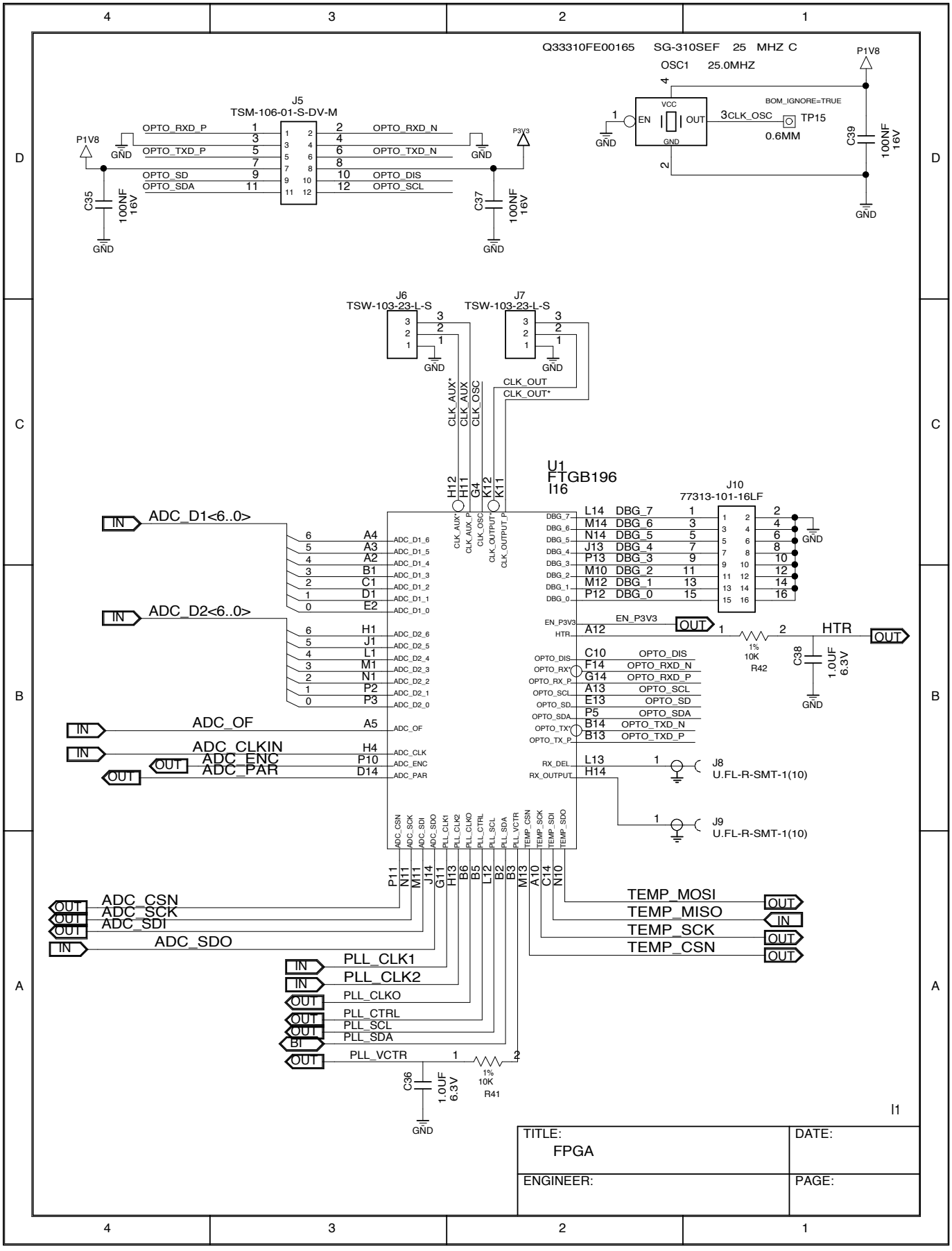
ASSEMBLE CRYSTAL AND CONNECT VCTR
AND OMIT LINK TO EXTERNAL CLOCK FOR VXCO.

FIT LINK TO EXTERNAL CLOCK AND OMIT CRYSTAL
AND LINK TO CLK_PLL FOR USE AS CLOCK BUFFER/GEN



I1

TITLE: PLL	DATE:
ENGINEER:	PAGE:


Q33310FE00165 SG-310SEF 25 MHZ C
OSC1 25.0MHZ
P1V8
VCC
EN
OUT
GND
3CLK_OSC
BOM_IGNORE=TRUE
TP15
0.6MM
C39
100NF
16V
J5
TSM-106-01-S-DV-M
OPTO_RXD_P
OPTO_TXD_P
OPTO_SD
OPTO_SDA
OPTO_RXD_N
OPTO_TXD_N
OPTO_DIS
OPTO_SCL
P3V3
C35
C37
J6
TSW-103-23-L-S
J7
TSW-103-23-L-S
CLK_AUX*
CLK_AUX
CLK_OSC
CLK_OUT
CLK_OUT*
U1
FTGB196
I16
J10
77313-101-16LF
DBG_7
DBG_6
DBG_5
DBG_4
DBG_3
DBG_2
DBG_1
DBG_0
EN_P3V3
HTR
R42
C38
1.0UF
6.3V
ADC_D1<6..0>
ADC_D2<6..0>
ADC_OF
ADC_CLKIN
ADC_ENC
ADC_PAR
OPTO_RX*
OPTO_RX_P
OPTO_TX*
OPTO_TX_P
RX_DEL
RX_OUTPUT
J8
U.FL-R-SMT-1(10)
J9
U.FL-R-SMT-1(10)
ADC_CSN
ADC_SCK
ADC_SDI
ADC_SDO
TEMP_MOSI
TEMP_MISO
TEMP_SCK
TEMP_CSN
PLL_CLK1
PLL_CLK2
PLL_CLKO
PLL_CTRL
PLL_SCL
PLL_SDA
PLL_VCTR
R41
C36
I1
TITLE:
FPGA
DATE:
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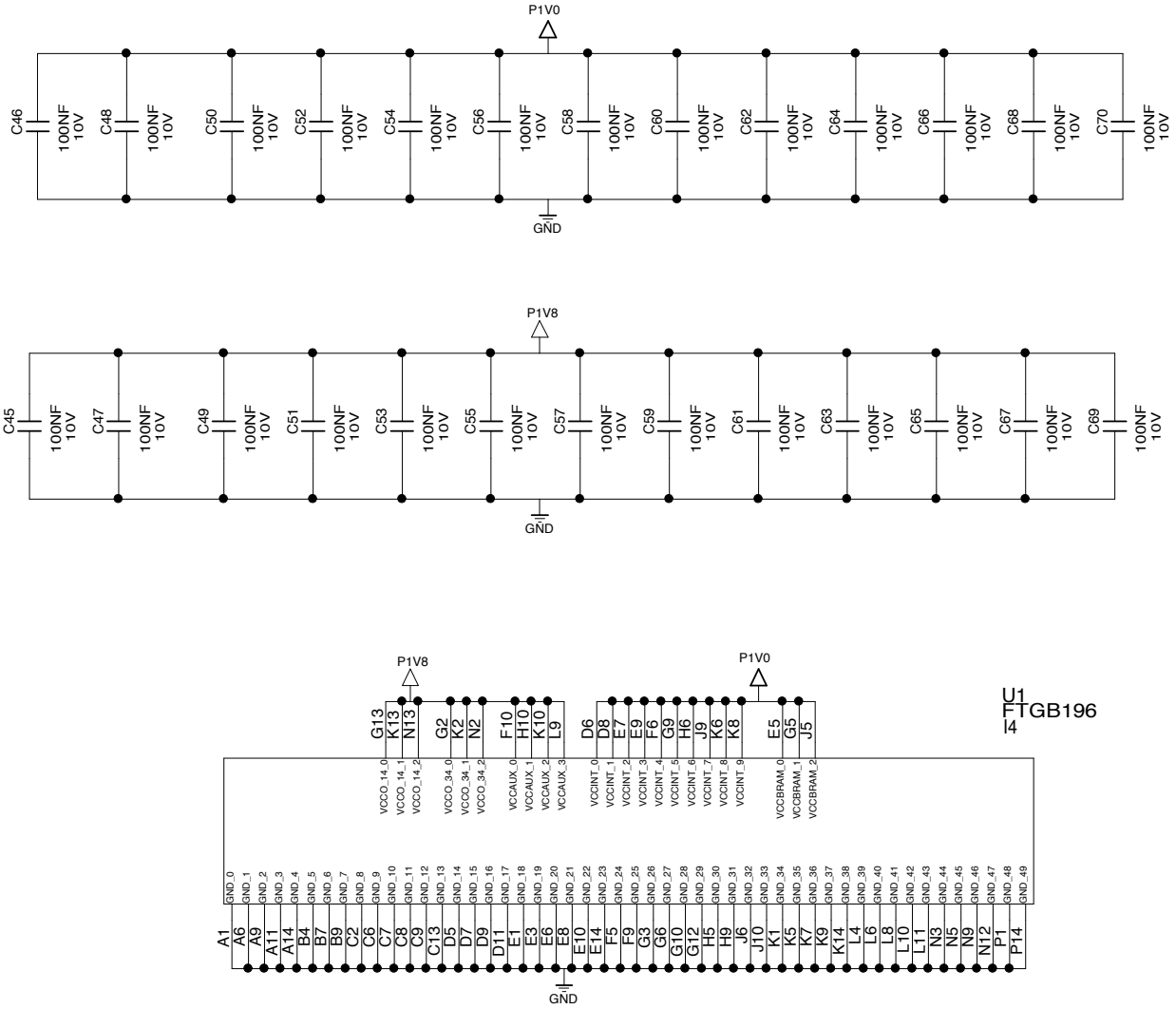
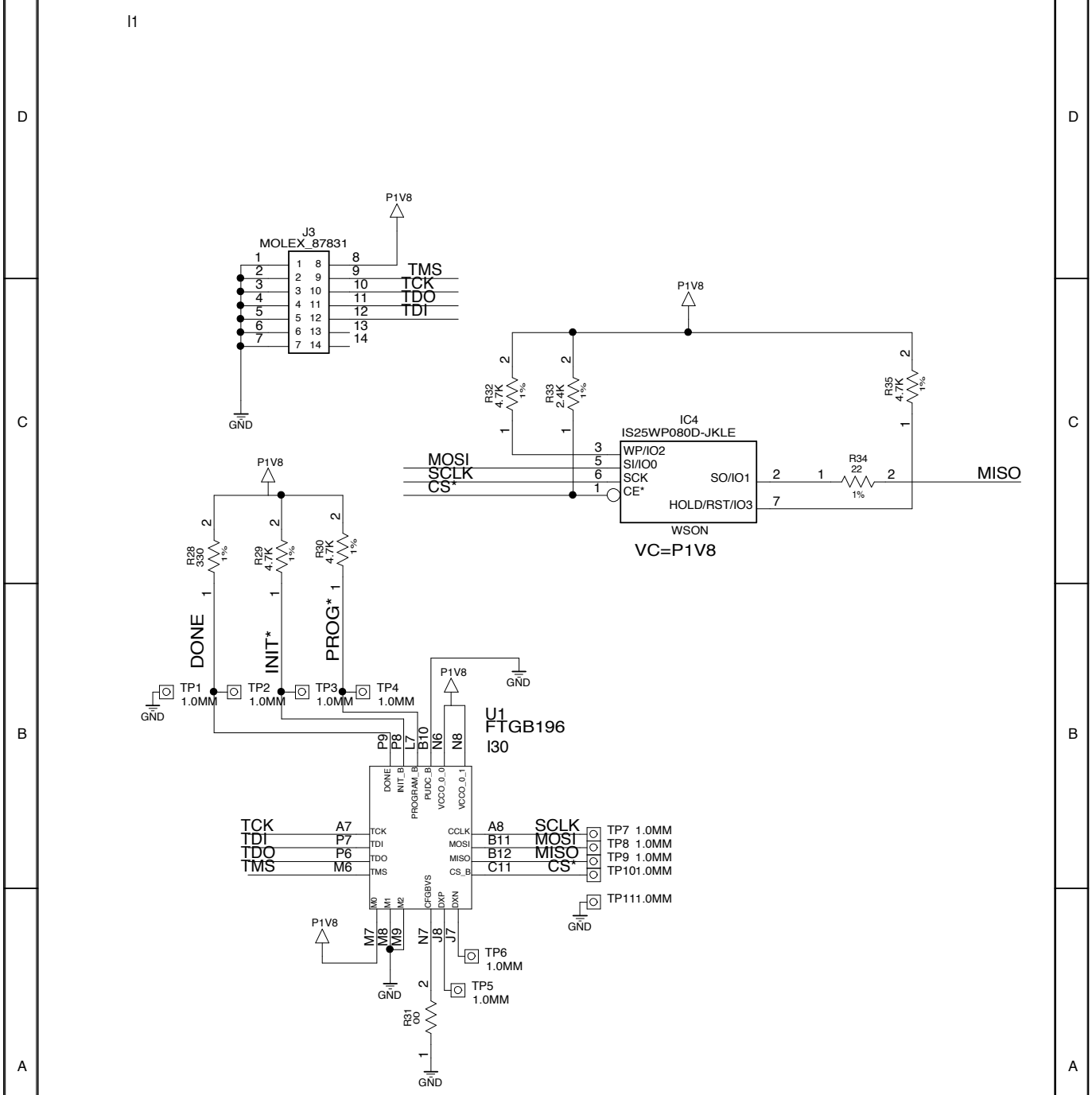
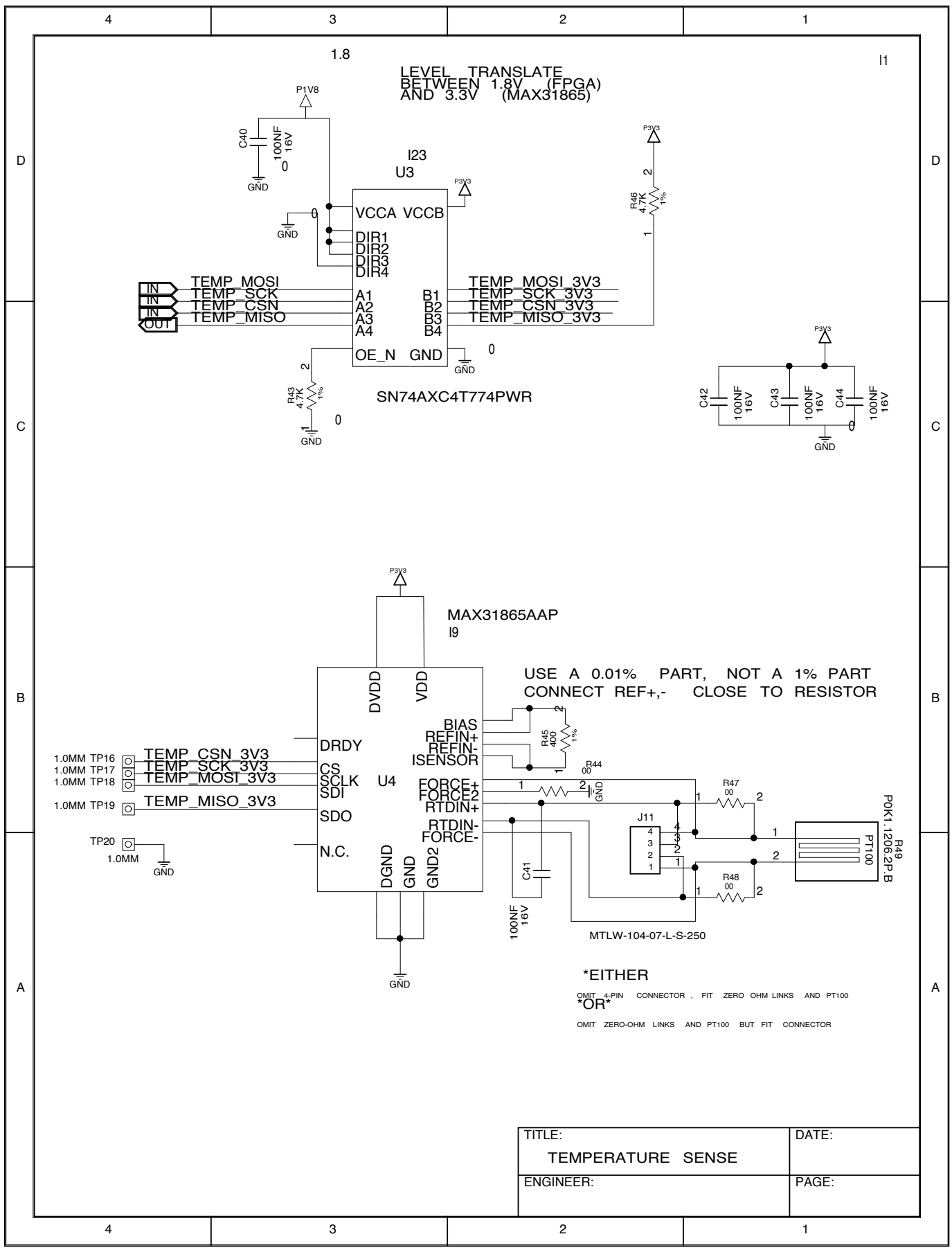


TITLE: FPGA POWER	DATE:
ENGINEER:	PAGE:


I1
P1V8
J3
MOLEX_87831
TMS
TCK
TDO
TDI
GND
R32 4.7K 1%
R33 2.4K 1%
R35 4.7K 1%
IC4
IS25WP080D-JKLE
WP/IO2
SI/IO0
SCK
CE*
SO/IO1
HOLD/RST/IO3
WSON
MOSI
SCLK
CS*
MISO
R34 22 1%
VC=P1V8
R28 330 1%
R29 4.7K 1%
R30 4.7K 1%
DONE
INIT*
PROG*
TP1 1.0MM
TP2 1.0MM
TP3 1.0MM
TP4 1.0MM
U1
FTGB196
I30
DONE
INIT_B
PROGRAM_B
PUDC_B
VCCO_0_0
VCCO_0_1
TCK
TDI
TDO
TMS
CCLK
MOSI
MISO
CS_B
SCLK
MISO
CS*
TP7 1.0MM
TP8 1.0MM
TP9 1.0MM
TP10 1.0MM
TP11 1.0MM
M0
M1
M2
CFGBVS
DXP
DXN
TP6 1.0MM
TP5 1.0MM
R31 00
TITLE:
FPGA CONFIGURATION
DATE:
ENGINEER:
PAGE:


1.8
LEVEL TRANSLATE
BETWEEN 1.8V (FPGA)
AND 3.3V (MAX31865)
I1
P1V8
C40
100NF
16V
GND
I23
U3
P3V3
VCCA VCCB
DIR1
DIR2
DIR3
DIR4
TEMP_MOSI
TEMP_SCK
TEMP_CSN
TEMP_MISO
A1
A2
A3
A4
B1
B2
B3
B4
TEMP_MOSI_3V3
TEMP_SCK_3V3
TEMP_CSN_3V3
TEMP_MISO_3V3
OE_N GND
R46
4.7K
1%
R43
4.7K
1%
SN74AXC4T774PWR
C42
C43
C44
100NF
16V
MAX31865AAP
I9
DVDD
VDD
DRDY
CS
SCLK
SDI
SDO
N.C.
DGND
GND
GND2
BIAS
REFIN+
REFIN-
ISENSOR
FORCE+
FORCE2
RTDIN+
RTDIN-
FORCE-
U4
TEMP_CSN_3V3
TEMP_SCK_3V3
TEMP_MOSI_3V3
TEMP_MISO_3V3
1.0MM TP16
1.0MM TP17
1.0MM TP18
1.0MM TP19
TP20
1.0MM
USE A 0.01% PART, NOT A 1% PART
CONNECT REF+,- CLOSE TO RESISTOR
R45
400
1%
R44
00
R47
00
R48
00
J11
MTLW-104-07-L-S-250
P0K1.1206.2P.B
PT100
R49
C41
100NF
16V
*EITHER
OMIT 4-PIN CONNECTOR , FIT ZERO OHM LINKS AND PT100
OR
OMIT ZERO-OHM LINKS AND PT100 BUT FIT CONNECTOR
TITLE:
TEMPERATURE SENSE
DATE:
ENGINEER:
PAGE: