Journal of Instrumentation

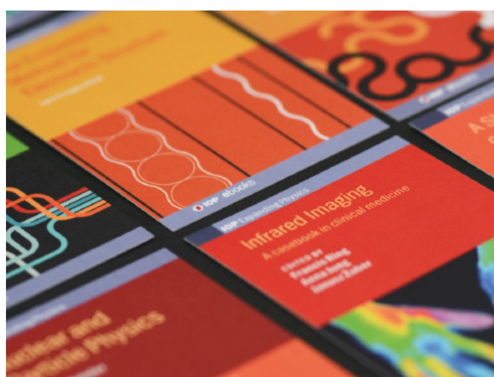
Evaluation and lifetime study of a cryogenic SAR ADC for HPGe detectors in low-background physics experiments

To cite this article: F. Liu *et al* 2019 *JINST* **14** T07005

View the article online for updates and enhancements.

Recent citations

- Cryogenic Bandgap Reference Circuit With Compact Model Parameter Extraction of MOSFETs and BJTs for HPGe Detectors
Feng Liu *et al*
- Development of the full-chain cryogenic readout electronics for the point-contact HPGe detectors
Feng Liu *et al*



IOP ebooks™

Bringing together innovative digital publishing with leading authors from the global scientific community.

Start exploring the collection–download the first chapter of every title for free.

This content was downloaded from IP address 131.225.82.153 on 04/02/2021 at 19:36

Jinst

PUBLISHED BY IOP PUBLISHING FOR SISSA MEDIALAB

RECEIVED: *May 27, 2019*
ACCEPTED: *July 4, 2019*
PUBLISHED: *July 22, 2019*

TECHNICAL REPORT

Evaluation and lifetime study of a cryogenic SAR ADC for HPGe detectors in low-background physics experiments

F. Liu, T. Xue, Z. Deng[1] and Y. Liu

Key Laboratory of Particle & Radiation Imaging, Ministry of Education, Qinghuayuan Street No. 1, Beijing, 100084, China
Department of Engineering Physics, Tsinghua University, Qinghuayuan Street No. 1, Beijing, 100084, China

E-mail: dengz@mail.tsinghua.edu.cn

ABSTRACT: Cryogenic ADCs can be a promising solution for ton-scale HPGe detectors for dark matter and neutrino-less double beta decay experiments for improved signal integrity and decreased cables and penetrations. This paper presents the characterization and lifetime study of a SAR ADC at liquid nitrogen temperature for CDEX and future LEGEND experiments. The chip is implemented in standard 65 nm CMOS process. It works well at liquid nitrogen temperature with proper biasing. The power consumptions of the SAR ADC are measured to be 6.1 mW and 6.5 mW at 300 K and 77 K respectively. The ENOB of the ADC is decreased from 8.94 bits at 300 K to 8.72 bits at 77 K at 100 MS/s sampling rate. For reasons of efficiency and economics, the lifetime of the cryogenic operation circuits must be in excess tens of years. Hot carrier effect (HCE) is the dominate mechanism that substantially affects the device lifetime at cryogenic temperature and the accelerated lifetime study has also been conducted. The predicted lifetime is $\sim 5.7 \times 10^4$ years at 1.24 V operation at 77 K, which means the ADC is cryogenic qualified to remain outside of the HCE degradation.

KEYWORDS: Analogue electronic circuits; Cryogenics; Electronic detector readout concepts (solid-state); Front-end electronics for detector readout

[1]Corresponding author.

© 2019 IOP Publishing Ltd and Sissa Medialab

https://doi.org/10.1088/1748-0221/14/07/T07005

2019 JINST 14 T07005

Contents

1 Introduction **1**

2 The SAR ADC **2**

3 ADC characterization at cryogenic temperature **3**
3.1 The cryogenic test setup 3
3.2 The power consumption 4
3.3 The ENOB performance 4
3.4 The non-linearity performance 5

4 Lifetime study at cryogenic temperature **6**
4.1 The test procedure 6
4.2 Lifetime prediction 8

5 Conclusions **10**

1 Introduction

The HPGe (High Purity Germanium) detectors have been used for dark matter search CDEX (China Dark matter EXperiment) [1], CoGeNT [2] and neutrino experiments GERDA [3], MAJORANA [4] due to excellent energy resolution and low noise. HPGe detectors are read out by charge sensitive preamplifiers and analogue shapers with optimum shaping times. For low-background experiments both amplitudes and signal shapes need to be measured. The outputs of the preamplifiers are directly sampled and digitized by high-speed, high-resolution and low-power ADCs (Analog to Digital Converters). The entire pulse shape is recorded for distinguishing the surface and bulk events, or the single-site and multi-site events [5], which helps background reduction. To optimize low noise, the preamplifiers or at least the input transistors of the preamplifiers have to be mounted close to the HPGe detectors and operate at cryogenic temperature. Various cryogenic preamplifiers have been developed [6, 7]. Meanwhile cryogenic ADCs are rarely reported for HPGe detectors in current experiments [1–4]. In current experiments the transmission of analogue outputs of the preamplifiers to the room temperature digital section is performed through long shield cables, resulting in electronic interference and increasing the material budget. In order to improve the detection sensitivity, ton-scale HPGe detectors have been proposed in the next generation experiment LEGEND (The Large Enriched Germanium Experiment for Neutrinoless Double Beta Decay) with background level lowered by at least one order of magnitude [8]. Cable reduction and less penetrations benefit from digitization and multiplexing at cryogenic temperature, especially for the detectors with thousands of channels. Several techniques are under development including cryogenic ADCs and SCA (Switched Capacitor Array) based waveform recorders with multiplexed outputs [9, 10].

2019 JINST 14 T07005

The paper firstly presents the performance of a SAR (Successive Approximation Register) ADC at cryogenic temperature. In general, CMOS transistor benefits from lower thermal noise and lower leakage current and faster speed of transistors at cryogenic tempatature [11, 12]. Unfortunately commercial ADCs are not designed for cryogenic operation and their performance can be dramatically degraded or may fail to work at low temperature [13, 14]. In addition the hot carrier effect (HCE) will deteriorate the lifetime of transistors at low temperature, especially when the devices scale down [15–17]. The lifetime study of the ADC will also be presented in this paper. Detailed test setup and results will be discussed in the following sections.

2 The SAR ADC

SAR architectures are widely used because of its low power consumption, compact size, medium to high resolution and speed [18–21]. This architecture is suitable for cryogenic operation as it mostly consists of passive components and CMOS logic modules, which are functional at low temperature. Several cryogenic SAR ADCs have been developed in mega samples per second sampling rate and the opearting temperature could be down to 4 K [18, 19].

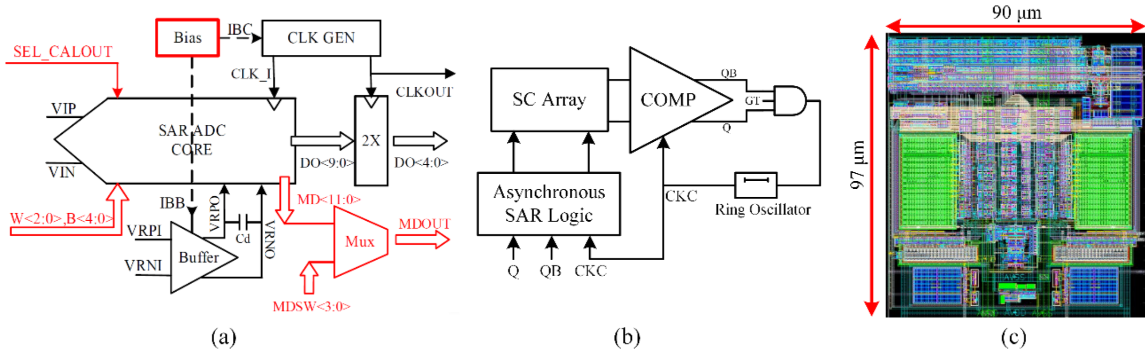


Figure 1. (a) The architecture of the SAR ADC [22]. The bias module sets the currents of the ADC core, the reference buffer and the clock generator module. It can be adjusted externally for cryogenic operation. (b) The architecture of the SAR ADC core. (c) The layout of the SAR ADC core circuits with the size of $90\,\mu m \times 97\,\mu m$.

Figure 1a shows the simplified architecutre of the SAR ADC used for this study [22]. The ADC core consists of a sampling and hold (S/H) stage, a comparator, a digital-analog converter (DAC), and control logics units, as shown in figure 1b. Besides, auxiliary modules are also integrated in the prototype chip. The master bias module sets the currents of the analog circuits in ADC core, the reference buffer and the clock generator module. Proper biasing is the key for cryogenic operations and it can be adjusted externally. In the DAC the values of the capacitor array can be digitally fine-tuned to compensate the non-linearity caused by the capacitor mismatch. On-chip calibration has been integrated to generate the fine-tune values, including a ramp signal generator and logic units for code density statistics. The calibration procedure can also be done off-chip using an external signal generator. In our tests the on-chip calibration module does not work well at cryogenic temperature and all the tests were done by off-chip calibration. Figure 1c shows the layout of the SAR ADC core circuits with the size of $90\,\mu m \times 97\,\mu m$.

The main characteristics of the SAR ADC are summarized in table 1.

2019 JINST 14 T07005

Table 1. The Main Characteristics of the SAR ADC.

Parameter	Performance
Architecture	SAR ADC with calibration
Sample rate	100 MS/s
Resolution	10 bits
Process	65 nm CMOS
Power supply	1.2 V
Power consumption (whole)	5 mW
Layout size	90 µm × 97 µm

2019 JINST 14 T07005

3 ADC characterization at cryogenic temperature

3.1 The cryogenic test setup

The cryogenic test setup for the SAR ADC is shown in figure 2. A dedicated front-end board is developed. The ADC is mounted in the front-end board along with other screened components which can work at 77 K. The front-end board is immersed into liquid nitrogen (LN) Dewar during the testing. A back-end board is built to power and configure the ADC through Micro-coax cables (Samtec). The ADC data is acquired by a FPGA evaluation board TSW1400-EVM for performance analysis. Low distortion sine wave signals are generated by the signal generator AFG3252 with band-pass filters to measure the ADC performance. A power supply (DP832) and a digital multi-meter (DMM7511) are controlled by a LabView program for supply voltage adjustment and current monitoring.

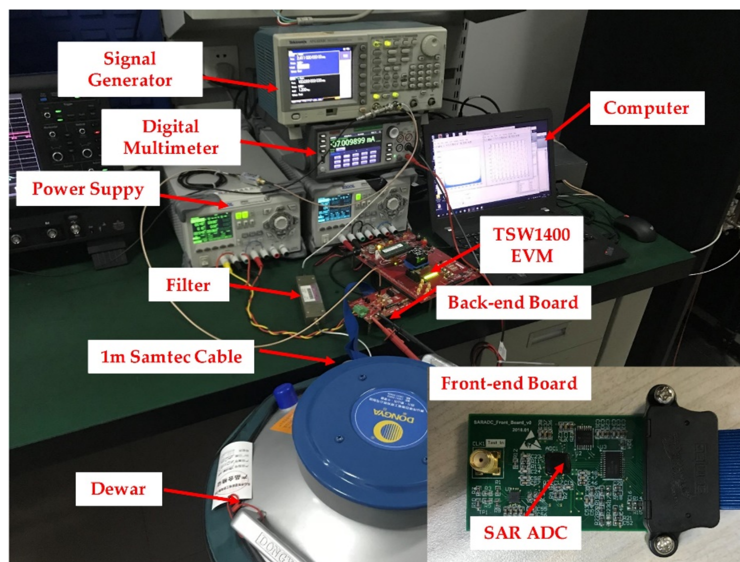


Figure 2. The cryogenic test setup for the SAR ADC. The front-end board mounted with the ADC is immersed in LN Dewar. A back-end board is built to power and configure the ADC. The digital multi-meter is used to monitor the current of power supply with the accuracy at µA level.

3.2 The power consumption

The measured master bias current decreases from 50 µA at room temperature to 37 µA at LN temperature. It is adjusted back to the designed value of 50 µA by an external resistor. Key factor to cryogenic operation circuits is proper biasing and the bias current of 50 µA is used for all the tests below unless otherwise specified.

The power consumption of the ADC core is about 1/4 of the SAR ADC according to simulation, as shown in figure 3a. Figure 3b shows the measured power consumptions of the whole SAR ADC over different sampling rates at room and LN temperatures. The prototype chip needs the power supply of 1.3V to work at 100MS/s sampling rate at room temperature. The power consumption of SAR ADC increases from 6.1 mW at room temperature to 6.5 mW at LN temperature at 50 MS/s sampling rate. The increase rate of the power consumption over the sampling rate is minor.

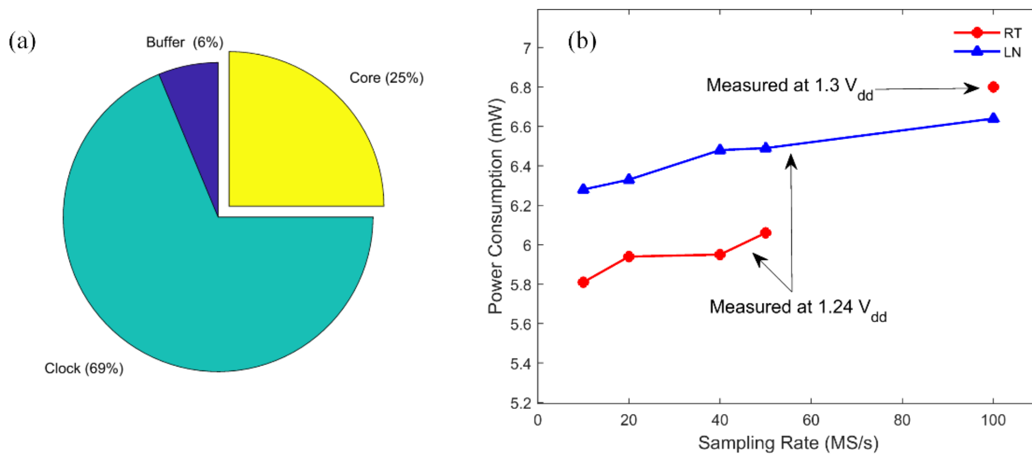


Figure 3. (a) The distribution of the SAR ADC power consumption at 1.24 V power supply. (b) The power consumptions of the whole SAR ADC over different sampling rates at room and LN temperatures.

3.3 The ENOB performance

The performance of the SAR ADC has been evaluated at both room and LN temperatures. The sine wave signals of 2.4 MHz are sampled by the ADC and the output spectrum is obtained by the Fast Fourier Transform (FFT) of 1 million output samples. Figure 4 shows the typical output spectrums of the ADC at room and LN temperatures at 100 MS/s sampling rate. It can be seen that the distortion floor becomes more significant at LN temperature with respect to that at room temperature. The SNDRs (Signal-to-Noise-plus-Distortion Ratios) are estimated to be 55.6 dB at room and 54.2 dB at LN temperatures. The corresponding ENOBs (Effective Number of Bits) are 8.94 bits and 8.72 bits respectively: $ENOB = [SNDR\,(dB) - 1.76]\,/6.02$.

Figure 5a shows the measured ENOBs of the SAR ADC at room and LN temperatures at different sampling rates. At the sampling rates below 20 MS/s, the ENOBs are almost the same (9.05 bits) at room and LN temperatures with calibration. As the sampling rate increased from 20 MS/s to 100 MS/s, the ENOB smoothly decreases about 0.1-bit at room temperature. In comparison the ENOB sharply decreases by 0.2-bit at 40 MS/s and keeps almost constant up to 100 MS/s at LN temperature. This is due to the insufficient settling time of the DAC. As temperature decreased,

2019 JINST 14 T07005

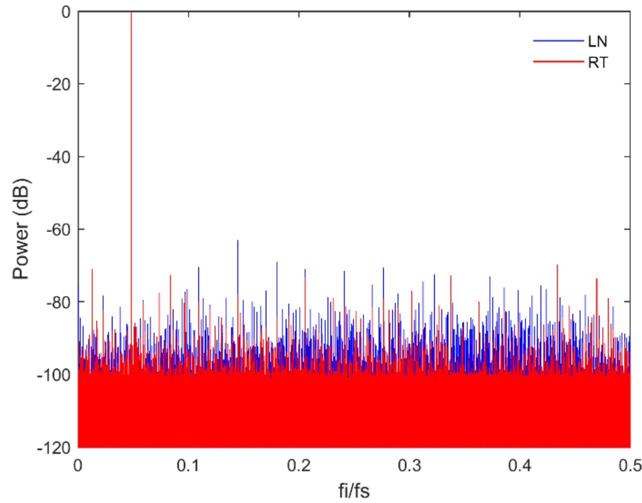


Figure 4. The output spectrums of the ADC at room and LN temperatures at 100 MS/s sampling rate.

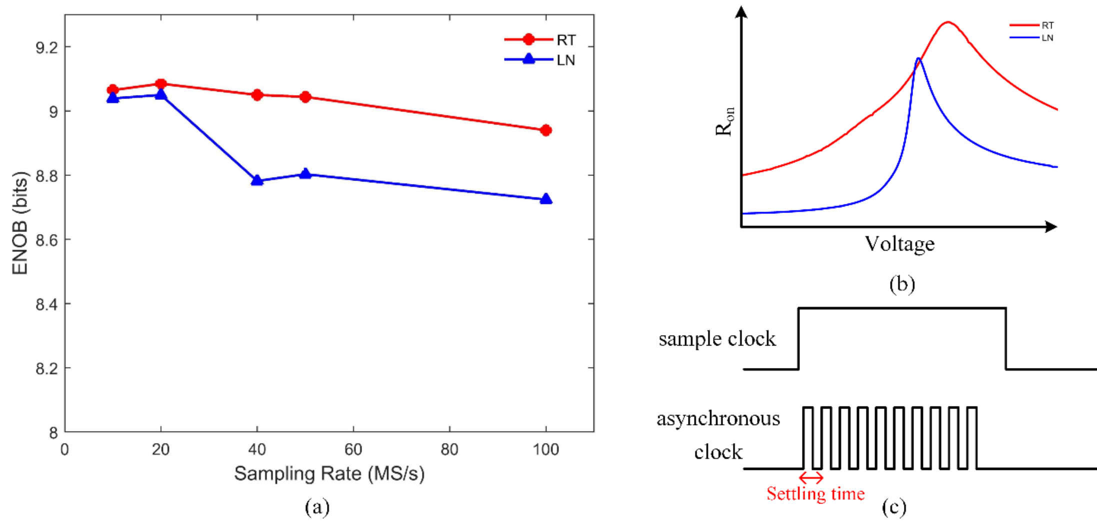


Figure 5. (a) The ENOB performance of the SAR ADC at 300 K and 77 K at different sampling rates with calibration; (b) The simulated switch resistance with input voltage; (c) The schematic of the sample clock and asynchronous clock.

the threshold and the mobility of the MOSFETs increase, resulting in larger variation of the switch resistance and hence the RC time constant, as shown in figure 5b. Besides, this SAR ADC require 10 comparison cycles to complete each conversion, as shown in figure 5c, the frequency of the ring oscillator for the asynchronous clock also increases and the time window generated for DAC settling becomes shorter.

3.4 The non-linearity performance

The non-linearity performance is measured using the dynamic test method [23]. Figure 6 shows the differential nonlinearities (DNLs) and the integral nonlinearities (INLs) for different temperatures measured at 100 MS/s sampling rate. Both DNLs and INLs at LN temperature become worse than

2019 JINST 14 T07005

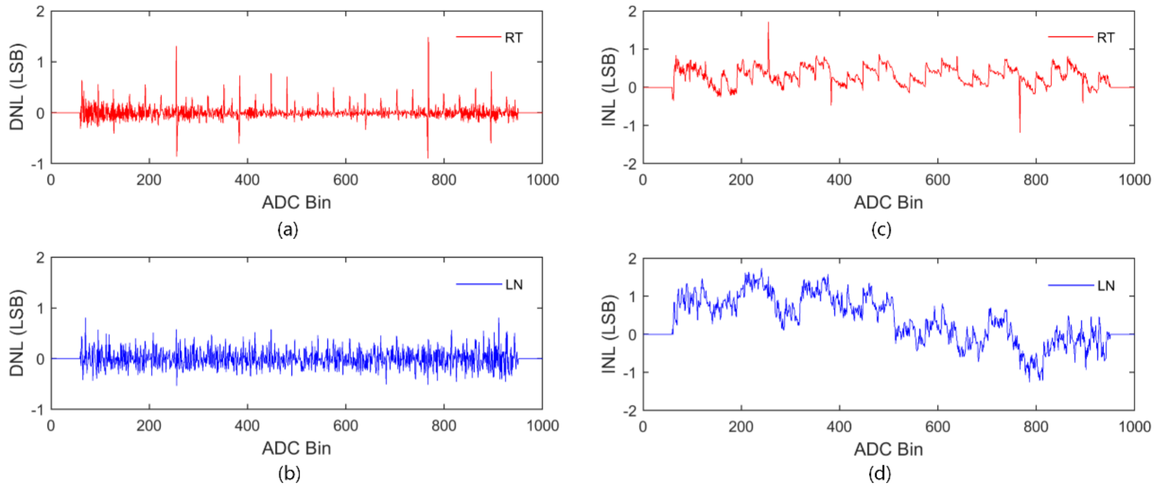


Figure 6. The measured DNLs of the SAR ADC at (a) room and (b) LN temperatures, and the measured INLs of the SAR ADC at (c) room and (d) LN temperatures. All the measurements are done with calibration and at 100 MS/s sampling rate.

those at room temperature, except for a few spikes at specific ADC bins. The INLs are less than 2 LSB at room and LN temperatures.

4 Lifetime study at cryogenic temperature

HCE is the dominate mechanism that substantially affect the device lifetime at cryogenic temperature. Other mechanisms are temperature dependent and become negligible at cryogenic temperature [24].

Most components of the SAR ADC work in dynamic operation. According to the quasi-static model [25], HCE can still be accelerated by increasing the power supply voltage excess the normal operation value. The model of the lifetime acceleration and prediction has been verified for various CMOS processes and circuits at cryogenic temperature. As a rule of thumb, the lifetime will be increased by an order of magnitude as the power supply reduces roughly 6% [26–28].

4.1 The test procedure

Figure 7 shows the flow chart of the stress test at LN temperature. At the beginning of the stress test, the ENOBs and the power supply currents of the SAR ADC at normal voltage (I_{vdd_n}) and stress voltage (I_{vdd_s}) are measured as the initial performance. Then the ADC is applied with the stress voltage and the corresponding performance will be monitored until a defined degradation criteria is reached. The total accumulated stress time will be recorded as the lifetime at the specific stress voltage.

The ENOB and the power supply currents at normal and stress voltages are monitored during the stress test. These parameters are measured at different stress time intervals, which vary from 5 minutes to 12 hours as the ADC performance deteriorated following a power law even down to submicron process [27]. Three stress voltages of 1.95 V, 2.1 V, and 2.2 V are applied to different fresh samples.

2019 JINST 14 T07005

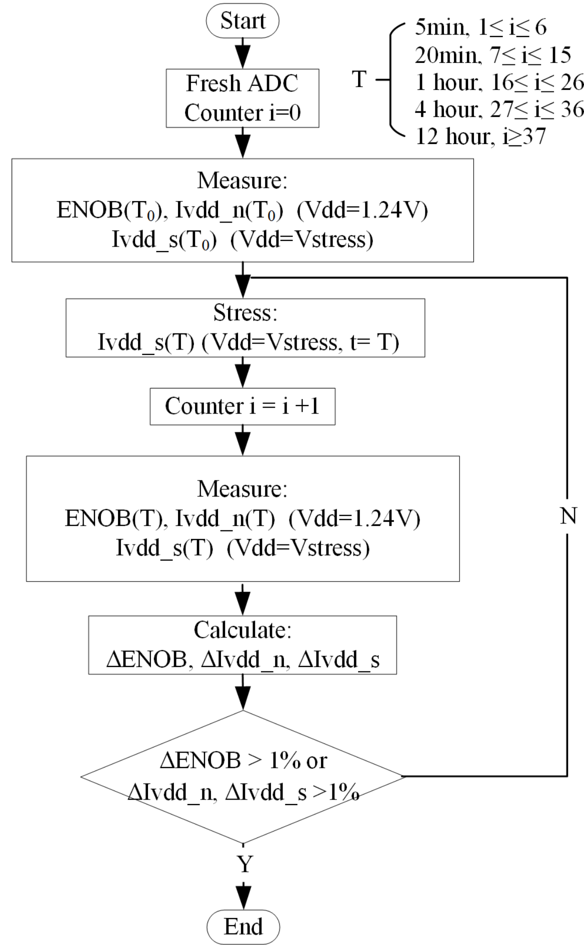


Figure 7. The flow chart of the stress test. First the initial performance is measured. Then the ADC is applied with the stress voltage and the corresponding performance will be monitored. Finally, the loop continues until the degradation criteria is reached.

The relative degradations of the ENOB and the power supply currents at normal and stress voltages are defined as:

$$\frac{\Delta \mathrm{ENOB}}{\mathrm{ENOB}} = \frac{\mathrm{ENOB}\,(\mathrm{T}_0) - \mathrm{ENOB}\,(\mathrm{T})}{\mathrm{ENOB}\,(\mathrm{T}_0)} \tag{4.1}$$

$$\frac{\Delta \mathrm{I}_{\mathrm{vdd_n}}}{\mathrm{I}_{\mathrm{vdd_n}}} = \frac{\mathrm{I}_{\mathrm{vdd_n}}\,(\mathrm{T}_0) - \mathrm{I}_{\mathrm{vdd_n}}\,(\mathrm{T})}{\mathrm{I}_{\mathrm{vdd_n}}\,(\mathrm{T}_0)} \tag{4.2}$$

$$\frac{\Delta \mathrm{I}_{\mathrm{vdd_s}}}{\mathrm{I}_{\mathrm{vdd_s}}} = \frac{\mathrm{I}_{\mathrm{vdd_s}}\,(\mathrm{T}_0) - \mathrm{I}_{\mathrm{vdd_s}}\,(\mathrm{T})}{\mathrm{I}_{\mathrm{vdd_s}}\,(\mathrm{T}_0)} \tag{4.3}$$

where T is the accumulated stress time, and T_0 is the initial time.

In order to find the proper degradation criteria for the lifetime study, a test run has been conducted using 1.95 V stress voltage with the accumulated stress time of 200 hours. The degradations of the ENOBs running at 100 MS/s sampling rate are shown in figure 8. Both the ENOBs with and without calibration decrease overall with the stress time. However, the non-monotonic behavior can be clearly seen and hence ENOBs are not suitable as the end-of-lifetime criteria. Figure 9 shows the

2019 JINST 14 T07005

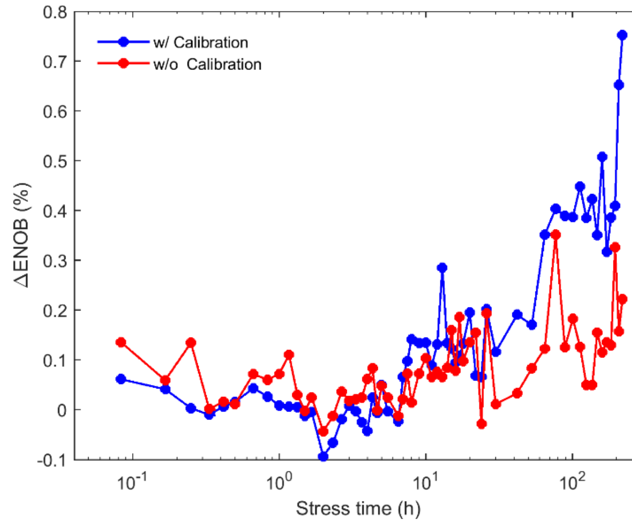


Figure 8. The relative degradations of the ENOBs over stress time at LN temperature. The ENOBs are measured at 100 MS/s sampling rate with and without calibration. The stress voltage is set to 1.95 V.

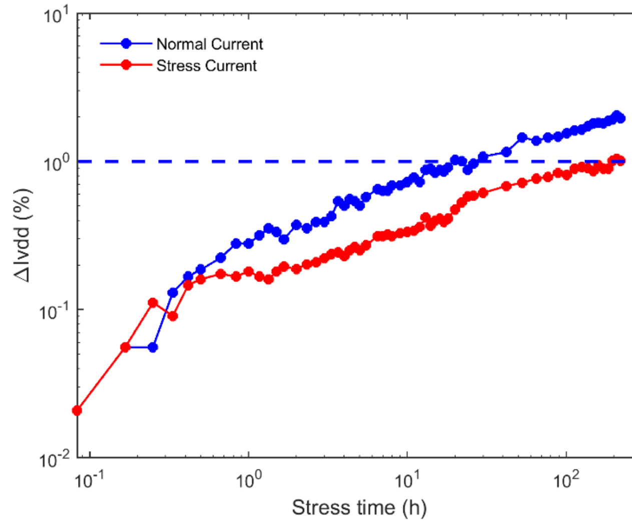


Figure 9. The relative degradations of the normal current (I_{vdd_n}) and the stress current (I_{vdd_s}) over stress time at LN temperature. The stress voltage is set to 1.95 V.

2019 JINST 14 T07005

degradations of the currents at normal and stress voltages with stress time, both currents decrease monotonically with the stress time. The normal current deteriorates faster than the stress current, indicating a shorter predicted lifetime. As a conservative estimation, the 1% normal current (I_{vdd_n}) decrease is determined as the degradation criteria for the lifetime study [28].

4.2 Lifetime prediction

In order to predict the lifetime of the ADC at normal condition, individual fresh ADC samples are stressed under different stress voltages. The relative degradation of the normal currents over stress time are shown in figure 10. All the normal currents of the devices decrease consistently with the

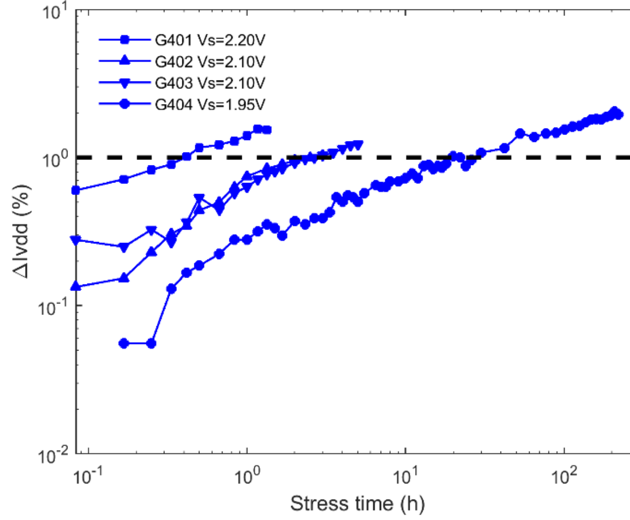


Figure 10. The relative degradations of the normal current over stress time at LN temperature for different stress voltages.

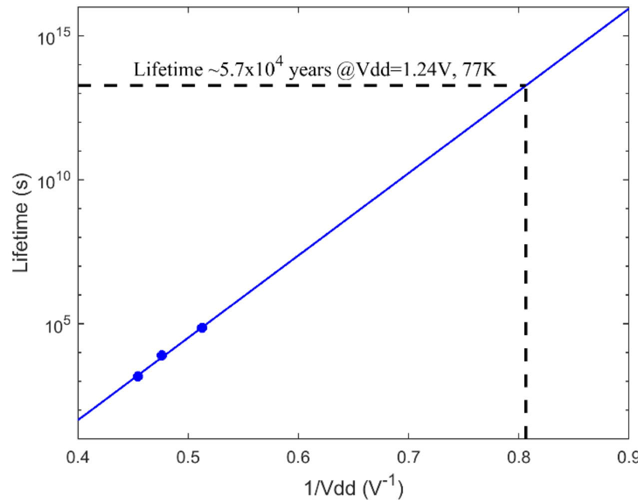


Figure 11. The lifetime extrapolation of the SAR ADC at 1.24 V normal voltage at LN temperature.

stress time. The higher stress voltage, the faster the normal current decreases with stress time. For crosscheck, two samples are stressed at the 2.1 V and the degradations of the normal currents fit quite well.

The dependence of the lifetime (τ) on the stress voltage (V_{dd}) can be described as [26, 28]:

$$\log_{10} \tau \propto 1/V_{dd} \tag{4.4}$$

Using equation (4.4), the lifetime under 1.24 V normal voltage is extrapolated to be $\sim 5.7 \times 10^4$ years at LN temperature, as shown in figure 11. As a result, the lifetime failure caused by the HCE for the SAR ADC is not a concern for the HPGe detector readout for dark matter and neutrino experiments.

2019 JINST 14 T07005

5 Conclusions

Cryogenic digitization and multiplexing can be potentially used for ton-scale HPGe detectors for low-background physics experiments. A prototype ASIC of 100 MS/s 10 bits SAR ADC in 65 nm CMOS has been evaluated at 77 K. Proper biasing at cryogenic temperature is achieved by adjusting an external resistor. The power consumption of the SAR ADC is measured to be 6.5 mW and the ENOBs of 9.0 bits and 8.7 bits are achieved at 20 MS/s and 100 MS/s at 77 K. Comparing to the performance at 300 K, the power consumption slightly increases about 0.4 mW and the ENOB is almost the same at 20 MS/s and decreases 0.2-bit at 100 MS/s. This is due to the insufficient settling time of the DAC and can be improved in the future design. Accelerated lifetime test has also been conducted and the lifetime of the SAR ADC is predicted to be $\sim 5.7 \times 10^4$ years under 1.24 V at 77 K, thus the ADC is cryogenic qualified to remain outside of the HCE degradation. The evaluation of the SAR ADC shows very promising results. However, a dedicated ADC needs to be developed with higher resolution.

Acknowledgments

The authors would like to thank Xian Gu and Fule Li at the Institute of Microelectronics, Tsinghua University for providing the ADC and for their valuable discussions and supporting during the evaluation. This work was supported by the national key research and development program under grant no. 2017YFA0402202.

References

[1] CDEX collaboration, *Introduction to the CDEX experiment*, *Front. Phys. (Beijing)* **8** (2013) 412 [arXiv:1303.0601].

[2] CoGeNT collaboration, *CoGeNT: A Search for Low-Mass Dark Matter using p-type Point Contact Germanium Detectors*, *Phys. Rev.* **D 88** (2013) 012002 [arXiv:1208.5737].

[3] GERDA collaboration, *The GERDA experiment for the search of $0\nu\beta\beta$ decay in ^{76}Ge*, *Eur. Phys. J.* **C 73** (2013) 2330 [arXiv:1212.4067].

[4] Majorana collaboration, *The Majorana Demonstrator: A Search for Neutrinoless Double-beta Decay of ^{76}Ge*, *J. Phys. Conf. Ser.* **606** (2015) 012004 [arXiv:1501.03089].

[5] T. Kröll and D. Bazzacco, *Simulation and analysis of pulse shapes from highly segmented HPGe detectors for the γ-ray tracking array MARS*, *Nucl. Instrum. Meth.* **A 463** (2001) 227.

[6] A. Pullia, F. Zocca and S. Riboldi, *A JFET-CMOS fast preamplifier for segmented germanium detectors*, *IEEE Trans. Nucl. Sci.* **55** (2008) 591.

[7] Z. Deng, L. He, F. Liu, Y. Liu, Y. Li and Q. Yue, *An ultra-low noise cryogenic CMOS charge sensitive preamplifier for large volume point-contact HPGe detectors*, 2018 *JINST* **13** P08019.

[8] LEGEND collaboration, *The Large Enriched Germanium Experiment for Neutrinoless Double Beta Decay (LEGEND)*, *AIP Conf. Proc.* **1894** (2017) 020027 [arXiv:1709.01980].

[9] S. Gao et al., *The Development of Front-End Readout Electronics for ProtoDUNE-SP LAr TPC*, PoS TWEPP-17(2017)060.

2019 JINST 14 T07005

[10] Z. Deng et al., *Development of cryogenic CMOS Readout ASICs for the Point-Contact HPGe Detectors for Dark Matter Search and Neutrino Experiments*, *J. Phys. Conf. Ser.* **834** (2017) 012004.

[11] W.F. Clark, B.E. Kareh, R.G. Pires, S.L. Titcomb and R.L.Anderson, *Low temperature CMOS — A brief review*, *IEEE Trans. Compon. Hybrids Manuf. Technol.* **15** (1992) 397.

[12] R.K. Kirschman, *Low-temperature electronics*, *IEEE Circuits Devices Mag.* **6** (1990) 12.

[13] R. Ramesham, N. Kumar, J. Mao, D. Keymeulen, R.S. Zebulum and A. Stoica, *Data converters performance at extreme temperatures*, *IEEE Aerospace Conf.* (2006) 1.

[14] F. Liu et al., *Cold Electronics System Development for ProtoDUNE-SP and SBND LAr TPC*, *IEEE Nucl. Sci. Symp. Med. Imag. Conf.* (2017) 1.

[15] C. Hu, S.C. Tam, F.C. Hsu, P.K. Ko, T.Y. Chan and K.W. Terrill, *Hot-Electron-Induced MOSFET Degradation — Model, Monitor, and Improvement*, *IEEE Trans. Electron Devices* **32** (1985) 375.

[16] J.J. Tzou, C.C. Yao, R. Cheung and H. Chan, *Hot-electron-induced MOSFET degradation at low temperatures*, *IEEE Electr. Device Lett.* **6** (1985) 450.

[17] A. Duncan, U. Ravaioli and J. Jakumeit, *Full-band Monte Carlo investigation of hot carrier trends in the scaling of metal-oxide-semiconductor field-effect transistors*, *IEEE Trans. Electron Devices* **45** (1998) 867.

[18] Y. Creten, P. Merken, W. Sansen, R. Mertens and C. Van Hoof, *A cryogenic ADC operating down to 4.2 K*, *IEEE Int. Solid-State Circuits Conf.* (2007) 468.

[19] B. Okcan, P. Merken, G. Gielen and C. Van Hoof, *A cryogenic analog to digital converter operating from 300 K down to 4.4 K*, *Rev. Sci. Instrum.* **81** (2010) 024702.

[20] C.C. Liu et al., *A 10-bit 50-MS/s SAR ADC with a monotonic capacitor switching procedure*, *IEEE J. Solid-State Circuits* **45** (2010) 731.

[21] H. Xu et al., *A 78.5dB-SNDR radiation- and metastability-tolerant two-step split SAR ADC operating up to 75MS/s with 24.9mW power consumption in 65nm CMOS*, *IEEE Int. Solid-State Circuits Conf.* (2017) 476.

[22] X. Gu, X. He and F. Li, *A calibration technique for SAR ADC based on code density test*, *IEEE Int. Conf. ASIC* (2015) 1.

[23] M.V. Bossche, J. Schoukens and J. Renneboog, *Dynamic testing and diagnostics of A/D converters*, *IEEE Trans. Circuits Syst.* **33** (1986) 775.

[24] J. Srinivasan, S.V. Adve, P. Bose and J.A. Rivers, *The impact of technology scaling on lifetime reliability*, *IEEE Int. Conf. Dependable Systems and Networks* (2004) 177.

[25] K.N. Quader. E.R. Minami, W. Huang, P.K. Ko and C. Hu, *Hot-carrier reliability design guidelines for CMOS logic circuits*, *IEEE J. Solid-State Circuits* **29** (1994) 253.

[26] S. Li, J. Ma, G. De Geronimo, H. Chen and V. Radeka, *LAr TPC Electronics CMOS Lifetime at 300 K and 77 K and Reliability Under Thermal Cycling*, *IEEE Trans. Nucl. Sci.* **60** (2013) 4737.

[27] J.R. Hoff et al., *Cryogenic Lifetime Studies of 130 nm and 65 nm nMOS Transistors for High-Energy Physics Experiments*, *IEEE Trans. Nucl. Sci.* **62** (2015) 1255.

[28] H. Chen et al., *Lifetime Study of COTS ADC for SBND LAr TPC Readout Electronics*, in *21st IEEE Real Time Conference (RT2018)*, Williamsburg, Virginia, June 11–15, 2018 (2018) [arXiv:1806.09226].

2019 JINST 14 T07005