Evaluation of Commercial-Off-The-Shelf (COTS) Electronics for Extreme Cold Environments

Miryeong Song, Jean Y. Yang-Scharlotta, Mohammad Ashtijou, and Mohammad Mojarradi
Jet Propulsion Laboratory, California Institute of Technology

Abstract—
Deep space and Icy Moon missions (Titan, Enceladus, Ceres, Europa, & Ganymede) will need qualified extreme environment capable components for electronic systems located in extremities of their rovers and spacecraft. Commercial off the shelf (COTS) components would be advantageous to use for some aspects of such projects, given that they are easier to procure and offer a broad range of functionalities. Furthermore, theoretical and experimental data suggest that many COTS parts are capable of operation, and not just storage, at temperatures well beyond the manufacturer specified temperature limits.

To help address the challenges presented at near cryogenic temperatures, a COTS selection knowledge base is being developed to estimate the performance of COTS components within cold environments. The knowledge base captures queries from a range of information sources such as cold functionality test results for part types and families, theoretical and experimental literature reviews and key findings are summarized here. In addition, a selection of components are planned to be examined for their performance to near cryogenic temperatures to generate a methodology for identification and verification of the COTS candidates. As the qualification of COTS parts for extreme environments can be very costly, this knowledge base can serve to reduce qualification time and cost by pre-selecting and limiting candidates.

TABLE OF CONTENTS

978-1-5386-2014-4/18/$31.00 ©2018 IEEE

1. INTRODUCTION

Space explorations, such as Deep Space and Icy Moon missions (Titan, Enceladus, Europa, & Ganymede), will need qualified extreme cold environment capable components for electronic systems located in extremities of their rovers and spacecraft. Electronic systems located in the extremities, such as motor controllers or sensor systems may be subject to extreme temperatures as they tend to reside outside of the central environmental isolation box of the spacecraft. Beyond spacecraft, terrestrial computing application such as cryogenic operations of electronic instrumentations for quantum computer/super conductor system developments and life science applications such as cryogenic biobanking also have need for extreme cold capable components.

For all of the above applications, integrating *commercial off the shelf* (COTS) components to build cryogenically capable electronic systems would be advantageous compared to employing the *application-specific integrated circuits* (ASIC's) approach since COTS parts are relatively inexpensive and easy to procure. However, most COTS electronics are tested and qualified for commercial specification temperature range (0°C to 85°C) with a few to military specification temperature range (-55°C to 125°C), even though theoretical and experimental data suggest that many COTS parts are capable of operation well past these temperature limits. This study seeks to examine the low temperature operational margin of COTS components outside of the datasheet limits, and to develop a knowledge base of test results which can serve to pre-select and limit candidates for cryogenic electronic systems.

This paper summarizes the key findings of a survey for COTS operational data at temperatures from room temperature down to *milliKelvin range*. The data include the extreme low temperature behaviors of a wide selection of COTS electronics such as *field-programmable gate arrays* (FPGA), *Analog to Digital Converters* (ADC) *operational amplifiers* (OpAmp), memory ICs, transistors, diodes, and passive components. Experimental works conducted at JPL/NASA as well as from broader literature reviews are included. Based on these published data, we discuss the limitations, benefits, and key concerns of COTS usage under extreme cold environments. In addition, we explore potential reliability issues inherent to low temperature operations based on material properties and semiconductor device physics. These key reliability concerns should be addressed within qualification of COTS components for near cryogenic operations. Finally we outline our experimental work to explore COTs functionality at cold.

2. CRYOGENIC OPERATIONS OF COTS ELECTRONICS: DATA SURVEY AND DISCUSSIONS

(1) Resistors

Most COTS resistors with published data show only minor changes (<~5% change from -190°C to 25°C) in resistance values at cryogenic temperatures [1]-[3]. The few exceptions to this are carbon composition, ceramic composition, and metal oxide resistors, which can exhibit much larger changes (> 10%) in resistance at cryogenic temperatures (Table 1). Therefore, most film resistors and wire-wound resistors are suitable candidates for cryogenic temperature operations based on the available data [1]-[3]. It is also reported that the resistance changes with temperature can be considered to be independent of frequencies from DC to 100kHz even at extreme low temperatures [2]-[3].

Table 1. Change in resistance from 25°C to -190°C (measured at 1kHz) [2]

Type	Value (Ω)	Resistance (Ω) at 25 °C	Resistance (Ω) at -190 °C	% Change in Resistance at -190 °C
Metal Film	10	10	9.99	0
	1K	999.15	1001.86	0.3
Wirewound	10	9.7	9.62	-0.9
	1K	984.8	979.31	-0.6
Thin Film	33	33.07	34.32	3.8
	1K	995.41	1007.88	1.3
Thick Film	100	99.99	105.42	5.4
	1K	998.7	1003.22	0.5
Carbon Film	10	9.96	10.46	5.1
	1K	980.3	1035.83	5.7
Carbon Composition	15	14.65	16.34	11.6
	1K	1013.29	1296.54	28
Ceramic Composition	10	9.49	10.99	15.8
	1K	993.09	1167.51	17.6
Power Film	10	10	10.48	4.9
	1K	996.2	1037.06	4.1

(2) Capacitors

Various types of COTS capacitors have been studied at extreme low temperatures [1],[3]-[5]. Fig. 1 shows the change in capacitance as a function of temperature (from 4K to 300K) for various capacitor types.

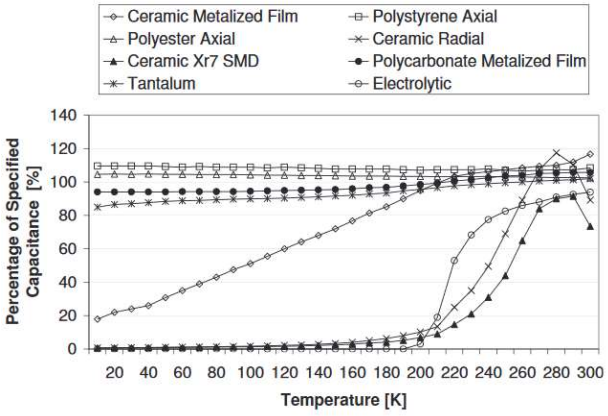

Figure 1. Capacitance vs. Temperature [1]

Solid tantalum, polystyrene, polyester, and polycarbonate capacitor types seem to be good candidates for extreme low temperature operations based on the capacitance variation at low temperatures. NP0 (C0G) ceramic capacitors are also good candidates for cryogenic operations since the NP0 (C0G) capacitor studies conducted in NASA Electronics Parts and Packaging Program (NEPP) [3], [4] show a very stable capacitance behavior down to liquid nitrogen temperature (LNT) (Fig. 2).

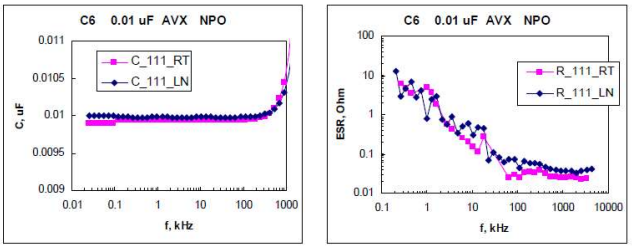

Fig 2. NP0 (C0G) ceramic capacitor behavior at room temperature (RT) and liquid nitrogen temperature (LN) [4]

However, high k-dielectric constant ceramic capacitors such as X7R, X5R and ferroelectric based capacitors were found not suitable for cold temperature environments due to extreme variance in capacitance at low temperatures. Wet electrolytic tantalum capacitors are not suitable for cryogenic operations due to freeze-out of the liquid electrolyte causing capacitance drop to near zero at cryogenic temperatures.

The extensive study of solid tantalum capacitors (with manganese cathode) by Teverovsky [4], [5] showed that the roll-off frequency (*f*r) of tantalum capacitors has a strong temperature dependency, especially at cryogenic temperatures [4]. For example, *f*r is ~10 to 30 kHz at room temperature and decreases to ~1 kHz at 77K. *f*r further decreases to ~0.1 kHz at 15K for the various tantalum capacitors tested in his work. The decrease in the roll-off frequency at low temperatures is attributed to the increasing resistance of the manganese cathode layer with lowering temperature. Also, the capacitance degradation behavior of solid tantalum capacitors (with manganese cathode) at low temperatures as shown in Fig 3 could be explained by the increase in manganese cathode resistance causing substantial decrease in capacitance at higher frequencies (frequencies above *f*r) and by variation of dielectric constant of tantalum pentoxide causing small decrease in capacitance at lower frequencies (frequencies below *f*r). In contrast, ceramic NP0 capacitors do not show any significant dependence on frequencies (Fig. 2).

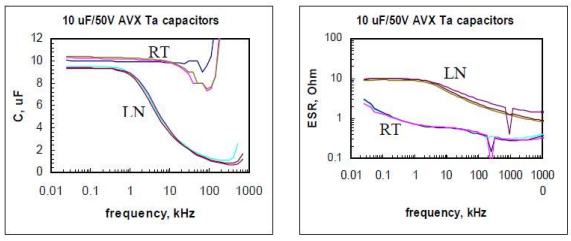

Fig 3. Solid tantalum capacitor frequency behavior at room temperature (RT) and liquid nitrogen temperature (LN) [4]

Polymer cathode tantalum capacitors are another type of solid tantalum capacitor that can perform better than manganese tantalum capacitors at cryogenic temperatures since the conductivity of polymer cathode does not degrade significantly at cryogenic conditions. Polymer based tantalum capacitors typically maintained most of their capacitance up to 100 kHz or beyond and displayed much less variation of the onset of capacitance roll-off as the temperature was varied down to -194°C [29]. Therefore, tantalum polymer capacitors are good candidates for cryogenic applications, which require exceptionally low ESR and/or very stable capacitance versus frequency and temperature.

(3) Diodes

At low temperatures, diodes typically show an increase in the forward voltage and increase in the slope of the I-V curve (increased forward conductance), which can be predicted from the classical theory of diode current equation. All the various COTS diodes (including high current, small signal, Zener, Schottky, and SiGe diodes) tested between 25°C and -190°C at NASA [6], [7] show the characteristic shifts of diode I-V curves as a function of temperature as shown in Fig 4.

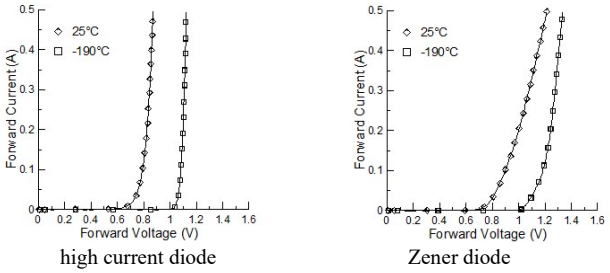

Figure 4. Diode I-V charactersistics at 25°C and -190°C [7]

The change in the forward voltage and the change in the slope of I-V curve will depend on the fabrication technology and the electrical design of the diodes. The functionality pronouncements of diodes will largely depend on application requirements and the assessment of the design margin for a given application and the available options to compensate for the diode parameter shifts at low temperatures. It should be noted that the Si diode forward voltage increases drastically below ~20K-25K, as shown in Figure 5 [8], [9].

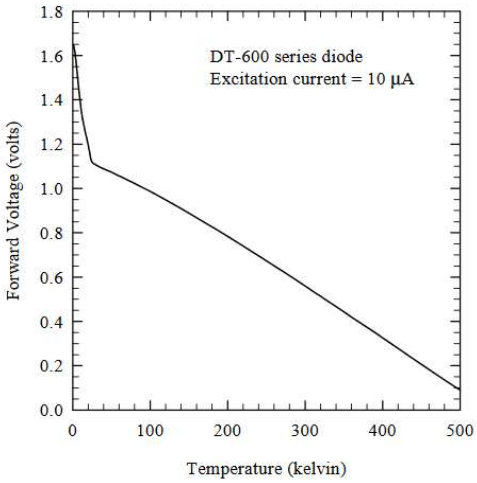

Figure 5. Diode forward voltage (at 10uA) vs. tempetures [9]

(4) Transistors

MOS transistors are known to operate down to Liquid Helium Temperature (LHT), 4K, and below and Table 3 below shows an example of the MOSFET electrical parameter comparisons between 300K and 4K for bulk Si CMOS process [10]. Also, silicon-on-insulator (SOI) MOSFETs processed at a commercial foundry were tested from 300K down to 30mK and were shown to retain transistor functionality even at 30mK with some deviations from ideal transistor characteristics (Fig. 6) [19]. The qualitative characteristic of MOSFET operating at cryogenic temperatures (i.e. higher |Vth|, sharper sub-threshold slope (faster turn-on), larger Gm and Gds, lower off-state leakage current, etc.) are expected based on classical MOS devices physics. However, the quantitative performance of MOSFET is a very complicated function of many technology (process and transistor design) parameters in addition to temperature effects. For example, the increase in current drive due to higher mobility at low temperatures can be mitigated by partial carrier freeze-out depending on the doping profiles and the operating temperature. The kinks and hysteresis in SOI transistor I-V curves can be observed depending on the technology and bias conditions at low temperatures.

Table 3. Measured VTH, sub-threshold slope (SS), Ion/Ioff, gm, and gds ratios for two CMOS processes, N & P polarities at RT and LHT. Vgs and Vds were chosen to guarantee maximum gm and gds (|Vgs|= |Vds|= 1.8V for160nm; |Vgs| = |Vds| = 1.1V for 40nm) [10]

Type	W / L	V_{TH} [V]		SS [mV/dec]		I_{on}/I_{off}		g_m/g_m	g_{ds}/g_{ds}
		LHT	RT	LHT	RT	LHT	RT	LHT/ RT	LHT/ RT
NMOS 160nm	2320 160	0.7	0.55	22.8	87	$10^{-3}/10^{-11}$	$10^{-3}/10^{-10}$	1.31	1.91
NMOS 40nm	1200 40	0.65	0.55	27.7	88	$10^{-4}/10^{-12}$	$10^{-4}/10^{-10}$	1.27	1.30
PMOS 160nm	2320 160	-0.7	-0.50	38.9	93	$10^{-3}/10^{-12}$	$10^{-3}/10^{-10}$	1.15	1.07
PMOS 40nm	1200 40	-0.7	-0.55	27.3	90	$10^{-4}/10^{-12}$	$10^{-4}/10^{-10}$	4.36	1.00

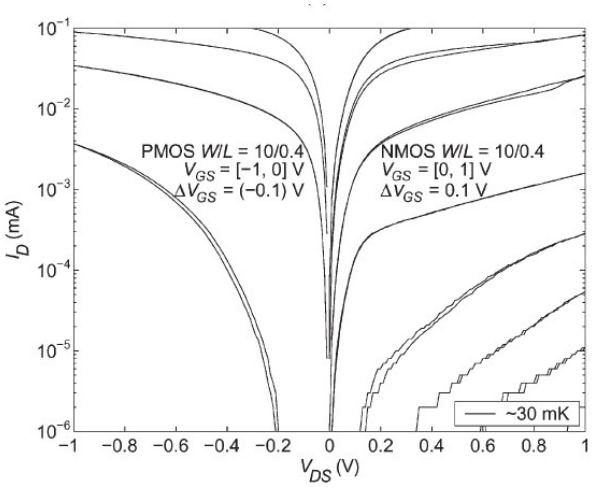

Figure 6. SOI transistor I-V characteristics measured at 30mK [19]

A power MOSFET, which is one of the most widely used discrete COTS components, shares the common MOSFET characteristics at low temperatures as discussed beforehand. The two most important parameters, on-resistance and breakdown voltage for power transistors, require special attention in selecting process for cold applications. Leong et al. studied COTS power MOSFETs and compared three COTS power MOSFETs from three different technologies. The results showed that power MOSFETs are functional down to 20K with significant improvements in the on-state resistances at cryogenic temperatures but with reduced breakdown voltage as shown in Fig. 7 [14].

The three different COTS (two super junction FETs – MDMesh and CoolMOS and one conventional FET-HEXFET) tested in their study showed that the power MOSFETs can have similar characteristics at room temperatures but show significant variations in the device characteristics (such as breakdown voltages and on-state resistances) at cryogenic temperatures depending on the technology and the manufacturer as shown in Fig.7 (a), (b). Therefore, selecting the best COTS power MOSFET for a specific application will require thorough characterization of the device at the operating temperatures considering all the trade-offs in cryogenic device characteristics (Fig 7 (c)).

Cryogenic characterizations of silicon-based BJTs have been limited to temperatures above 77 K because at extreme lower temperatures, Si BJTs exhibit a strong decrease of the DC current gain, beta (β=Ic/Ib), and a large increase in the base resistance [12]. As shown in Fig. 8, a COTS Si NPN power BJT current gain degrades significantly due to a combination of the reduced emitter injection efficiency and base transport factor at cryogenic temperatures [15]. Another example is shown in Fig. 9 which demonstrates the gain degradation of a parasitic PNP bipolar (inherent to standard Si CMOS processes) at low temperatures [12].

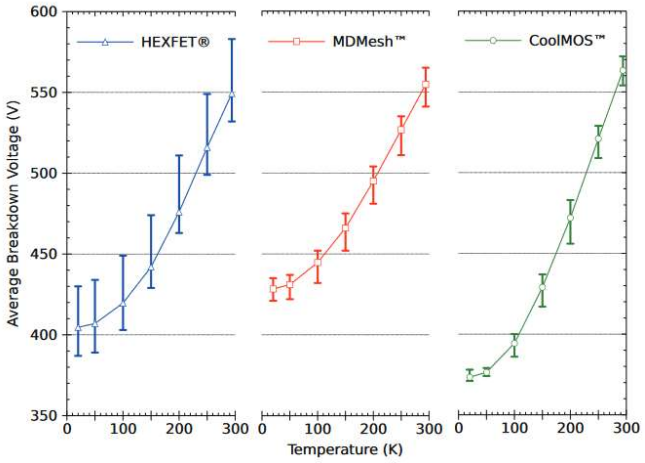

Figure 7 (a). Comparison of breakdown voltages of between three different COTS power MOSFETs [14]

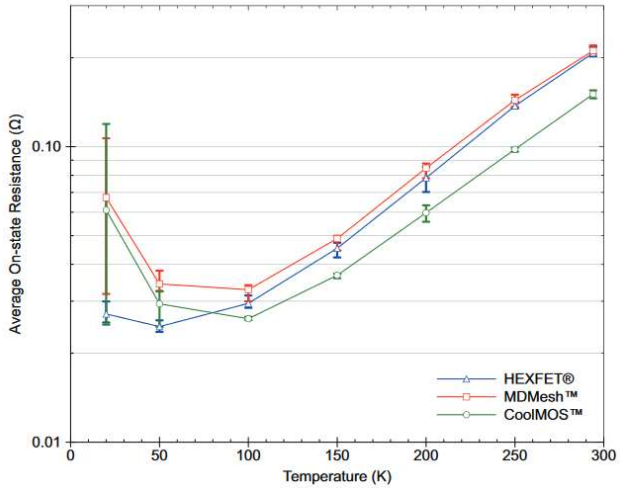

Figure 7 (b). Comparison of on-state resistance of three different COTS power MOSFETs [14]

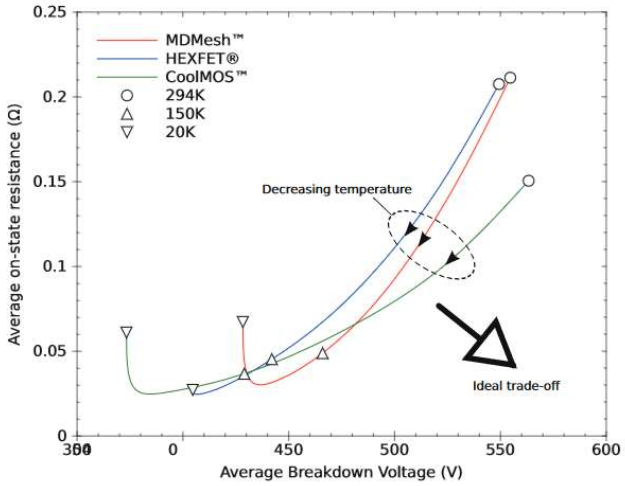

Figure 7 (c). Tradeoff between breakdown voltage and on-resistance as a function of temperature [14]

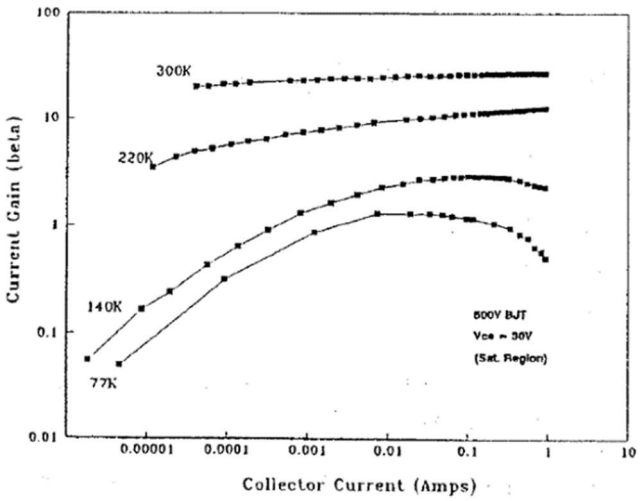

Figure 8. Si NPN BJT DC gain (beta) vs. Ic at various temperatures [15]

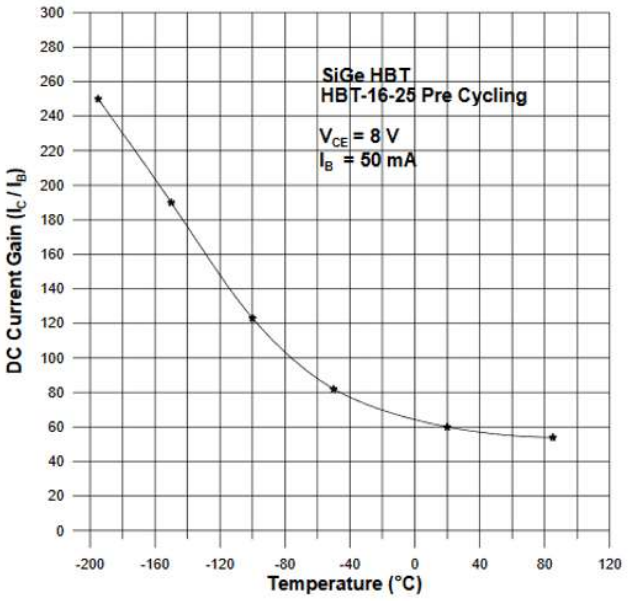

Figure 10. DC (Ic/Ib) gain as a function of temperature for SiGe power HBT [6]

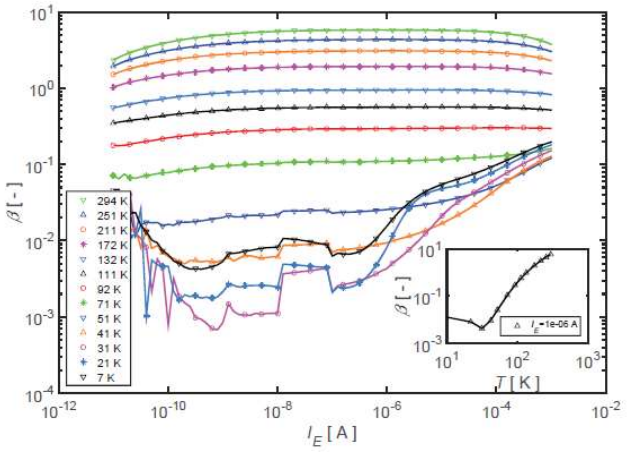

Figure 9. Parasitic PNP BJT DC gain degradation at low temperatures [12]

Therefore, Si BJT's have limited usages at temperatures below LNT. In contrast, SiGe heterojunction bipolar transistors (HBT) with bandgap engineering typically show substantial increase in current gain with decreasing temperature, which makes them much better candidates for cryogenic operations (Fig. 10) [6]. Table 4 shows SiGe HBT dc current gain from 300K down to 18K for various technologies. Even though there is a general trend of SiGe HBT dc gain which increases as temperature decreases, the enhancement of dc current gain at cryogenic temperatures strongly depends on the technology (due to exponential dependence of gain on Ge content in the base) and the gain can vary over a few orders of magnitude among the technologies [13].

Table 4. Comparison of SiGe HBT DC gain between various technologies [13]

Foundry	Process name	Tech. node		$\beta_{DC,pk}$				
		μm	T_a, K	300	200	77	50	18
IBM	BiCMOS8HP	0.12	IBM-G4	351	839	3400	4040	4340
IHP	SG13	0.13	IHP-G4	466	1320	3660	3890	3850
ST	BiCMOS9MW	0.13	ST-G4	1840	5490	51600	56600	63600
ST	BipX2	0.15	ST-X1	2720	15000	36800	37800	38200
ST	BipX1	0.17	ST-X2	1630	5830	34800	36000	35000
ST	BipX3	0.17	ST-X3	2810	15000	44800	45600	45900
JAZZ	SBC18	0.18	JAZZ-G3	118	189	566	623	651
NXP	Qubic4Xi	0.25	NXP-G3	801	1400	1150	1110	958

(5) Integrated Circuit (IC) COTS

Commonly used IC COTS parts (such as FPGA's, OpAmp's, ADC's and voltage regulators) have been demonstrated to be operational at cryogenic temperatures with various electrical parameter shifts (compared to nominal spec) or with partial functionality. As discussed in the discrete semiconductor devices, IC functionality also needs to be defined in the context of application specific requirements and tolerance of the whole system for the electrical parameter deviations (from the datasheet limits) at cryogenic temperatures. In addition, it should be noted that COTS IC Parts with similar datasheet spec might show wide variation on the electrical characteristic at cryogenic temperatures depending on the testing conditions and technology.

(i) FPGA

The functionality of COTS FPGAs at cryogenic temperatures has been demonstrated by many researchers [16]-[19]. Table 5 shows a brief comparison of the performance among various types of COTS FPGAs tested down to -150℃ [18].

Table 5. COTS FPGAs functionality comparison at low temperatures [18]

Vendor	FPGA	PCB	Results
Microsemi	AS54SX32A	Custom	Functional
Xilinx	XCVR300	Custom	Functional and reprogrammable. Large surge, temperature dependent surge current.
Xilinx	XC2VP20	Custom	Functional and reprogrammable
Microsemi	AX500	Custom	Functional <5% variation of 150MHz clock, power independent of temperature
Microsemi	AGLN250V2	COTS	Functional with 10X current drop at -130C. Flash freeze functional with 100X in reduction in standby current.
Microsemi	AGL125	COTS	Functional and reprogrammable to -140C, clock stability issues at -120C
Microsemi	AGL1000	Custom	Functional digital modem to -130C, core power drops 30% at -140C,
Xilinx	XC3S250	Custom	Functional <2% change in power down to -150C
Xilinx	XCV5VLX30	Custom	Functional and reprogrammable. Core current drops 66% at -150C. On board flash failed @ -130C

Another study on FPGA functionality [17] comparing Artix7, Spartan3, and Spartan6 reported that all three FPGA's retained most of the functionality at cryogenic temperatures. However, they also reported that PLLs were not operational at cryogenic temperatures and the serial Low Voltage Differential Signal (LVDS) output voltage parameter varies the most during cryogenic operation of FPGA as shown in Table 6. Only the Spartan-3 FPGA exhibits functioning differential output signaling. In contrast, Artix7 and Spartan6 show dramatic changes in the output voltages. The operation of LVDS outputs are likely linked to internal bandgap voltage reference offsets occurring at low temperature.

Table 6. Comparison of FPGA IO parameters between room temperature and 4K [17]. Common mode voltage of 1.2V used for LVDS.

	Artix-7		Spartan-6		Spartan-3	
	300 K	4 K	300 K	4 K	300 K	4 K
V_{IH} single-ended LVCMOS (V)	1.16	1.22	2.39	2.51	1.50	1.61
V_{IL} single-ended LVCMOS (V)	1.09	1.11	2.14	2.24	1.42	1.47
V_{IH} differential LVDS (mV)	5	18	11	11	18	13
V_{IL} differential LVDS (mV)	-39	-55	18	-33	-39	-35
Pull-up resistance (kΩ)	20	17	10	7.7	10	6.6
Differential resistance (Ω)	96	86	101	93	108	105
Differential output voltage (mV)	435	42	372	1569*	387	582*
Common-mode differential output voltage (mV)	1120	227	1242	1202*	1056	1652*

More extensive characterizations of Artix7 FPGA were done by Homulle et al. [16] and the summary of the functionality data of Artix7 at 4K in comparison with room temperature is shown in Table 7. In their study, the operating voltage range of the FPGA changes significantly over temperature. Compared to the range of 0.85V-1.1V at room temperature, it reduces significantly on both ends at 4K resulting in the voltage range of 0.92V-1.02V.

Table 7. Artix7 FPGA performance at 4K in comparison with room temperature [16]

Module	Functional	Test	Performance w.r.t. RT
IOs	✓		
LVDS	✓		
LUTs	✓	LUTs connected to form oscillator of approximately 100 MHz at RT	Oscillation frequency changes < 5%, jitter increases < 15% (11.8 to 13.5 ps)
CARRY4	✓	Carrychains connected to form oscillator of approximately 100 MHz at RT	Oscillation frequency changes < 2%, jitter increases < 3% (11.5 to 11.8 ps)
BRAM	✓	Transfers of 8 kB (write & read)	No corruption in 10 test sets of 80 kB
MMCM	✓	100 MHz differential input clock multiplied by 10 and divided by 20 to 50 MHz single ended output	Jitter reduction of roughly 20% (11.4 to 8.9 ps)
PLL	✓	100 MHz differential input clock multiplied by 10 and divided by 20 to 50 MHz single ended output	Jitter reduction of roughly 20% (12.2 to 9.7 ps)
IDELAYE2	✓	IDELAYE2 elements connected to form a tunable oscillator (output frequency variable 13-70 MHz)	Delay change of up to 30%, jitter increase up to 50%

(ii) OpAmp

The behaviors of various COTS OpAmps tested at cryogenic temperatures are shown in Table 8 [1]. They were tested in the inverting amplitude configuration with a gain of 10. There is wide variation on failure temperatures (when measured where the output swing started to clip, gain-bandwidth (GBW) decreased, or the output clipped to the rails) among the parts tested.

Table 8. Low temperature limits of OpAmps [1]

Op-amp	Type	GBW* [MHz]	Temperature [K]
LM412	BJT with JFET input	3	120
OPA277	CMOS	1	73
OPA727	CMOS	20	48
TLV2211	CMOS	0.056	30
LMC6064	Silicon-gate CMOS	0.1	63
LMC6462	CMOS	0.05	70
LMC7101	CMOS	1	44

*The specified gain-bandwidth product of the op-amp

Another study [21] also showed the large variation of the gain bandwidth depending on the technology at cryogenic temperatures. Gunaseelan et al. compared CMOS (AD8572), Bipolar (LM6144), and BiCMOS (AD627) OpAmps and their data showed the BiCMOS OpAmp showed the least amount of variation in performance at low temperatures as expected. They speculated that the poor performance of CMOS OpAmp at extremely low temperature was due to hot carrier effects, and the deterioration of Bipolar OpAmp performance at low temperature was due to the strong current gain reduction inherent to bipolar technology.

One example of BiCMOS OpAmp (OP181GP) behaviors at extremely low temperatures is shown in Fig. 11 [31]. Even though the tested OpAmp remained functional close to LNT, the degradation of the corner frequency and phase shift with decreasing temperature has been observed in addition to output signal distortion at extremely low temperature.

In addition, Table 9 below show the performance of four different CMOS OpAmps from three different manufactures at 77K in comparison with room temperature (300K) based on a high-pass filter circuit [22]. Even though all four OpAmps are based on CMOS technology, the change in their performance at 77K (compared to RT) vary among the parts tested.

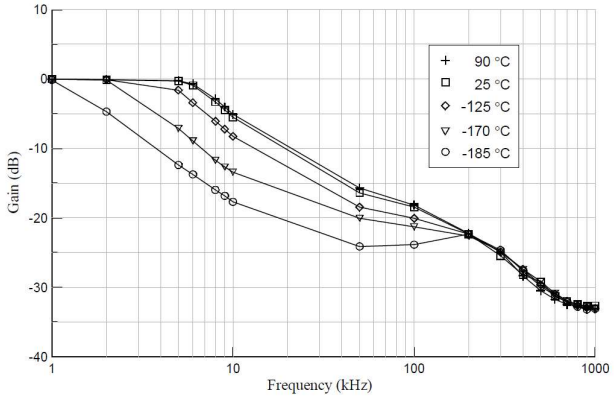

Figure 11 (a) OpAmp Gain versus Frequency at various temperatures [31]

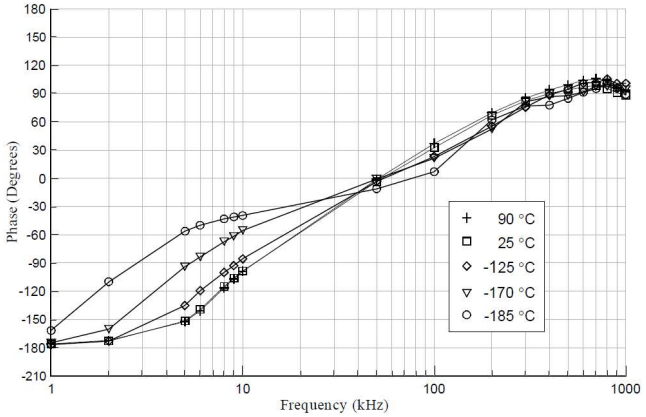

Figure 11 (b) Phase Shift versus Frequency at various temperatures [31]

Table 9. Comparison of OpAmp characteristics between 77K and room temperature [22]

	OP80GP	TLC271BCP	LMC662CN	LMC6081AIN
Experimental low-pass cutoff frequency (300K)	90 kHz	400 kHz	310 kHz	400 kHz
Experimental low-pass cutoff frequency (77K)	120 kHz	600 kHz	390 kHz	200 kHz
Experimental gain crossover frequency (300K)	230 kHz	800 kHz	800 kHz	600 kHz
Experimental gain crossover frequency (77K)	300 kHz	1.1 MHz	700 kHz	440 kHz

(iii) Voltage Regulator

The extremely low temperature behaviors of COTS voltage regulators (DCDC converters and Low Drop Out (LDO) voltage regulators) show a wide variation depending on the manufacturers and the test conditions as shown in Figure 12 [30] and Table 10 [2]. The temperature at which the COTS parts started to show abnormal behavior varies between -40**℃** (233K) to LNT (77K). Also, the output voltage degradation as a function of temperature does not show any predictable trend among the various parts tested (Fig. 12). Based on the surveyed data, most of the COTS voltage regulators lose their functionality or become unreliable when operated near LNT.

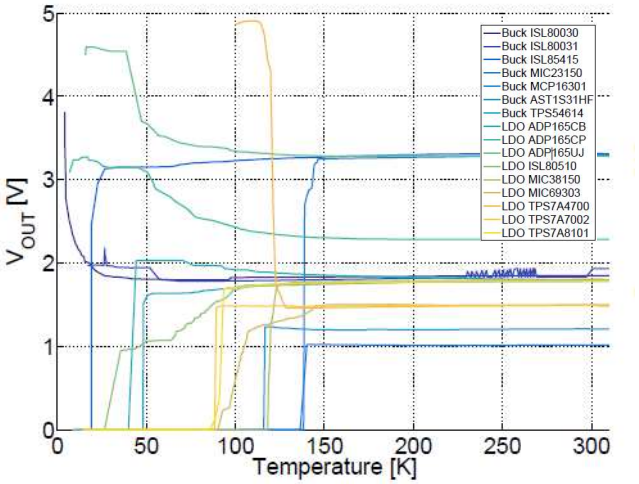

Figure 12. Output voltages of commercial DC/DC converters at various temperatures [30]

Table 10. COTS DC/DC converter output voltage and efficiency versus temperature at various loads and input voltage of 16 V [2]

Manufacturer	Experimental Observations	Decisive* Temp (°C)
Astrodyne	V_{out} dropped to 2.4 V at –140 °C. Chip functioned down to –160 °C.	-160
Power Trend	V_{out} lost regulation at –100 °C. Converter still functioned to –195 °C.	----
Lambda	Chip worked very well down to -120 °C. Input current oscillations occurred at all temperatures under heavy loading.	-120
Power One	Oscillations in input current started at –80 °C.	-120
CDI	Oscillations in input current observed at –140 °C under heavy loading.	-180
Interpoint	Low frequency oscillations with high peaks observed in input current at –120 °C and below.	-160
Calex	Although the module ceased to work at -40 °C during steady state, it worked down to -100 when tested under a step change in load from full to no-load and vice-versa.	-40
SynQor	Output voltage increased as temperature was lowered below 20 °C.	-80
Vicor	Oscillation in input current started at –40 °C; more noticeable under heavy load conditions.	-120

* Temperature at which module ceased to operate but recovered afterwards

(iv) ADC

Since most of COTS ADCs are based on CMOS technology, Si bandgap increase, transistor parameter shifts and abnormalities (kinks, hysteresis), and carrier freezeout inherent to CMOS can adversely affect the functionality of ADC at cryogenic temperatures. Based on the surveyed data, COTS ADCs have been shown to be functional down to LNT with reduced resolution. For example, a COTS 14-bit ADC (AD6645) loses about 5 to 6 bits of accuracy leaving 8 to 9 effective number of bits (ENOB) at -180**℃** [33] and a COTS 12bit ADC can be reduced to 10 bit accuracy at -160**℃** according to the work by Mojarradi et al. [32].

It is worth noting that when ADC was implemented with a completely digital building block inside the FPGA (Artix7), ENOB performance appear to be less susceptible to cold and is only lowered by roughly one bit at 15K when compared to room temperature (Fig. 13) [16]. This small performance loss is more likely to be tolerated by some applications.

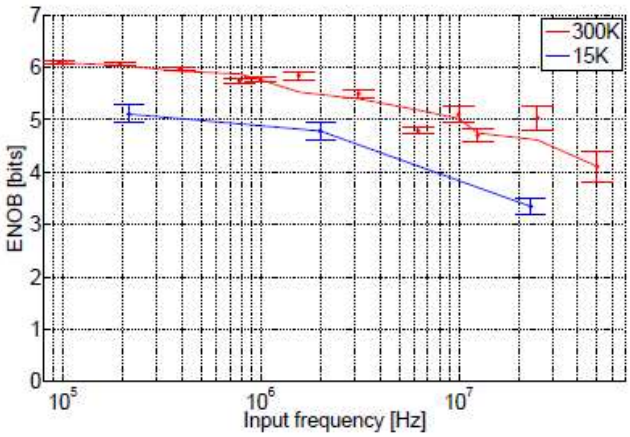

Figure 13. Effective number of bits versus input signal frequency at room temperature and 15K for the FPGA ADC sampling with 1.2 GSa/s [16]

(6) Memory

In general, due to the inherent benefit of operating CMOS at low temperatures (higher mobility and lower leakage current etc.), both SRAMs and DRAMs have been reported to be functional down to 77K (LNT) with the improvement in the access time for SRAMs and DRAMs (1.5-2 times at 77K) and the improvement of retention time for DRAMs (orders of magnitude at 89K) at low temperatures compared to room temperature [23]-[26]. Flash memories were also reported to be operational down to 77K [24]. However, when total 6 batches (differ by date code, technology, and assembly line) of COTS low voltage flash memories from the same manufacturer were tested, the failure rates at cryogenic temperatures and failure signatures varied widely from batch to batch (Fig. 14). Most of the failures occurred during the erase and programming operations at temperatures below 108 K and both erase and programming times increase by a factor of 4–6 at −196 °C for most of the samples. The failure signatures provide two important findings for use of these parts at cold: 1) the degradation of charge pumping circuitry efficiency may be a possible source of the reported failures. 2) large batch-to-batch variation can be the norm as one seeks to use COTs components outside of the specified temperature range. The test results from the 3600 samples of COTS flash ICs also showed that only the selective parts are functional down to 77K [24].

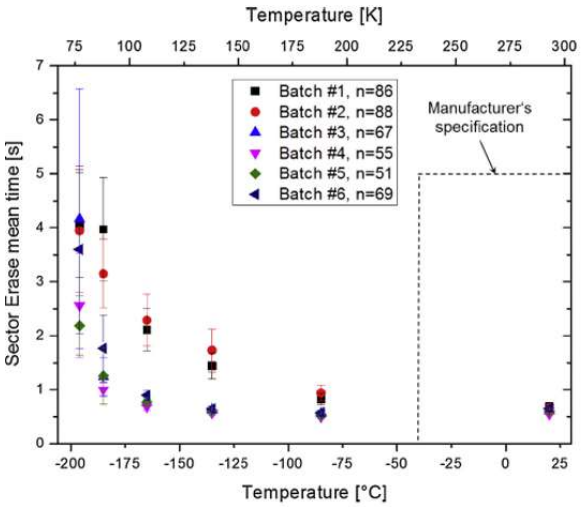

Figure 14 (a). Flash Memory Sector erase mean time as a function of temperature. Dotted line shows manufacturer's maximum value specified down to -40°C[24].

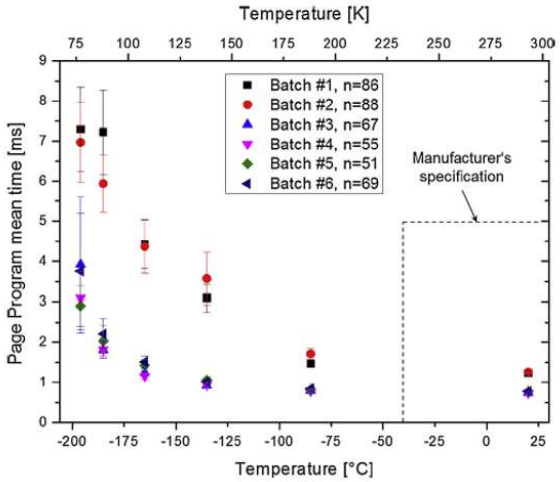

Figure 14 (b). Page program mean time as a function of temperature. Dotted line shows manufacturer's maximum value specified down to -40°C[24].

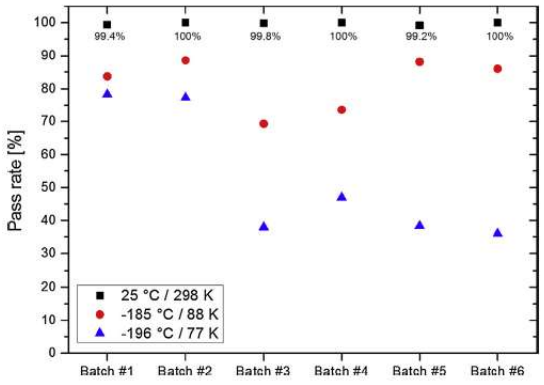

Figure 14 (c). Batch evolution for different test temperatures. Note the batch-to-batch variation of the pass rate[24].

3. COTS RELIABILITY CONCERNS AT CRYOGENIC TEMPERATURES

As discussed in section 2, many COTS electronics can operate at cryogenic temperature with minor or major changes in performance. The temperature related performance change can be understood in many cases in terms of the underlying physics based on the technology of the electronic part. The performance may improve or degrade in cryogenic temperature when compared to operation within specification or typical temperatures.

In fact, the inherent benefits of operating COTS electronic parts at cryogenic temperatures include fast switching speed of CMOS circuits, low thermal noise, low thermal leakage current (low stand-by power consumption), increase in memory retention time, high metal conductivity, and the suppression of thermally activated aging process such as electromigration. On the other hand, there are also inherent adverse cold temperature effects on the functionality and the reliability of COTS such as carrier freezeout in semiconductor devices, increase in mechanical stress due to thermal coefficient mismatch between different materials, timing failure due to variation in device performance as a function of temperature, exacerbation of hot carrier induced transistor reliability, reduction in semiconductor device breakdown voltage, change in dielectric constants, which can cause both short term and/or long term reliability issues.

On the discrete component level, hot carrier reliability is one of the major concerns at cryogenic temperatures since low temperatures exacerbate hot carrier induced damage and the impact on device lifetime and performance strongly depend on the operating conditions, technology, design, and lifetime criteria [27, 28]. In addition, the hot degradation behaviors at extreme low temperatures deviate from the classical hot carrier induced degradation model, which make it difficult to predict hot carrier device reliability at cryogenic temperatures without experimental data for the specific devices in use. Also, gate dielectric reliability of any MOS devices needs special attention due to the experimental observation that an increase in gate current at low temperatures could have significant impact on the gate dielectric reliability.

Tantalum capacitors can be good candidates for cryogenic operations, but their breakdown voltages measured during step surge current testing decrease by ~40% at 77 K compared to room temperature, which could be a reliability concern for low-impedance applications [4].

For resistors, failures at cryogenic temperatures are typically caused by mechanical stress due to thermal coefficient mismatch, such as a cracked case, a broken lead, or delamination and thermal cycling is usually required to screen out the potential reliability hazard.

For these discreet components, most of data available in literature focused on functionality and very limited data is available on reliability. Therefore, significant empirical study for establishing understanding for the major failure mechanisms at extremely low temperatures would be useful. Such understanding would be necessary to establish comprehensive parts cold screening guidelines for reliability and also to develop a qualification procedure for cryogenic operations of COTS discrete components. It may be possible, however, to establish key trends by executing selected, well-designed studies.

On the IC level, understanding the device level reliability including hot carrier effect and CMOS gate dielectric reliability is critical for evaluation of any COTS ICs reliability risks, since CMOS is a building block for most COTS ICs. In addition, COTS IC functionality/reliability also needs to be defined in the context of application specific requirements and tolerance of the whole system for the electrical parameter deviations at cryogenic temperatures. Previous qualification methodology for near cryogenic temperatures entails burn-in and life testing at the high and low temperatures as well as electrical testing spanning the temperature range during the tests [34].

Also, it should be noted that COTS IC parts with similar datasheet spec might show wide variation in the electrical characteristics at cryogenic temperatures depending on the testing conditions and the fabrication technology. The design margin and the reliability guard band implemented by manufacturers do not generally apply to cryogenic temperatures since the devices are being operated outside the manufacturer's spec limits. Operating beyond the manufacturer's spec limits tends to result in wide batch to batch performance variation as documented in the memory IC study [24], which requires screening methodology.

Therefore, further study is required to define functionality criteria for COTS at cryogenic temperatures, which can vary depending on the specific applications. For example, improved performance of COTS ICs at low temperatures might cause timing issues within individual components or at the system level depending on the requirements between interfaces among various components. Reduction in accuracy (ENOB) of ADCs at cryogenic temperature could be tolerated depending on the applications. For COTS ICs reliability assessment at cryogenic temperatures, a thorough device level reliability study should be performed to minimize the potential risks using COTS ICs for cryogenic operations and provide the guideline for IC part selection procedure, which will require the understanding of the system level requirements. In addition, system design changes might be necessary to compensate and accommodate parameter shifts and partial functionality, and reduce reliability risks at cryogenic temperatures.

One of the major challenges in studying COTS reliability is the difficulty in acquiring the fabrication technology information and the design details for COTS ICs, which can be crucial in interpreting experimental data and developing a general model for cryogenic reliability of COTS parts. Also, since batch to batch variation has been observed in most of the COTS parts tested, extensive temperature screening tests, such as cold start/re-start, thermal cycles/shock, cold soak, etc., should be performed for each COTS component prior to selecting parts for long term reliability, which can be costly.

5. SUMMARY

Based on the surveyed low temperature data, it seems likely that carefully selected COTS parts can be operational well beyond the datasheet limit temperatures and in some cases even below liquid nitrogen temperature (77K). COTS ICs were demonstrated to be operational at cryogenic temperatures even with various electrical parameter shifts (compared to nominal spec); however, they exhibit at least partial functionality in some cases depending on the applications and test conditions. Most of previous works on COTS operating at extreme low temperatures focused on the feasibility and functionality study. Further work would be needed to develop characterization methodology and knowledge base for COTSs pre-screening to provide the most viable candidates for cryogenic applications. Establishing reliability evaluation methodology and qualification procedures will be required to meet the reliability challenges for COTSs cryogenic applications.

ACKNOWLEDGEMENT

The authors thank Dr. R. Rouse of Microsoft Corporation, S. Gore and Dr. K. M. Han of JPL for helpful discussions. This work was supported by the JPL Research and Technology Development Program and it was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under contract with the National Aeronautics and Space Administration.

REFERENCES

[1] P. C. van Niekerk and C. J. Fourie, "Cryogenic CMOS based control system," AFRICON, 2007

[2] R. L. Patterson, A. Hommoud, "Evaluation of COTS SiGe, SOI, and Mixed Signal Electronic Parts for Extreme Temperature Use in NASA Missions," NEPP Electronic Technology Workshop, 2011

[3] R. Patterson et al., "Evaluation of Advanced COTS Passive Devices for Extreme Temperature Operation," NASA Technical Report, 2009

[4] A. Teverovsky, "Reliability of Electronics at Cryogenic Temperatures," NASA Technical Report, 2005

[5] A. Teverovsky, "Performance and Reliability of Solid Tantalum Capacitors at Cryogenic Conditions," NASA Technical Report, 2006

[6] R. L. Patterson, "Electronic Components for Use in Extreme Temperature Aerospace Applications," International Components for Military and Space Electronics Conference, 2008

[7] R. Patterson, "Performance of Various Types of Diodes at Cryogenic Temperatures," NASA Technical Report, 2004

[8]A. Szmyrka-Grzebyk, and L. Lipinski, "Low Temperature Current-Voltage Characteristics of Silicon Diodes Used as Thermometers," Cryogenics, 1993.

[9] S. S. Courts, P. R. Swinehart, and C. J. Yeager, "A New Cryogenic Diode Thermometer," Advances in Cryogenic Engineering, 2002

[10] E. Charbon, "Cryo-CMOS for quantum computing," IEDM, 2016

[11] J. C. Bardin et al., "Silicon Germanium Cryogenic Low Noise Amplifiers," Journal of Physics, 2017

[12] L. Song et al., "Characterization of Bipolar Transistors for Cryogenic Temperature Sensors in Standard CMOS," Sensors, 2016

[13] J. C. Bardin, "Silicon-Germanium Heterojunction Bipolar Transistors for Extremely Low-Noise Applications," Ph. D. dissertation, 2009

[14] K.K. Leong, A.T. Bryant, P.A. Mawby, "Power MOSFET Operation at Cryogenic Temperatures: Comparison between HEXFET, MDMesh, and CoolMOS," Power Semiconductor Devices & IC's, 2010

[15] R. Singh and B. J. Baliga, "Cryogenic Operation of Power Bipolar Transistors," Power Semiconductor Devices & IC's, 1994

[16] Homulle et al., "A Reconfigurable Cryogenic Platform for the Classical Control of Scalable Quantum Computers," Review of Scientific Instruments, 2017

[17] I. D. Conway et al.," An FPGA-based Instrumentation Platform for use at Deep Cryogenic Temperatures," Review of Scientific Instruments, 2016

[18]D. Sheldon, "Cryogenic Operation of Field Programmable Gate Arrays," NASA Technical Presentation, 2011

[19] S. R. Ekanayake et al., "Characterization of SOS-CMOS FETs at Low Temperatures for the Design of Integrated Circuits for Quantum Bit Control and Readout," IEEE TED, 2010

[20] M. E. Elbuluk et al., "Cryogenic Evaluation of an Advanced DC/DC Converter Module for Deep Space Applications," Industry Applications Conference, 2002

[21] S.T. Gunaseelan et al., "Low Temperature Performance of Operational Amplifiers for Space Applications," Electrical and Computer Engineering, 2003

[22] F. Torres, "Low Temperature Operation of CMOS Operational Amplifier ICs," Energy Conversion Engineering Conference, 1996

[23] S. Hanamura et al, "Operation of bulk CMOS devices at very low temperatures," IEEE Solid State Circuit, 1986

[24] F. R. Ihmig et al, "Batch screening of commercial serial flash-memory integrated circuits for low-temperature applications," Cryogenics, 2015

[25] P. Wyns, R.L. Anderson, "Low-Temperature Operation of Silicon Dynamic Random Access Memories," IEEE Trans Electron Dev, 1989

[26] W.H. Henkels, et al., "A 12-ns low-temperature DRAM," IEEE Trans Electron Dev, 1989

[27] J. Wang et al., "New Understanding of LDD CMOS Hot-Carrier Degradation and Device Lifetime at Cryogenic Temperatures," IEEE IRPS, 1997

[28] M. Song et al., "Comparison, of NMOS and PMOS Hot

Carrier Effects from 300K to 77K," IEEE Trans Electron Dev, 1997
[29] E. Reed, "Characterization of Tantalum Polymer Capacitors," NASA NEPP Technical Report, 2006
[30] Homulle et al., "FPGA Design Techniques for Stable Cryogenic Operation," Review of Scientific Instruments, 2017
[31] R. Patterson et al., "Effect of Extreme Temperature Thermal Cycling of 8-Pin Plastic Dip-Package Analog Devie OP181 GP Operational Amplifiers," NASA Technical Report, 2002
[32] M. Mojarradi et al., "Application of Commercial Electronics in the Motors and Actuator Systems for Mars Surface Missions," IEEE Aerospace Conference Proceedings, 2004
[33] R. Ramesham et al., "Data Converters Performance at Extreme Temperatures," IEEE Aerospace Conference Proceedings, 2005
[34] Yuan Chen et al., " A Case study: Design for Reliability for a Rail-to-Rail Operational Amplifier for Wide Temperature Range Operation for Mars Missions," International Reliability Physics Symposium, 2008.

BIOGRAPHY

Miryeong Song *received the B.S., M.S., and Ph. D. degrees in Electrical Engineering from University of California, Los Angeles in 1988, 1991, and 1994, respectively. She started her career at The Aerospace Corporation, where she conducted an extensive research on hot carrier effects at cryogenics temperatures. She also has worked for several major semiconductor companies including AMD, Xilinx, Connexant, Qualcomm, and Peregrine Semiconductor. Her work included CMOS process technology development, technology qualification, and device reliability research. She has taught at several universities including UCLA, Santa Clara University, and Hannam University. She is currently working at JPL studying COTS electronics for cryogenic operations.*

Jean Y. Yang-Scharlotta *(M'07) received her B.S. in chemical engineering from The University of Texas in Austin, in 1990 followed by M.S. and Ph.D. in chemical engineering from Stanford University in 1996. She participated in engineering and research activities at the Los Alamos National Laboratory from 1987-1991 in radioisotope chemistry prior to graduate research in self-assembled monolayers at Stanford University. Her interest in physical properties at interfaces drew her to the semiconductor industry. From 1996 to 2008, she was a device technology engineer then department manager at Advanced Micro Devices introducing and scaling new flash memory device technologies-- ushering in the first three generations of the MirrorBit™ devices and technologies. Following a stint in resistive memory development, she has been a senior microelectronics specialist in the components assurance office of the Jet Propulsion Laboratory of California Institute of Technology and the National Aeronautics and Space Administration of the United States. Dr. Yang-Scharlotta holds more than 70 U. S. patents and authored publications on memory devices and technologies. Her research interests include memory technologies, electronics and materials in radiation and extreme environments, physics of failure, interfacial phenomenon and technology development.*

Mohammad Ashtijou *is an Electronics Engineer at JPL. He received his B.S. in Electrical Engineering from Clemson University, Clemson, SC, and his M.S. and Ph.D. degrees in Electrical Engineering from the University of Alabama, Tuscaloosa, AL. He has 30 years of electronics engineering experience and was a tenured professor of electrical engineering at Texas A&M University-Kingsville. Since starting work at JPL in 2004, he has contributed and lead flight electronics subsystem development, testing, and advanced technology development for space craft avionics and radar instruments for Mars, Earth, and Deep Space Exploration.*

Mohammad Mojarradi *is a seasoned NASA expert in electronic components and the design of advanced integrated mixed signal/mixed voltage electronic circuits for extreme environments. He is presently the manager of Component Engineering and Assurance office at JPL. Prior to this position, he was the group supervisor for advanced instrument electronics and the acting group supervisor for flight instrument electronics. In this position, he has was involved with the successful completion and delivery of electronics for MSS, COWAR and has successfully developed, qualified and delivered low temperature integrated components for the Motor Controllers (DMC) for MSL. In addition to his present responsibilities, Dr. Mojarradi is also serving as the lead NASA SBIR subtopic manager on extreme environment systems and as the chair for the Extreme Environment session of the IEEE Aerospace conference. Dr. Mojarradi received his Ph.D. in Electrical Engineering from UCLA in 1986. He has more than thirty years of combined industrial and academic experience in his field. He holds twenty-seven patents and eighty refereed publications. Prior to joining Jet Propulsion Laboratory, he was an associate professor at the Washington State University and the manager of the mixed voltage specialty integrated circuits group at the Xerox Microelectronics Center in El Segundo California.*