

LArIAT Analog Electronics

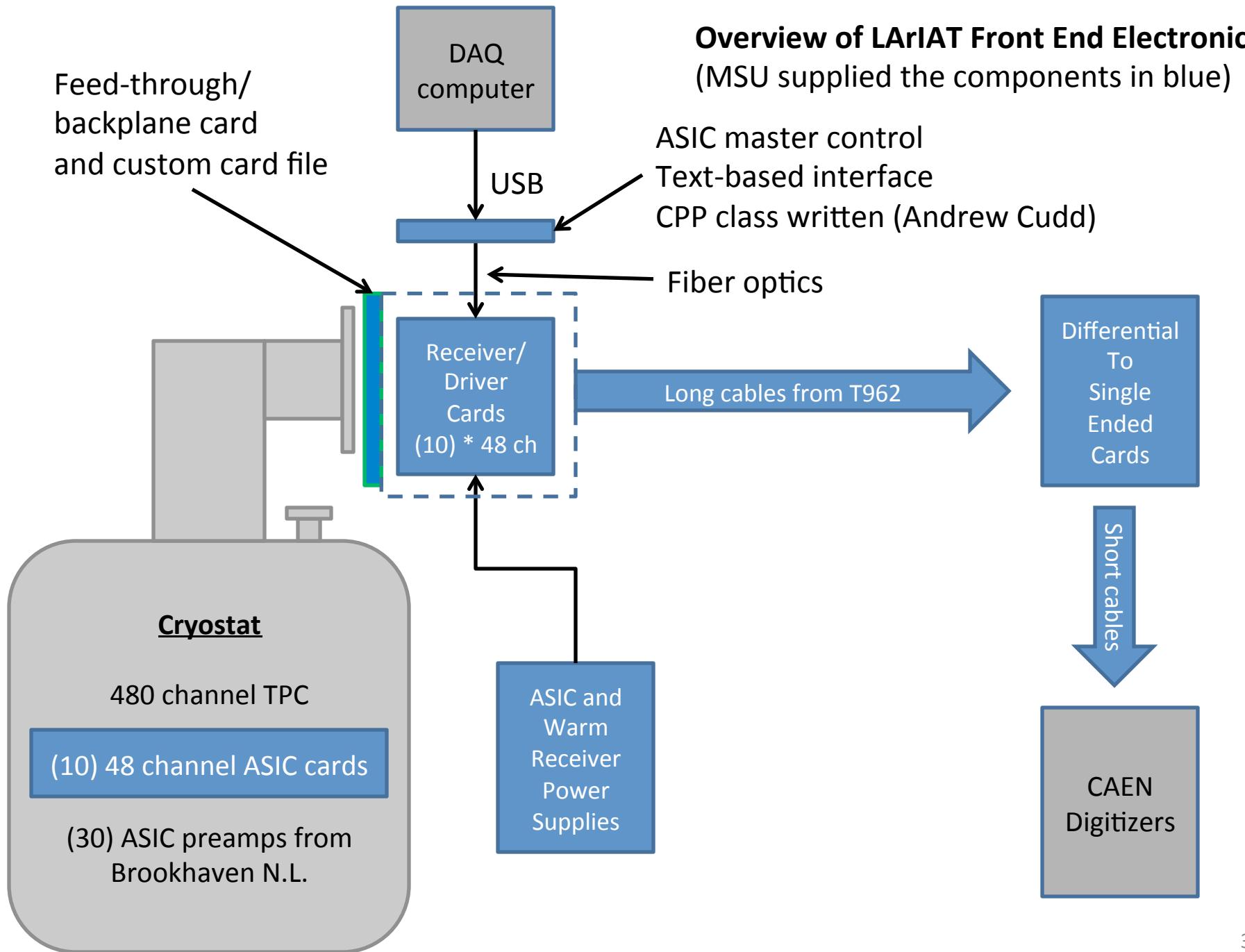
ORR October 13, 2015

Carl Bromberg, MSU
Dean Shultz, contract EE

Funding of LArIAT Analog Electronics

In response to specific requests
DOE directed funds (\$30k) for design/prototyping
NSF grant (\$45.5k) to MSU for production

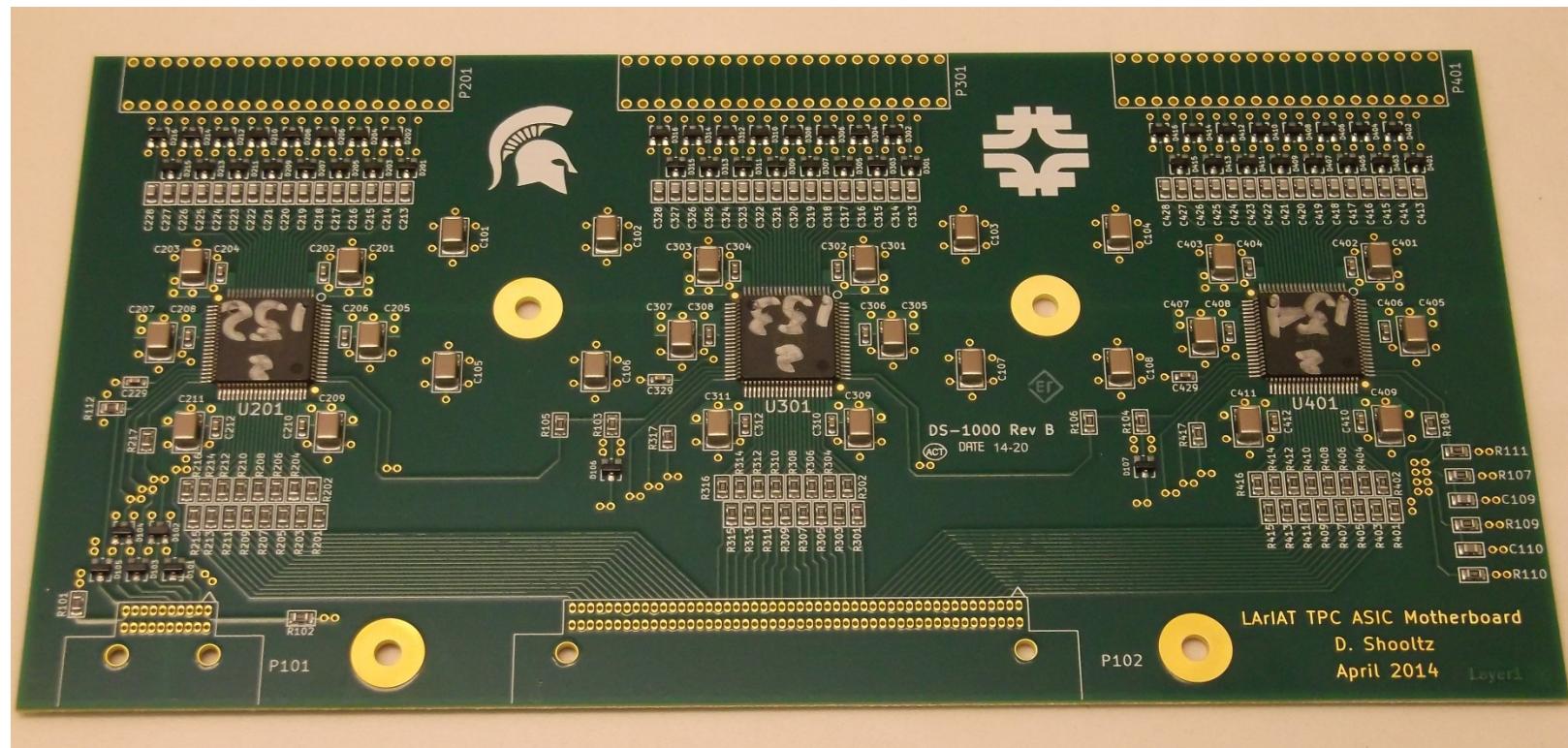
35 BNL ASICs from MicroBoone production run



BNL ASIC Preamp Motherboards (PMB)

14 cards were produced. 10 needed LArIAT TPC.

Basic operation tested warm at MSU and
at LN2 temperature just prior to installation.



10 PMB installed on TPC

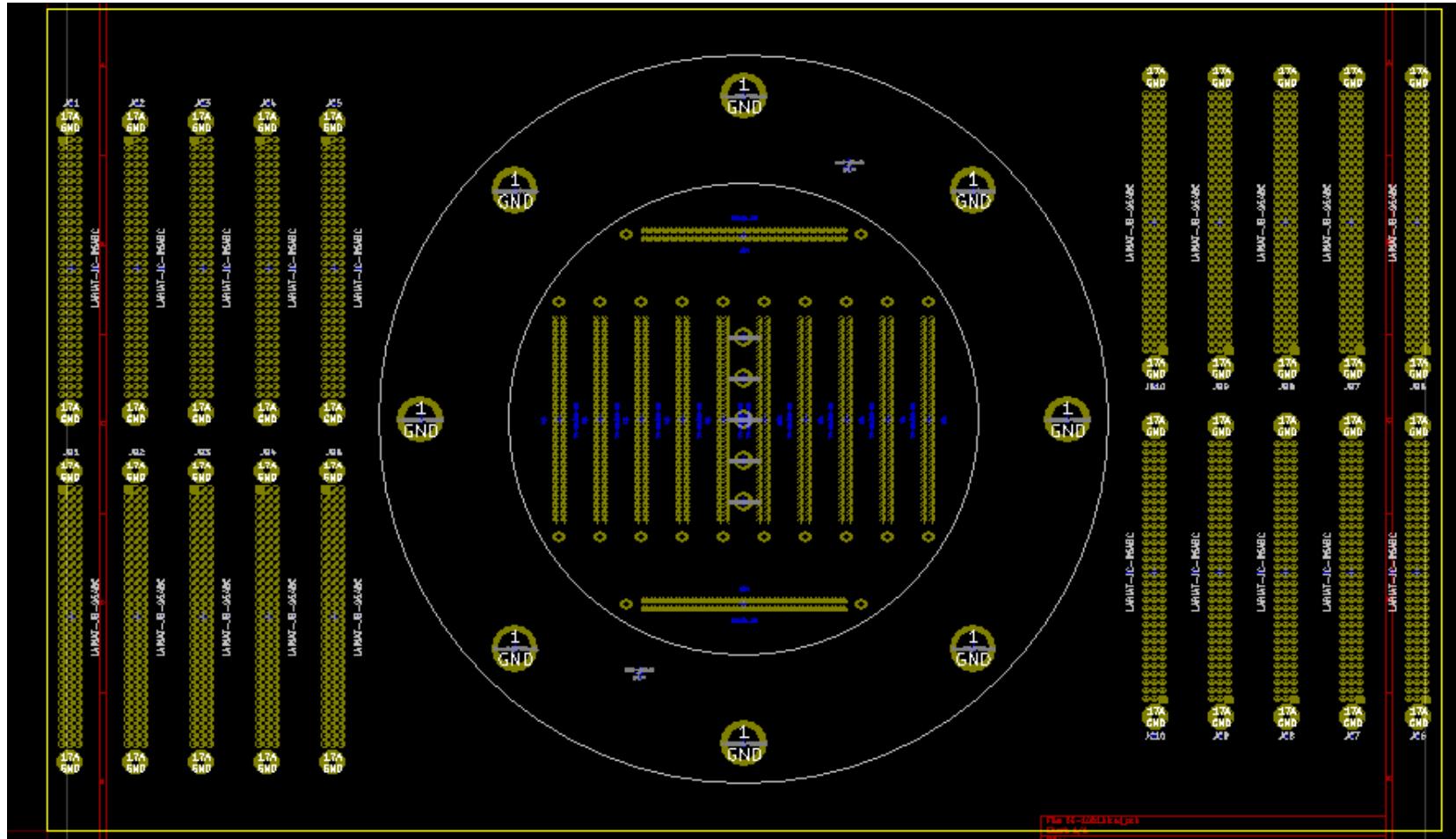
Cabled as TPC inserted in Cryostat.



New Cryostat feedthrough/backplane

17" x 10" 8-layer card.

Distributes PMB power & digital ASIC controls
Feed-through for analog signals to warm receivers



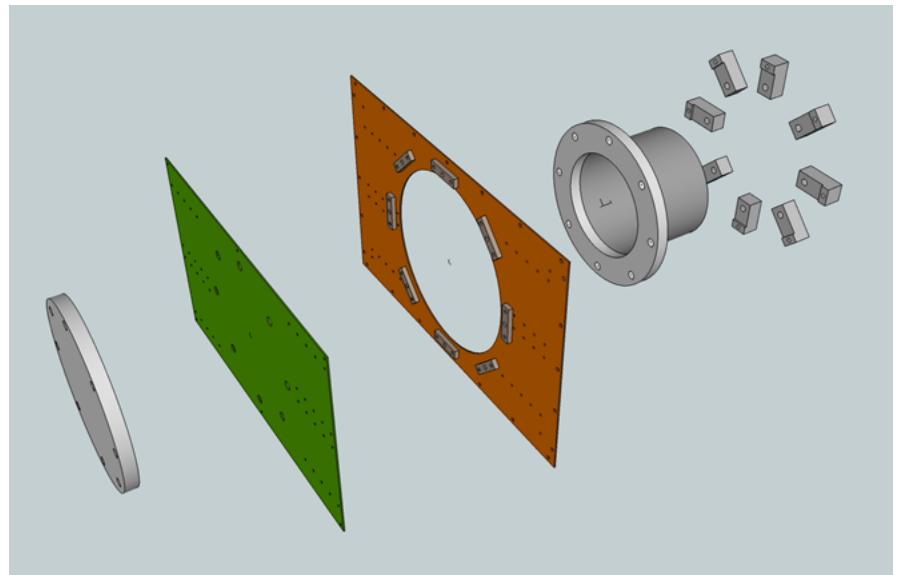
LArIAT TPC feed-through.

LArIAT TPC feed-through Installed

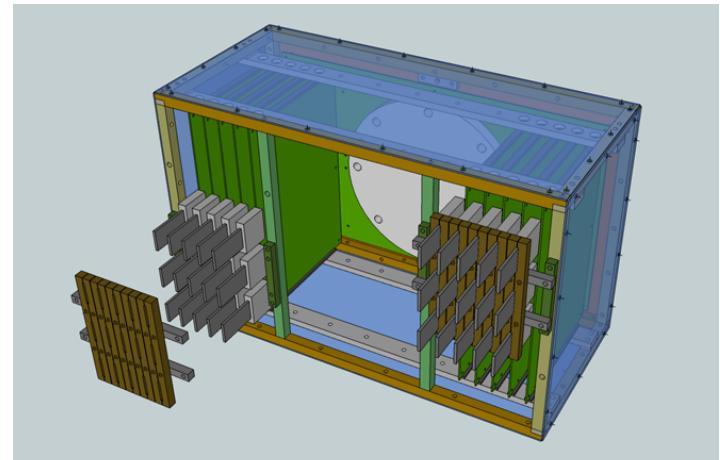
Feed-through/backplane card
mounted to the cryostat flange



Feed-through/backplane card assembly



Warm Receiver/Driver Crate

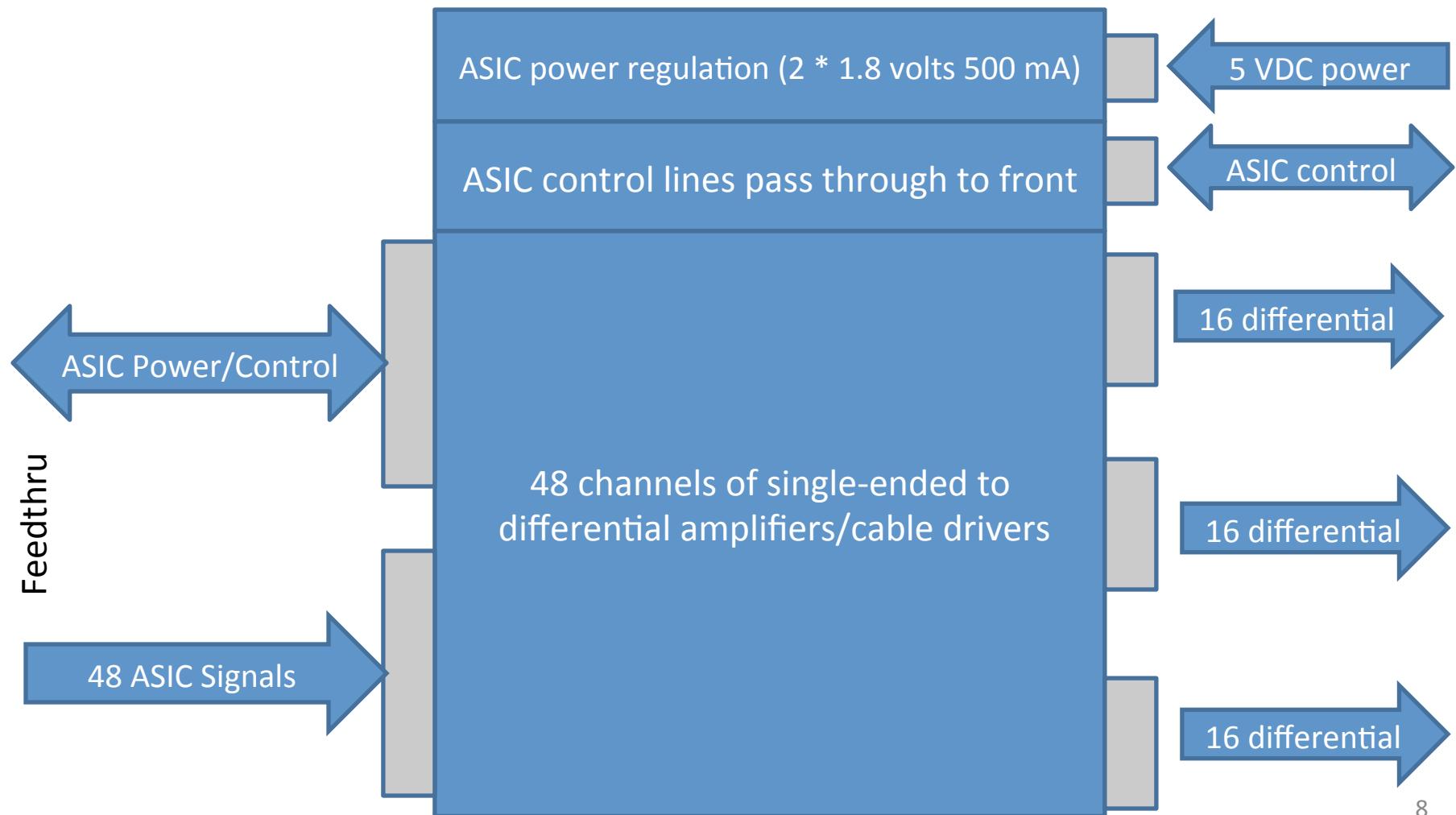


Warm Receiver/Driver (WRD) card layout

Each warm receiver card supplies power and control signals to one 48 channel ASIC motherboard.

The ASIC control lines are routed to the front panel.

From the front panel the ASIC control lines are daisy chained and then connected to fiber optic links.



Warm receiver/driver design: 10" x 7" pcb
(orientation reversed from previous slide)

Voltage monitor lines

Analog test signal input

Status LEDs

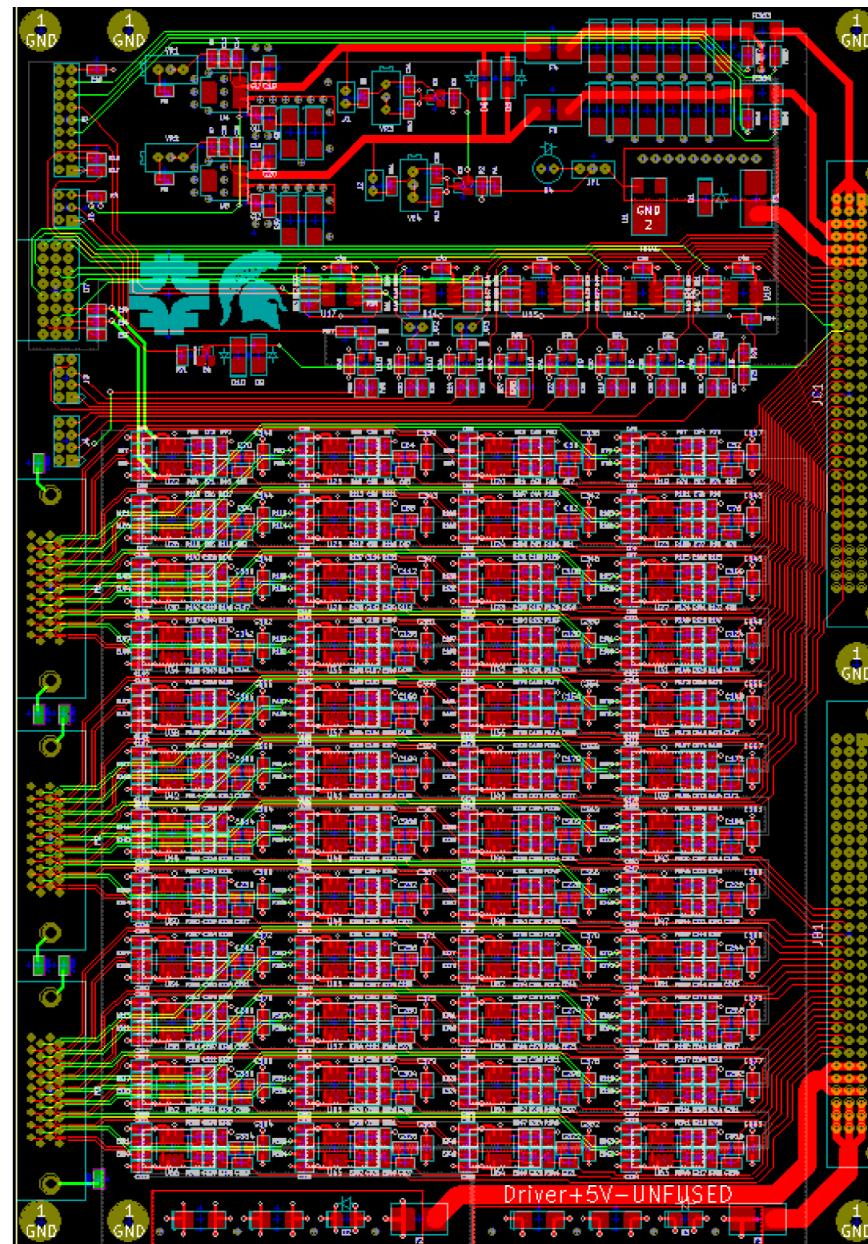
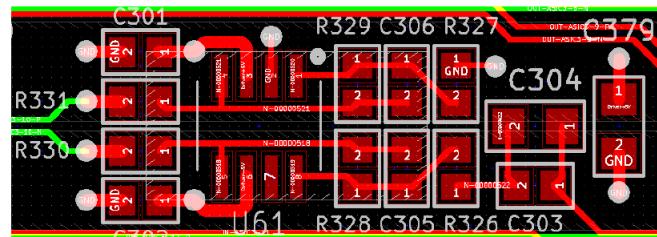
ASIC control

4 bus lines (CLK, CS, RESET, TEST)
1 daisy chained line (SDO → SDI)

16 differential signal outputs

16 differential signal outputs

1 of the 48 differential driver channels



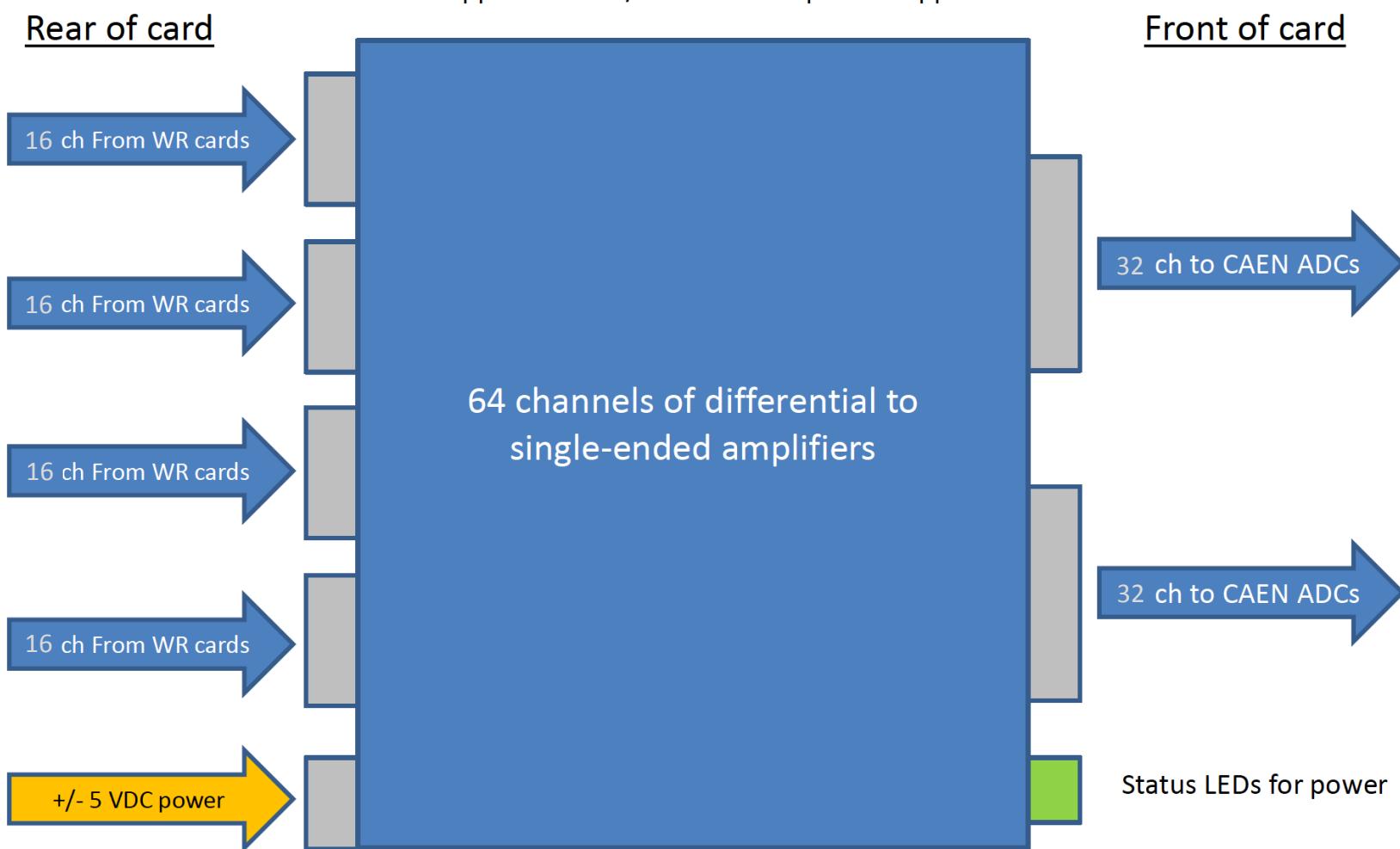
Backplane connector
Backplane connector

D2S (64 channels of differential to single-ended) card

Cards reside above CAEN ADCs in VME crate

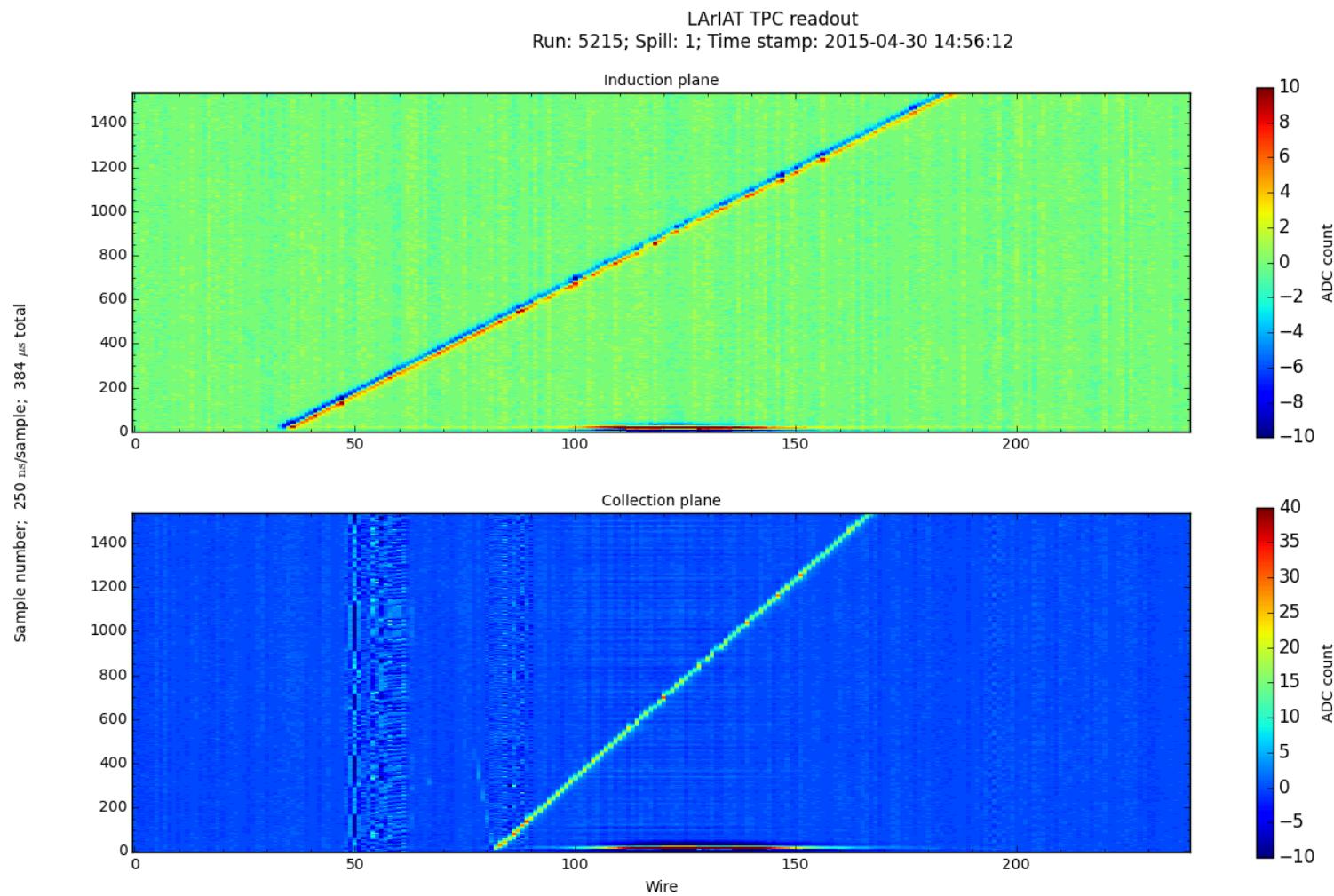
Cards supplied from MSU 5 volt power supplies.

Outputs to CAEN units on ~30 cm ribbon cables (rear of D2S to front of CAEN)

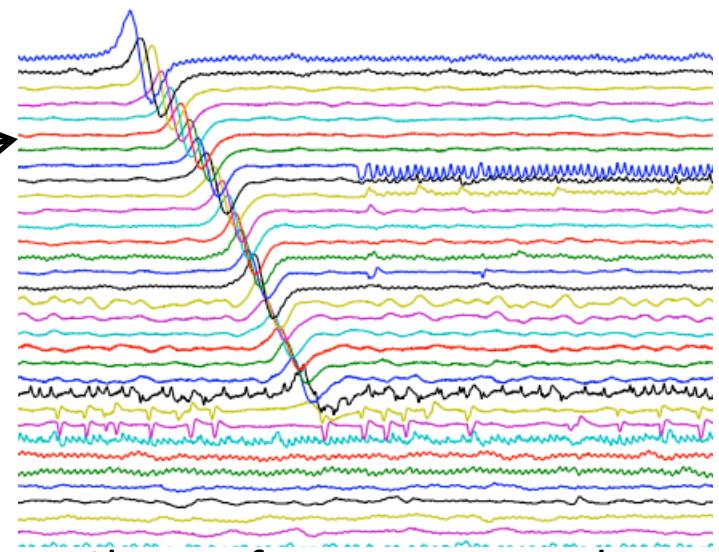
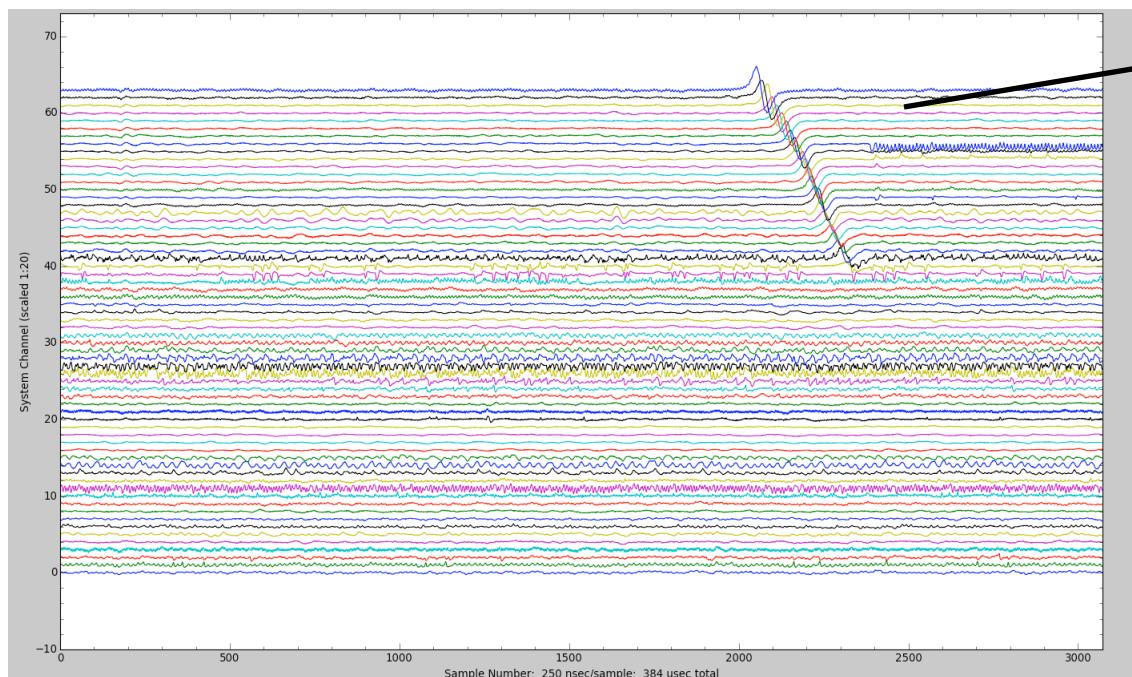
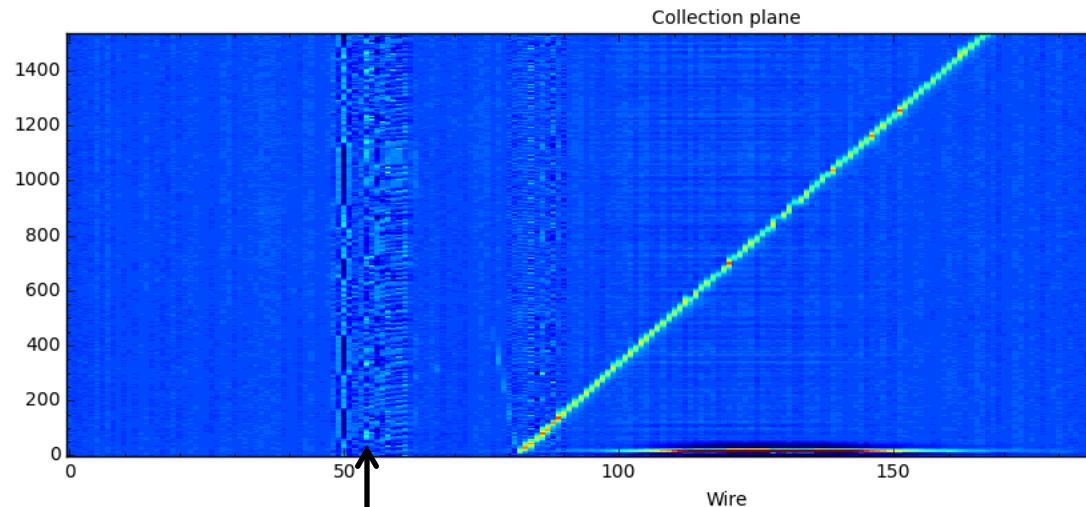


Excellent S/N Performance

(Raw signal to noise ~50/1)



An Issue of concern



Clears after a power cycle
Slowly returns over 10's of spills
Can be filtered out

Another Issue of concern

Corruption of ASIC Digital Controls in the Continuous shift register of 30 x 136 bits

Correct bits
are shifted up

A few times/day

Correct bits are shifted up

To minimize the amount of data affected
correct bits downloaded after each spill

Intentionally generated noise sources DON'T cause the corruption

0 or 1 bits
inserted

\longleftrightarrow 30 ASICs \longrightarrow

Action Items

Corruption and oscillation issues reported to BNL, but they cannot duplicate these issues on the bench.

Could still be a problem with our warm components.

Further investigations being planned before beam returns.

But analysis indicates that LArIAT physics goals are NOT in jeopardy.

Nevertheless, BNL ASIC is the baseline preamp for SBN and DUNE so a resolution is of considerable interest.