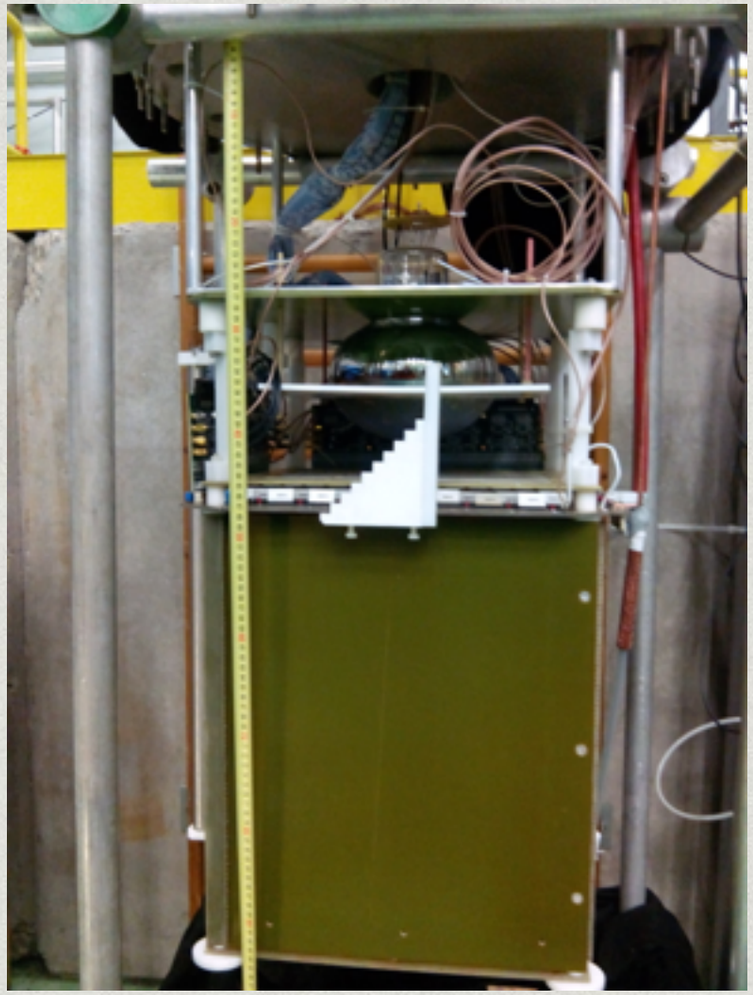
Idea for a FELIX demonstrator

in the 50 l LAr-TPC @ CERN

FLIC test-facility

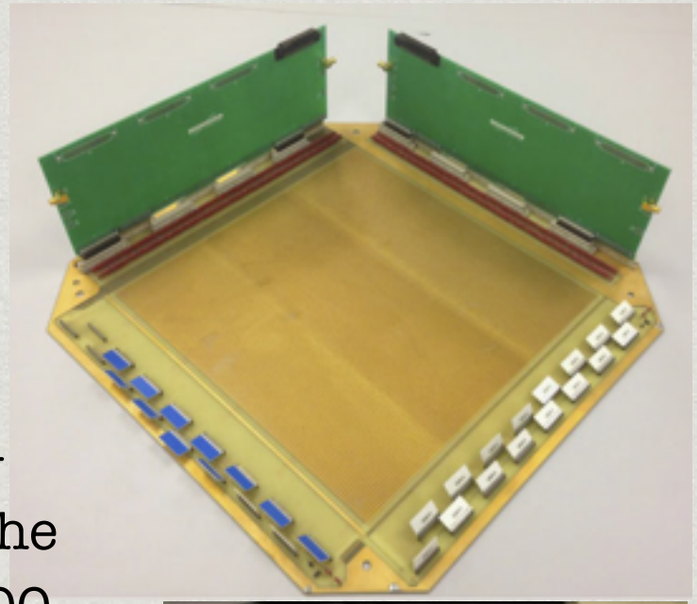
Possible application of the FELIX cards to neutrino detectors might be investigated exploiting the ~ 50 l LAr-TPC test facility (FLIC) installed @ CERN building 182, presently being used for several tests in the framework of ICARUS-WA104 activities.



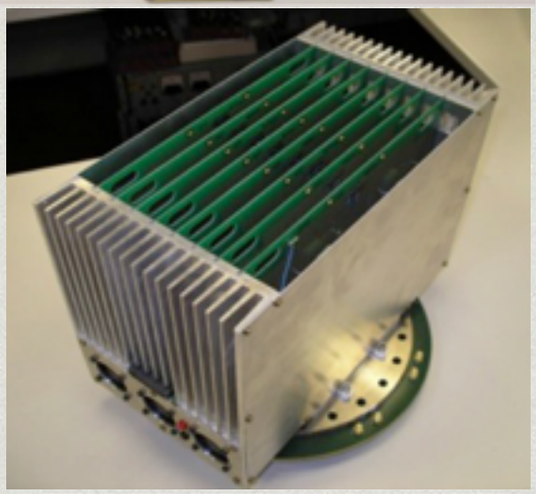
- The TPC has 2 32 x 32 cm^2 horizontal electrode planes, 47 cm drift ==> 65 kg of active mass.
- The anode consists of 2 parallel wire planes (Induction and Collection) spaced by 4 mm, each made of an array of 128 stainless steel wires, 100 μm diameter and 2.54 mm pitch; wires directions in these two planes are orthogonal with respect to each other.
  An additional grid 5 mm in from of Induction plane, electrically biased but not read-out, acts as electromagnetic shield.
- Uniform 500 V/cm electric field in the drift volume; biasing of grid, Induction and Collection -350, 0 and +400 V respectively to ensure full transparency.
- Trigger:
  - 1 Hamamatsu R5912-02MOD (14 dynodes) PMT, 8” diameter, evaporated with a TPB layer for wavelength shifting, installed on top of anodic planes over an additional shielding grid for mitigating induction of PMT signals on wires;
  - 2 external plastic 10*30 cm^2 scintillation slabs, equipped with 1 PMT each.

Readout electronics: setup & upgrades

- Signals extracted from the 128 TPC wires in each plane are pre-amplified in cold by a set of CMOS ASIC's with customisable gain and shaping time, mounted on a PCB mother board directly connected to the TPC wire frame.
  Design developed on purpose by a BNL team.



- A prototype of the new electronics, being developed by ICARUS-Padova group in collaboration with CAEN in the framework of the overhauling activities in view of the exploitation of ICARUS-T600 detector in the SBN Program at FNAL.

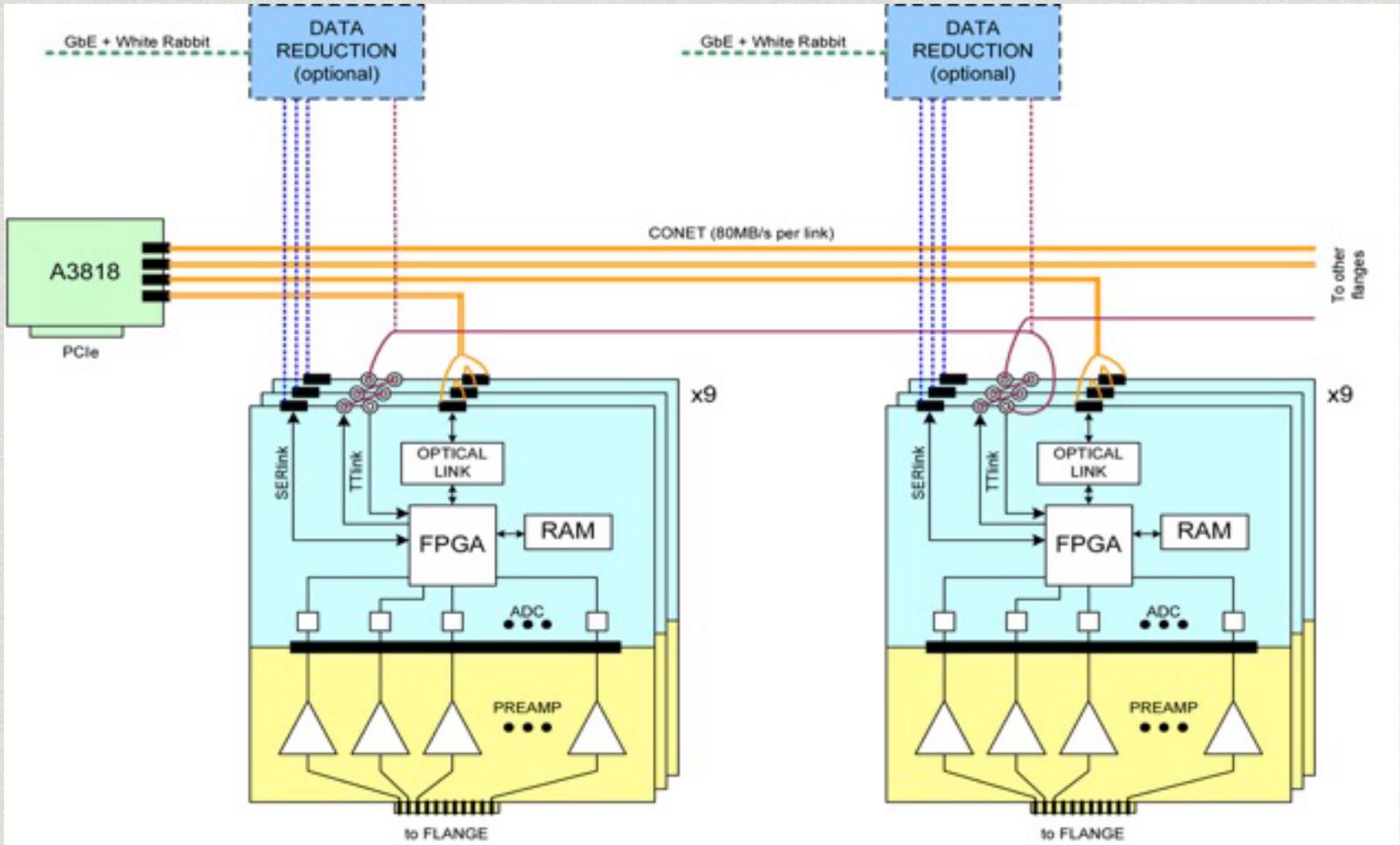


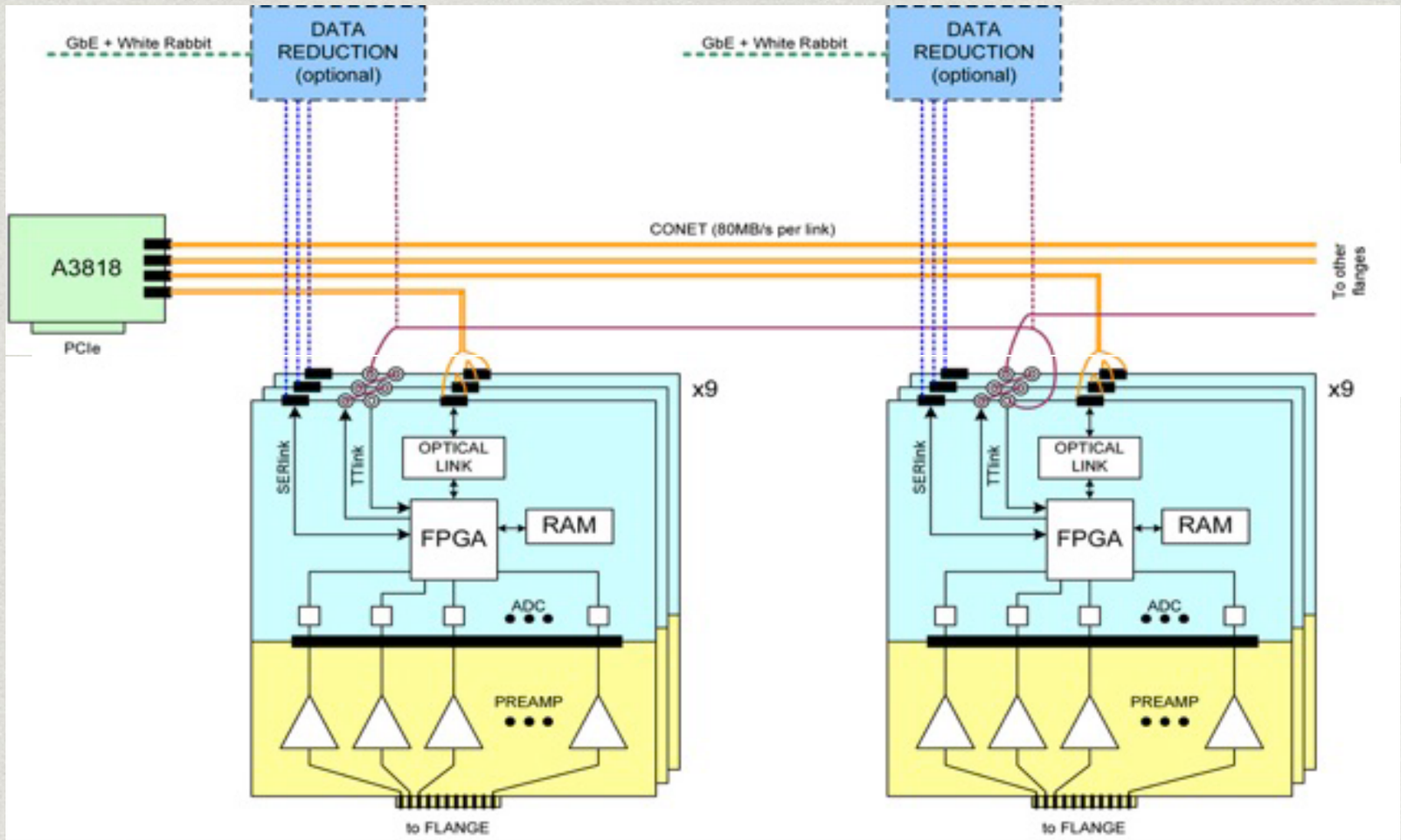
- A compact custom crate, mounted directly on the feed-through, houses 9 readout boards CAEN-A2795, serving 64 channels each. The backplane distributes the power lines, some control signals and the TT-Link and a differential M-LVDS signal used for distributing a 10 MHz clock and other global commands.

- The 64 signals are digitized by 12 bit 2.5MS/s serial ADCs and continuously readout in parallel by a single programmable Altera FPGA, which provides the trigger logic, the data storage in local circular memory buffers and the readout through a bi-directional 1.25 Gbit/s optical link.
- Readout of all boards in a crate is configured in daisy-chain.

Present DAQ architecture

- FPGA onboard drives the optical link over a proprietary CONET-2 (Chainable Optical NETwork) protocol, exploiting a multimode 62.5/125 μm fiber with maximum length of 200 m, equipped with a Duplex LC connector.
- A basic data format is adopted, i.e. header carrying info on crate and board IDs, followed by arrays of the absolute ADC value of the waveforms recorded by the 64 channels at each time sampling.
- The receiver at the other end is the CAEN PCI express board A3818, installed in a PC.
- A software package has already been developed to decode these packets and perform the event building to produce in output binary files with a ICARUS-like format.



Integration of FELIX

- FELIX cards might be adopted in place of the CAEN A3818 with the main advantage of replacing the private CONET-2 optical link with a commercial Ethernet one.
- The only requirement on the front-end side is the development of a new Firmware to be installed in the Altera FPGA's on the digital boards in order to drive the output optical link with a new protocol compatible with the FELIX (at present GBT).
- Event building must be modified.
  A possible approach is to start from the software developed to readout the A3818 boards and replace the libraries for the interface to the CONET-2 link with the ones used in ICARUS run at LNGS, provided that data packets are standard TCP/IP.
  ==> The rest of the data flow would be transparent.