R&D for Dark Energy Science

Imaging Sensors (Thanks to P. O'Connor (BNL), C. Bebek (LBNL), C. Leitz (LL)

- CCDs
- CMOS
- Ge-CCDs

21-cm Experiments (A. Liu will talk at SLAC Workshop)

Other Activities (not covered)

- Wide field adaptive optics
- Simulations, Algorithms, Computing

MKIDS J. Estrada

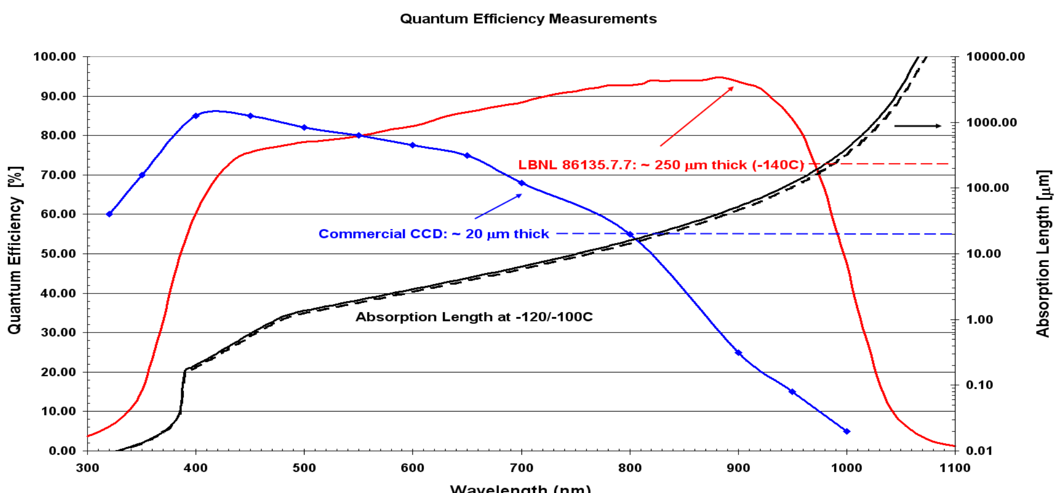
OH-Suppression With Ring-Resonators S. Kuhlman

K. Honscheid
Ohio State University
CV@FNAL 11/10/15

Detector R&D Critical for DE Missions

Intensive DoE-supported R&D enabled current DE missions.

– Fully depleted red-sensitive CCDsdeveloped by LBNL currently in use for DES and to be used for DESI.

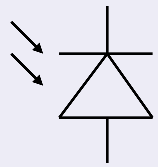
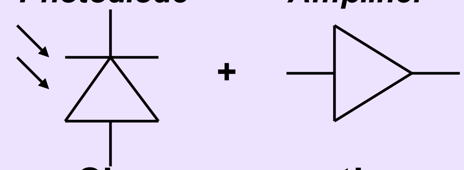
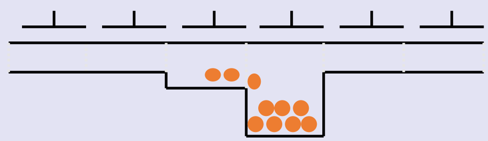
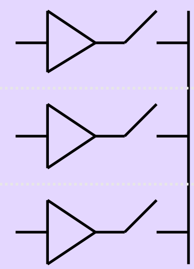
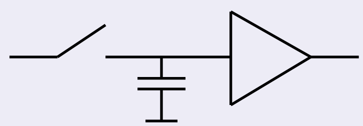


– Detailed studies of HgCdTe FPAs has led to greatly improved properties (QE, read noise, dark current…) and has led to a new detailed understanding of photometric response.

– What will be the next enabling technology?

Greg Tarle
Snowmass 2013

CCD and CMOS Detector Concepts

	CCD Approach	CMOS Approach
Pixel	*Photodiode*  Charge generation & charge integration	*Photodiode* + *Amplifier*  Charge generation, charge integration & charge-to-voltage conversion
Array Readout	 Charge transfer from pixel to pixel	 Multiplexing of pixel voltages: Successively connect amplifiers to common bus
Sensor Output	 Output amplifier performs charge-to-voltage conversion	Various options possible: - no further circuitry (analog out) - add. amplifiers (analog output) - A/D conversion (digital output)

M. Loose
Rockwell Scientific

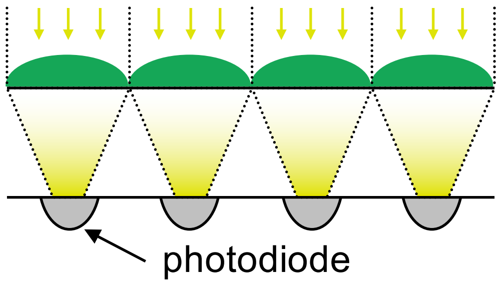
CMOS Common Features

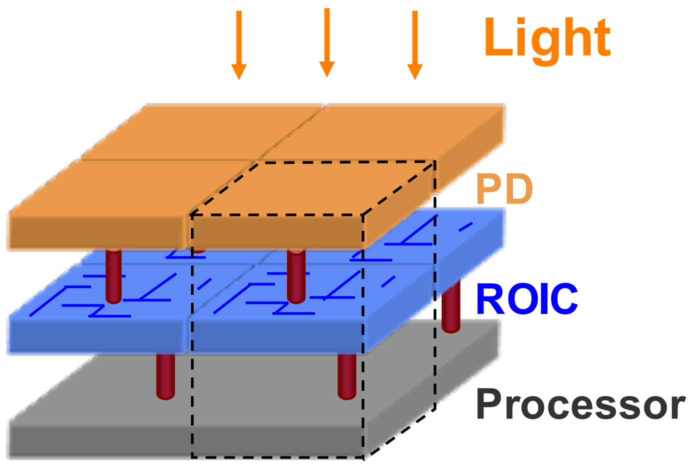
- CMOS sensors/multiplexers utilize the same process as modern microchips
  - Many foundries available worldwide
  - Cost efficient
  - Latest processes available down to 0.13 µm
- CMOS process enables integration of many additional features
  - Various pixel circuits from 3 transistors up to many 100 transistors per pixel
  - Random pixel access, windowing, subsampling and binning
  - Bias generation (DACs)
  - Analog signal processing (e.g. CDS, programmable gain, noise filter)
  - A/D conversion
  - Logic (timing control, digital signal processing, etc.)
- Electronic shutter (snapshot, rolling shutter, non-destructive reads)
  - No mechanical shutter required
- Low power consumption
- Radiation tolerant (by process and by design)

CMOS Status and R&D

- **Photodiode and transistors share the area -> less than 100 % fill factor**

Microlenses increase fill factor:





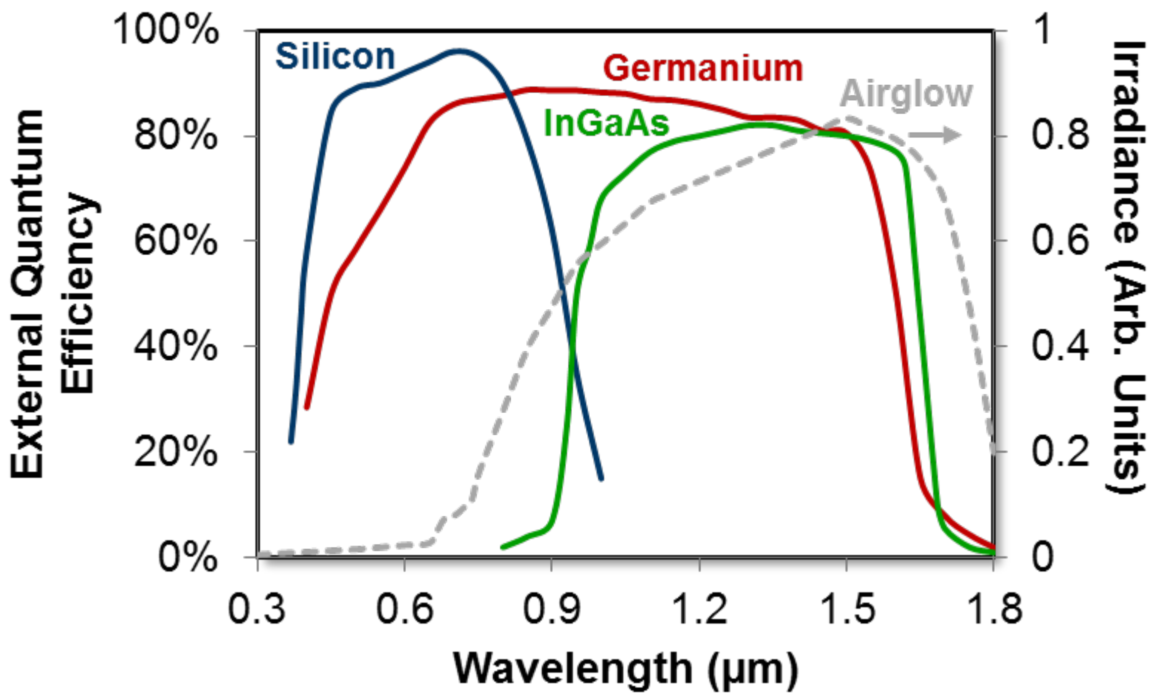
Vertical Integration

- **Fast readout rates (MHz) and low noise (1e-); low power**
- **Ongoing efforts on back side illumination and high resitivity, thick devices**
- **Low full well, low QE, low(er) chip size compared to CCDs**
- **So far disappointing performance when hybradized to silicon**
- **Commercial advantage not fully realized (spezialized processing needs)**

Ge CCD R&D

(thanks to Chris Leitz, Lincoln Labs)

- **Strong absorption from UV through short-wave infrared (SWIR)**



- **Recent advances in Germanium process technology enables fabrication of large, high quality devices**
- **200 mm wafers available (larger than for other SWIR technologies)**
- **Relatively high dark current due to high intrinsic carrier concentration**
  Requires cooling (goal 400 e-/pixel/s)

Germanium CCD Roadmap

2016: 512 × 512

2017: 1k × 1k

2019: 2k × 2k

Metric	2016 Goal
Frame Rate	4 fps
Read Noise	10 e^-
QE	> 60% (400-1600 nm)
Well capacity	> 100 ke^-
Features	• TDI / Pushbroom easily implemented • On-chip binning w/o read noise penalty

Increase format as high charge-transfer efficiency and uniformity realized.

C. Leitz
Lincoln Labs