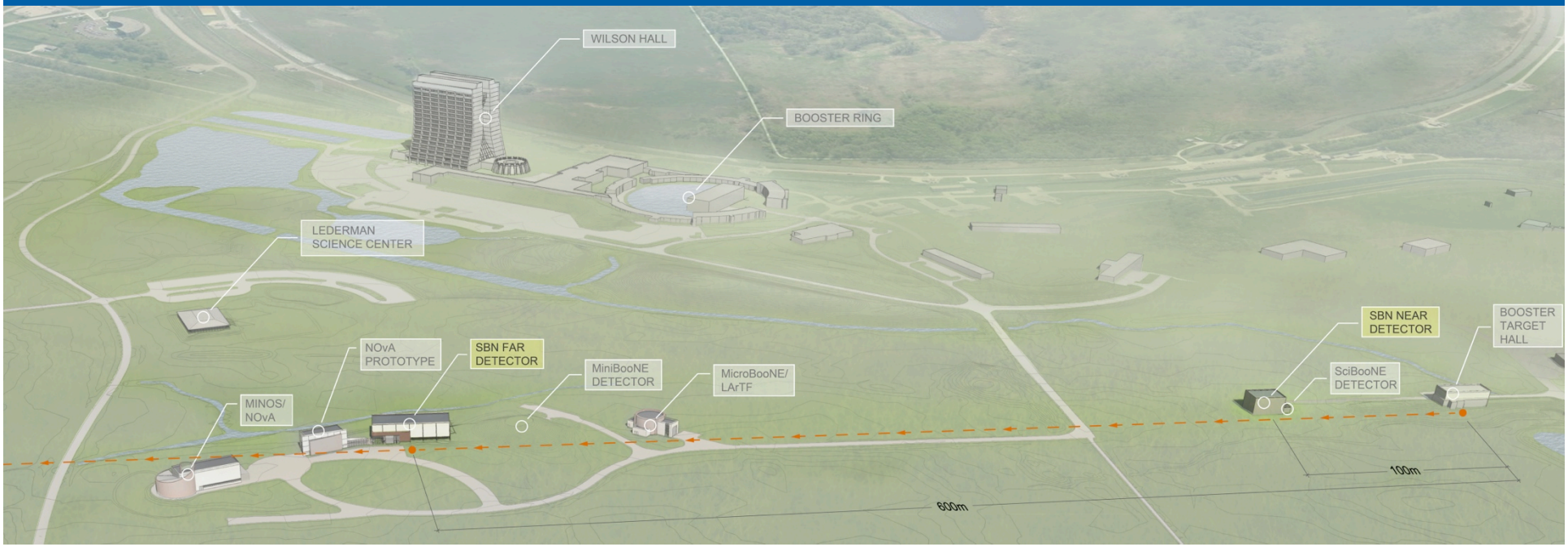


SBND TPC Electronics System

Hucheng Chen – Brookhaven National Laboratory

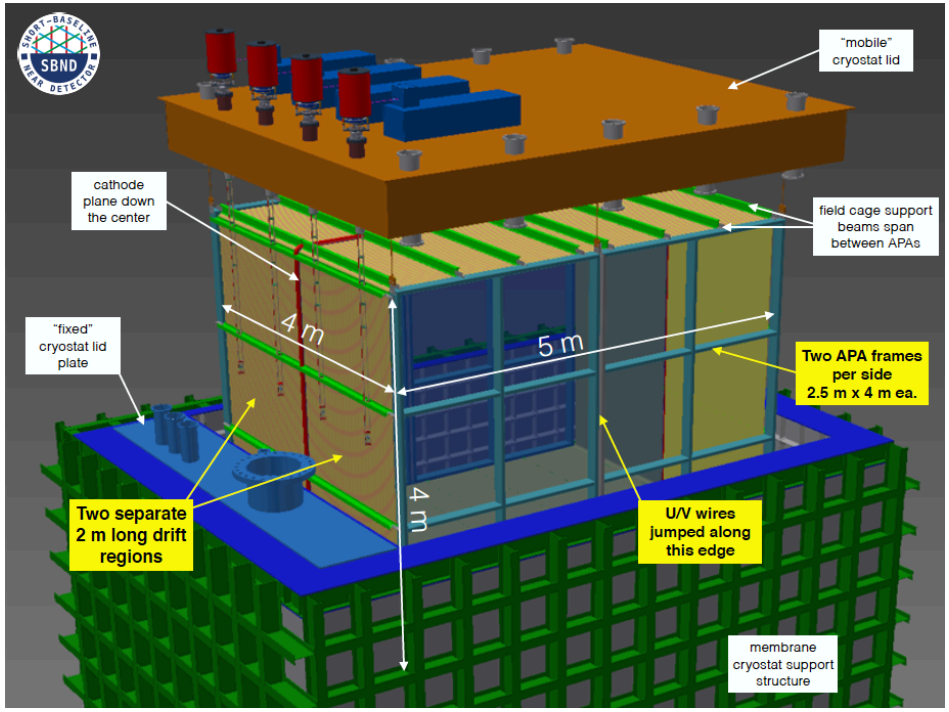
Director's Progress Review of SBN

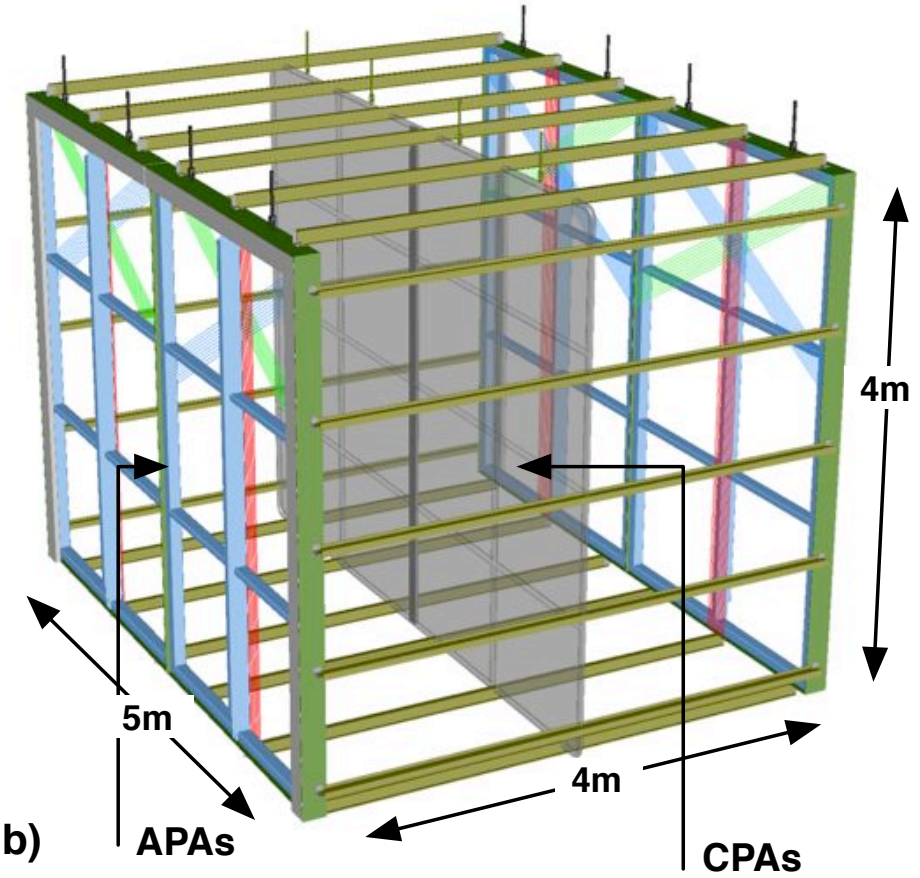
15-17 December 2015

Outline

- System Overview
- Interfaces
- Resources
- Basis of Estimate
- Schedule and Cost Summary
- ES&H and QA
- Response to technical review recommendations
- Status of design

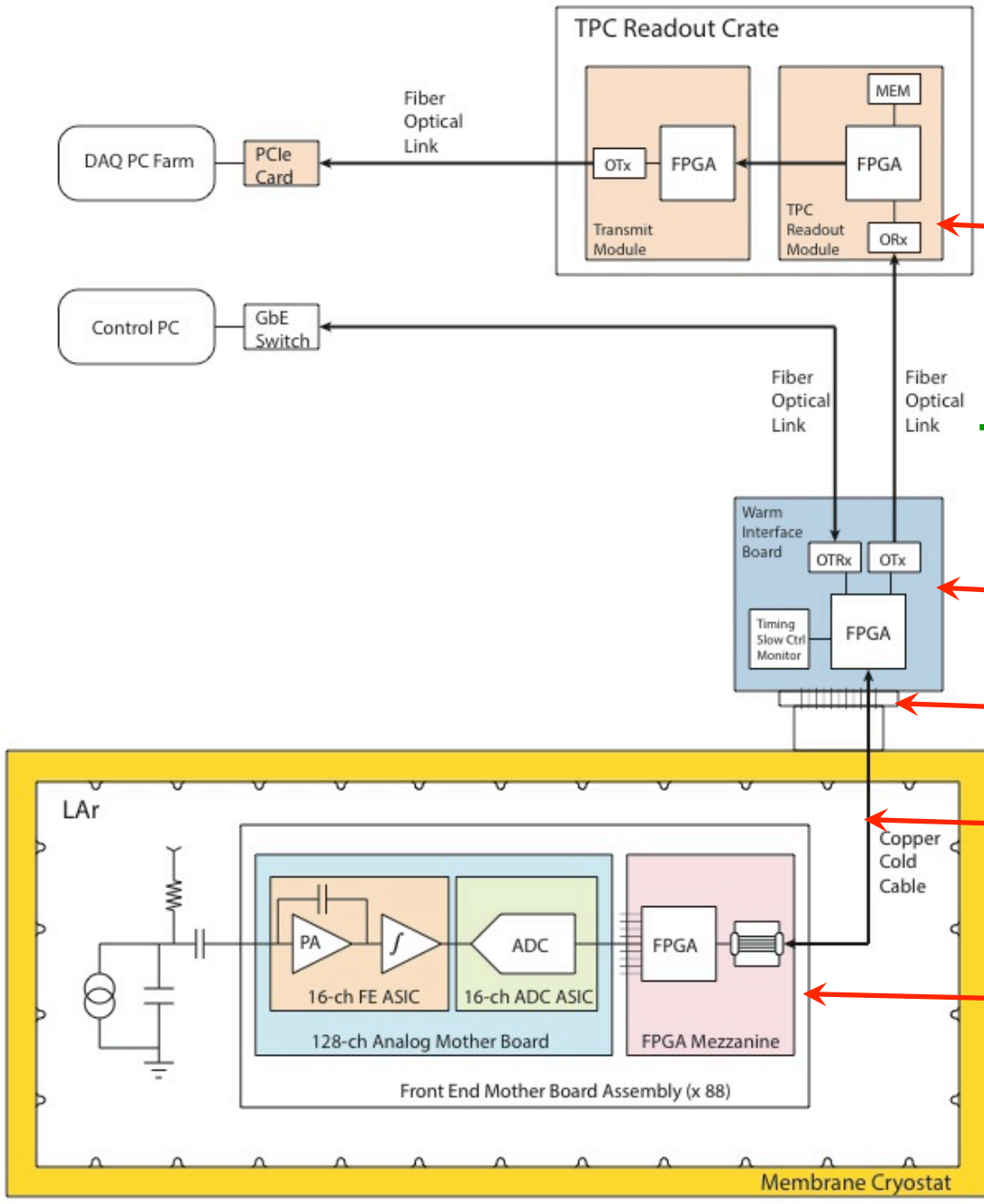
SBND TPC





- SBND TPC: 4 APAs and 2 CPA

SBND TPC Electronics System



TPC Readout Electronics

Back End Electronics

Front End Electronics

Warm Interface Electronics

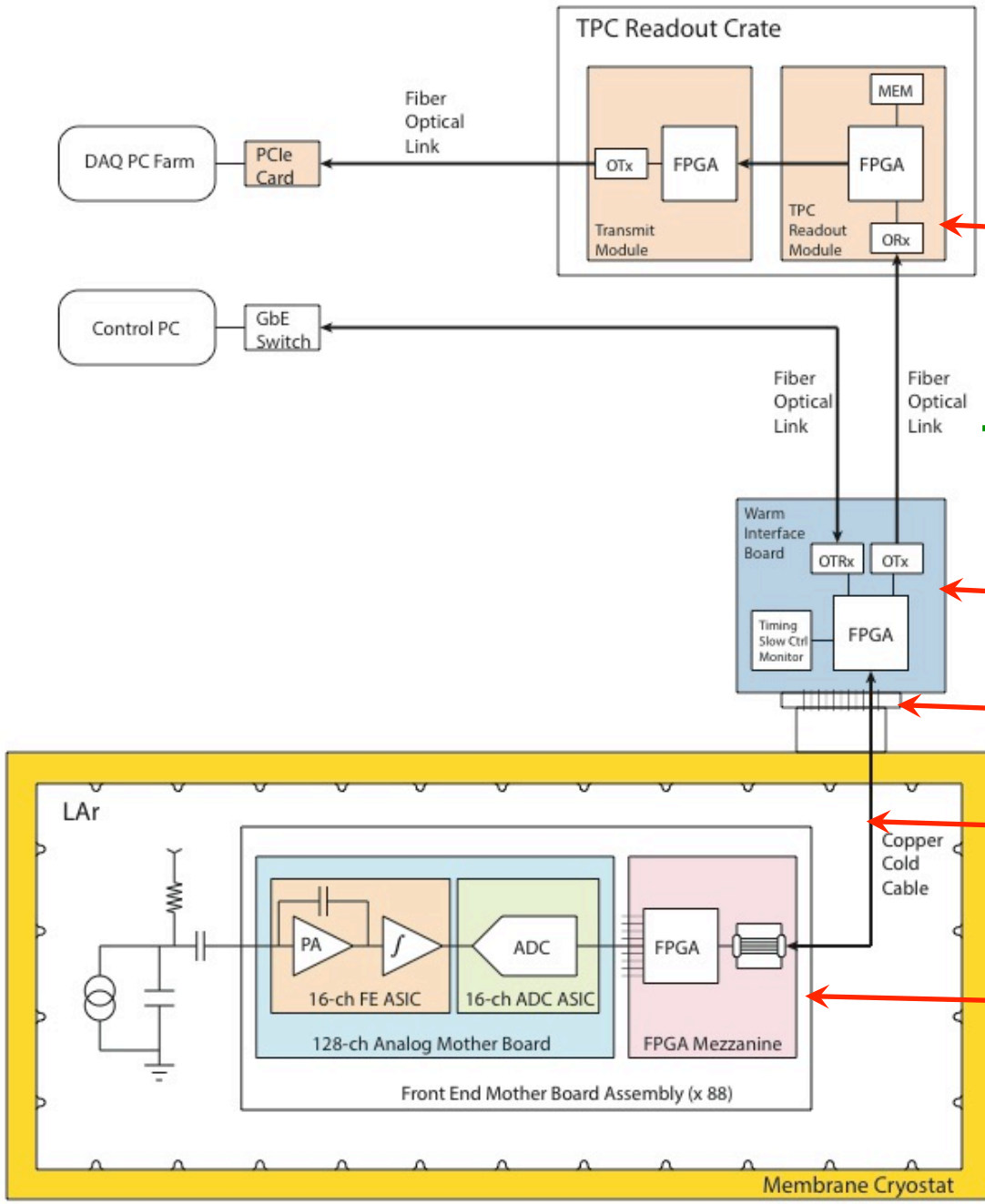
Signal Feed-through

Cold Cable

Cold Electronics

Fermilab

SBND TPC Electronics System



TPC Readout Electronics

NSF – BE Electronics

DOE – FE Electronics

Warm Interface Electronics

Signal Feed-through

Cold Cable

Cold Electronics

Fermilab

System Requirements

- Read out 11,264 channels of TPC sense wires
  - 3968 U channels, 3968 V channels, 3328 Y channels
- Noise: ENC < 820 electrons with 1 us shaper peaking time
  - Signal to noise ratio is better than 10:1, *a conservative estimate*
  - Distinguish 3 fC (18k electrons) wire signal (1 MIP) from noise with high efficiency at the longest drift time (1.25 ms) with an electron lifetime of 1.6 ms
- Dynamic Range: < 500:1
  - Physics signal dynamic range * 10:1 signal/noise requirement
- Shaper Peaking Time: ~ 1 us
  - The average electron diffusion over the drift distance is ~ 1 us
- ADC Sampling Rate: ~ 2 MHz
  - The sampling rate should be at least 2/(shaper peaking time)
- ADC Resolution: ~ 12 bit
  - Minimize the rate of ADC overflow for low momentum, highly ionizing particles

System Requirements

- Neutrino Stream
  - Readout neutrino data upon appropriate trigger, compress it losslessly, format it and send it on to storage
- SuperNova Stream
  - Readout SuperNova data continuously using a lossy compression and store it temporarily awaiting for external SNEWs network alert

Difference/Similarity between MB and SBND

- MicroBooNE and SBND TPC readout electronics systems share many common features in the BE
- Major differences
  - ADC is moved from warm (MicroBooNE) to cold (SBND)
  - Cabling between FE and BE is changed from copper cable for analog signal transmission (MicroBooNE) to fiber optical links for digital signal transmission (SBND)
- Similarity
  - Common FEM design for BE electronics, with a new functionalities for optical transceiver and deserializer
  - Same readout hardware (XMIT, CC, PCIe etc.) for DAQ system
  - Great leverage of past experience from MicroBooNE
  - Ease the development of both readout and DAQ system

Difference/Similarity between 35 Ton and SBND

- 35 Ton and SBND TPC readout electronics systems share many common features in the FE
- Major differences
  - Simplified cold cable design to eliminate the cold cable adapter board and improve the reliability
  - Optimized signal feed-through design and flexible warm interface electronics to interface to readout and DAQ system
- Similarity
  - Cold front end ASIC and ADC ASIC for TPC readout, with improved revision for SBND
  - Cold analog mother board and FPGA mezzanine to instrument APA, with different wire pitch for SBND
  - Great leverage of past experience from 35 ton for both board design and test stand development

System Scope

- ***11,264 channels (sense wires)***
- Cold Electronics
  - 704 FE ASICs
  - 704 ADC ASICs
  - 88 cold FPGA mezzanines
  - 88 cold mother boards

  } 88 front end mother board (FEMB) assemblies
- Cold Cable
  - 4 sets of cold cable
- Signal Feed-through
  - 4 sets of signal feed-through assemblies
- Warm Interface Electronics
  - 24 warm interface boards (WIB)
  - 4 power and timing backplanes (PTB)
  - 4 power and timing cards (PTC)
  - 1 slow control and timing interface board – magic blue box (MBB)

System Scope

- TPC Readout Electronics
  - 11 6U crates at 16 boards/crate
  - 176 Front End Modules (FEM)
  - 11 Backplanes
  - 11 Transmitter modules (XMIT)
  - 11 Controller modules
  - 11 Clock modules
  - 33 PCIe modules
  - 1 Fanout module
  - 1 Trigger module

Interfaces

- TPC Electronics System (WBS 2.6) have interfaces to the following systems
  - TPC (WBS 2.3)
  - PMT Light Detector (WBS 2.4)
  - Readout and DAQ (WBS 2.7)
  - Installation Coordination (WBS 2.8)
  - Cryostat (WBS 2.9)

Resources

- Institutes
  - Brookhaven National Laboratory (DOE)
  - Columbia University Nevis Labs (NSF)
- Individuals
  - Hucheng Chen (BNL)
    - Level 2 Manager
  - Leslie Camilleri (Nevis)
    - Deputy L2 Manager for TPC Readout Electronics
  - Elizabeth Worcester (BNL)
    - Deputy L2 Manager for System Integration & Installation
  - Bo Yu (BNL)
    - L3 Manager for Signal Feed-through and Cold Cable
  - Jack Fried (BNL)
    - L3 Manager for Warm Interface Electronics
  - New Hire acting by H. Chen (BNL)
    - L3 Manager for Cold Electronics

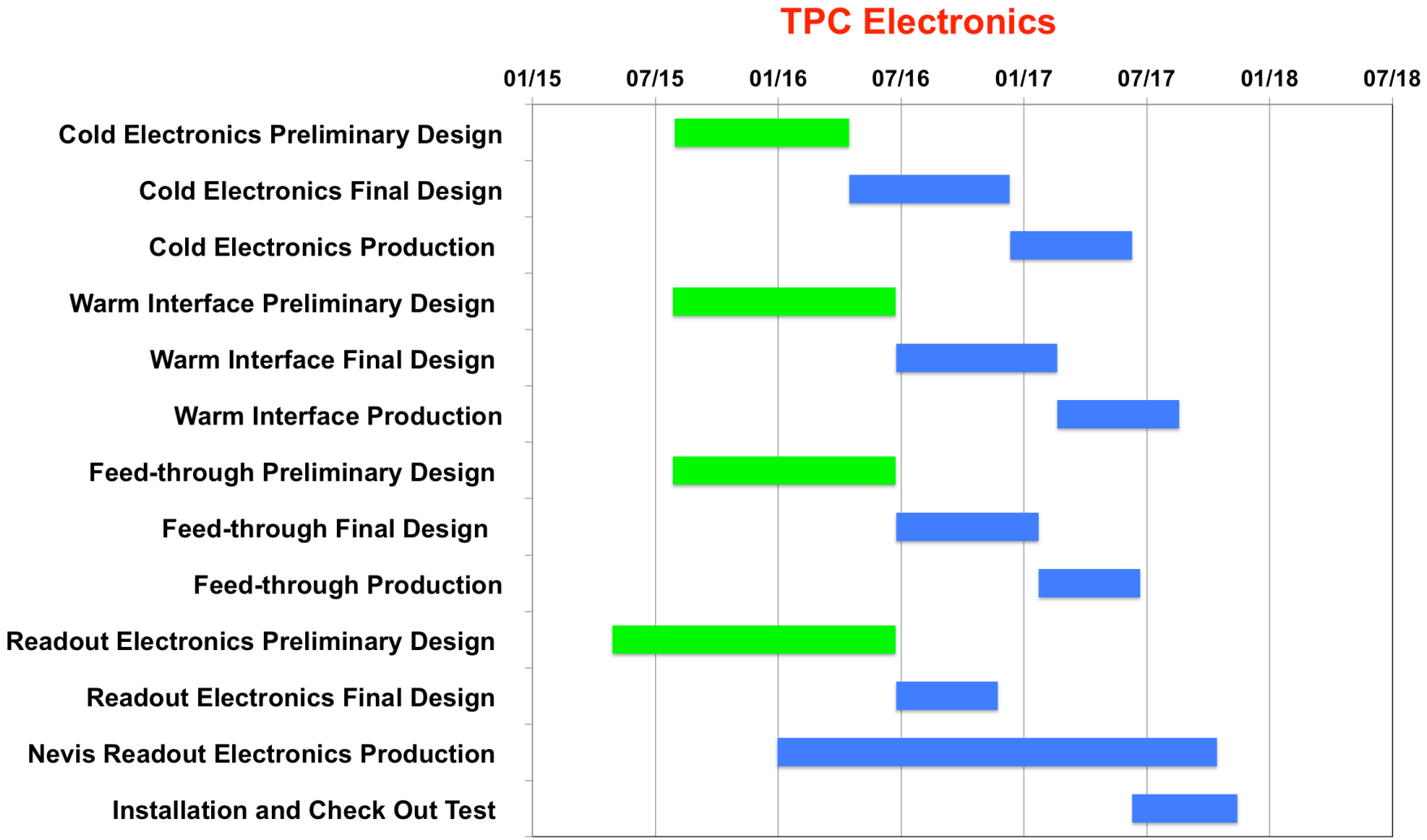
Resources

- BNL and Nevis Labs have been deeply involved in the MicroBooNE experiment, and had close collaboration on TPC readout electronics system for MicroBooNE
- BNL has started CMOS cold electronics R&D since 2008. Instrumentation Division microelectronics group has developed FE ASIC and ADC ASIC used in MicroBooNE and 35 ton
- Microelectronics group will continue the CMOS cold ASICs development for SBND and DUNE
- Currently 3 ASIC design engineers (G. De Geronimo, N. Nambiar and E. Vernon) and 2 ASIC design Ph.D. students (W. Hou and K. Yethiraj) are actively working on the cold ASIC design

Basis of Estimate

- Cost Estimate of TPC Front End Electronics
  - Cold electronics
    - SBND DocDB #239
    - Past experience (MicroBooNE, DUNE 35 Ton) and vendor quotes
  - Signal feed-through & cold cable
    - SBND DocDB #241
    - Past experience (MicroBooNE, ATLAS)
  - Warm interface electronics
    - SBND DocDB #240
    - Past experience (MicroBooNE)
  - Installation and Check Out Test
    - SBND DocDB #665
    - Past experience (MicroBooNE, ATLAS)
  - TPC readout electronics (NSF)
    - Past experience (MicroBooNE)

Schedule and Cost



Schedule and Cost

- Major milestones
  - Final Design Review
    - 2016/04: Cold electronics
    - 2016/06: Warm interface electronics
    - 2016/06: Signal feed-through and cold cable
    - 2016/06: TPC readout electronics
    - 2016/06: Joint BNL/Nevis integration test
  - Production Readiness Review
    - 2016/12: Cold electronics
    - 2017/02: Warm interface electronics
    - 2017/01: Signal feed-through and cold cable
    - 2016/12: TPC readout electronics
  - pORC Review and production completion
    - 2017/06: Cold electronics
    - 2017/06: Warm interface electronics
    - 2017/06: Signal feed-through and cold cable
    - 2017/10: TPC readout electronics
  - 2017/11: FE installation and check out test complete

Schedule and Cost

WBS	Task	Total Project Cost
2.6	**TPC Electronics**	**$ 4,461,488**
2.6.1	***TPC Cold Electronics***	**$ 2,077,432**
2.6.1.1	TPC Cold Electronics Preliminary Design	$ 616,412
2.6.1.2	TPC Cold Electronics Final Design	$ 651,938
2.6.1.3	TPC Cold Electronics Production	$ 809,082
2.6.2	***TPC Warm Interface Electronics***	**$ 706,357**
2.6.2.1	TPC Warm Interface Electronics Preliminary Design	$ 279,843
2.6.2.2	TPC Warm Interface Electronics Final Design	$ 236,475
2.6.2.3	TPC Warm Interface Electronics Production	$ 190,039
2.6.3	***TPC Signal Feed-through and Cold Cable***	**$ 1,038,216**
2.6.3.1	TPC Signal Feed-through and Cold Cable Preliminary Design	$ 341,922
2.6.3.2	TPC Signal Feed-through and Cold Cable Final Design	$ 345,861
2.6.3.3	TPC Signal Feed-through and Cold Cable Production	$ 350,433
2.6.4	***Nevis TPC Readout Electronics Design***	**$ 538,879**
2.6.4.1	TPC Readout Electronics Preliminary Design	$ 69,129
2.6.4.2	TPC Readout Electronics Final Design	$ 64,824
2.6.4.3	Nevis TPC Readout Electronics Production	$ 404,926
2.6.5	***TPC Front-End Electronics Installation and Check Out Test***	**$ 100,604**

ES&H, QA

- ES&H
  - All custom designed components will go through EDR & ORC before final production
  - Review documentations including drawings, schematics and layout etc. will be prepared by BNL and Nevis
  - Review will be organized by Linda Bagby at FNAL
- Quality Assurance Program
  - All custom designed components will go through QA/QC procedure before they are delivered to FNAL
  - Dedicated test stands will be developed and used to test ASICs and readout boards
  - Integration test stand will be developed and used to certify complete readout chain in the final configuration
  - Leak check will be performed on signal feed-through assemblies

QA and Integration Test Stand

- ASIC Test Stand
  - Individual test stand for each ASIC
    - All ASICs should be screening tested individually at RT
  - ASIC cold test board to verify the yield of ASIC operating in cold
    - This will help determine if all ASICs need to go through the cold test
- Electronics Board Test Stand
  - Focus on board level evaluation test
  - Simple readout and DAQ system for easy debug test
  - Can be re-purposed to the dedicated debug test station once the system integration test stand becomes available
- System Integration Test Stand
  - Focus on system integration of various components
  - Complete system with golden setup can be used to test individual components, for both prototype and production
  - Multiple system integration test stands to serve different purposes
    - Test stand at BNL will focus on the FE evaluation test
    - Test stand at Nevis will focus on the BE evaluation test
    - Test stand at FNAL will focus on the DAQ development and detector integration

Response to Review Recommendations

- Recommendation 1
  - The main argument to adopt double flanges seems to be the issue of argon gas purity possibly impaired by a less than one meter length cables. Anyway the SBND has in argon gas phase a sizable amount of components that could be a source of pollution that will require recirculation in any case, in accordance with the results form other liquid argon TPC. In this perspective double flanges look as an overhead that could be a source of extra problems rather than a solution. The statement that double flange would relax tightness requirements ignores the back-diffusion effect that will allow oxygen contamination, even if reduces, that will limit electron lifetime. Not to mention the increased costs and number of connections that will be at least doubled.
- Response 1
  - PCB based double signal feed-through is a ***targeted*** R&D for SBND experiment, which will be concluded by Spring 2016
  - It is being investigated how to optimize the fabrication and assembly of signal feed-through, value engineering will be conducted at the same time
  - The development of PCB based double signal feed-through has low risk, with the fall back solutions of either single PCB based warm flange, or single warm flange with ATLAS pin carrier

Response to Review Recommendations

- Recommendation 2
  - In general the mechanics of the cold electronics (connectors, mezzanine boards, piggy-back etc.) looks rather complex and the number of connections (see also the previous recommendation) are a potential cause of failures.
- Response 2
  - Mechanics design of cold electronics has taken into account of both reliability and value engineering
  - Same FPGA mezzanine design will be used to interface to both top analog mother board and side analog mother board
  - Development is based on past experience (DUNE 35 Ton) with optimization, the cold cable adapter board has been eliminated to improve the reliability
  - All cold electronics boards will go through QA/QC procedure before final installation, both warm test and cold test (multiple thermal cycles) will be carried out

Response to Review Recommendations

- Recommendation 3
  - A plan for board revision should be developed including additional boards from early revisions for testing by the data acquisition and slow monitoring groups.
- Response 3
  - Electronics boards will have two prototype cycles in preliminary design and final design
  - System integration test with DAQ and slow control has been planned at the end of each prototype cycles
- Recommendation 4
  - Bring the plans for testing and qualification of all circuit boards to the same level.
- Response 4
  - Warm interface electronics development has been advancing in past few months
  - System integration test stand will be used to certify all electronics boards, both cold electronics and warm interface electronics
  - Dedicated test stand will be developed and used to test ASICs

Response to Review Recommendations

- Recommendation 5
  - The trigger strategy is well known and defined however the hardware implementation is not yet fully defined. In an liquid argon detector the light signal must play a fundamental role and this issue has not been described in any phase of this review.
- Response 5
  - Light detection system development has started to ramp up in past few months
  - Discussion of the trigger electronics has been ongoing between electronics working group and light detection working group, with aim to define the trigger requirement in coming months

Status of Design

Revision of FE ASIC will aim to further improve the robustness of chip and simplify the system design of the front end readout electronics. Revisions are limited to fine adjustments with low risk

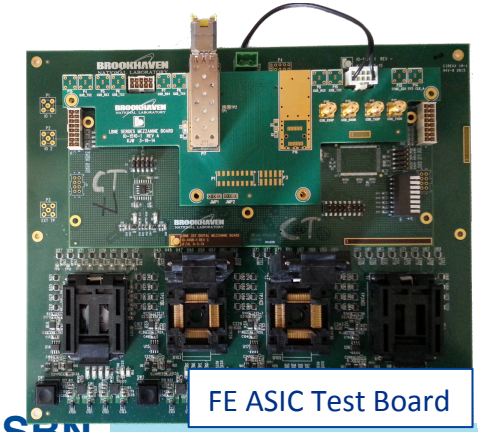
- Improve IO protection
- Implement smart reset
  - Use combination of CS and CK to generate reset internally
- Improve driving capability of the last stage of shaper
- Implement internal pulse generator
  - To perform precision charge calibration
- *Implement read back of internal serial configuration registers*

Revision of ADC ASIC will aim to further improve the performance, simplify the usage and interface. Revisions will be based on the test results and recently defined COLDATA interface

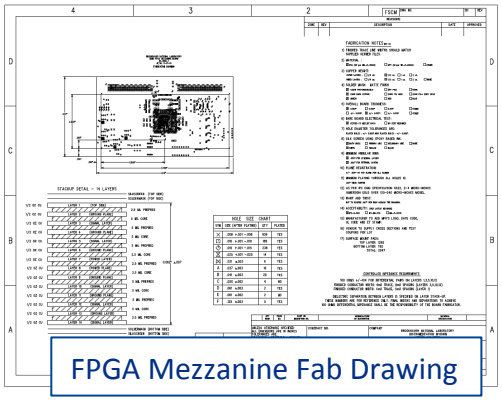
- Implement the power on default configuration
- Improve the IO protection
- Improve the ADC DNL/INL performance
- Implement user friendly interface
- Implement compatible SPI interface between FE ASIC and ADC ASIC
- Implement compatible interface to COLDATA ASIC
- *Implement read back of internal serial configuration registers*

Status of Design

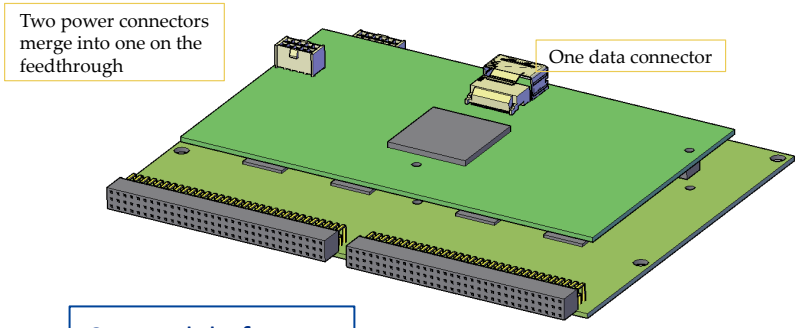
- Cold Electronics
  - Cold FE ASIC and ADC ASIC development has started in September, supported by both SBND and DUNE
  - Plan to have the technical review in January and the first chip submission in early February
    - Second submission is planned in August after full evaluation of the first submission
  - FE ASIC test board and ADC ASIC test board have been designed and being tested
  - Analog mother board and FPGA mezzanine have been designed and being fabricated



FE ASIC Test Board

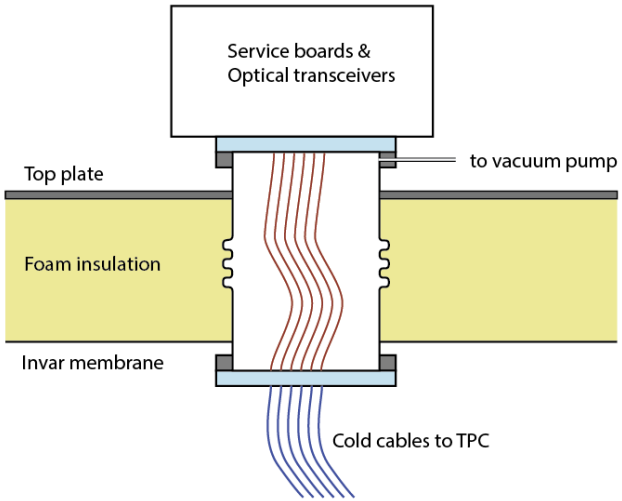


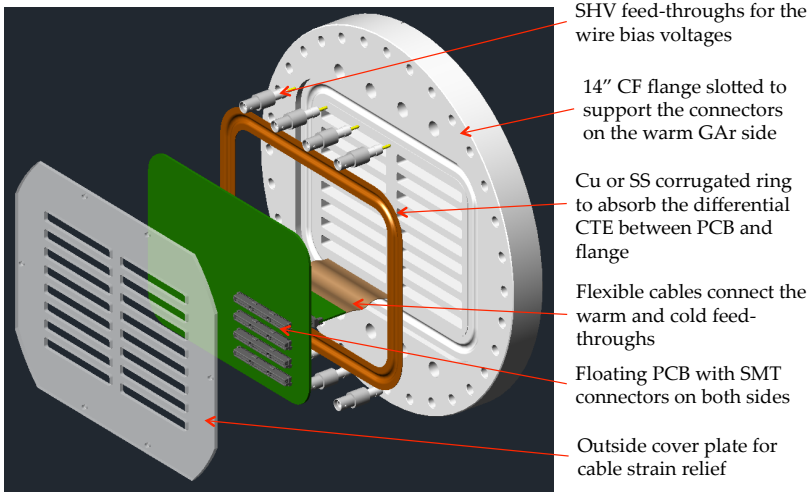
FPGA Mezzanine Fab Drawing



3D Model of FEMB

Status of Design



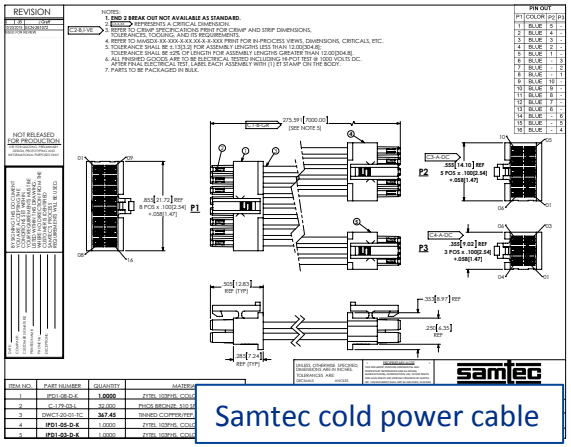


- Double feed-throughs to ease the LAr purity control
  - Cold flange is immersed in the cold GAr
- Baseline (backup) design is the ATLAS pin carrier
  - Double feed-throughs are used in LAr Calorimeter
  - Single warm feed-through is used in MicroBooNE
  - Working with Glasseal to arrive at a more affordable price
- Explore the option of a PCB based signal feed-through design
  - Working on collaboration with INFN Padova, to learn experience of ICARUS feed-through development
  - Working on collaboration with WA105, to learn experience of PCB base double feed-through development
  - Two ICARUS feed-throughs have been received at BNL, one ICARUS feed-through has been tested in LAr, which passed continuity test, even though the potting epoxy cracked

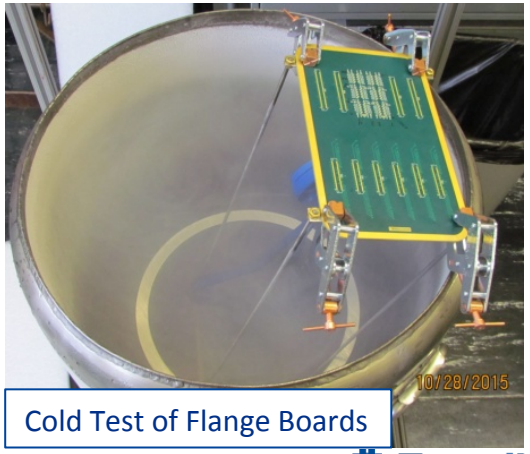
Status of Design

- Signal Feed-through and Cold Cable
  - Cold cable candidate has been identified and certified by FNAL MTS
  - Flange boards have been designed and tested
  - Signal feed-through design is ongoing, few assembly options are being explored
  - CF flange is being fabricated to prepare for assembly test with flange boards

3M miniSAS Cable

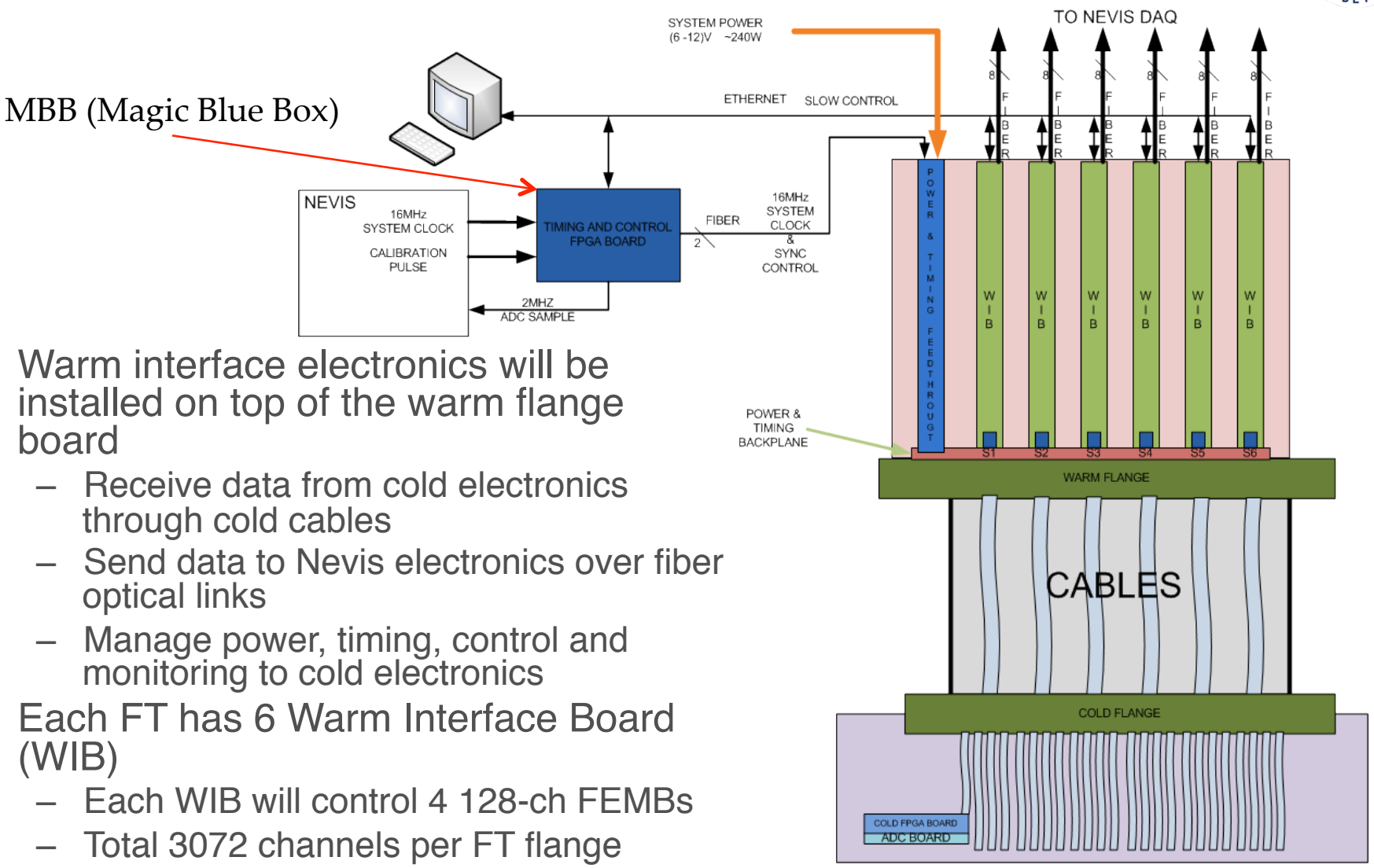


Samtec cold power cable



Cold Test of Flange Boards

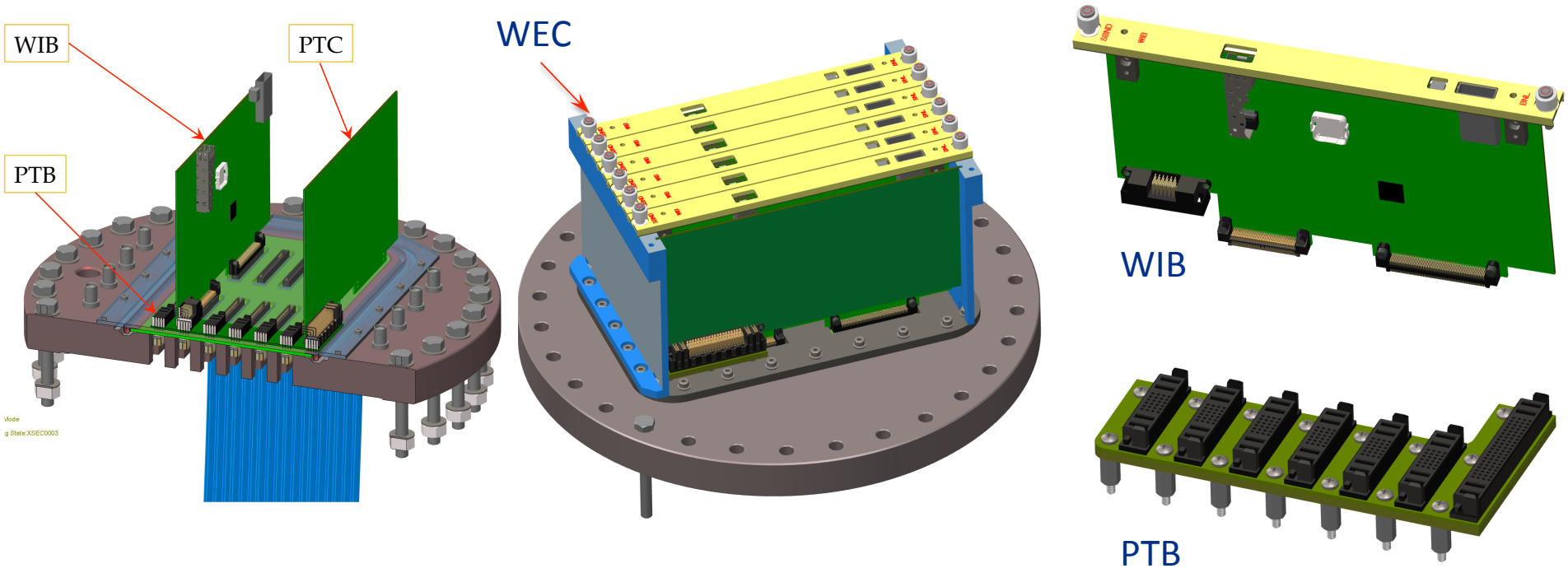
Status of Design



- Warm interface electronics will be installed on top of the warm flange board
  - Receive data from cold electronics through cold cables
  - Send data to Nevis electronics over fiber optical links
  - Manage power, timing, control and monitoring to cold electronics
- Each FT has 6 Warm Interface Board (WIB)
  - Each WIB will control 4 128-ch FEMBs
  - Total 3072 channels per FT flange

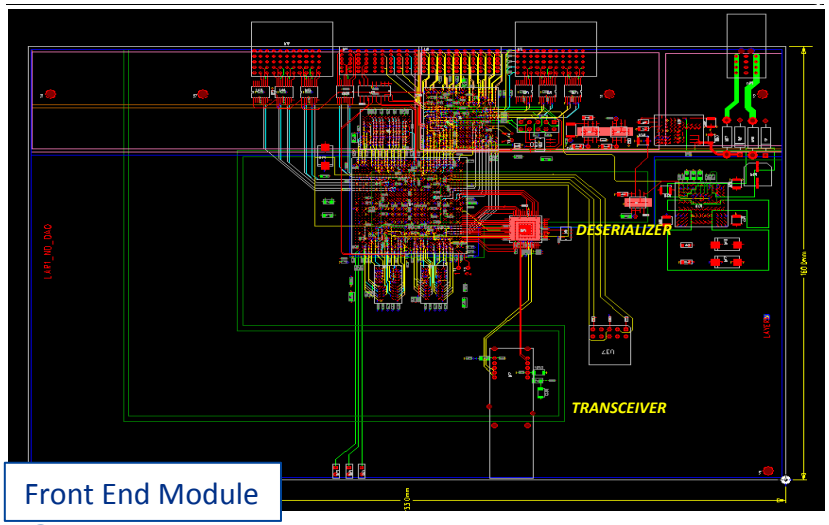
Status of Design

- Warm Interface Electronics
  - Schematics design of warm interface electronics (WIB, PTB & PTC) is being finalized, layout of WIB has started
  - Warm electronics crate (WEC) design has started

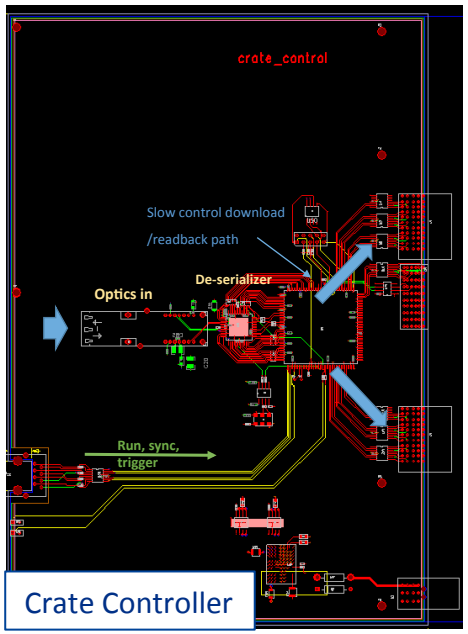


Status of Design

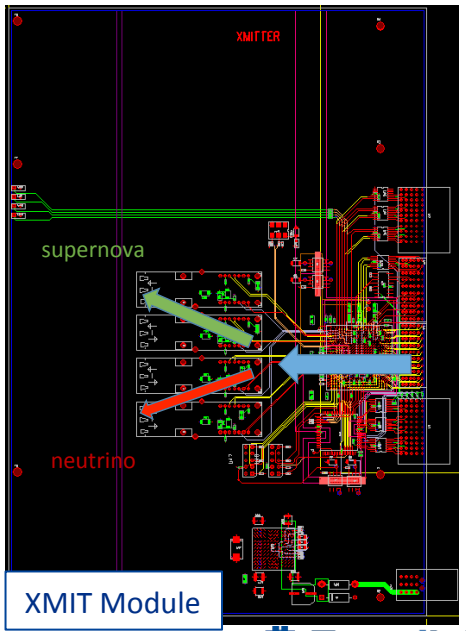
- TPC Readout Electronics
  - Prototype FEM is being fabricated
  - Prototype (only differ in dimensions from MicroBooNE) XMIT and Crate Controller boards also
  - Trigger electronics requirement is being discussed with light detection working group



Front End Module



Crate Controller



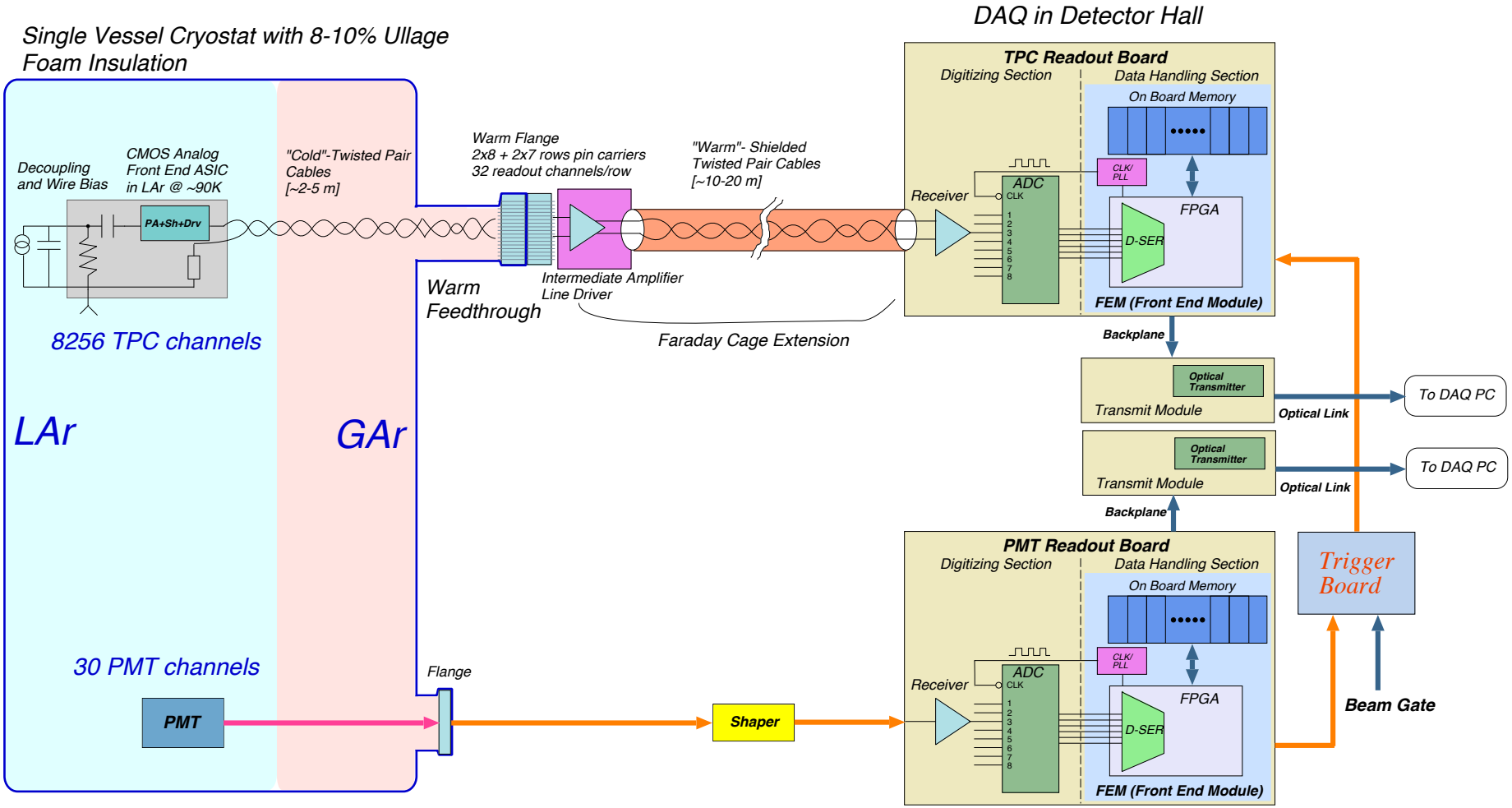
XMIT Module

Status of Design

- Reviews
  - Independent design review took place in September 2015
  - Preliminary design review is planned in June 2016 after the integration test of the preliminary design

Backup Slides

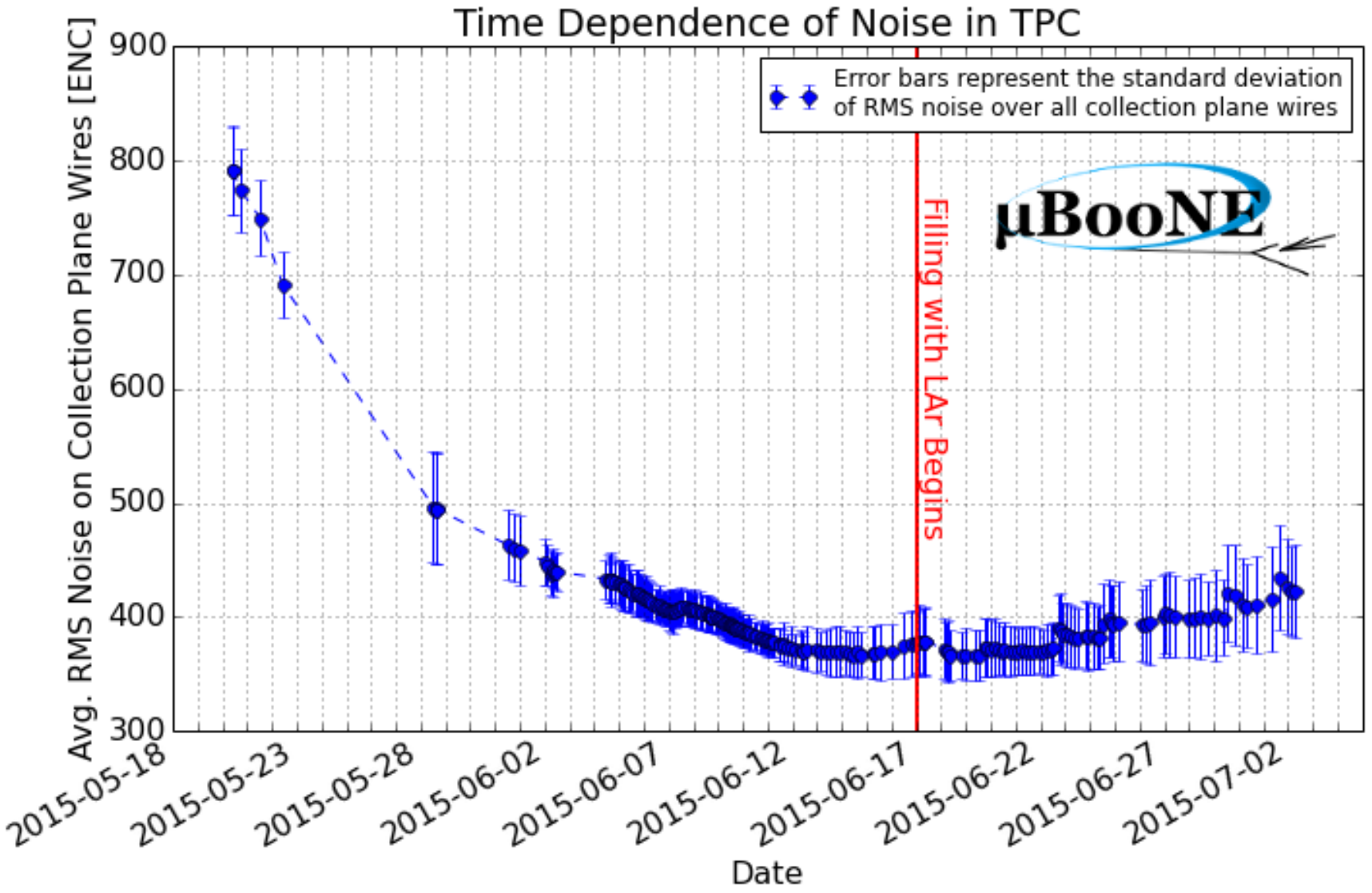
MicroBooNE Electronics System



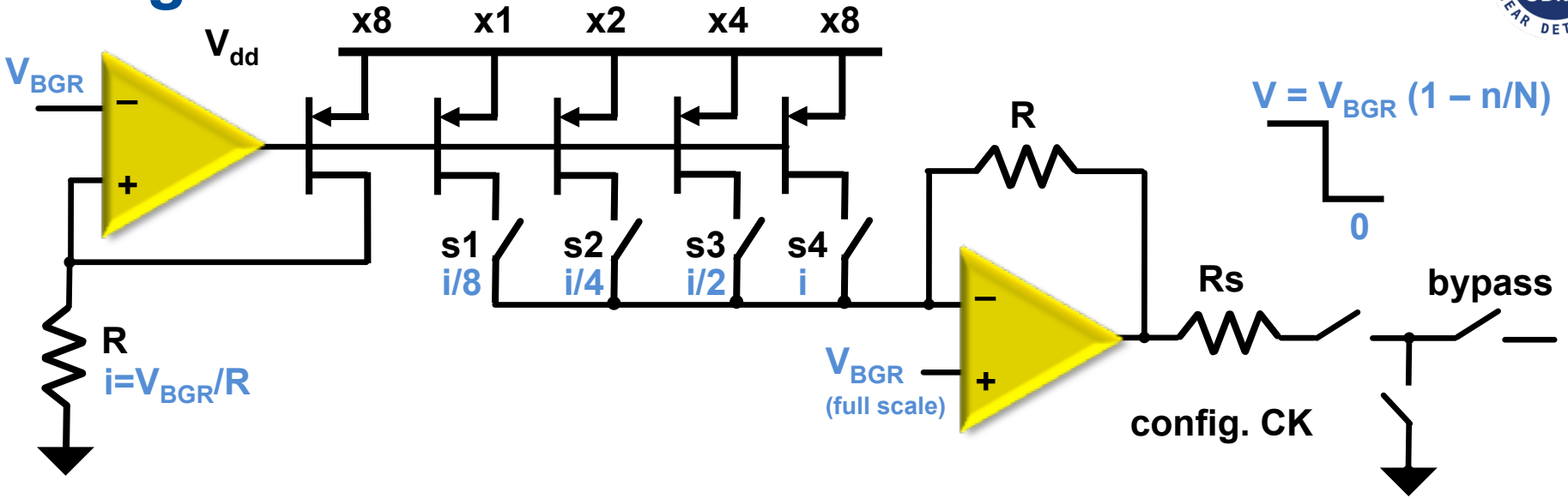
Update of Technical Design

- Front End Electronics
  - 09/29/2015 – SBN DocDB #621
  - 11/04/2015 – SBN DocDB #673 – Cold ASICs
  - 11/23/2015 – SBN DocDB #694 – Warm Interface Electronics
  - 12/02/2015 – SBN DocDB #705 – Signal Feed-through
- Back End Electronics
  - 09/29/2015 – SBN DocDB #622
  - 11/23/2015 – SBN DocDB #693

MicroBooNE Cold Electronics Temperature Dependence of Noise in TPC



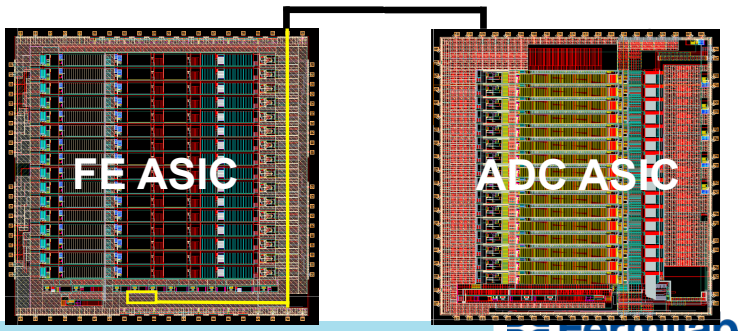
Integrated Calibration Circuit



- proven configuration, implemented in many front-end ASICs
- band-gap referenced (low temperature dependence)
- 6-bit programmable
- ~20mV to 1.2 V, ~20mV steps (> 5 points per gain)
- non-linearity < 0.5 %, non-uniformity < 2 %
- re-usage of amplifiers (low risk implementation)
- re-usage of signals (configuration clock)
- fully compatible with present scheme and pinout
- connect 8 FE-ASICs to reduce dispersion
- can be routed to calibrate ADCs as well

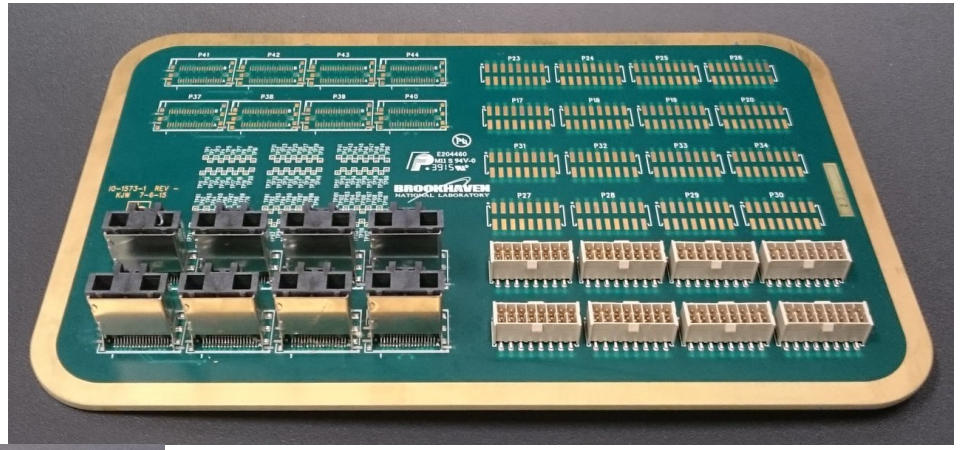
measured

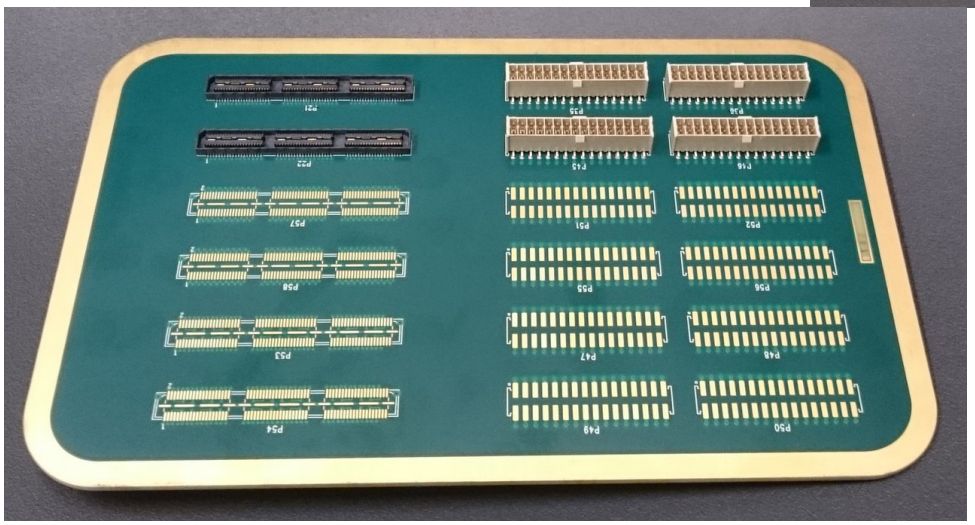
$$V_{BGR} \approx \begin{cases} 1.185\ V & \text{at } 300\ ^{\circ}K \\ 1.164\ V & \text{at } 77\ ^{\circ}K \end{cases}$$

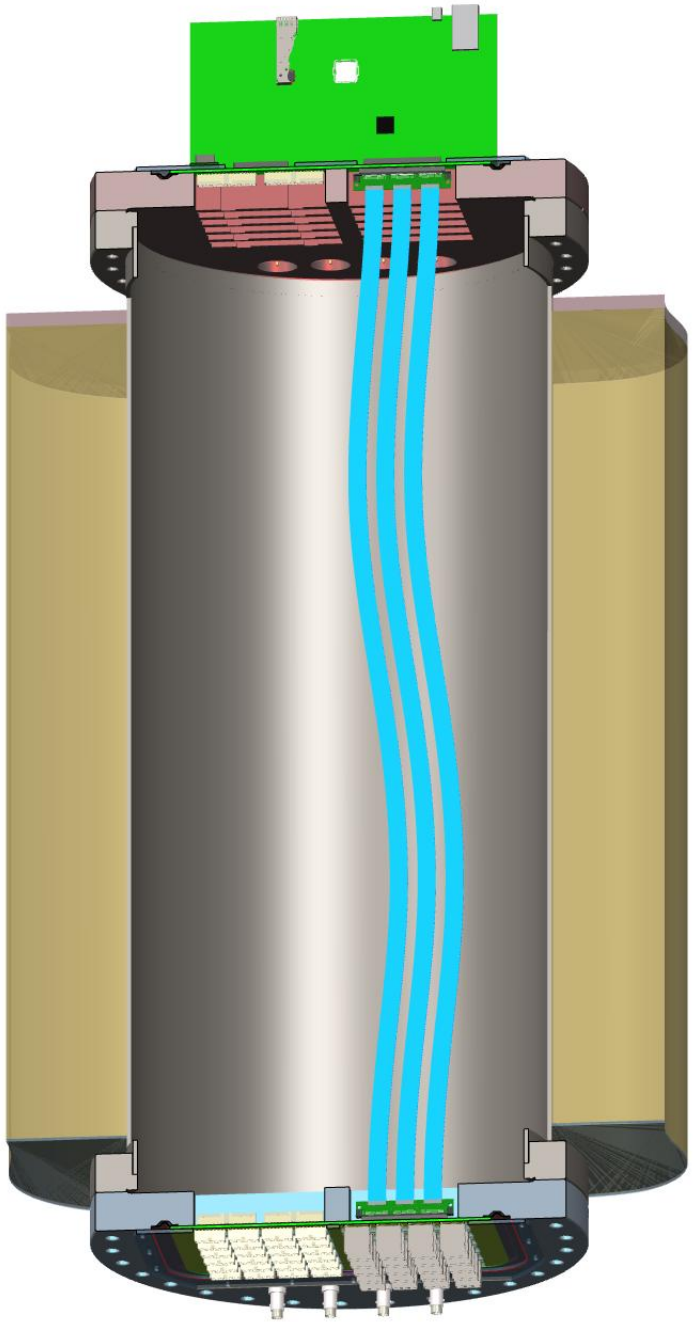


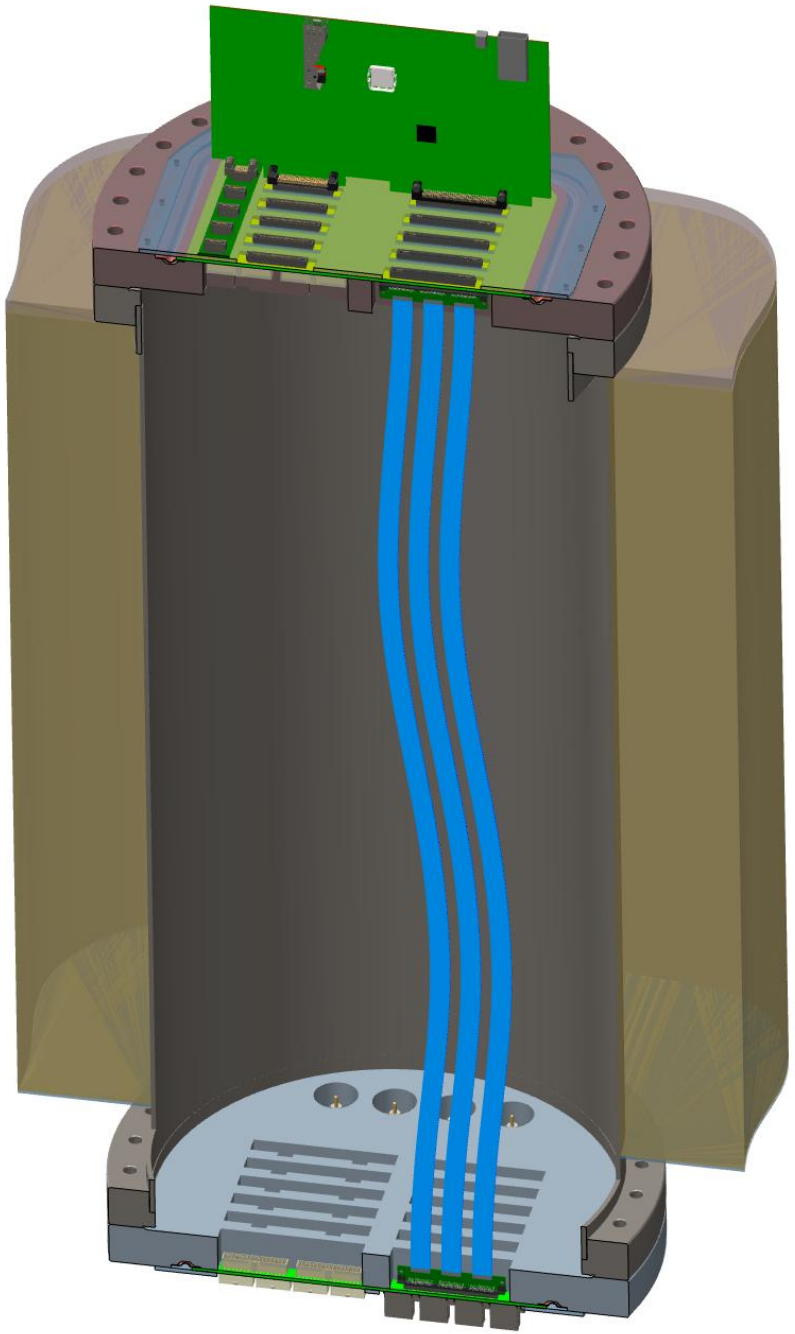
Test Flange Board

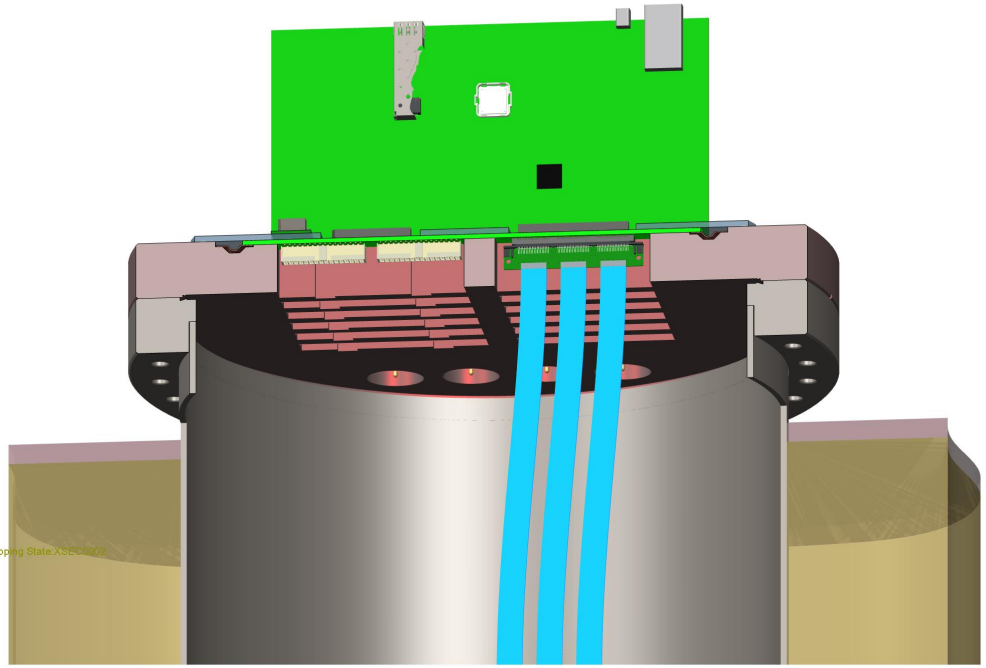
- Designed to test the reliability of plated through holes and cable connectors







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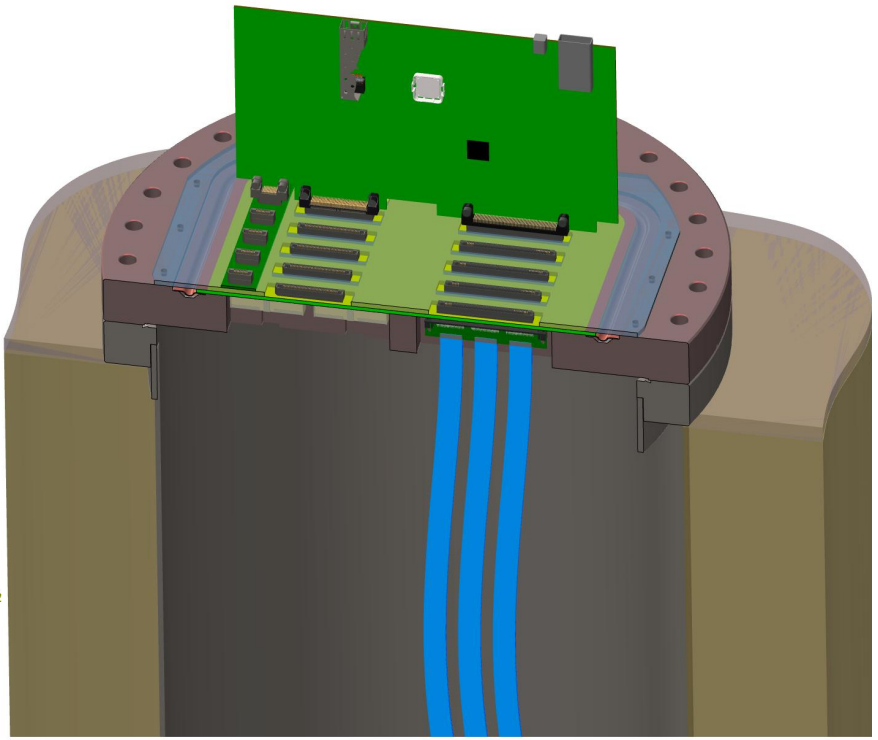
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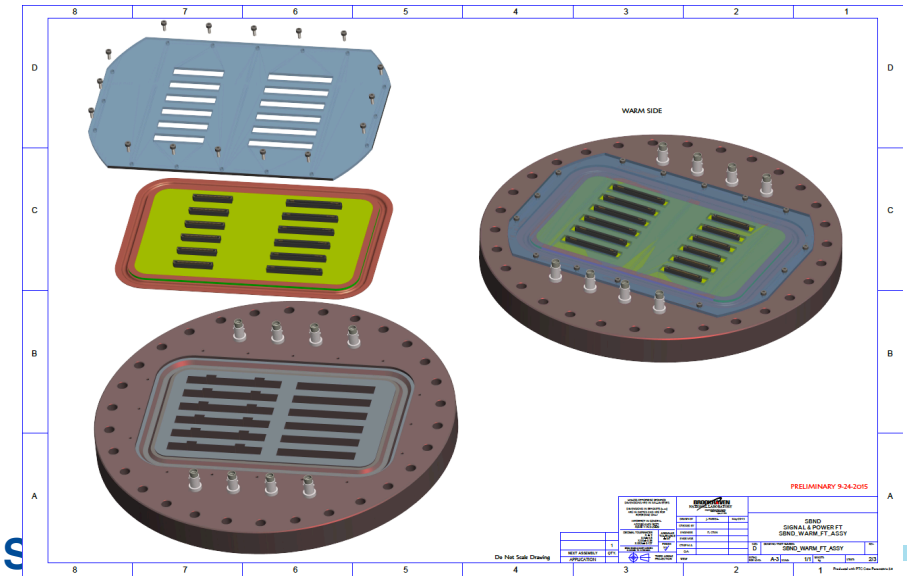
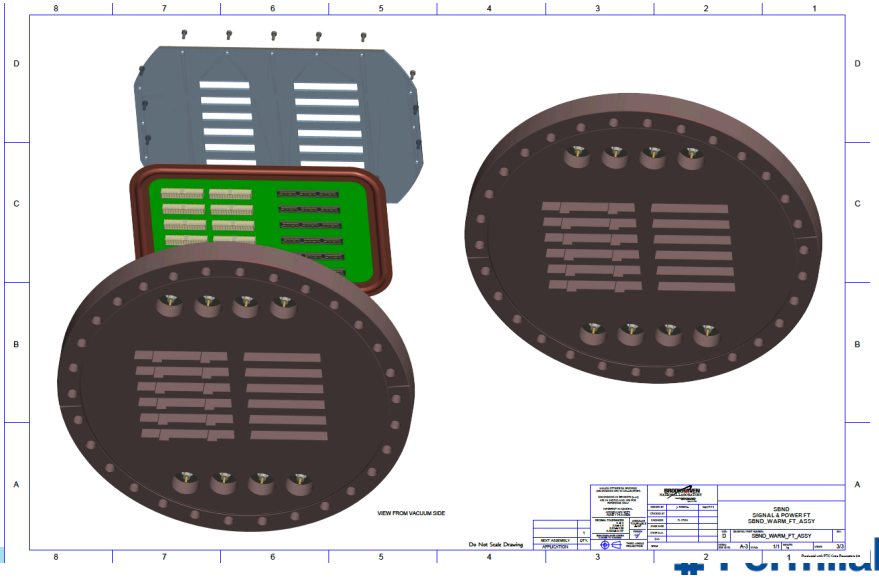
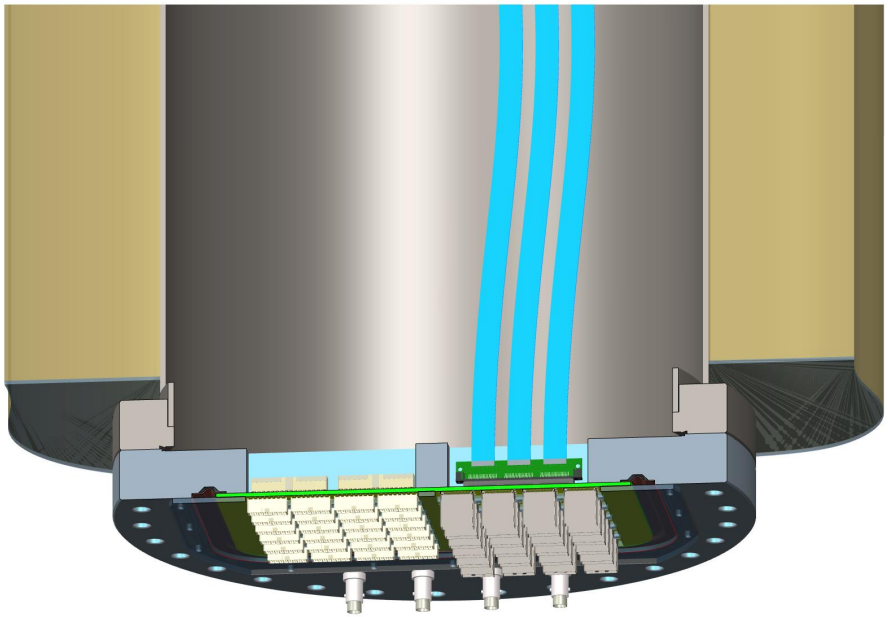
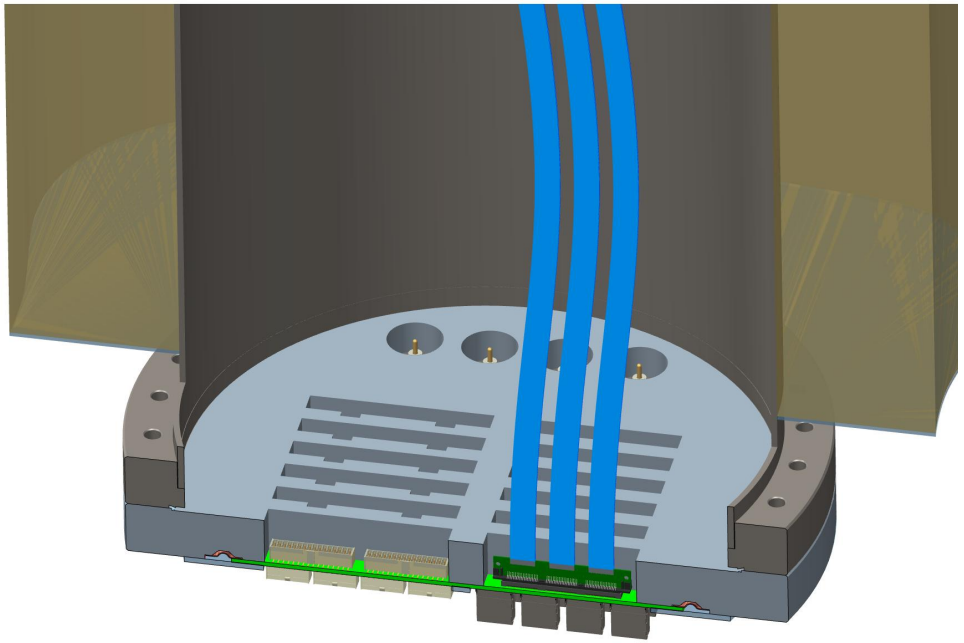
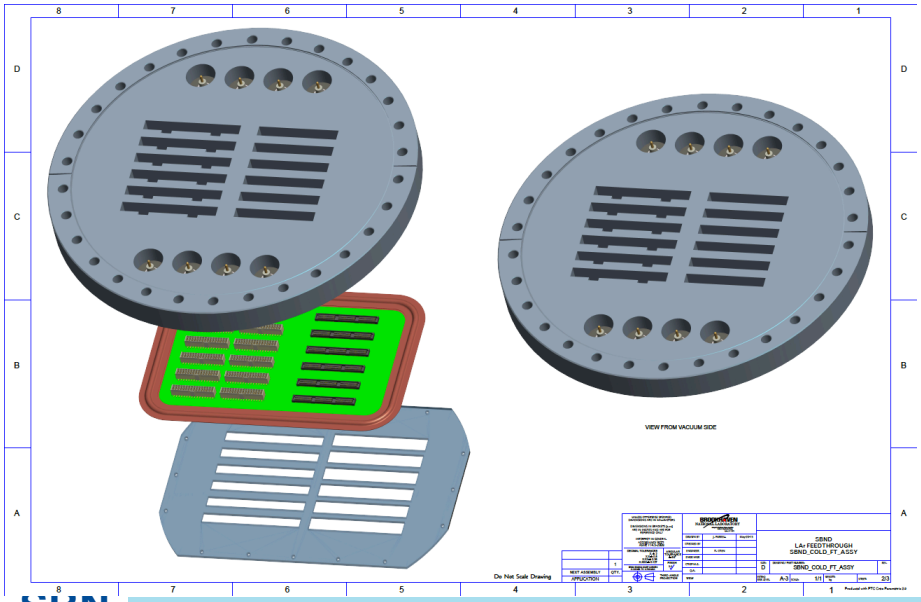
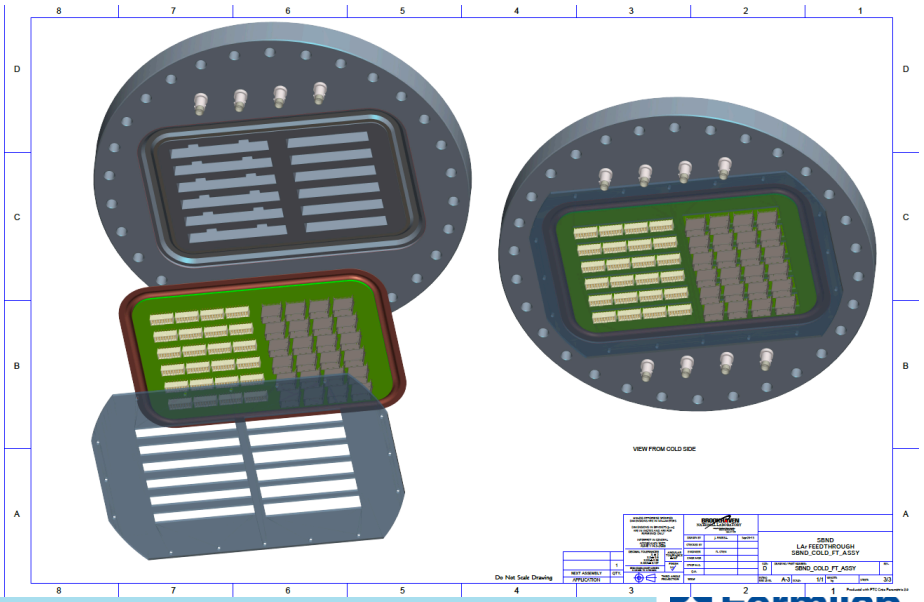

WARM SIDE
PRELIMINARY 9-24-2015
SBND
SIGNAL & POWER FT
SBND_WARM_FT_ASSY
Do Not Scale Drawing


VIEW FROM VACUUM SIDE
SBND
SIGNAL & POWER FT
SBND_WARM_FT_ASSY
Do Not Scale Drawing






VIEW FROM VACUUM SIDE
SBND
LAr FEEDTHROUGH
SBND_COLD_FT_ASSY
Do Not Scale Drawing


VIEW FROM COLD SIDE
SBND
LAr FEEDTHROUGH
SBND_COLD_FT_ASSY
Do Not Scale Drawing

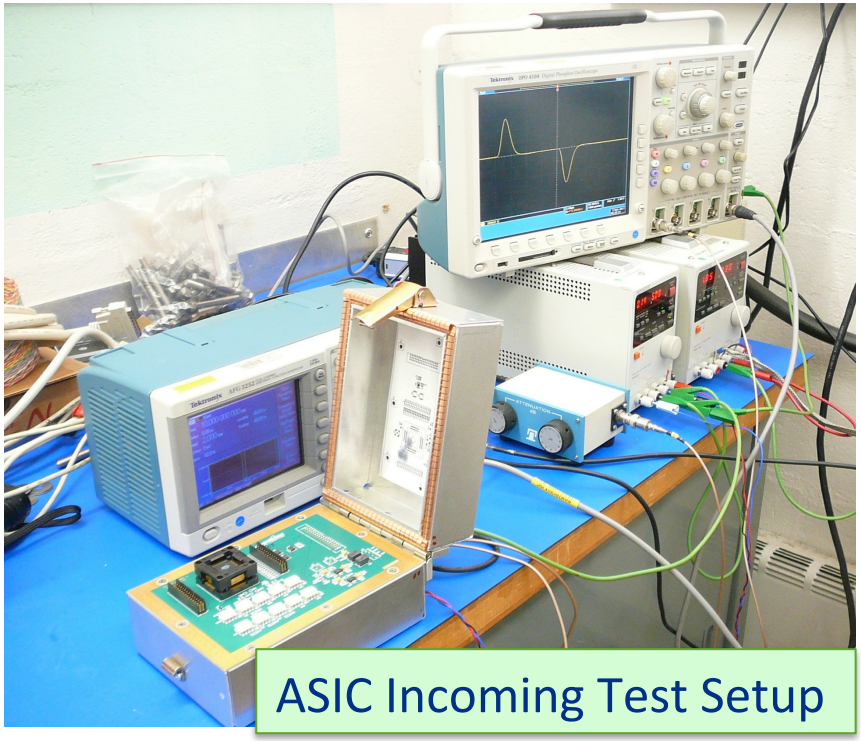
Cost Comparison of MB and SBND

	SBND	MicroBooNE
Design	$2,351,654	$ 1,127,313
Design of Cold ASICs	$ 604,427	
Design w/o Cold ASICs	***$1,747,227***	***$ 1,127,313***
Production	$1,261,809	$ 1,741,340
Total	$3,613,463	$ 2,868,653
Total w/o Cold ASICs	***$3,009,036***	***$ 2,868,653***

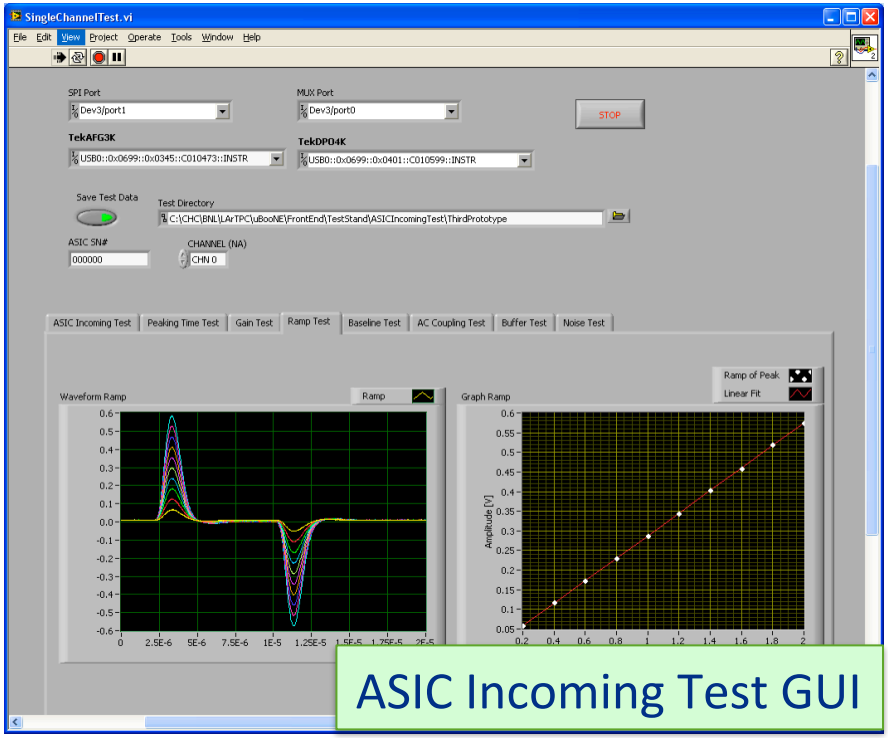
- MicroBooNE doesn't include cold ASIC design, while SBND supports 50% of ASIC design
- MicroBooNE front end electronics stops at ADC, doesn't have any FPGA design, while SBND has two FPGA related design, one is cold FPGA mezzanine, the other is warm interface board
  - MicroBooNE warm interface electronics is analog driver circuit, while SBND warm interface electronics has FPGA to deal data receiving, manipulation and transmission
- MicroBooNE feed-through design is based on the existing ATLAS pin carrier, while SBND is developing PCB based feed-through
  - MicroBooNE has single warm feed-through, while SBND has both warm and cold feed-throughs

MicroBooNE ASIC Incoming Test Stand

- All FE ASICs are fully qualified before populated on the cold mother boards

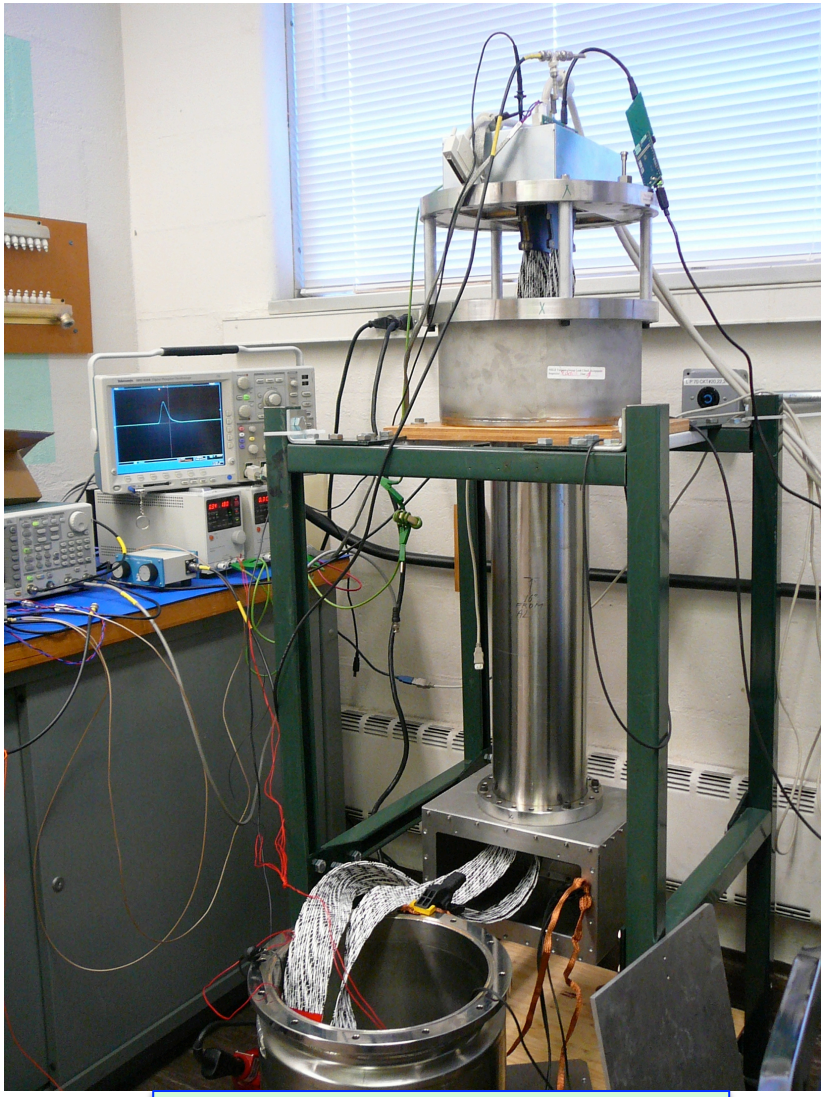


ASIC Incoming Test Setup

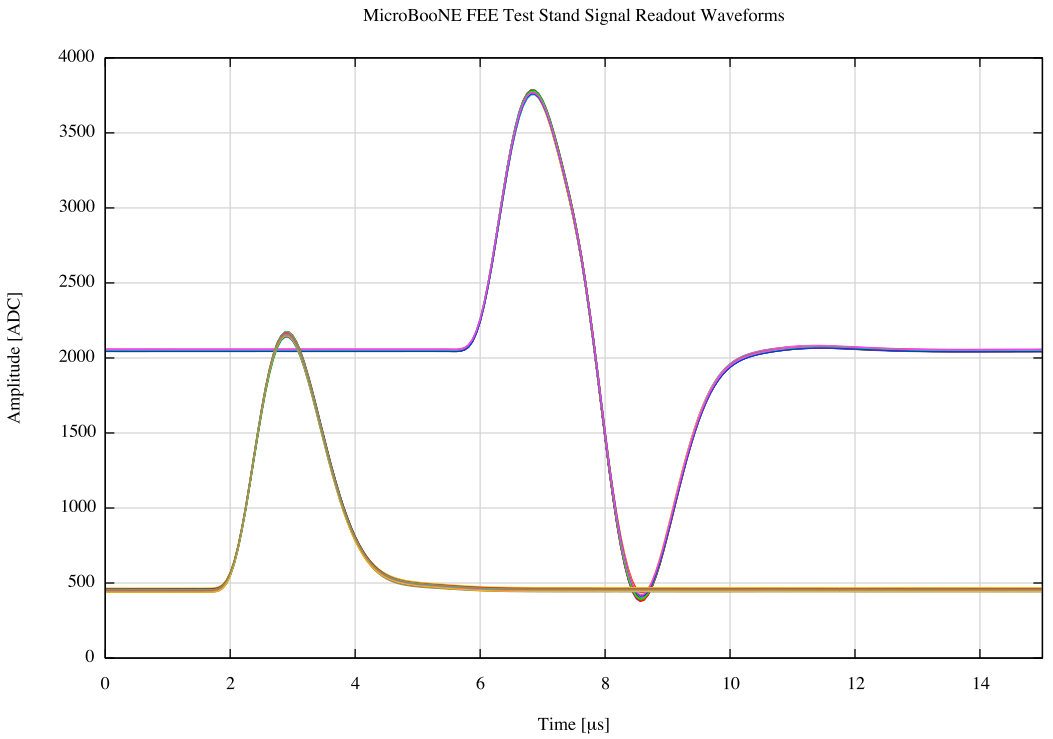


ASIC Incoming Test GUI

MicroBooNE FEE Test Stand



Cold Test of FEE Test Stand



64 channels of signal chain response overlapped

MicroBooNE Prototype 1 Integration Test Stand

MicroBooNE Prototype 2 Integration Test Stand

- Test stand at Nevis was later moved to FNAL for DAQ system development