Status of the Electronics upgrade for the ICARUS T600

Sandro Centro, Università di Padova & INFN

Director's Progress Review of SBN

15-17 December 2015

Outline

- T600 Electronics performance
- New Flange & new Electronics
- Integrating Analogue & Digital boards
- Improved Induction2 signal treatment
- Ongoing tests and performance
- Present status and schedule

The need for an electronics upgrade

- ICARUS-T600 electronics consists of analogue boards (VME-like) with **32 low noise amplifiers**, and a **tree** of **8** analog multiplexers, **4** 10-bit ADCs, **2** digital multiplexers, resulting in a 2.5 MHz AD conversion (400ns sampling). Each analogue board is connected (serial link) to a digital VME module that provides storage, data compression, read-out through VME bus.

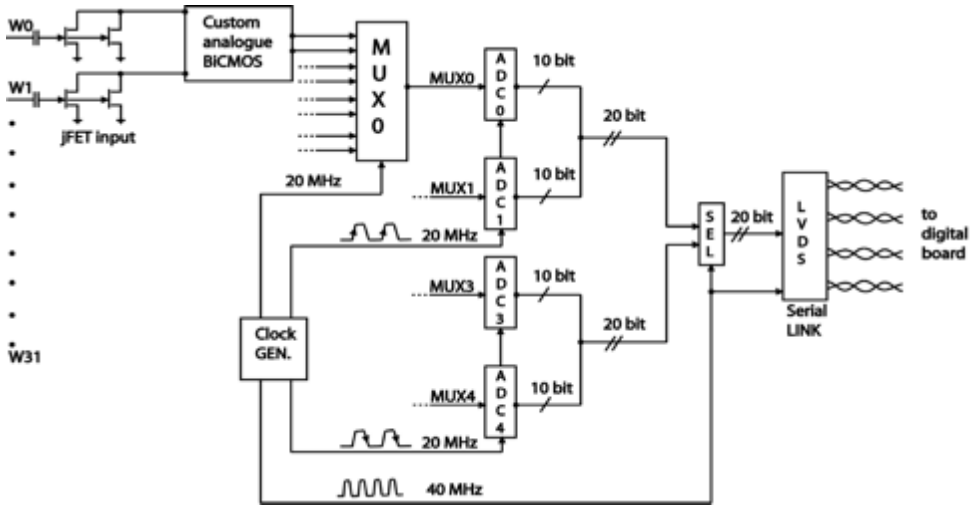
- Limitations of ICARUS-T600 electronics is only due to the technology available when electronics was first conceived (1998). Now days some spare part are difficult to find.

- Improvements concern:
  - adoption of **serial synchronous ADCs**, one per channel;
  - housing and **integration of electronics** on detector flanges;
  - adoption of a **modern serial bus architecture** (instead of VME) with optical links for faster transmission rate (Gbit/s) to sustain higher data rates.

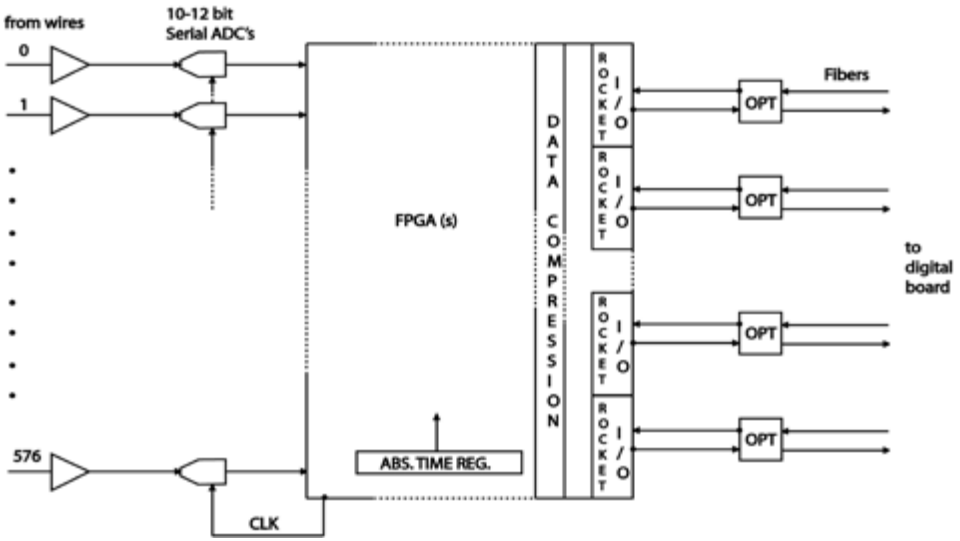
New simplified analogue/digital integration

- Block diagram of the classical old Icarus multiplexed ADC architecture, compared with the new parallel serial ADC feeding directly the digital part housed in a single high performance FPGA.

Present ICARUS Analogue board



Upgraded scheme integrating Analogue and Digital board into one single board

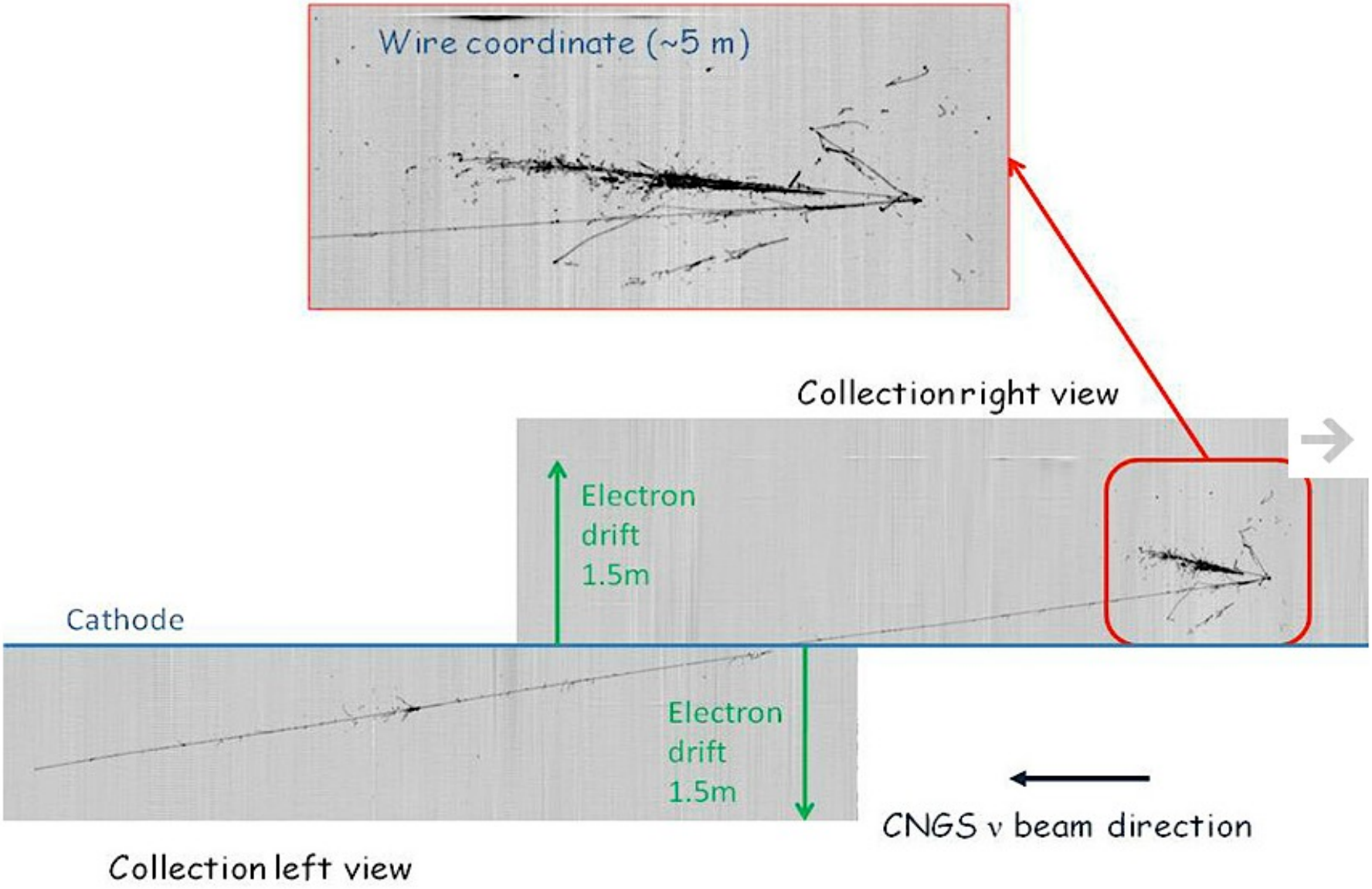


Basic architecture still competitive

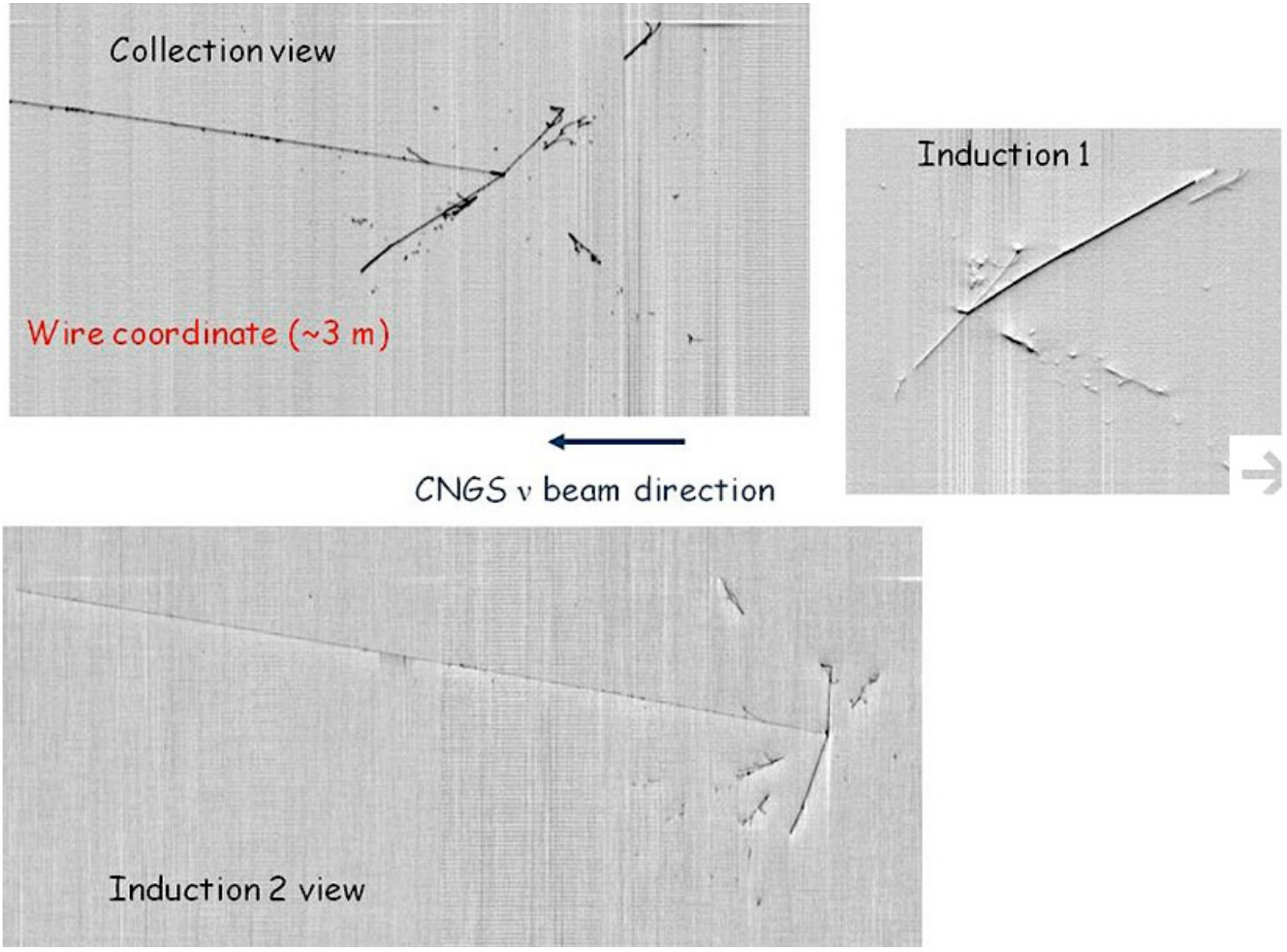
- The "quality" of a LAr TPC relies on *mechanical accuracy, LAr purity, and electronics*. In the next few slides we show why we don't need to change our basic architecture of the electronics, but only adopt more modern components for implementation.

- A signal to noise ratio better than 10 and a ~ 0.7 mm single point resolution were obtained during the LNGS run, allowing for measuring muon momentum by multiple scattering (MS) with $\Delta p/p$ ~16% in the 0.4-4 GeV/c range.

Typical T600 large image

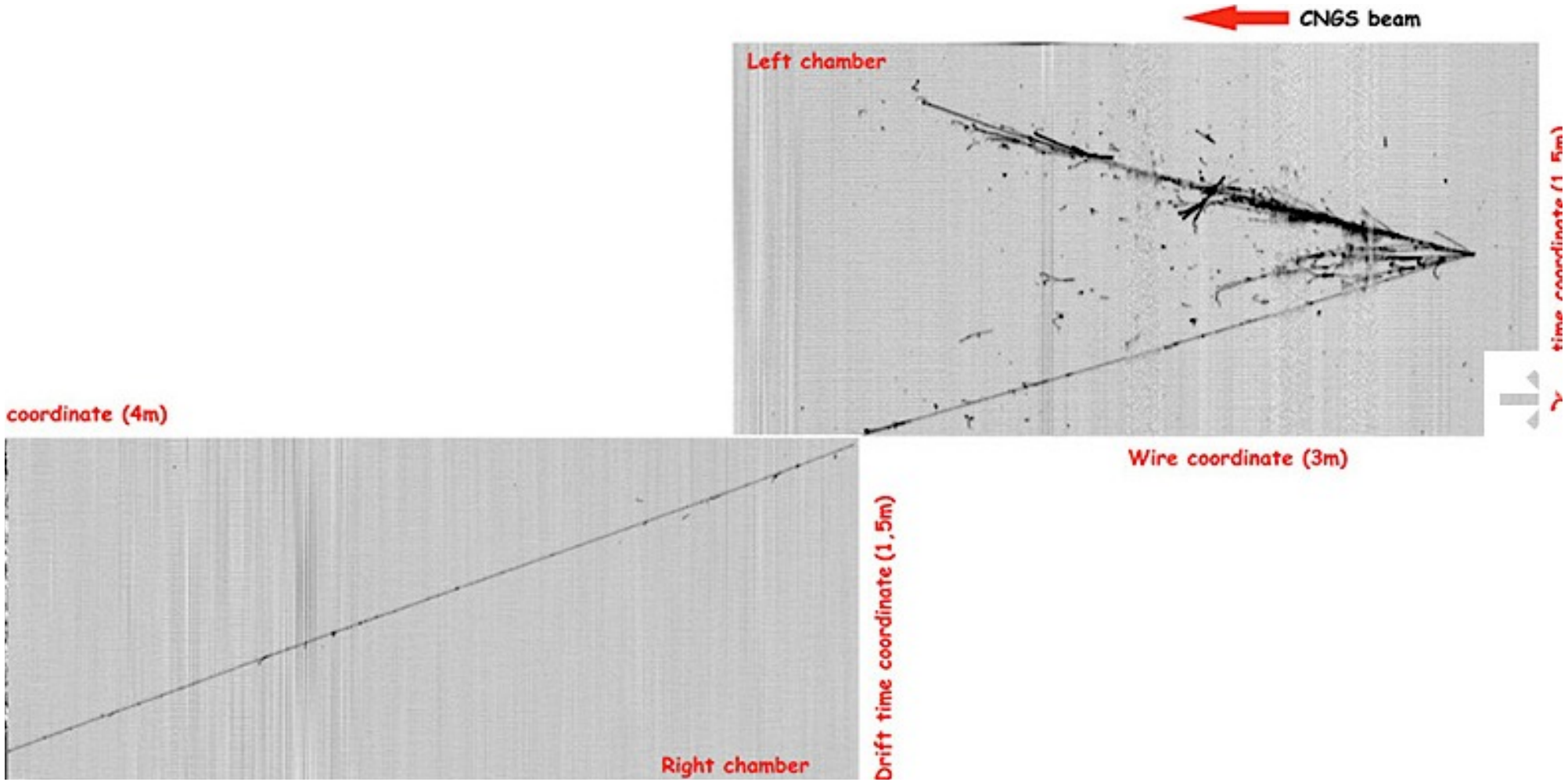


Typical T600 large image



Typical T600 large image

Image contrast gives an idea of the S/N, while background texture is related to *collective or synchronous* noise

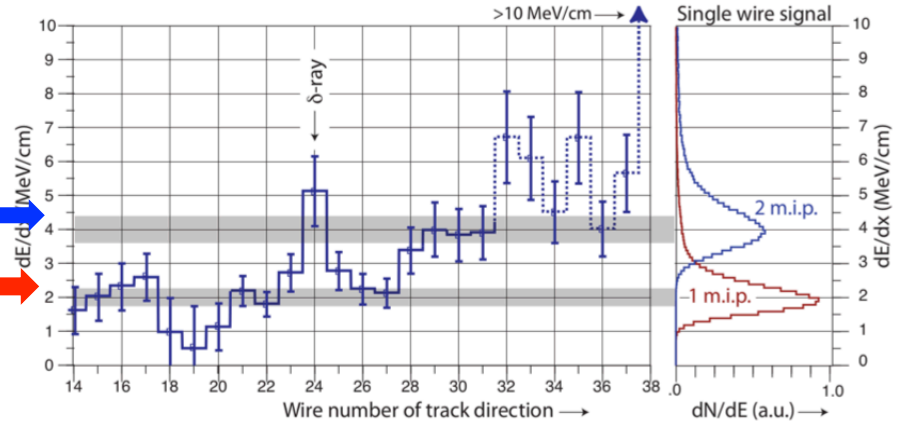


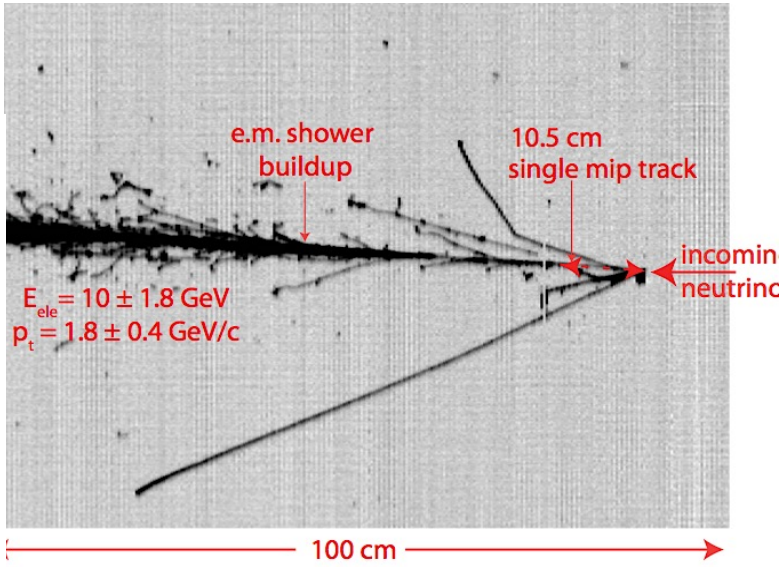
Two ν_e interactions

Run 10871 Event 9185:

Double M.I.P

Single M.I.P

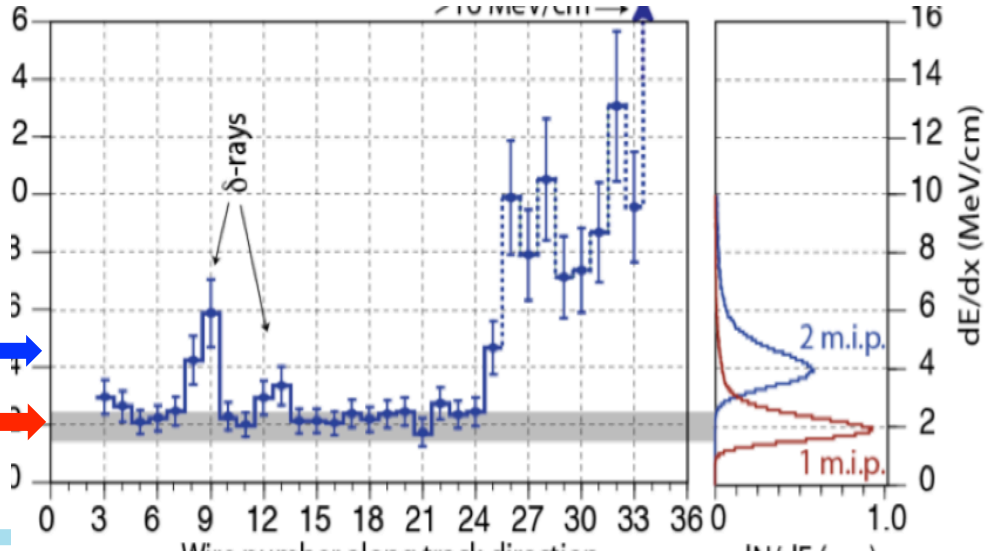


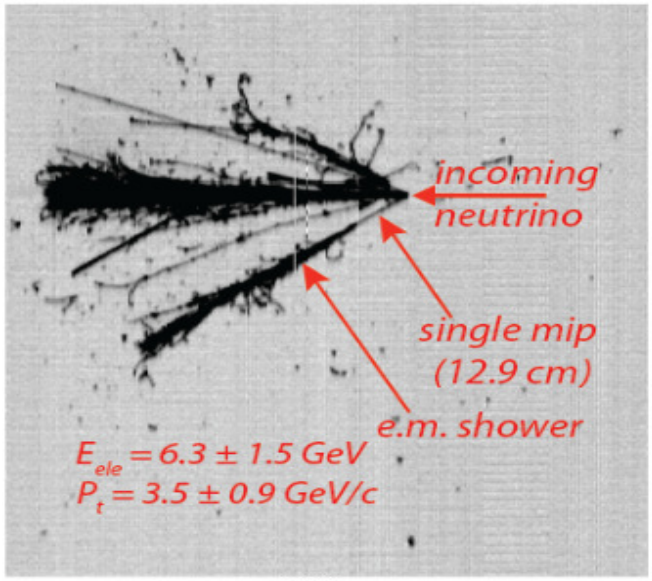


Run 11731 Event 4278:

Double M.I.P

Single M.I.P





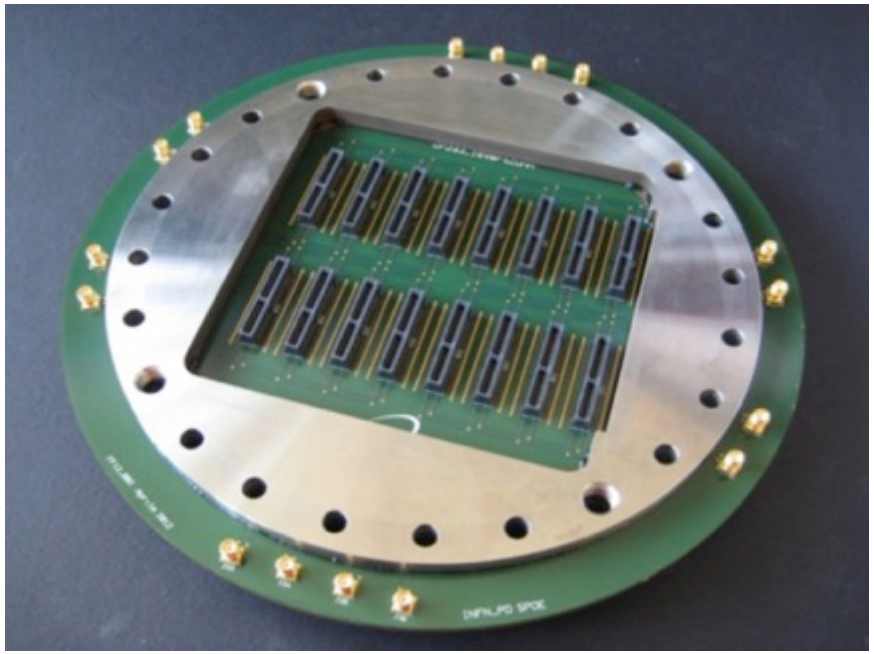
Electronics racks (54000 ch.) & Flanges

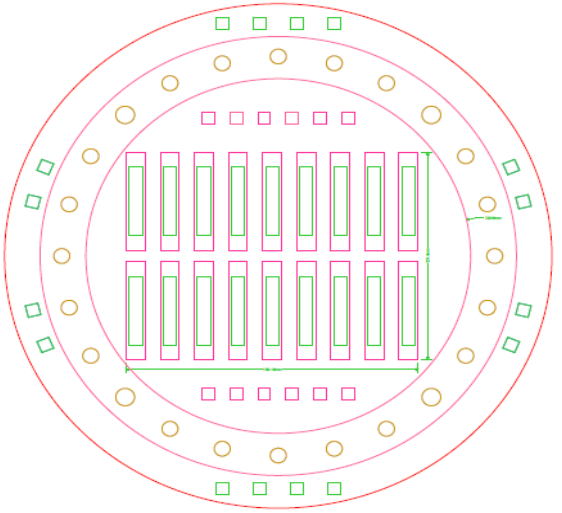
Signal flanges are connected to the back of the racks with a metal screen shielding twisted pair cables.

Two lines, one per chamber, of 96 electronics racks on top of Icarus.

The flange as electronics backplane

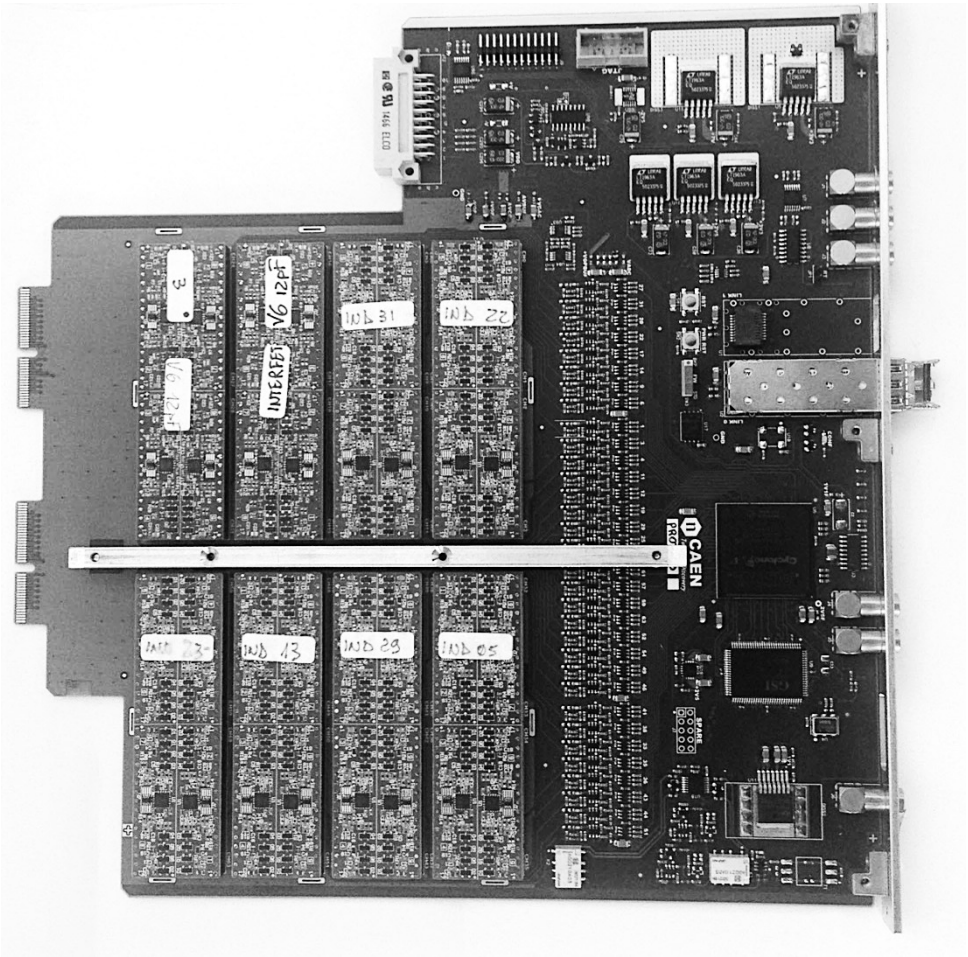
- A ***new flange***, that uses the same INFN proprietary design, used for T600, has been developed.
- The connectors on the external side allow for direct insertion of 9 electronics boards where both analogue and digital electronics are housed.
- The design will allow for reusing the original T600 cabling modularity and same number of signal feed-through.



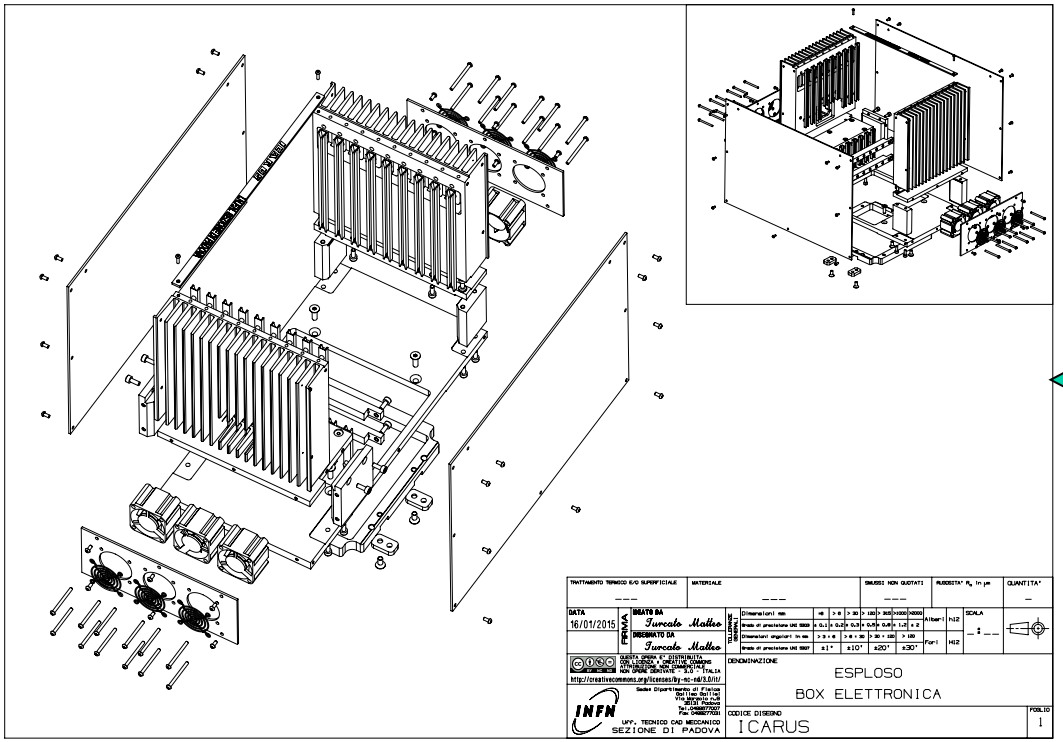


Analogue/Digital board

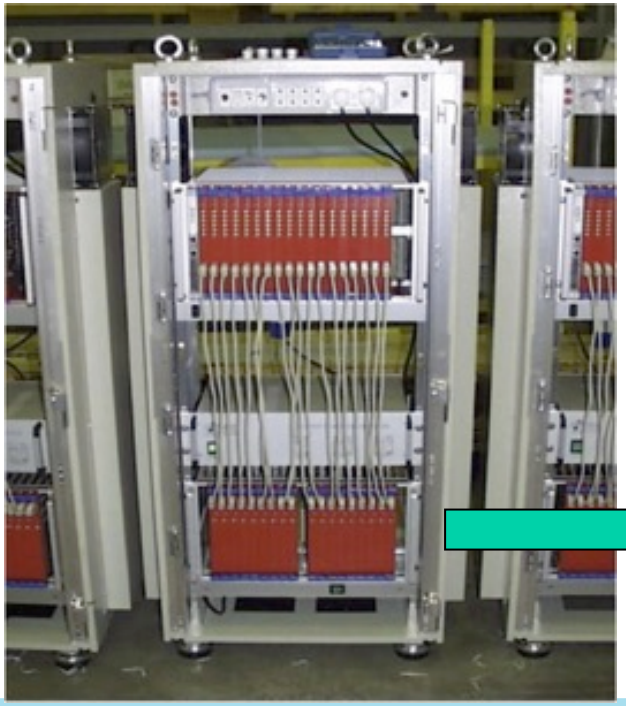
- Each one serves 64 channels and has serial optical link.
- Each channel has a 128kbyte memory buffer.
- The digital part is fully contained in a single high performance FPGA (Altera Cyclone V) per board.
- Firmware of the on-board FPGA will allow for online data processing, such as hit finding, and data compression if necessary.



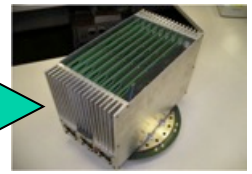
New simplified/compact design



Card cage, mounted onto the flanges, for hosting the boards (9).



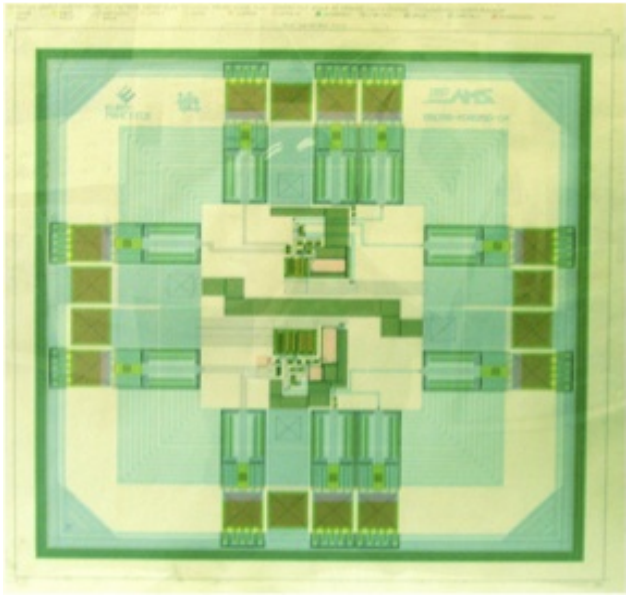
From 595 to 10 liters



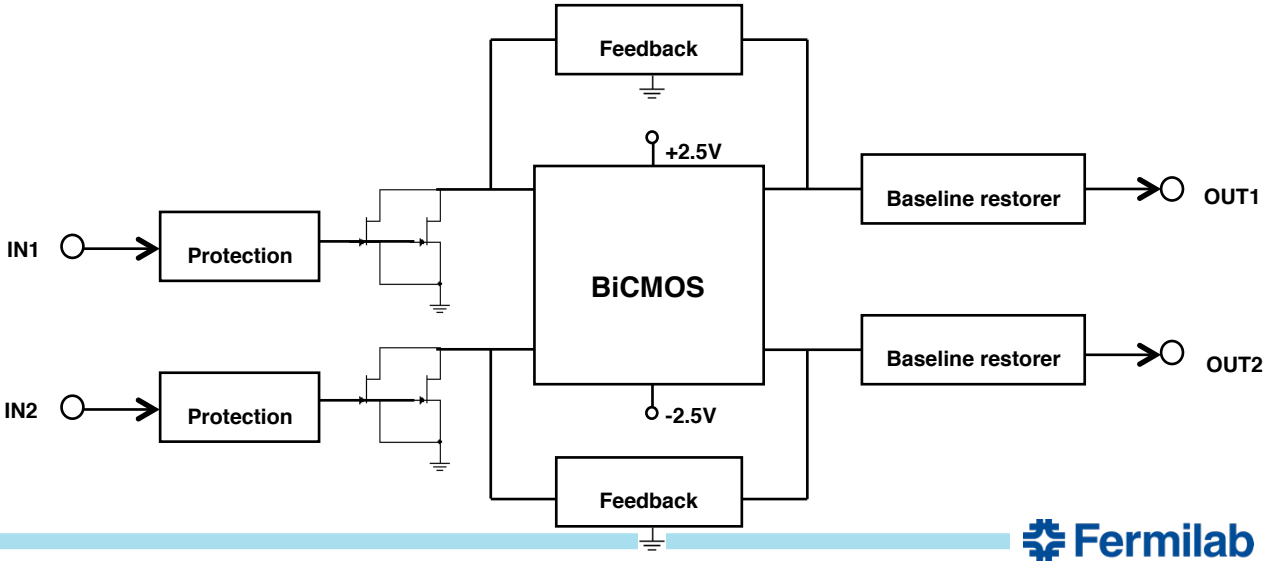
- Compact design allows for hosting both analogue and digital electronics directly on the proprietary flanges.

Improved analogue front-end

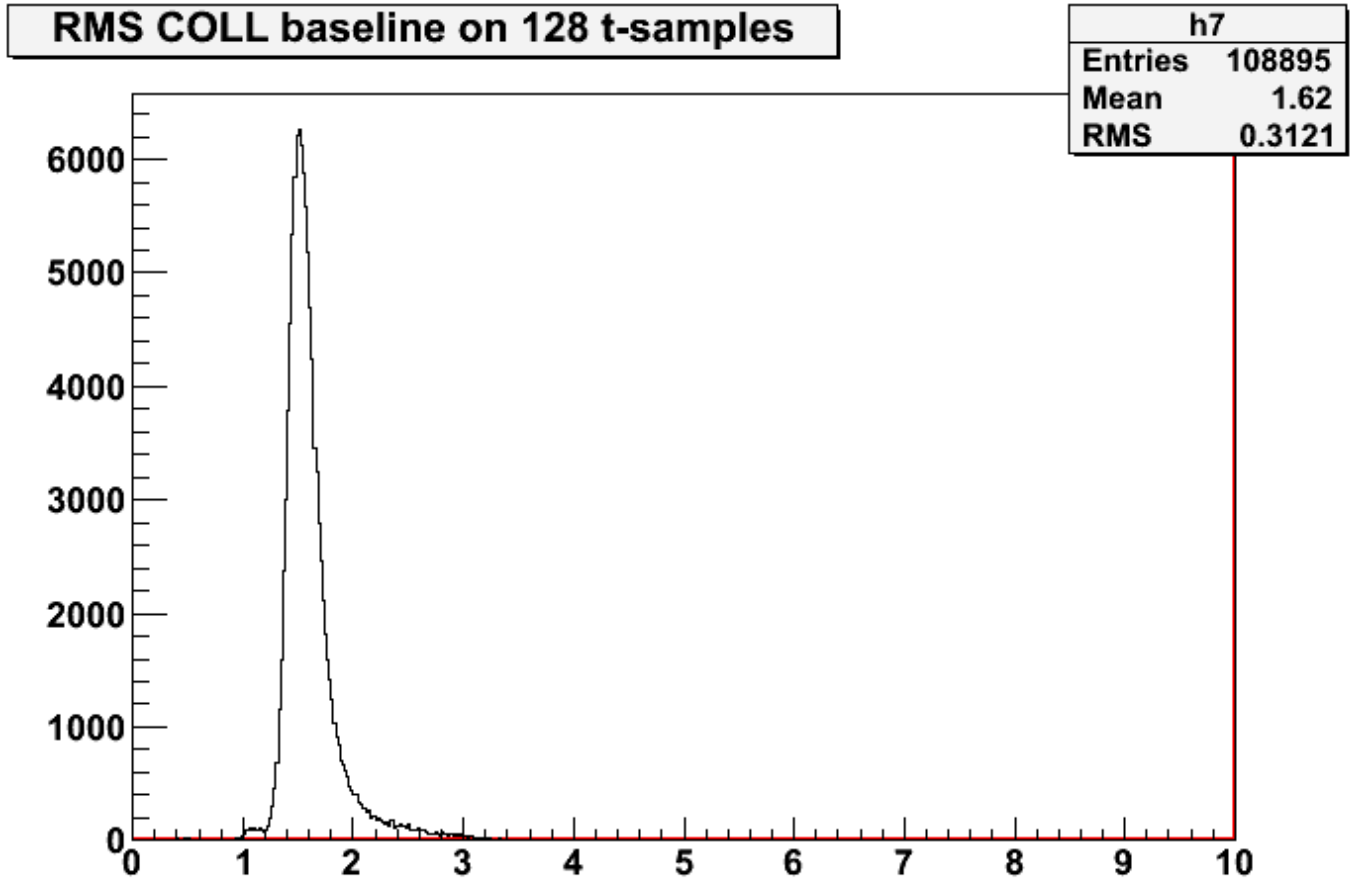
- The analogue front-end of the T600 is perfectly adequate: the only improvement is the adoption of a smaller package for the already available BiCMOS dual channel custom amplifier.



- The gain of the front-end amplifier and filter was *6mV/fC*. The *10bit* ADC had least count equivalent to 1000 electrons.



Noise measurement on collection wires at LNGS



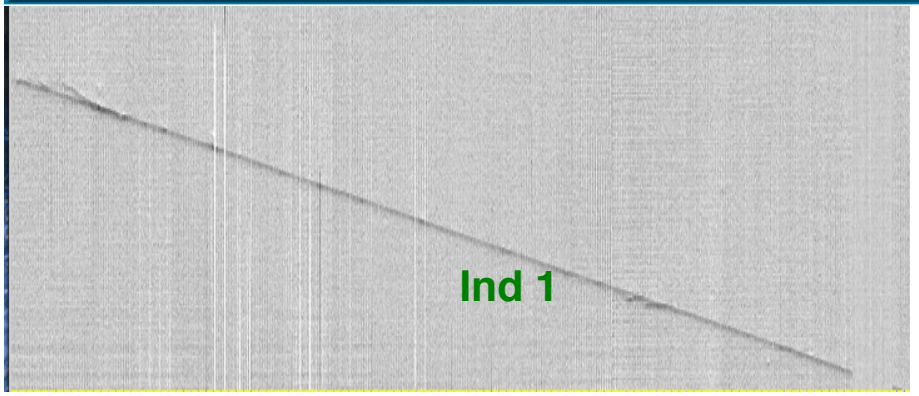
- The T600 run at LNGS on the CNGS neutrino beam confirmed a S/N better than 10 on about 53,000 channels.

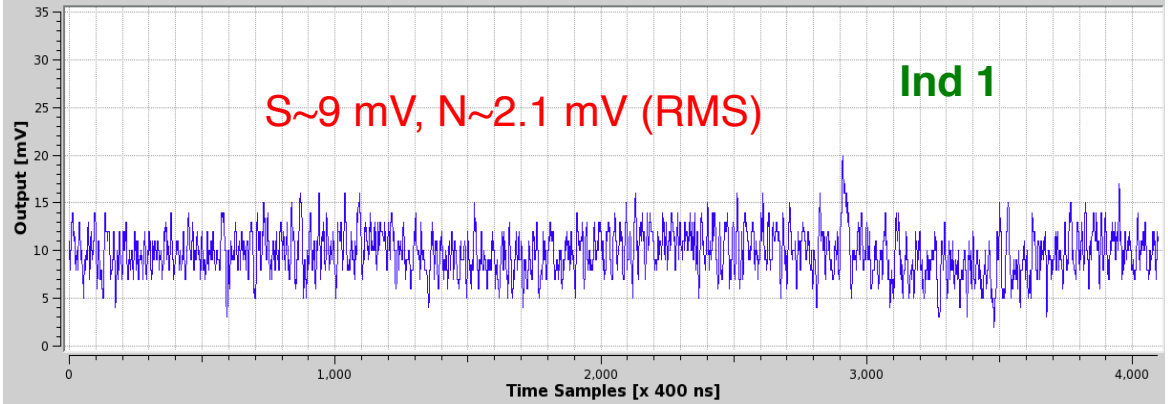
Measurement of E_dep in Induction views?

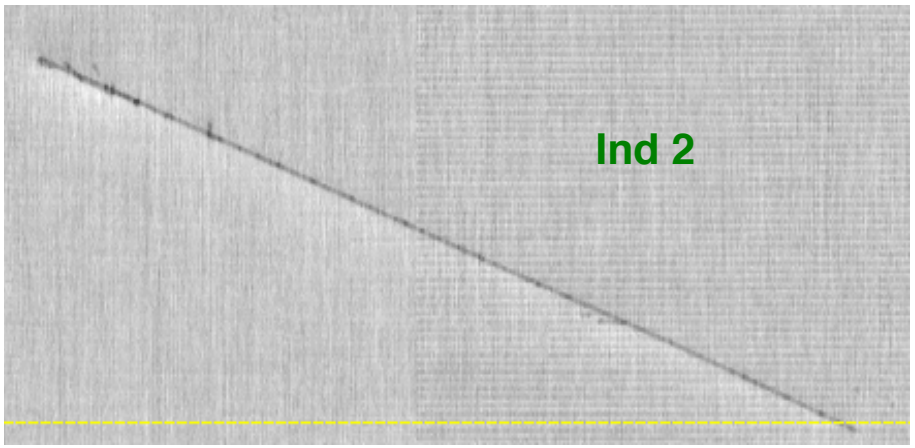
- In T600, the event energy deposition can be measured only in Collection views by the area of signals read-out with a short ~μs shaping time.

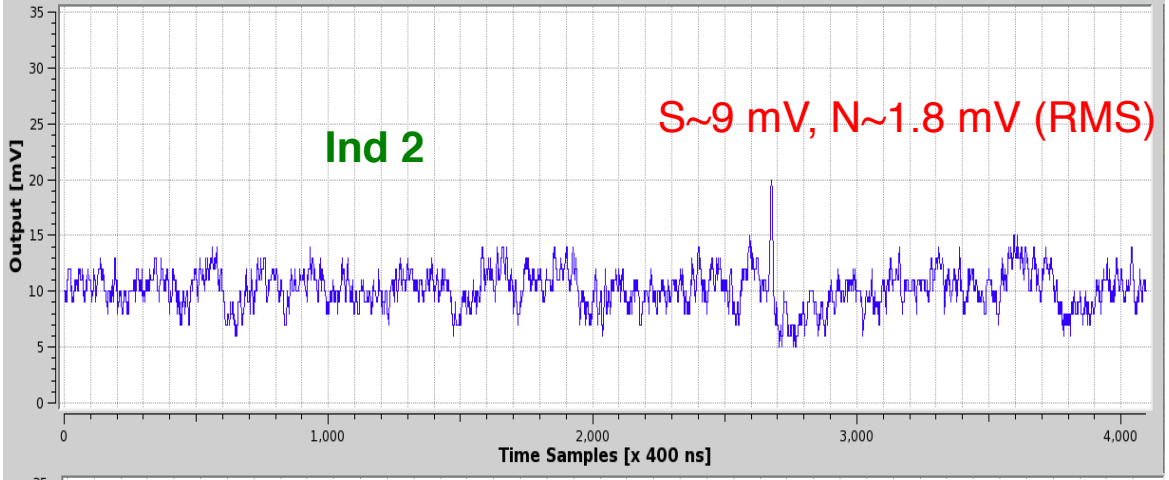
- In Induction views the bipolar signals are read-out with a ~100 μs long shaping time, to make them ~ unipolar similarly to Collection ones. However few effects prevented the charge measurement:
  - The induced charge is typically ~ 60-70% of the Collected one worsening the S/N;
  - The rise-time of the pre-amplifier is similar to the bipolar signal duration resulting in a partial cancellation of the integrated output;
  - A large signal undershoot degrade the signal base-line determination preventing the correct measurement of the signal area.

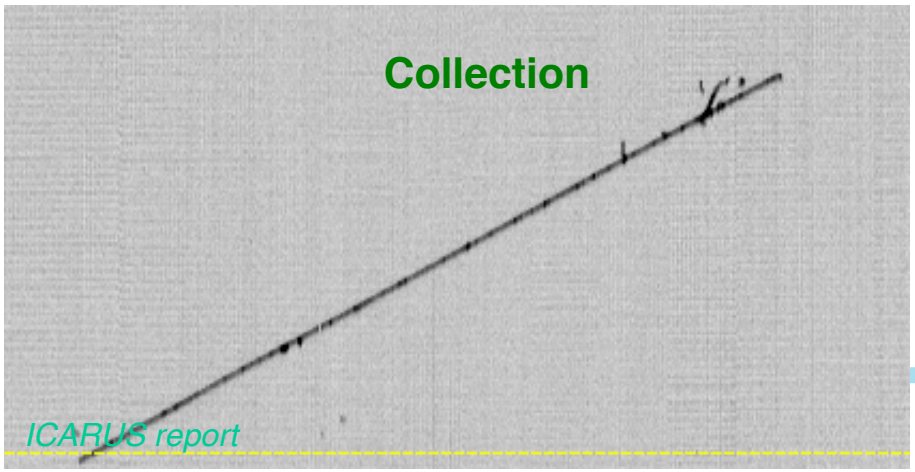
All views are fine for isolated tracks

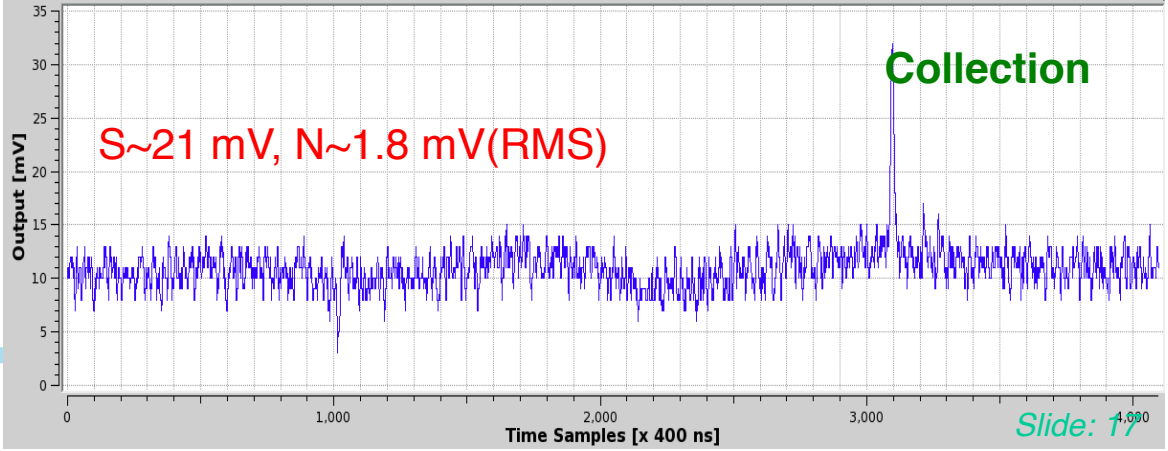






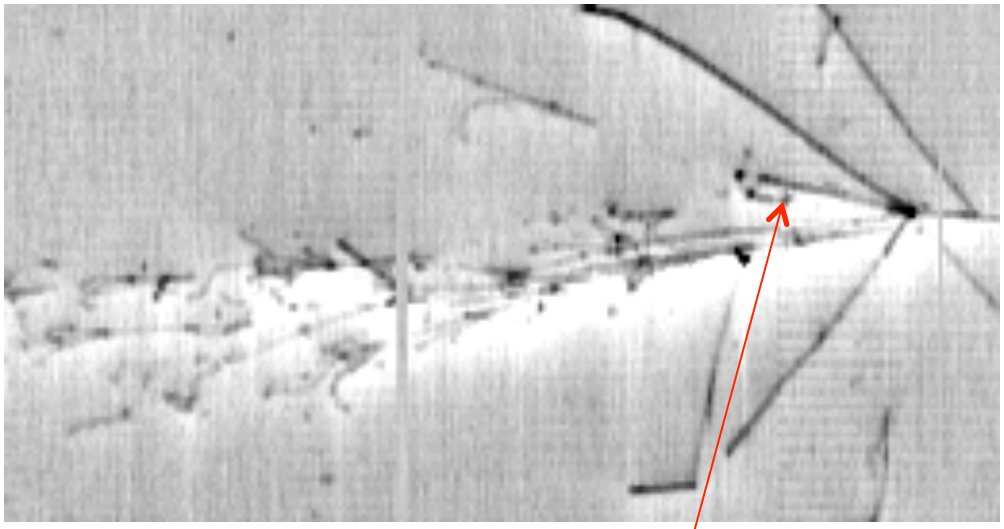




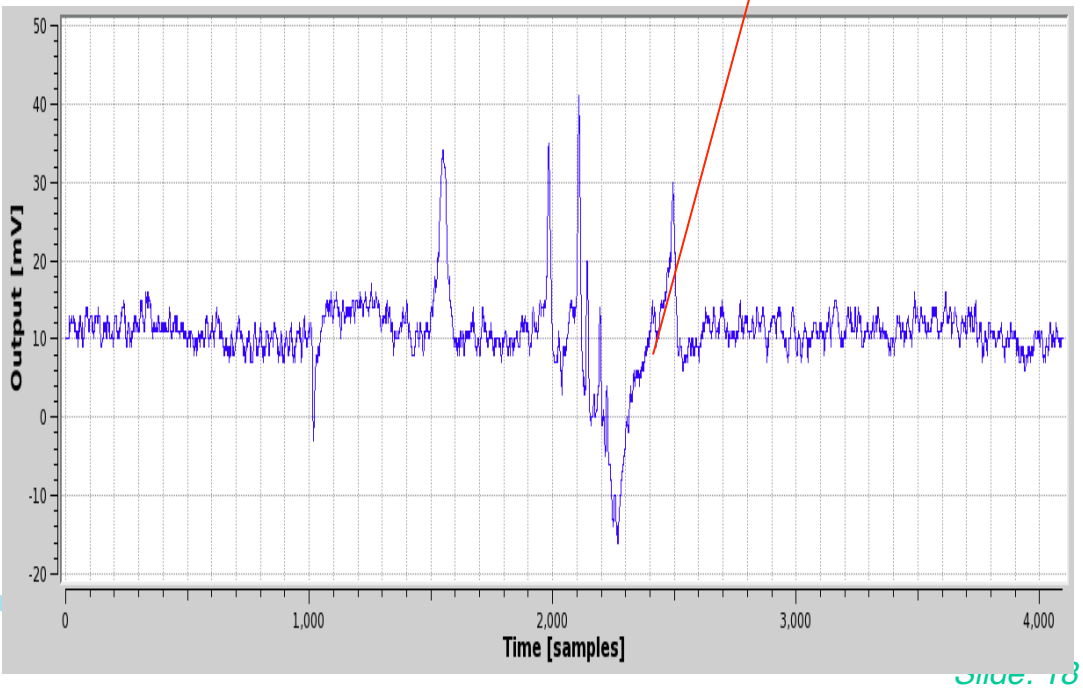


Ind2 performance limited for crowded events

- For large energy depositions (e.g. showers), the undershoot "covers" the positive signal from nearby particles.

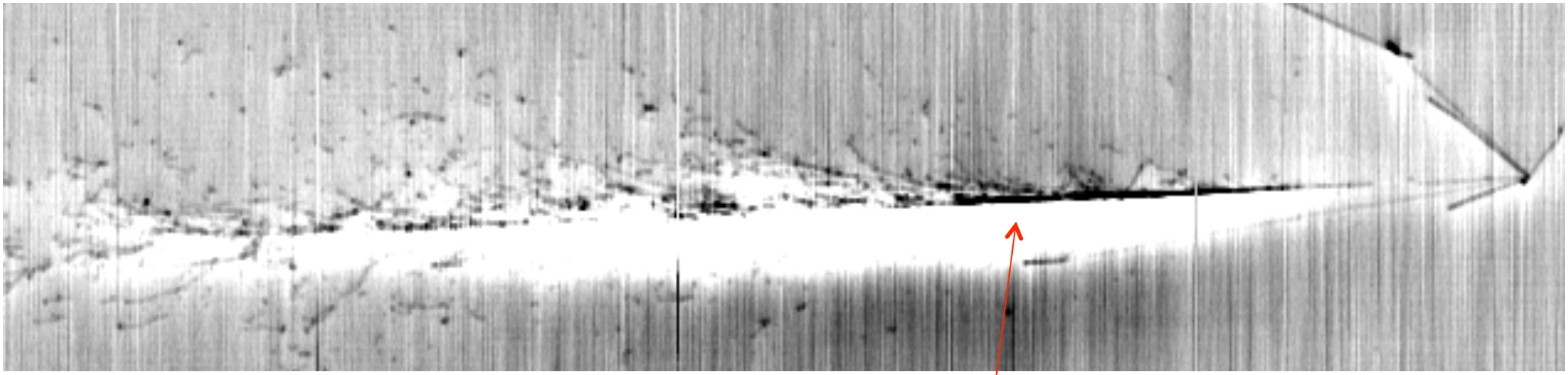


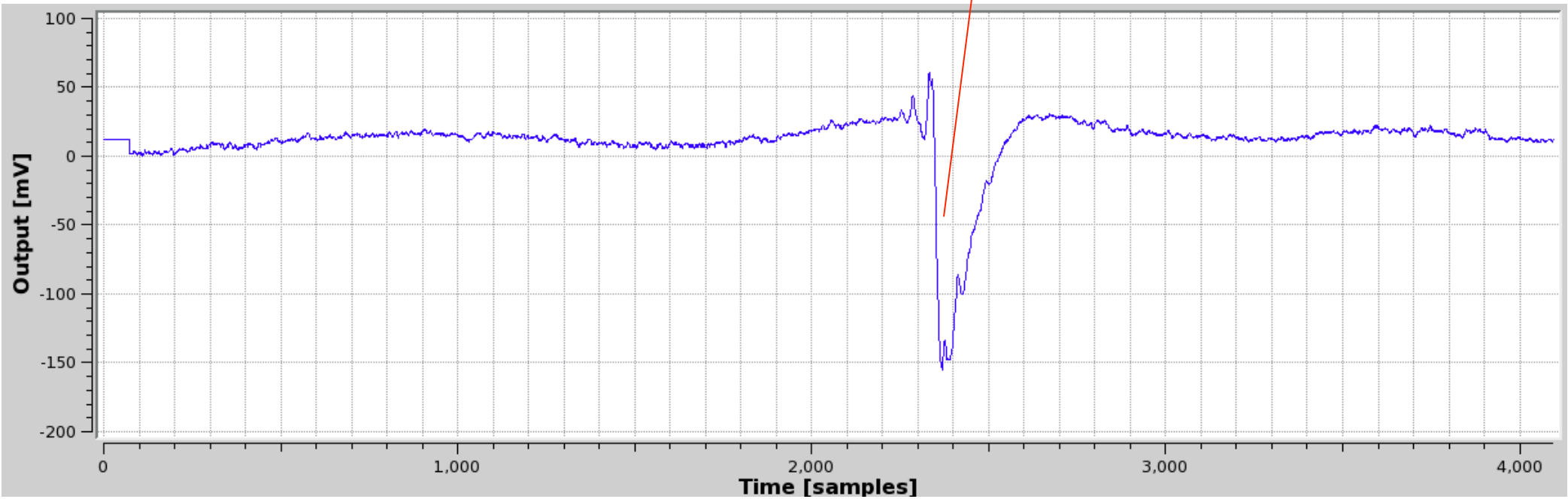
3.7 GeV deposited energy



- This significantly degrades Ind2 reconstruction capability in "crowded" topologies, like ν_e interactions.

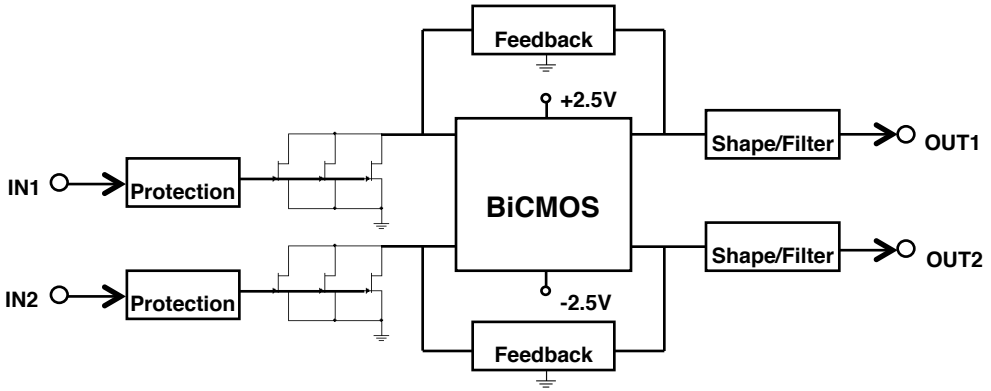
Ind2 shower in a CNGS event (23GeV)





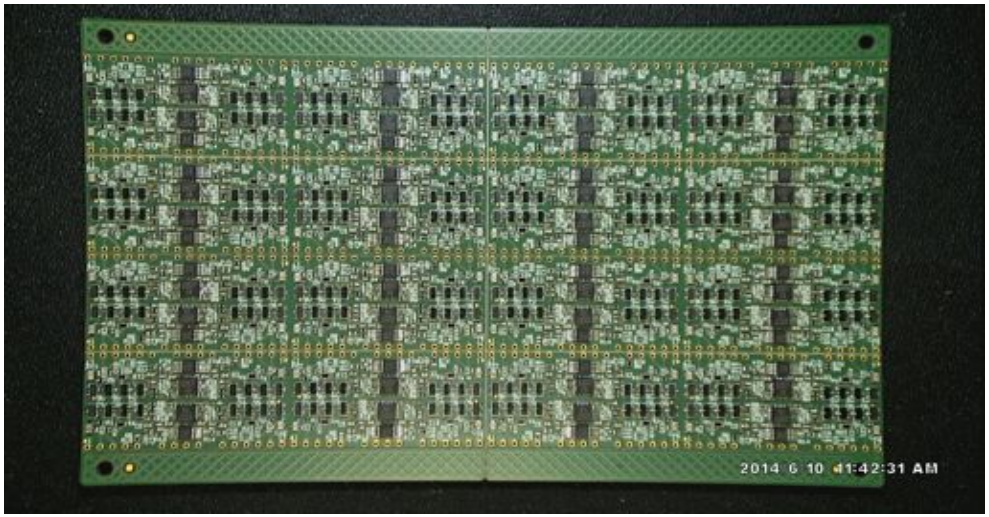
New preamplifiers

- **Two** jFet, IF4500 (Interfet) or BF861/2/3 (Philips), are connected in parallel to increase g_m (50-60 mS) at input.



- Amplifier gain set at *12mV/fC*.

- Independent optimization of the pre-amp response (shaping time and gain) is envisaged for collection and induction signals to overcome limitations in Induction 2 that were evident after the LNGS run.



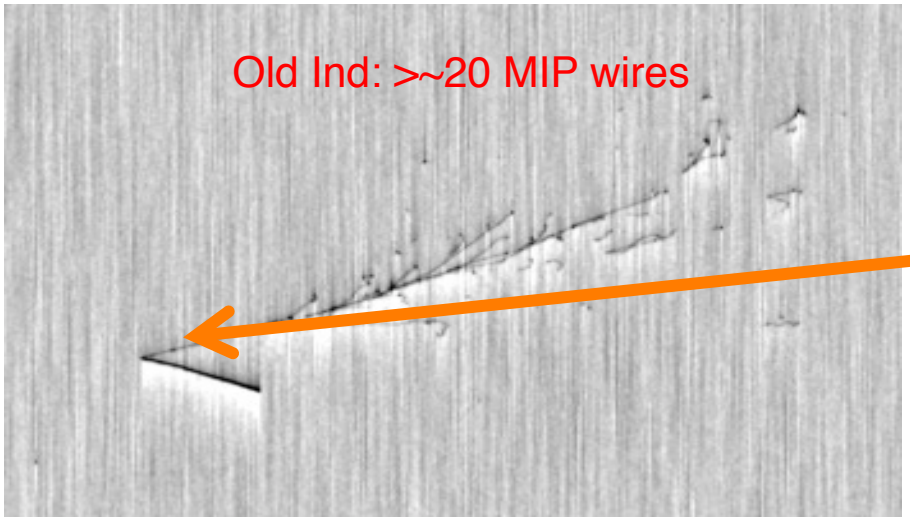
PC Board *"scored"* so the PCB circuits are *"snapped"* in eight sets of eight pre-amplifiers

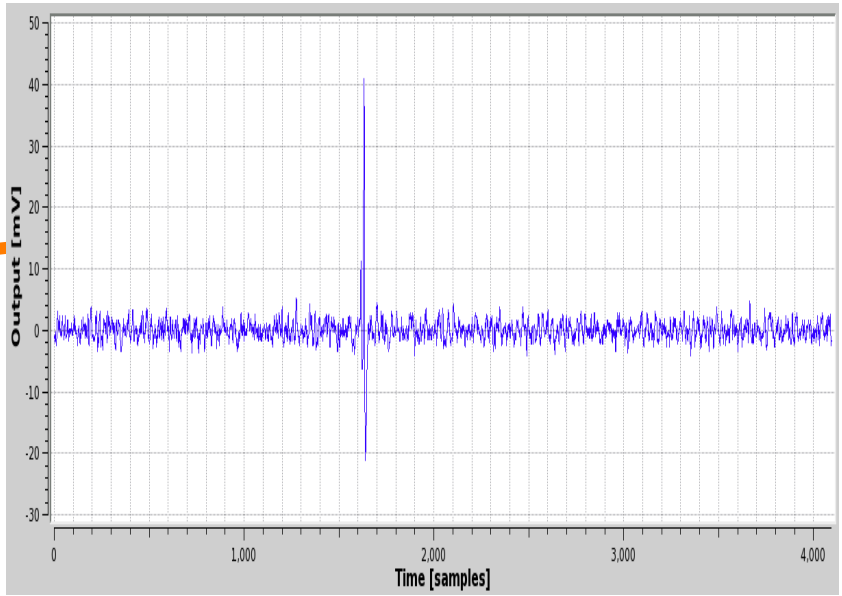
Electronics optimization

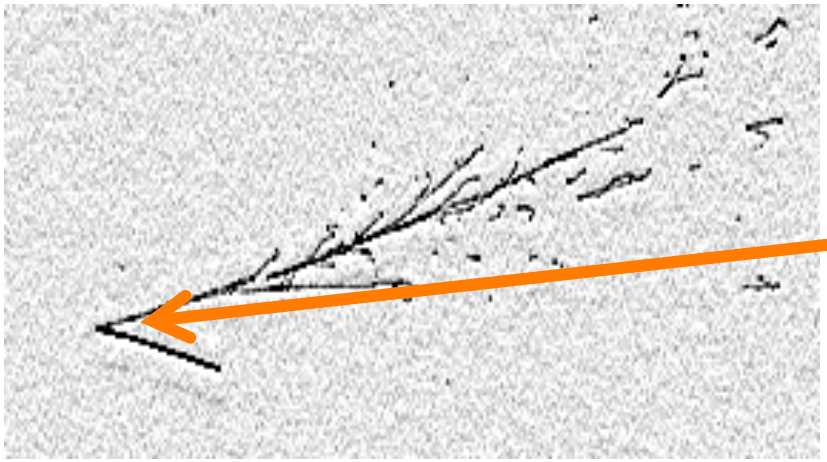
- The response of the new electronics is designed to be faster and without undershoot with shaping times optimized depending on the on-going studies. So far the best approach is:
  - signal integration by pre-amplifier (long shaping time) followed by zero-pole cancellation circuit;
  - short shaping time to preserve bipolar signals allowing for numerical integration of the digitized output.

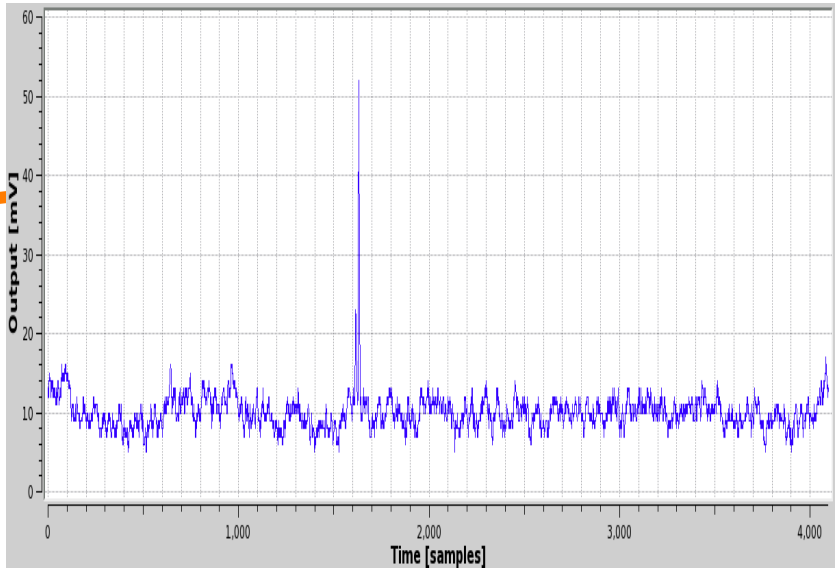
- The ongoing studies are based on signal simulations using the electronic noise recorded at LNGS run and direct measurement with ICARINO test facility and MC Fermilab events.

Some examples at FNAL (MC) – ev.150 (0.7GeV)









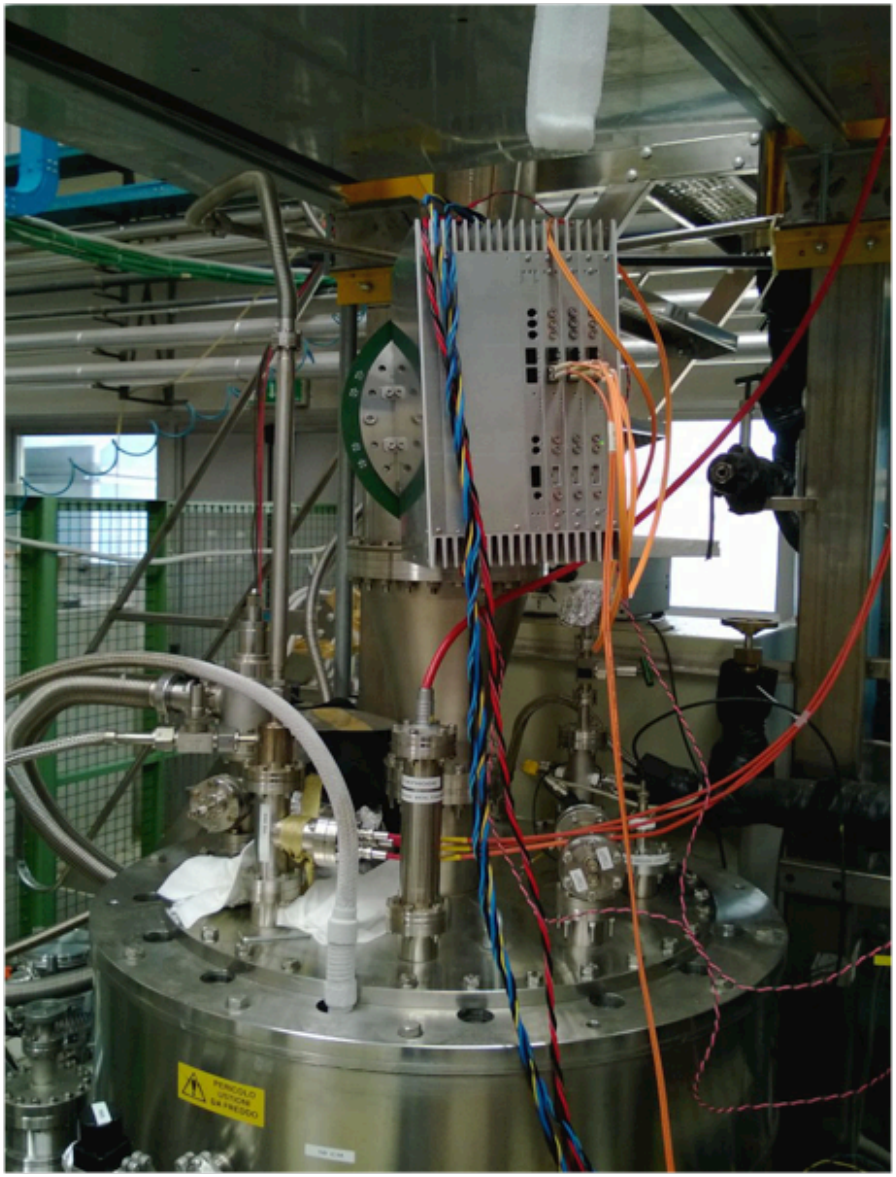
New Ind (filtered signal). Hits are resolved even very close to the vertex

Test set-up on Icarino at LNL

Icarino detector with first four boards on test.

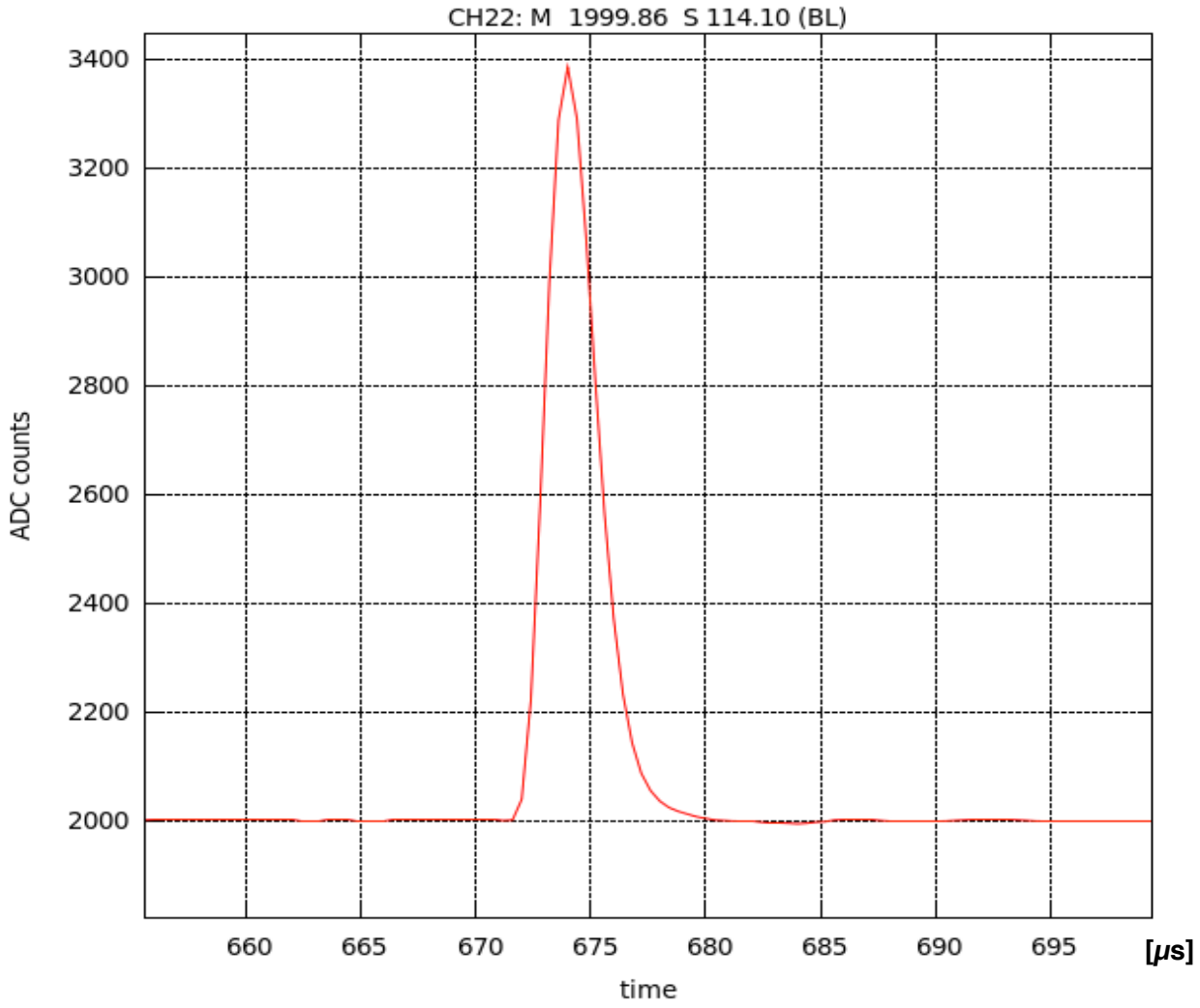
The flange can be mounted in different orientations.

In Icarus T600 likely they will be mounted on horizontal flanges.



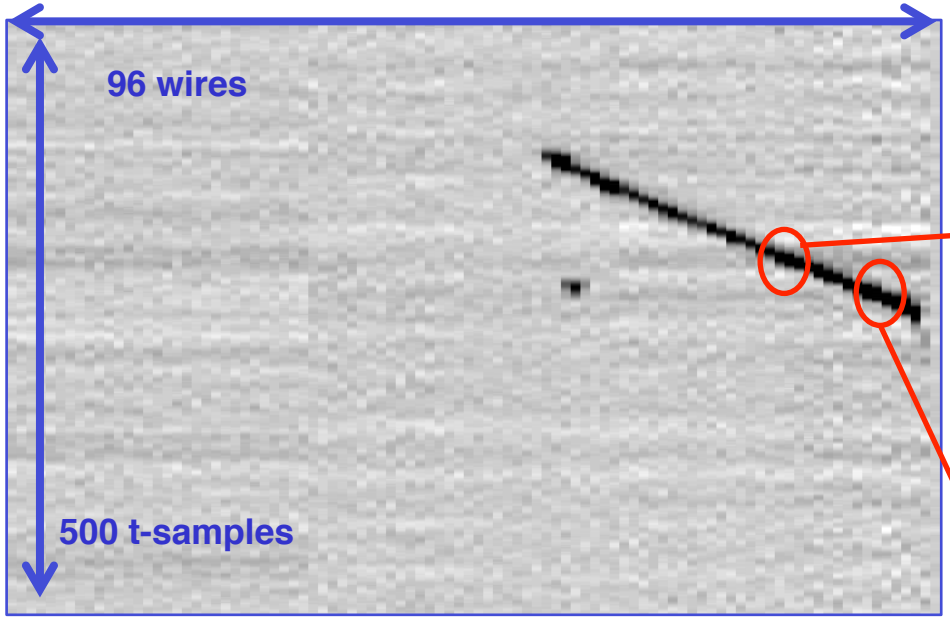
Detail of prototype boards on Icarino at LNL

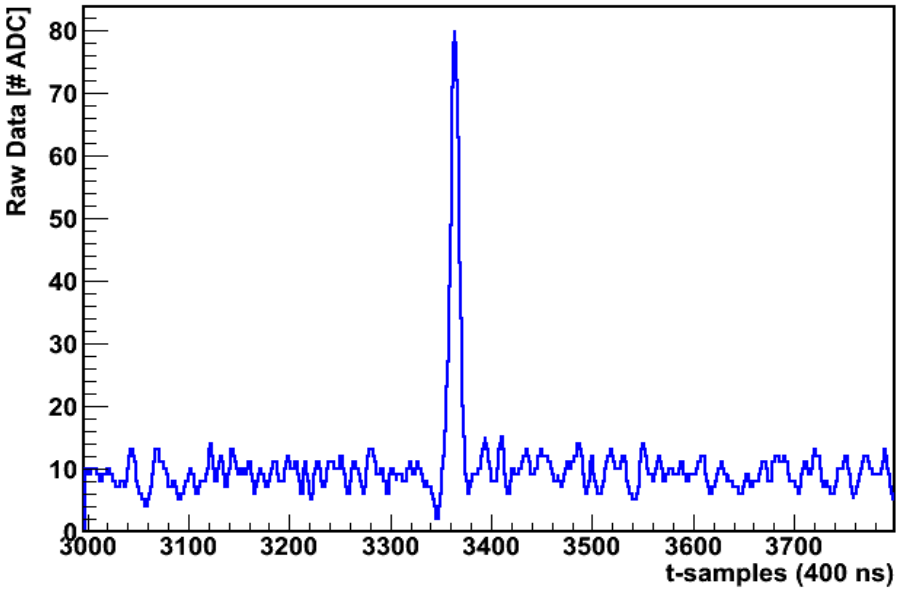
- The first eight pre-series boards mounted on a flange on Icarino.
- Daisy chained single fiber for read-out and slow control.

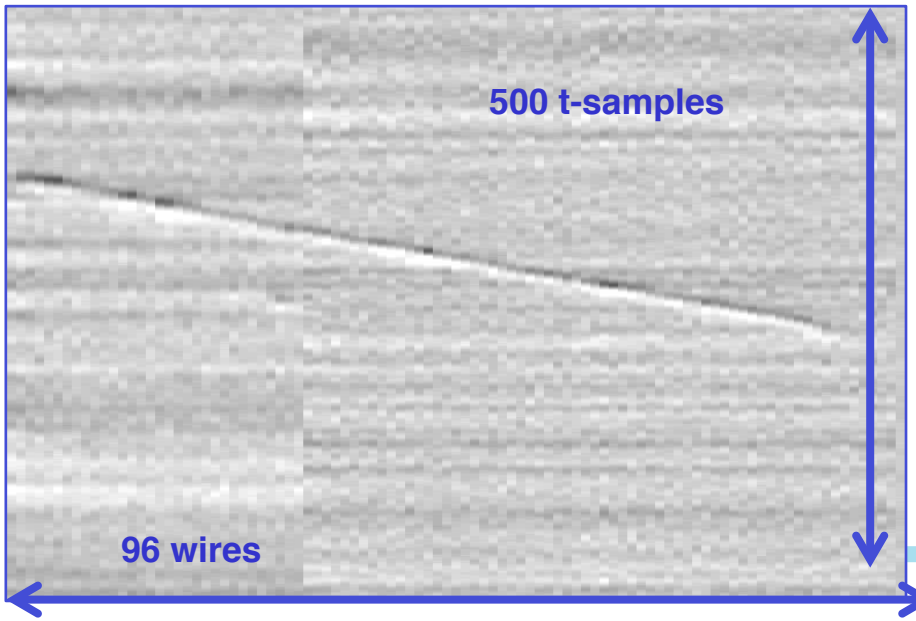


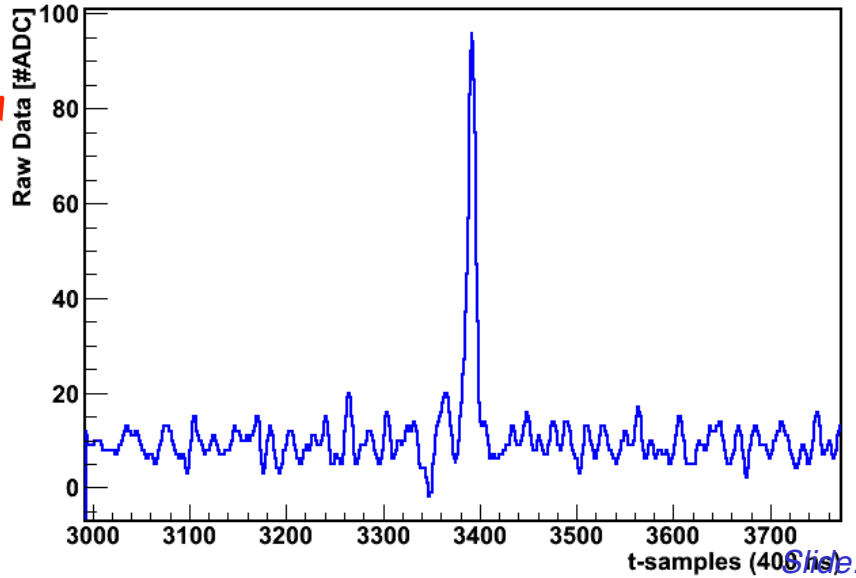
Test pulse at LNL with Icarino, dry, $C_{detector}$=410pF, 450el/count, $noise_{rms}$ 1.2-1.8counts

Run 6154 Event 24 (Icarino)

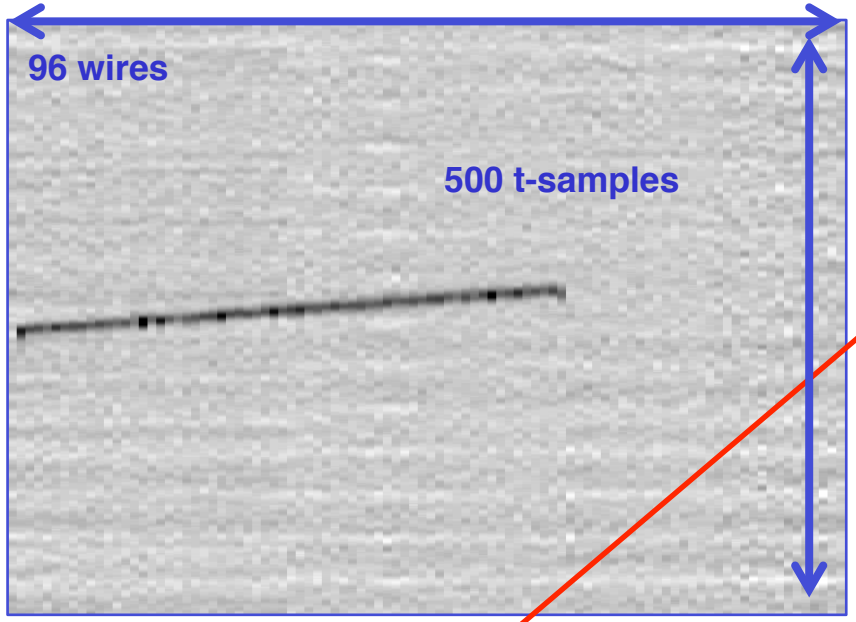


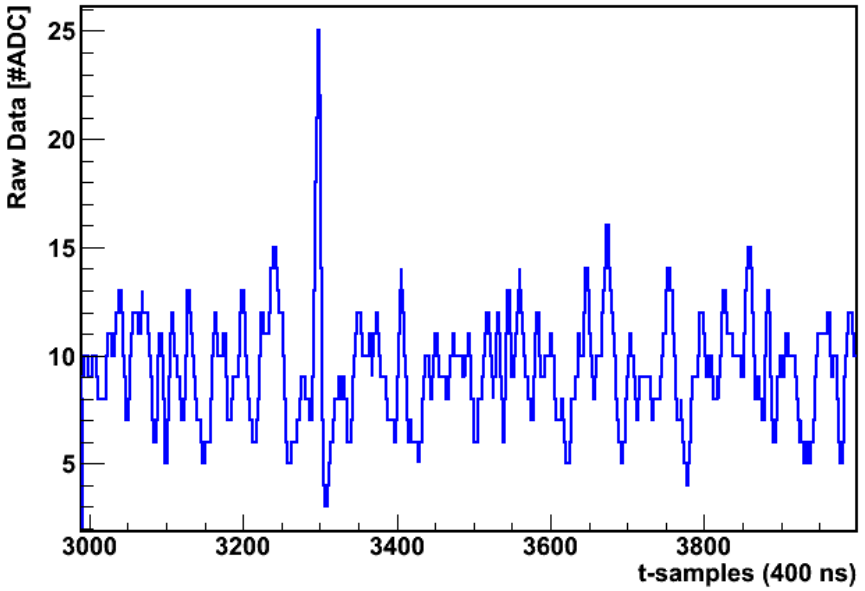


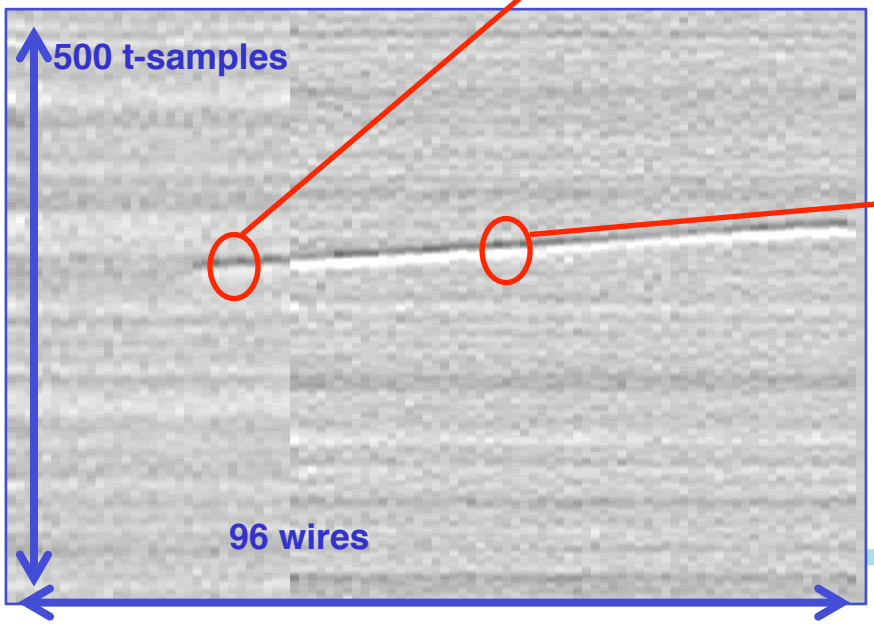


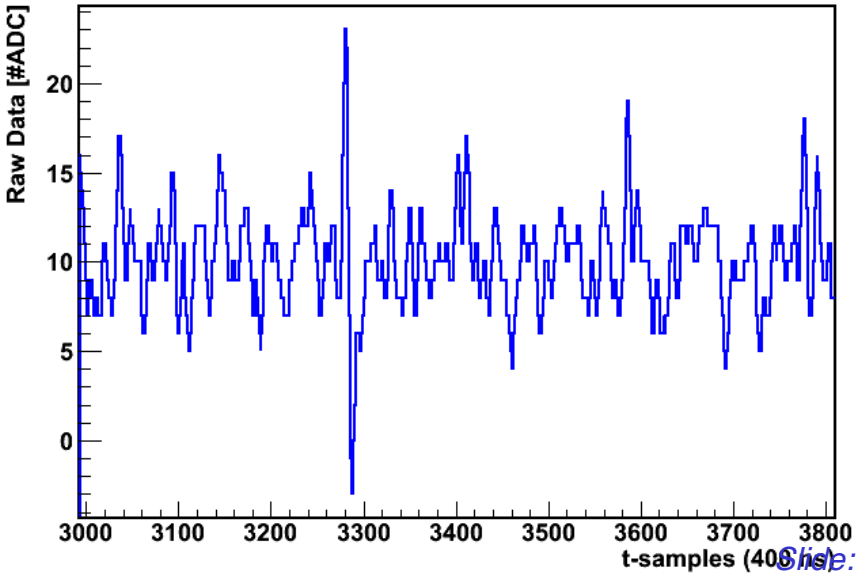


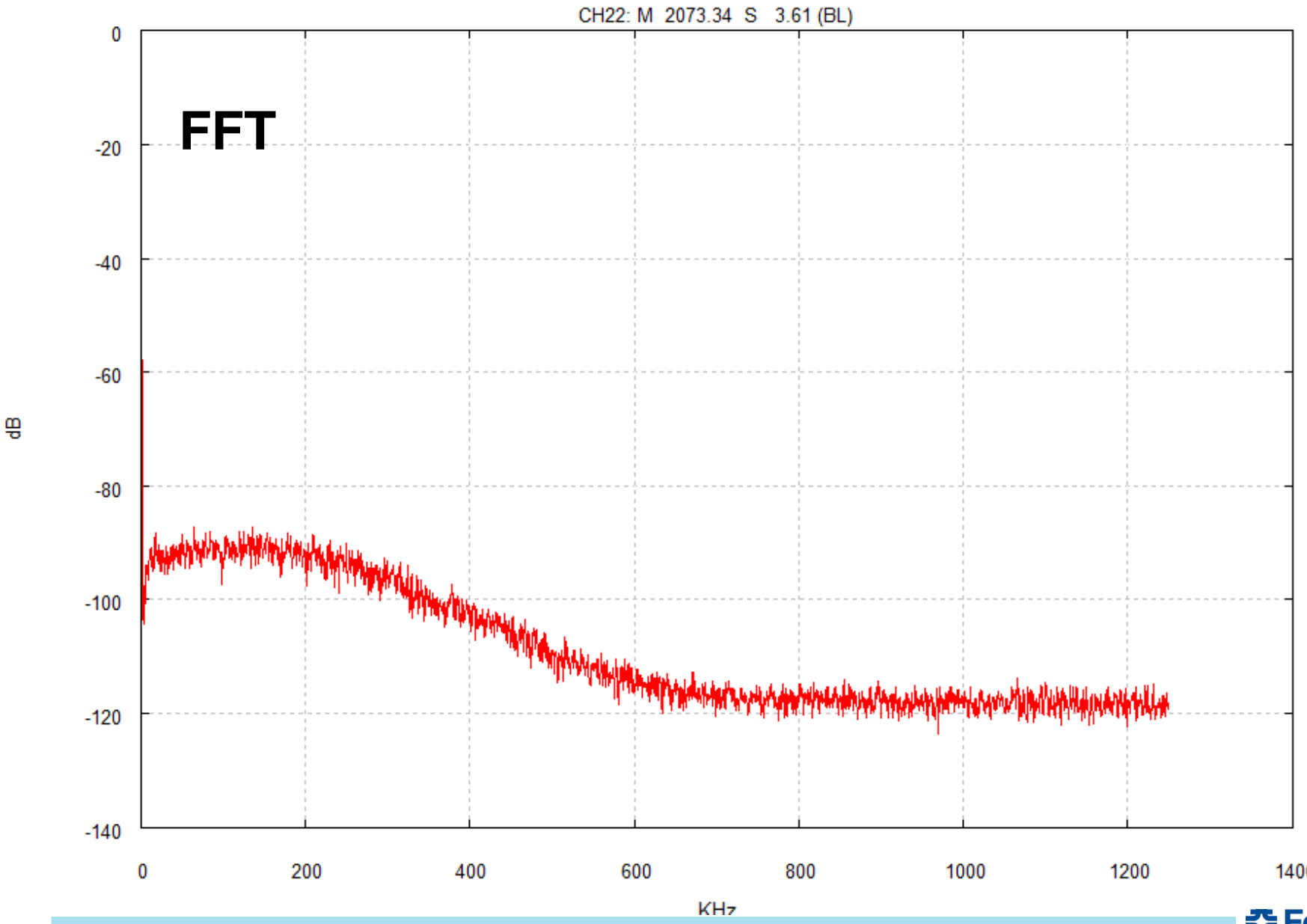
Run 6154 Event 29 (Icarino)










CH22: M 2073.34 S 3.61 (BL)
FFT
dB
0
-20
-40
-60
-80
-100
-120
-140
0
200
400
600
800
1000
1200
1400
KHz

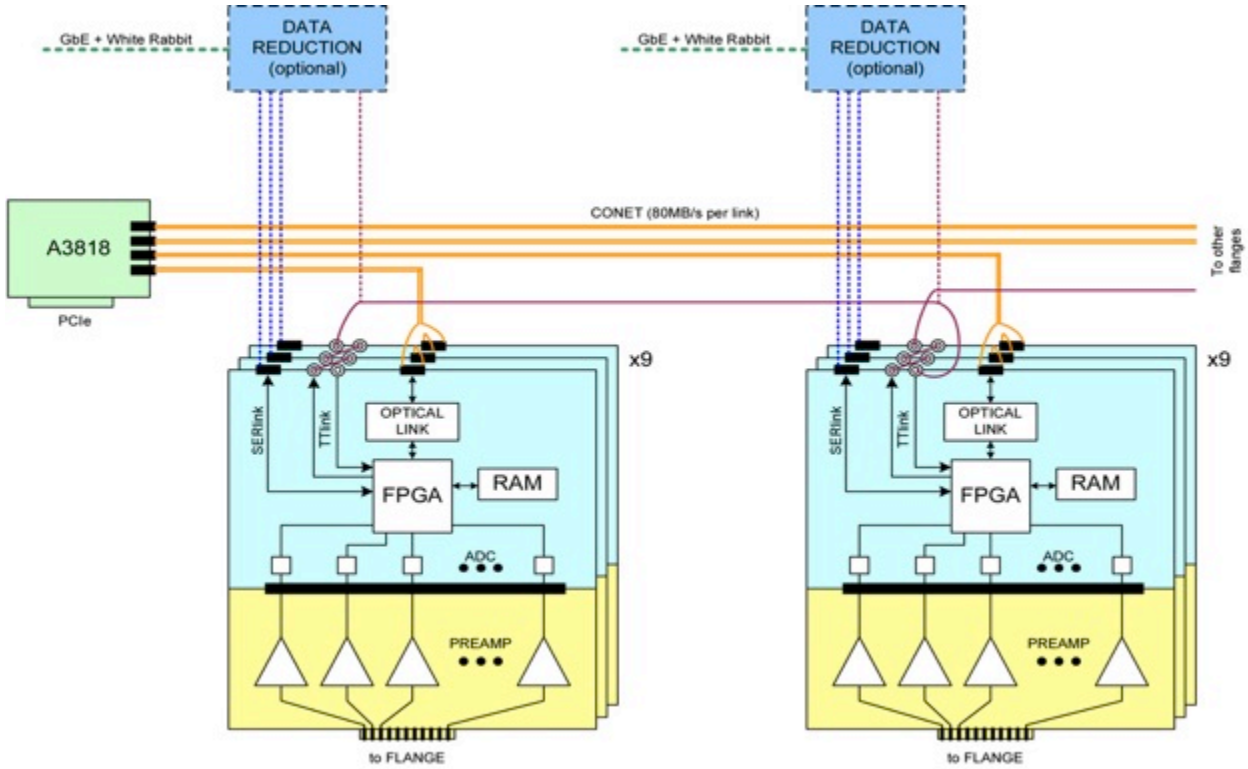
Tests on new readout

- First results with test pulses on new front-end with 1.5 us peaking-time show a noise level compatible with expectations (~450 electrons at C_d = 0).
- Bench tests in PD are underway on a complete DAQ set (from the flange to the optical data link receiver) with eight 64 channel boards.

- Several versions of the frontend preamps (with peaking-time ranging from 1.5 to 2.5 us) are under test to find the best match with the LAr-TPC induction/collection signals in terms of S/N and space/energy resolutions.
- Integration into the existing ICARUS event builder architecture is also underway and will be tested in LNL with ICARINO.

DAQ architecture

- Performance, in terms of throughput of the read-out system, has been improved replacing the VME (8 - 10 MB/s) and the sequential order single board access mode inherent to the shared bus architecture, with a modern switched I/O. Such I/O transaction can be carried over low cost optical Gigabit/s serial links.
- The prototype under development uses provisionally the CONET (by CAEN) transfer protocol and one A3818 controller for up to 2304 chs, four flanges.



Present activities

- One complete prototype set is now available for bench test in Padova :
  - Four new flanges (for 576 channels each)
  - Four mini-rack equipped with 9 boards each (analog + digital)
  - Two preamplifier versions with different shaping time
  - 12-bit ACD's and new optical data-link for data acquisition

- This provisional DAQ system is now mounted on the ICARINO test facility at LNL for qualification on real LAr-TPC data and for comparison with the old ICARUS read-out system.

Provisional schedule

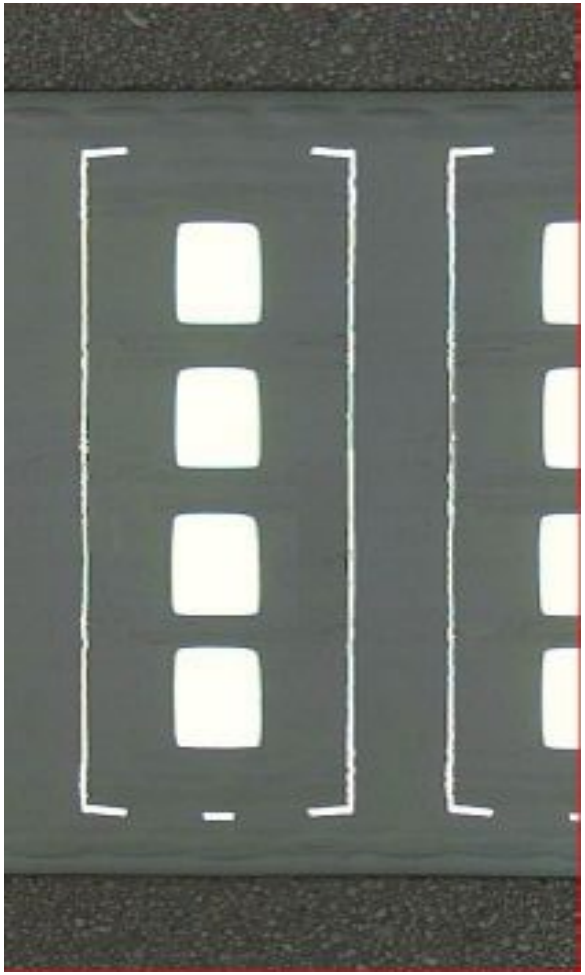
- Since November: read out electronics tests ongoing at LNL & CERN
- CSN2 has made available 137k€ that we used for 10 pre-series, *baseline solution*, 64-channels boards.
- Front-end chips (packaging and testing) already ordered to IMEC via Europractice for an amount of 57k€
- Flanges production is independent of the above choice and can start anytime as soon as it is funded. Previous experience with T600 at LNGS demonstrated that flanges can be produced in two months.
- Four complete sets (flanges and crates) has been ordered within CSN2 available funds.
- For 2016 fiscal year CSN2 has assigned 530k€. Total cost of electronics is 1950k€.

Thank you !

The ICARUS signal flanges

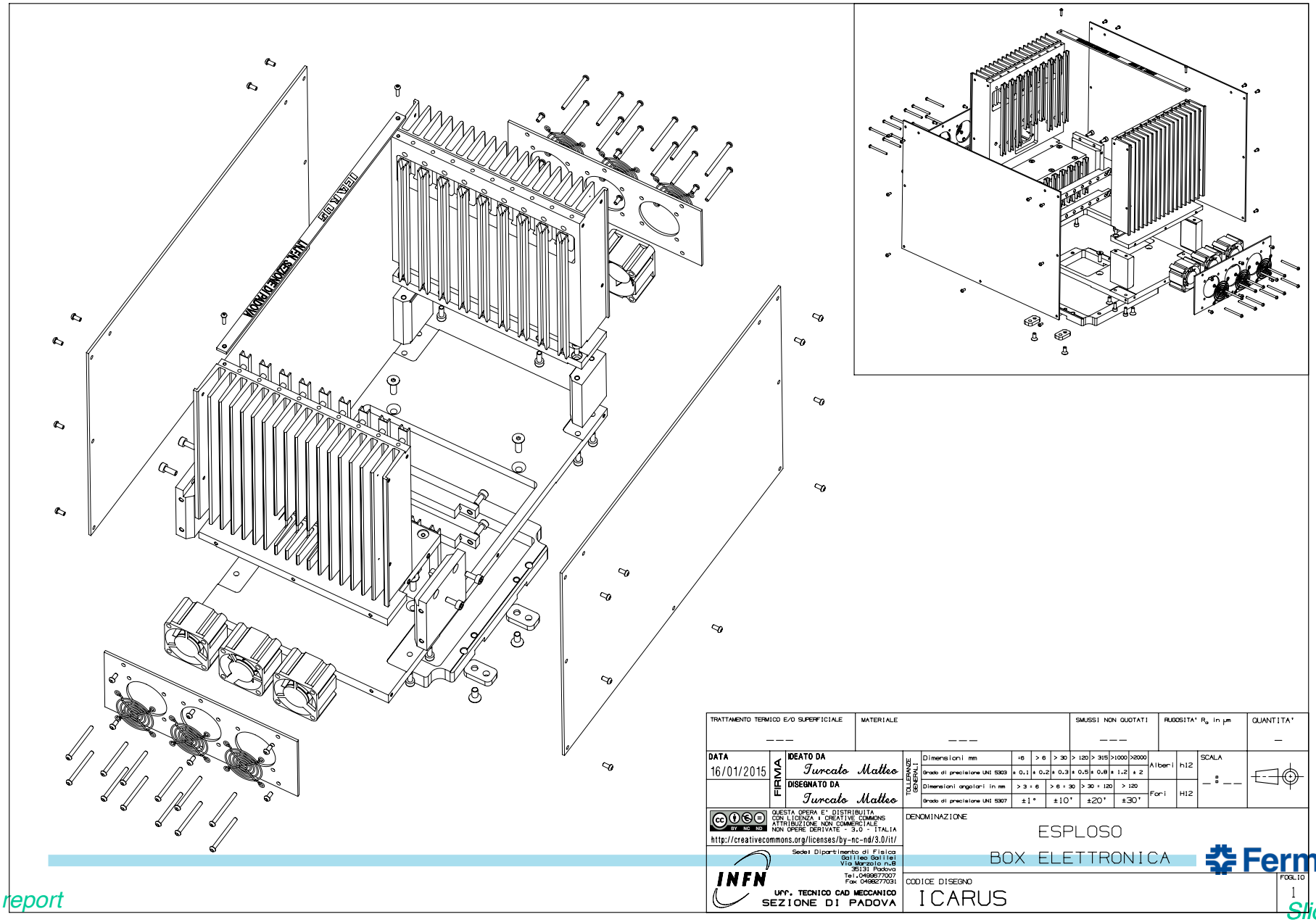
- For T600 detector a very reliable and cost effective feed-through flange (CF 200) was developed, which allows the connections of 18 cables, twisted pairs, each conveying 32 signals, from wire chamber to external electronics.

- The external contacts, on both sides, are on different planes with respect to the internal vias, allowing for SMD connectors use and guaranteeing vacuum tightness. The white squares are brass disks that reinforce the flange structure to stand atmospheric pressure without deformation in case of use in vacuum vessels.



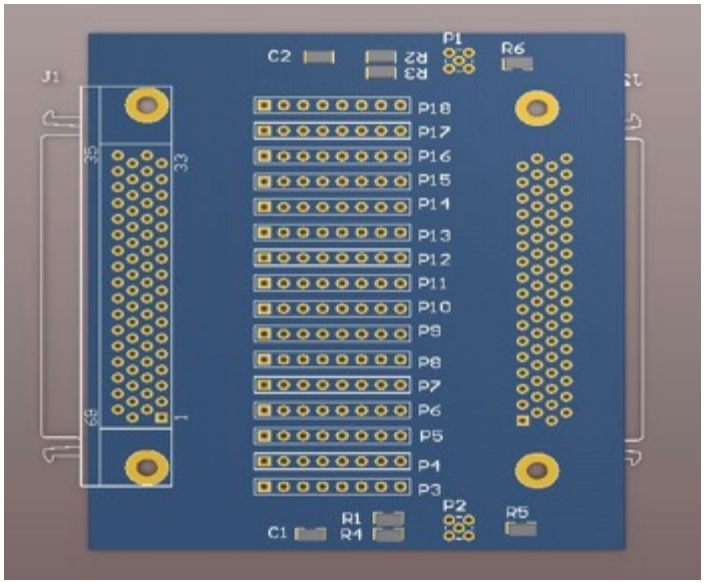
Feed-through section, 6mm thick

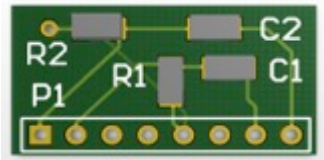
Card cage layout for T600 (4 proto ordered)



Re-cabling the T600 TPCs

- What will be redone:
  - The length of flat cable will be increased of at least 30 cm for all of them.
  - Decoupling capacitor and biasing resistors will be placed inside vessel (special adapter is under development with 32 decoupling capacitors and biasing resistors).
  - New coaxial biasing cable.
  - New mechanical support for the flat cables.



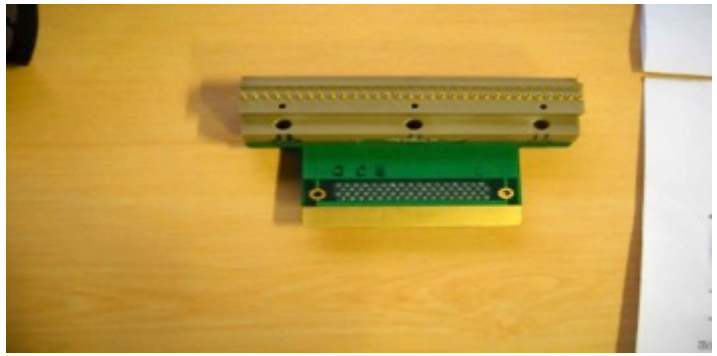


General layout of adapter board

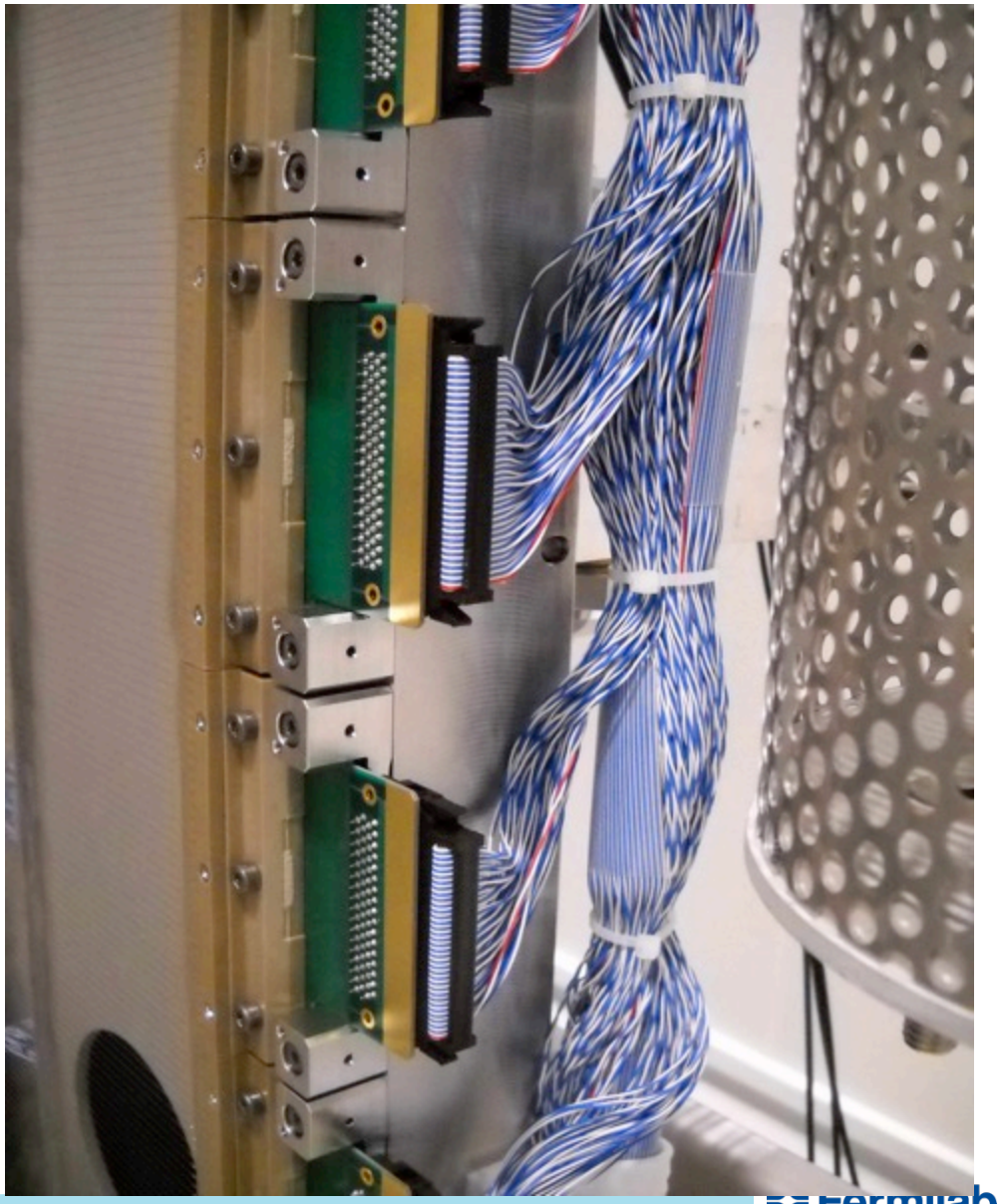
- Work in progress :
  - Capacitors reliability test at liquid argon temperature
  - Resistors reliability test at liquid argon temperature
  - High voltage cable leakage test
  - Layout of adapter board optimization.

Re-cabling the T600 TPCs

- What will not be changed:
  - The cabling mapping.
  - Type of the connector.



New type of flat twisted pair cable will be mounted.



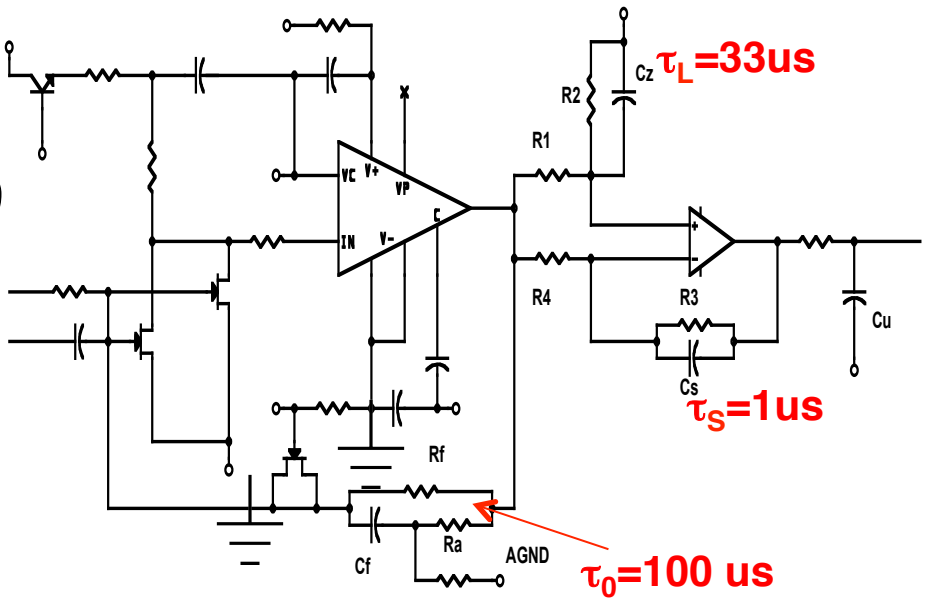
Ind2 undershoot

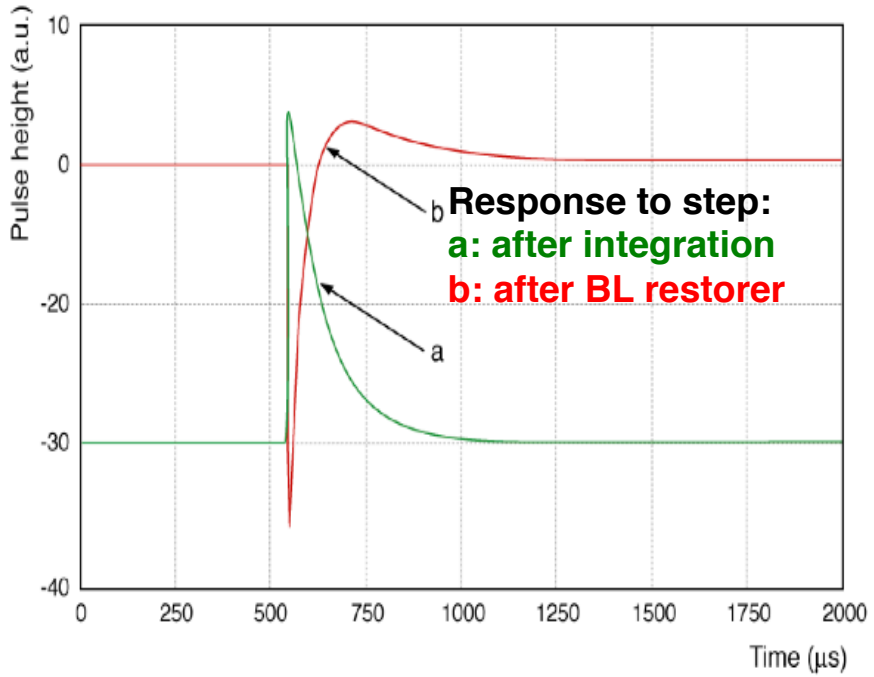
- The charge-mode Ind2 processing implemented in two stages:
  - First, an integration with τ_0~100 μs is performed. It produces unipolar signal but strongly enhances low-frequency noise
  - Low frequencies are then cut by a *baseline restorer*: difference between long (τ_L~33 μs) and short (τ_S=1 μs) integrations

Response function:

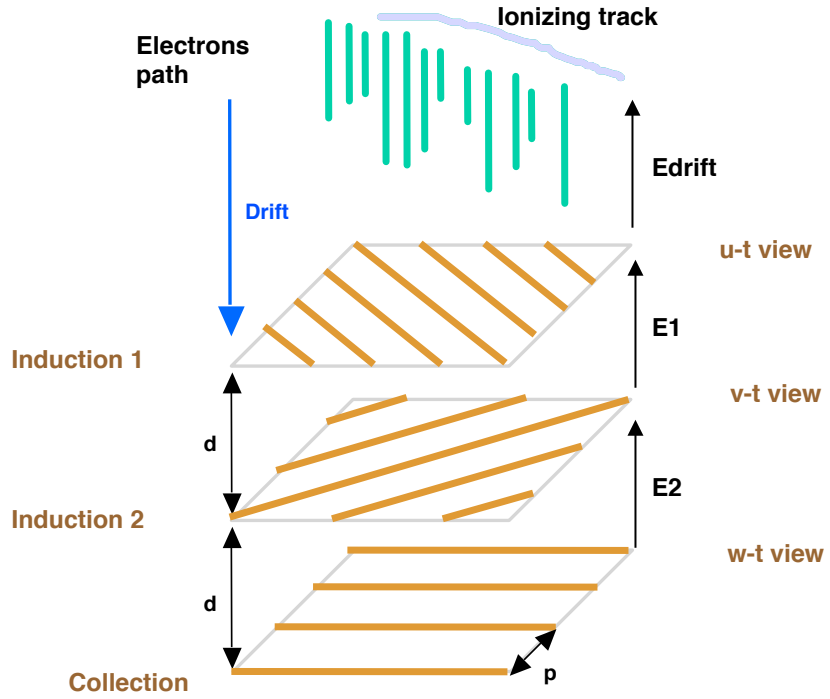
$$e^{-t/\tau_0} - e^{-t/\tau_L} - 3e^{-t/\tau_S}$$

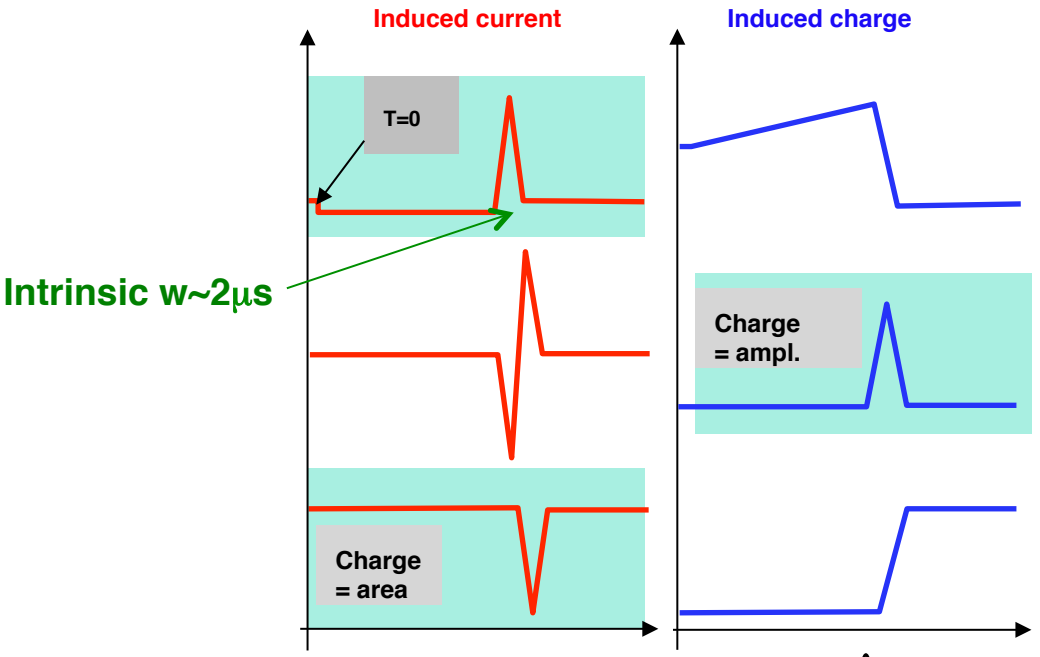
- The interference between τ_0 and τ_L produces long, unwanted undershoot

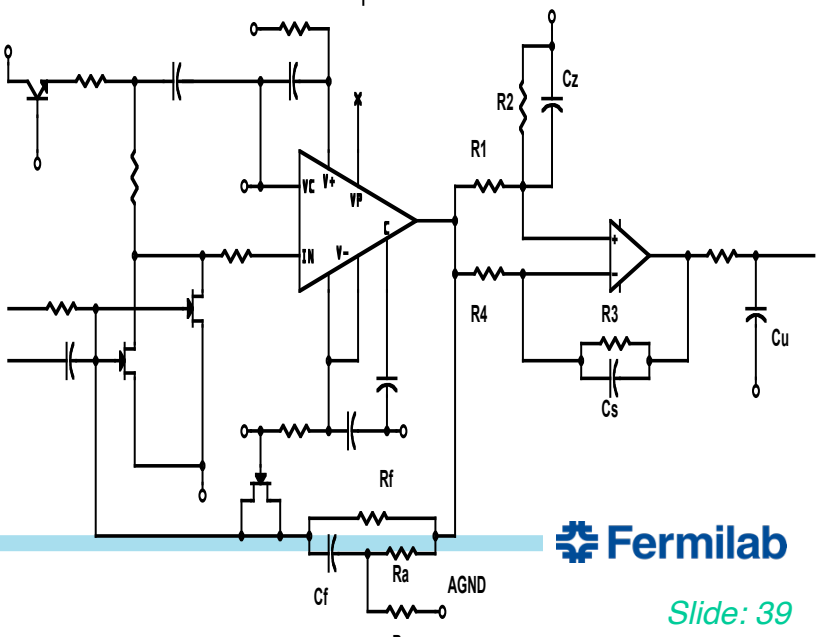




Present T600 readout electronics





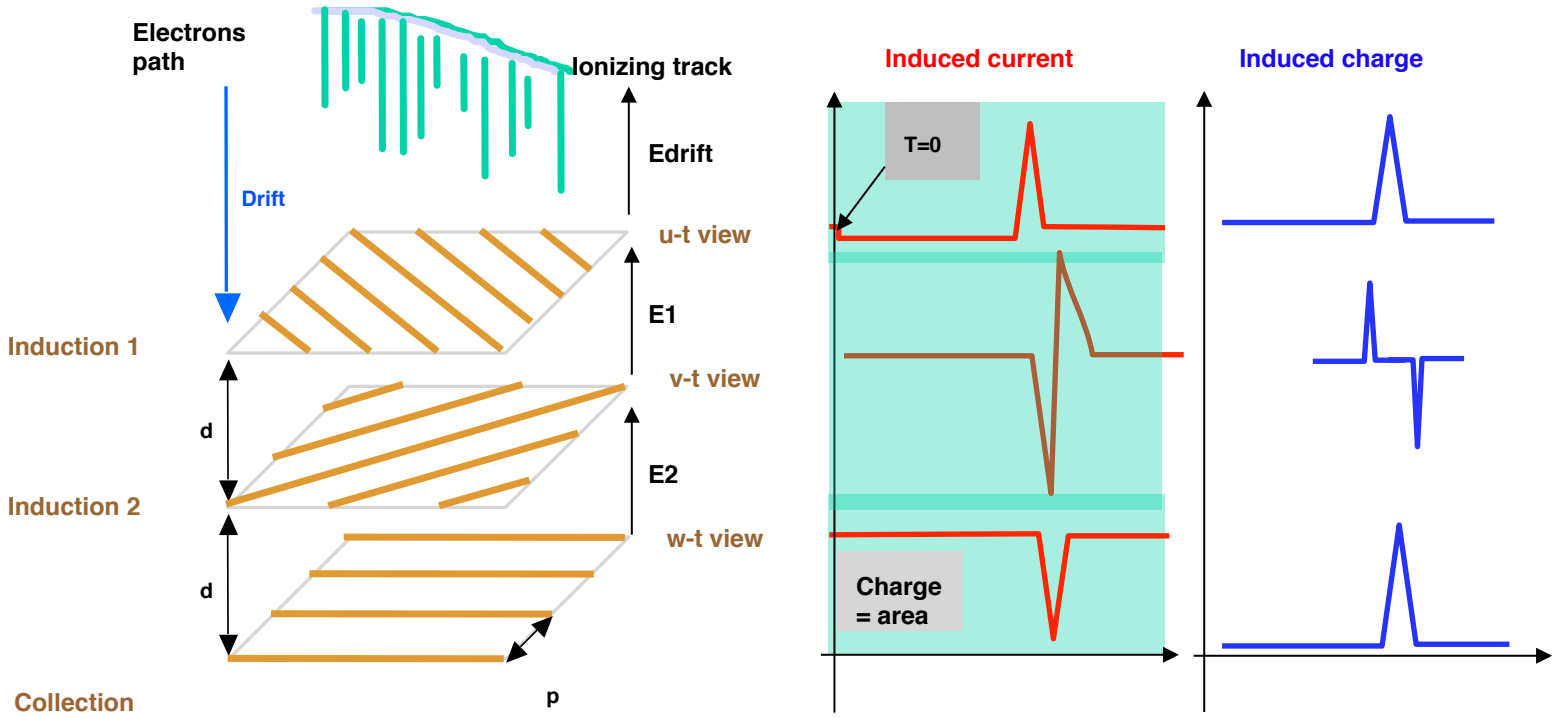


Shaping time determined by R_fC_f:

- CURRENT MODE (Induction 1, Collection): R_fC_f~3μs. Signal proportional to induced current. Integral of Collection signal area proportional to deposited charge.
- CHARGE MODE (Induction 2): R_fC_f~100 μs. Signal amplitude proportional to charge.

Front-end followed by 10-bit digitization.

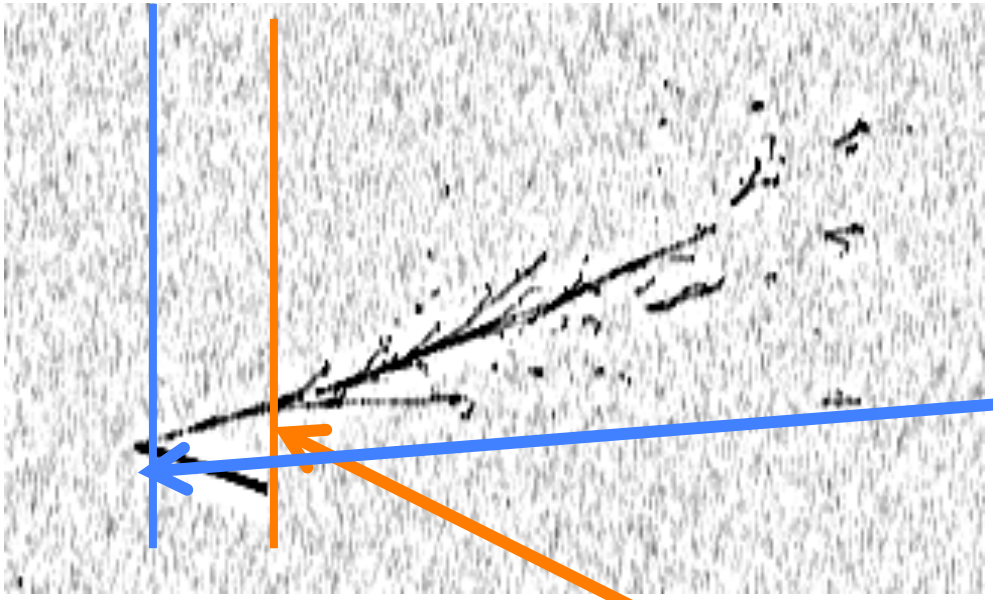
Proposed new readout electronics

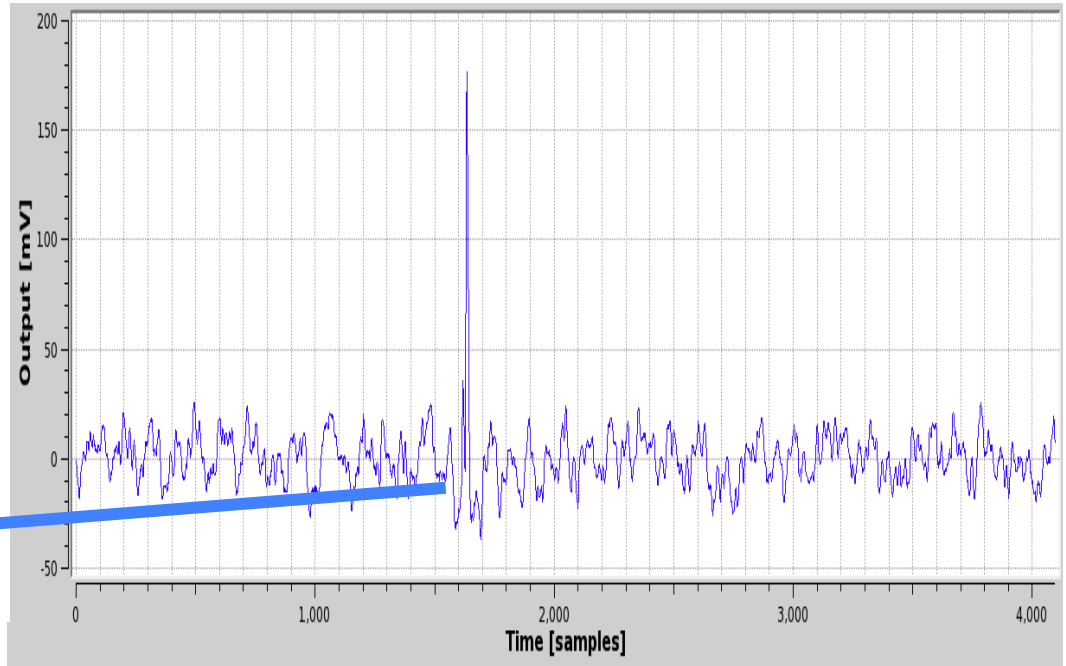


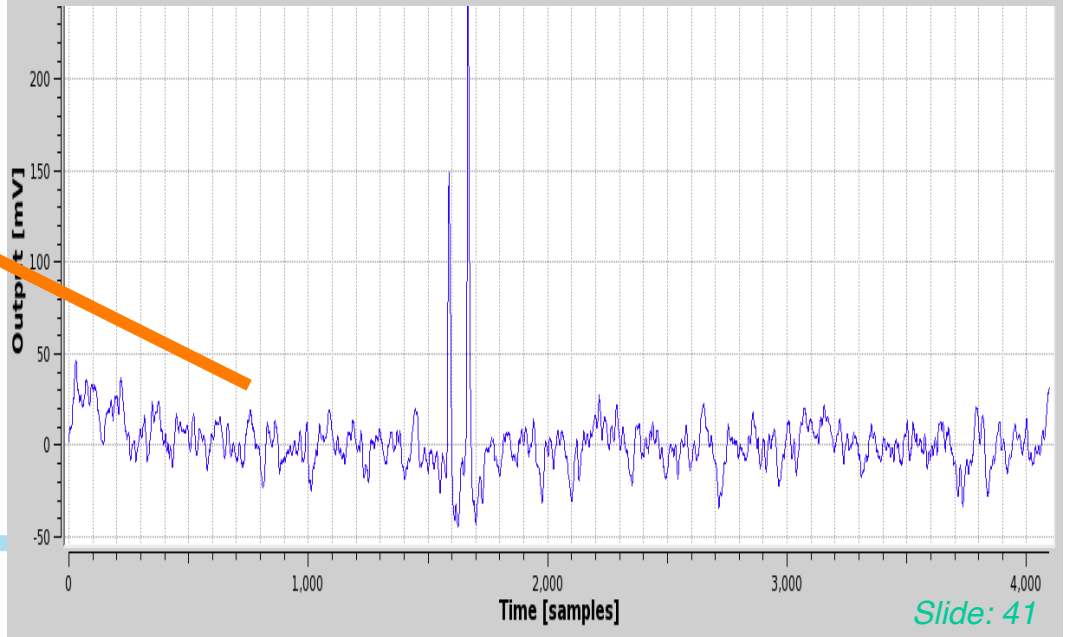
- All views (including Ind2) are read out with pole-zero shaping with τ =1.5μs .
- Response function: $\frac{t}{\tau} e^{-\frac{t}{\tau}}$

Example at FNAL (MC) – ev.150 (0.7GeV)

New Ind (integrated signal). Ugly display due to 12-bit; graphics to be tuned…



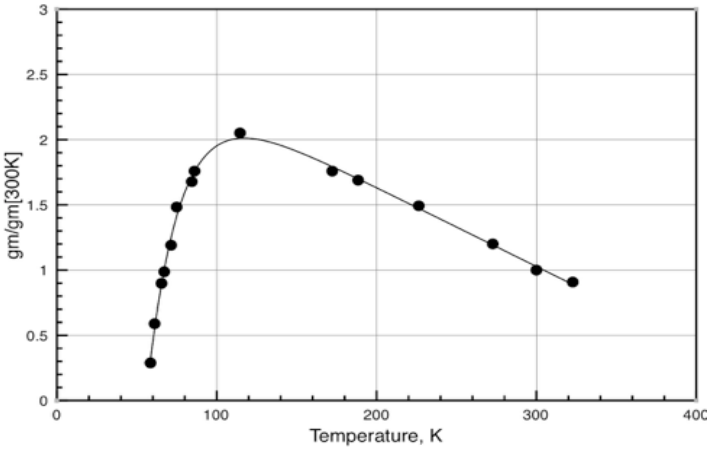




MIPs close to vertex (correctly identified) fall into undershoot.
MIPs start to be measurable at~10 wires from vertex. Event can be recovered

The "Cold" option

- The possibility of front-end in LAr has been investigated since the beginning of Icarus project (1987). The amplifier serial input noise, $e^2 \propto C_d^2/g_m$, linearly increases with detector and cable capacitance, C_d, and decreases with $\sqrt{g_m}$ input stage trans-conductance.



- *PRO: shorter cable and* 26% higher g_m at LAr temp. would allow S/N improvement of about 80% (collection wires S/N from 10 to 18). Next slide will show how this effect will be *masked in operation.*
- CONS: in case of large mass LAr-TPCs a detector lifetime in the order of ten years is expected. In this period, it is natural to foresee improvement programs in the electronics because of its natural evolution and progress.

The “Cold” option

- Average cable length inside T600 is 2,2m with C_{cable}=52pf/m, that means C=~114pf total;
- Detector itself has a wire capacitance of 21pF/m that means ~118pf;
- Cold electronics, assuming 50cm cable, means (118+25)/(118+114)=.6 capacitance reduction;
- Noise measured (~1600e) during LNGS run indicated an “equivalent” capacitance ≥400pf, much more than the cable plus detector (unavoidable) capacitance;
- That indicates that the major problem is NOT the cable capacitance but the general layout of the system;
- But the major issues are:

  -the new release of the cold FE will be available late 2016;

  -the housing of front end inside the T600 would imply **major mechanical interventions onto the the detector frame**.