Mu2e CD3c Review
WBS 9.2 Data Acquisition

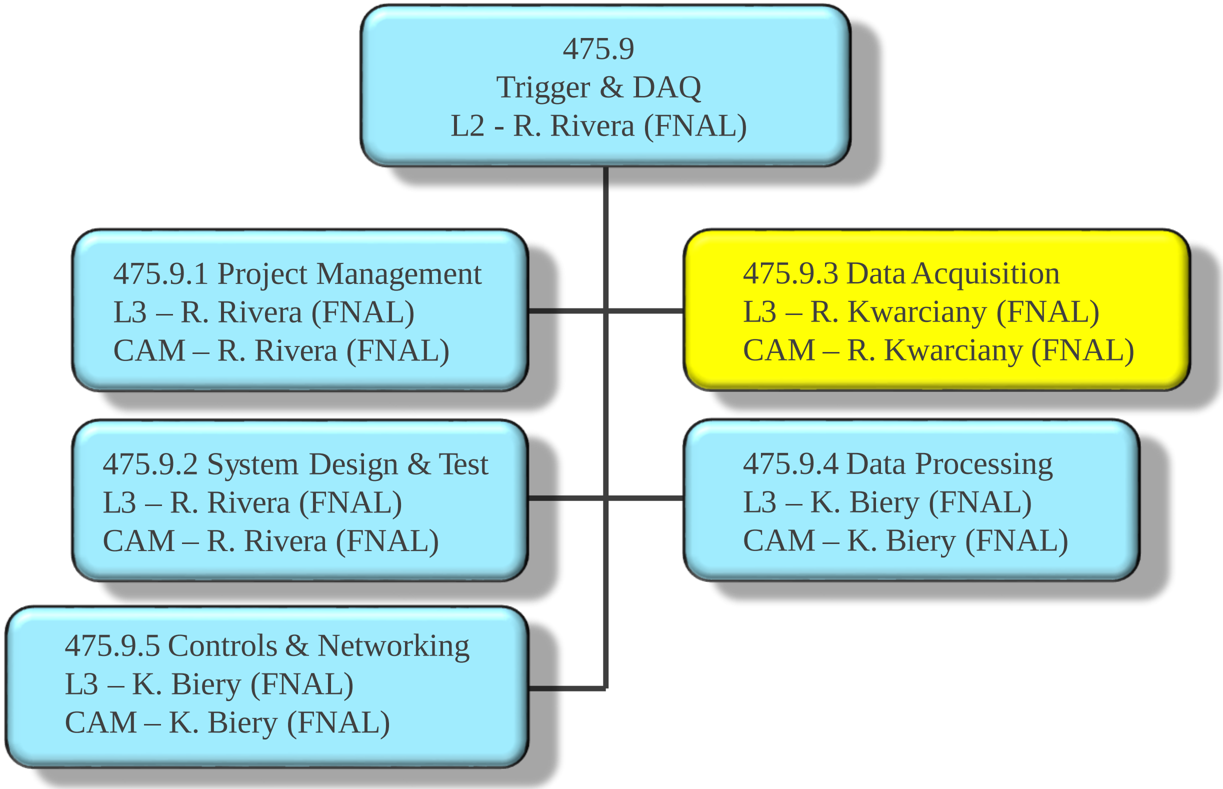
Rick Kwarciany
Mu2e Data Acquisition L3 Manager
4/20/16

Data Acquisition Team

Developed Data Acquisition systems for NOvA, CDF, BTeV, KTeV, others.

- Rick Kwarciany (FNAL):
  - Data Acquisition L3 Manager
- Mark Bowden (FNAL)
- John Chramowicz (FNAL)
- Greg Deuerling (FNAL)
- Eric Flumerfelt (FNAL)
- Ron Rechenmacher (FNAL)
- Tomo Miyashita (Caltech)

Mu2e TDAQ Organization



Scope

WBS 475.9.3
Data Acquisition
Rick Kwarciany / Fermilab

475.9.3.3 **Production System**
Procure, test, and install production DAQ hardware (DTCs, optical links, switch for event building network, timing system distribution). Complete development and test of artdaq software. Verify system performance. Optimize and debug software and firmware based on feedback from experiment.

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Requirements

- The TDAQ Requirements are described in docdb-1150
- The DAQ subsystem must meet the following requirements:
  - Provision for simultaneous operation of multiple readout partitions.
  - Generation and distribution of precision timing to all detector subsystems.
  - Provision for correlating accelerator timeline events with Mu2e events.

Requirements

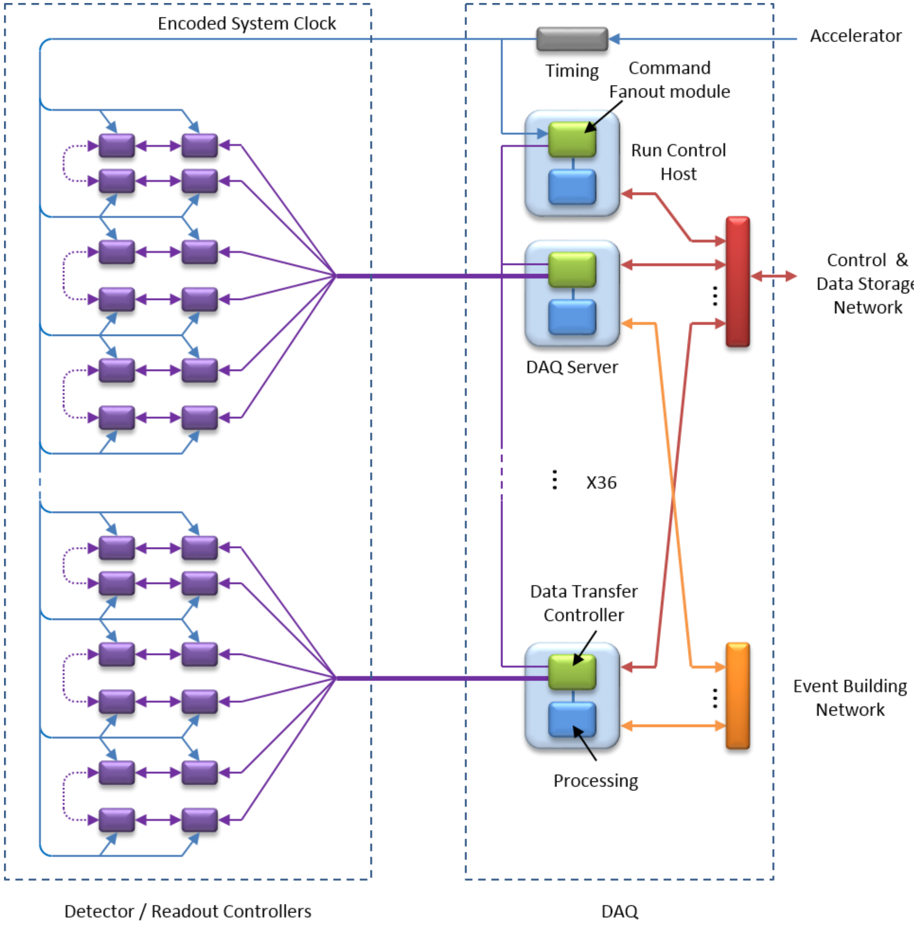
- Provision for consistent geographical and timestamp identification of all generated datasets at all levels of the readout to assure providence of data.
- The TDAQ should provide an average data bandwidth that is twice the expected overall data rate, which is the sum of the sub-detector data rates listed in this document.
- The TDAQ should provide a means of controlling front-end operating modes (data readout, calibration injection, etc.) for each revolution period of the delivery ring, regardless of beam status.

Requirements

- The TDAQ design should provide dataflow control mechanisms that prevent buffer overflow in any normal or calibration operating mode.
- The TDAQ design should support a mean time to repair (MTTR) of 1 hour or less, with a goal of > 95% uptime when beam is available.
- The TDAQ should be able to transition from a warm state to a running state within 5 minutes.
- The TDAQ should be readily configurable to support the acquisition of data from separate detector subsystems during both the commissioning and operating phases of the experiment.

Design

- TDAQ includes everything in the data stream downstream of the ROCs, outside of the cryostat.
  - Fibers from/to detector hall
  - Data Transfer Controllers (DTCs)
  - DAQ Servers
  - Event Building Network
  - System Clock distribution
  - Command Fanout module (CFO)



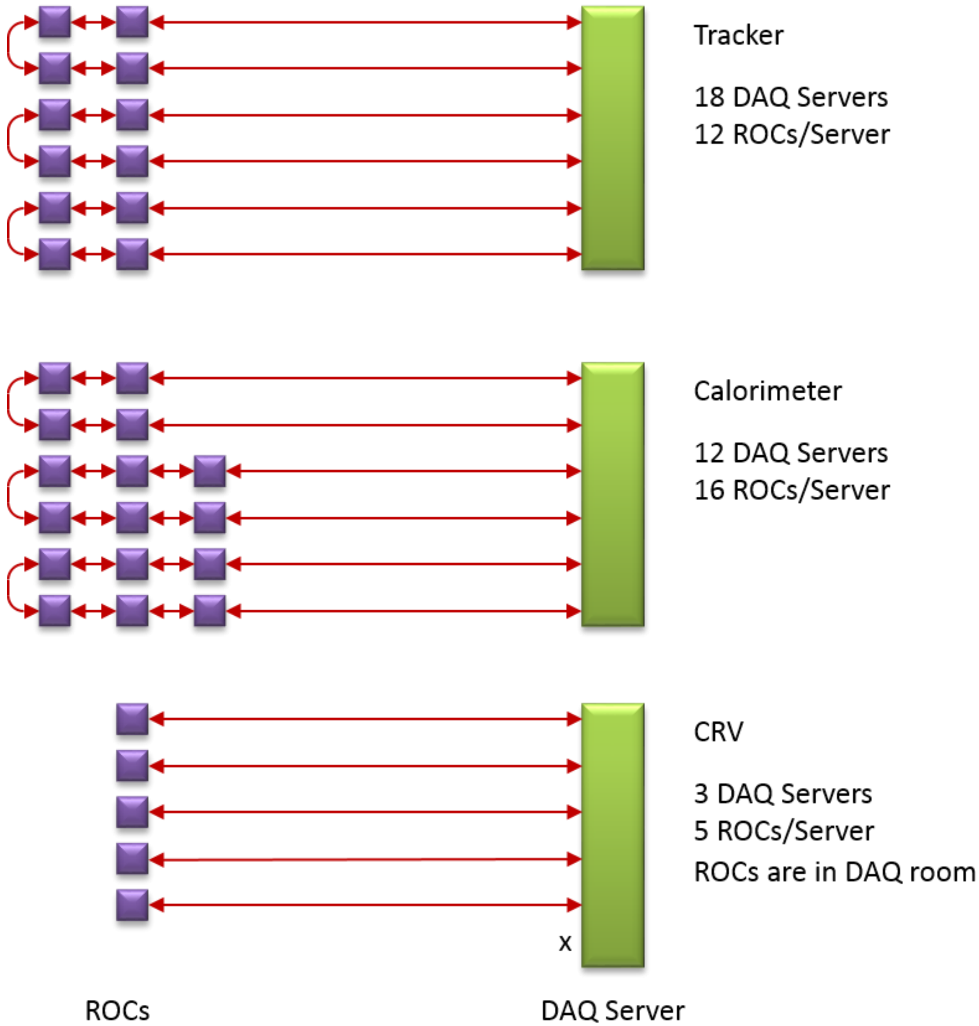
Design

- TDAQ is a data pull system. Data flow is initiated by the Run Control Host, via the Control Fanout module (CFO).
- Immediate and delayed triggering supported on each partition.
- The CFO is connected to the DTCs via optical link running at 3.125 Gbps (2.5 Gbps unencoded).
- All data in the mu2e DAQ system is packetized.
- The sub-detectors are responsible for ROCs and signal fanout inside the vacuum.
- Uses commercial hardware components as much as possible.

Design

- Mostly commercial hardware
  - A custom FMC card will be developed for the CFO.
  - Commercial FPGA card with PCIe and FMC interfaces will be used for the DTC and the CFO.
  - Commodity rack mounted computers (DAQ Servers).
  - Commodity Ethernet switch modules.

Design – Connection to ROCs



Tracker = 216 ROCs
Calorimeter = 192 ROCs
CRV = 14 ROCs
STM = 1 ROC
ExtMon = 1 ROC

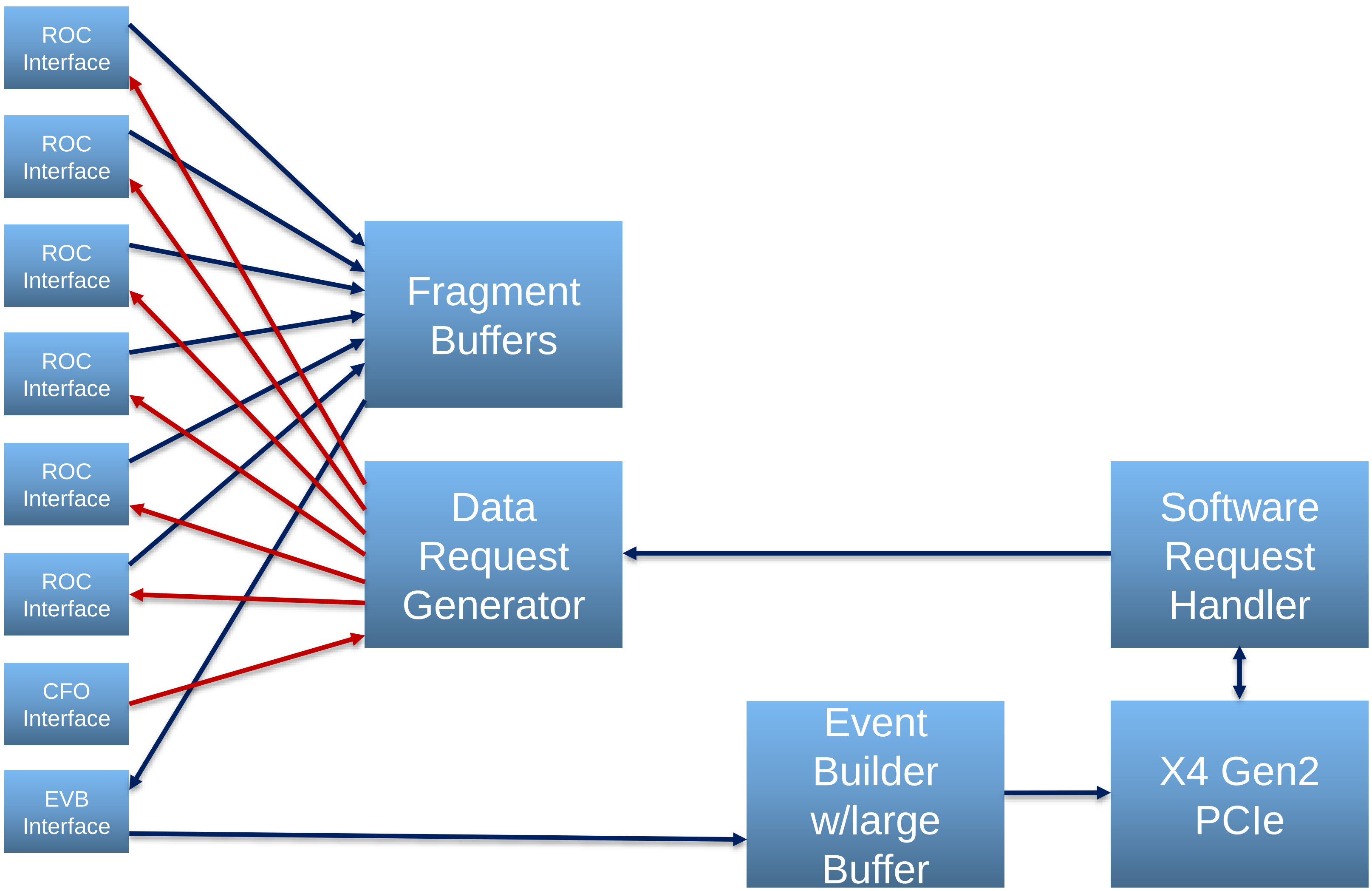
Design – Control Fanout Module (CFO)

- Commercial FPGA board with PCIe and custom FMC card.
- Installed in Run Control Host.
- Receives uBunch marker from Accelerator via custom FMC card, then generates encoded System Clock.
- CFO follows experiment provided Run Plan to generate a Heartbeat Packet in advance of each Event Window
- Run Plan is text file that is translated into RAM-based commands in CFO

Design – Data Transfer Controller (DTC)

- Same FPGA board as CFO.
- Commercial FMC card.
- One installed in each DAQ Server.
- Six transceivers used for connection to ROCS.
- One transceiver used for connection to CFO.
- One used for connection to Event Building Network.
- Supports simple firmware-based “level 0” filtering capacity to reject background events.

Design – Data Transfer Controller (DTC)



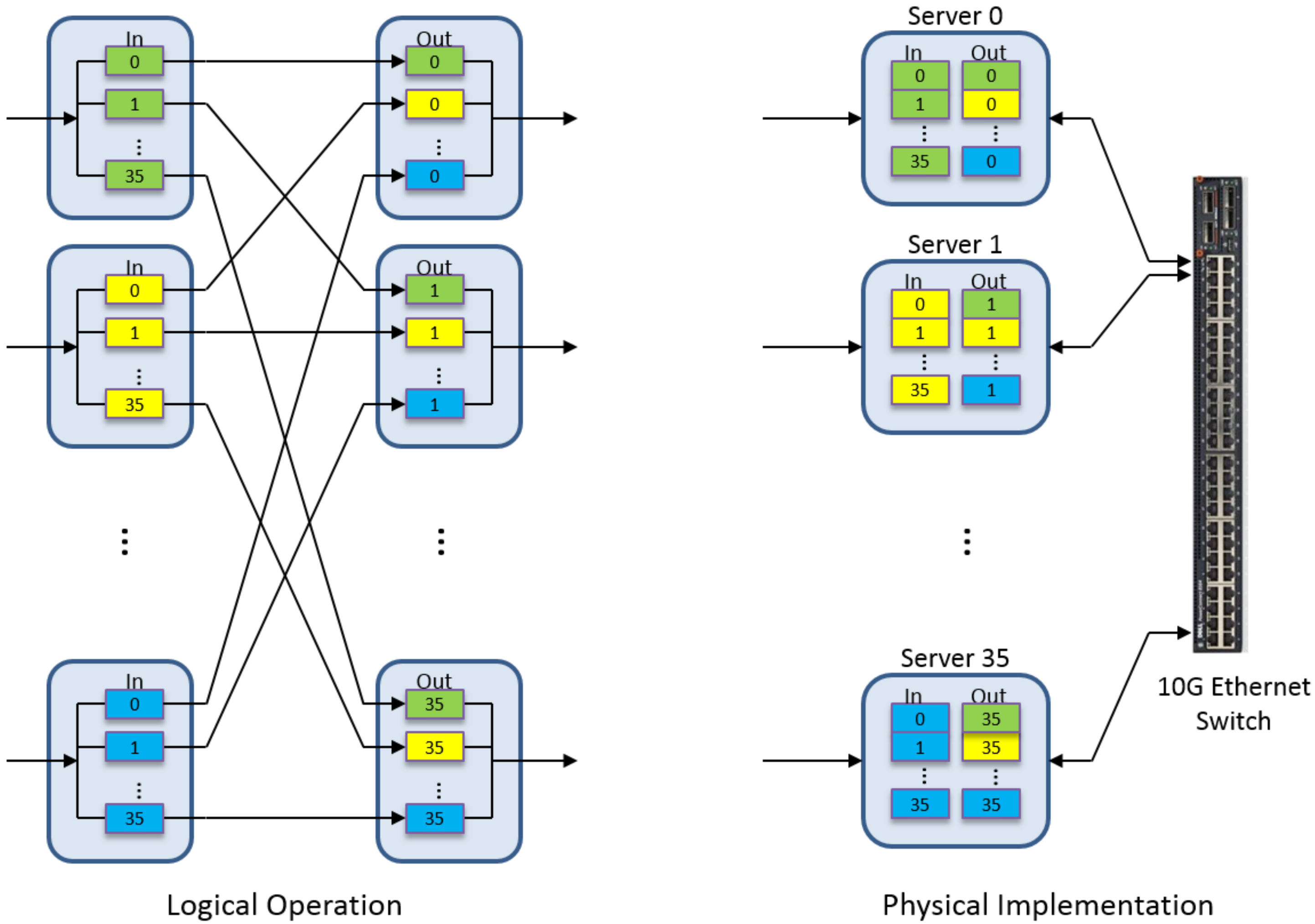
Design – Event Building

- Heartbeat packet informs ROCs how to uniquely identify their data for the next Event Window, including 48-bit event ID used for event building.
- For each Event Window, ROCs collect data from a small section of the detector.
- DTCs collect data from ROCs in a pull architecture.
- Experimenters want data packaged by Event Window, not by detector section.

Design – Event Building Network

- 48-port commercially available 10 Gbps Ethernet switch module.
- Detector data fragments for a given event arrive at DTCs at roughly the same time.
- For simplicity, DTC firmware transfers raw Ethernet frames over event building network, using time division multiplexing by destination.

Design – Event Building Network



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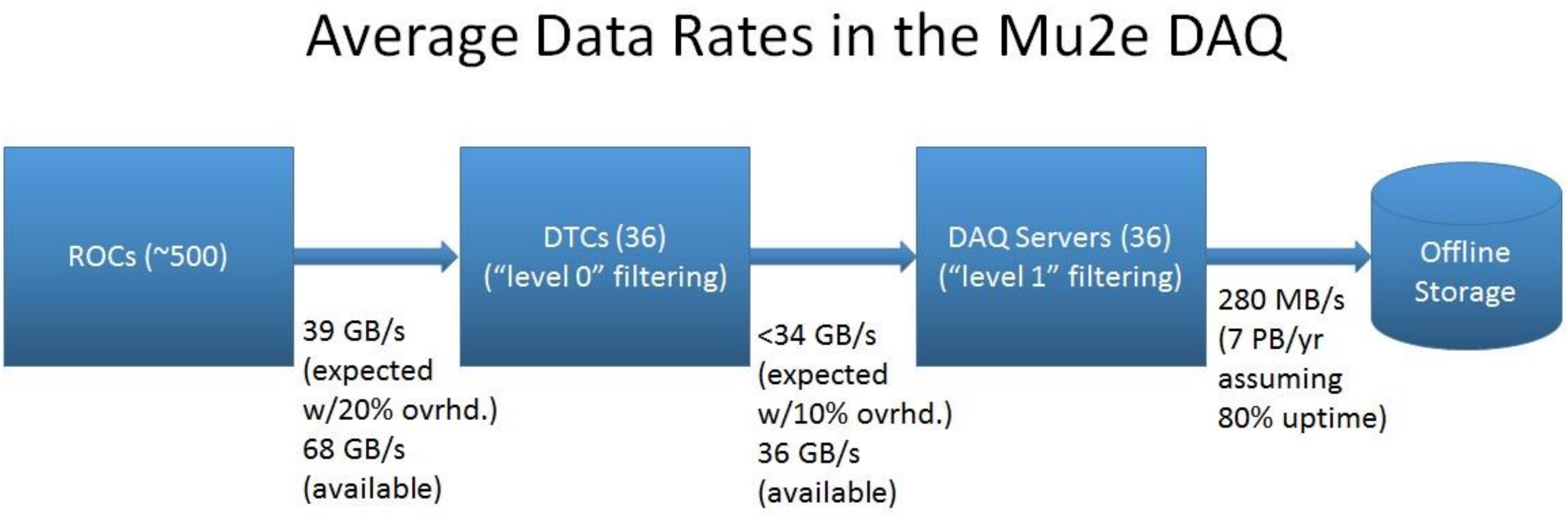
Performance



Design Maturity

- A DAQ Design Review was held on Jan 26, 2016
  – Committee included engineers and physicists/DAQ SW experts
- Committee answered yes to all charge questions
- Design is 90% complete.
- Primary risk to DAQ is an underestimation of detector rates
  – DAQ has been designed to be flexible, scalable and with significant headroom to mitigate this risk.
- Final report is in mu2e-docdb 6377
  – This includes the recommendations from the committee and our responses

Review Recommendation Highlights

- 2. The committee requests that the recovery algorithm employed by the TDAQ system for single and multibit errors in the timing messages be explicitly listed in the documentation.
  - The use of 8b-10b and CRC bytes is detailed in Mu2e-docdb #4097.
- 4. The committee is of the opinion that the TDAQ specifications should at minimum enumerate in their documentation all DAQ data that will be distributed outside of Mu2e TDAQ to ensure that such interfaces are fully covered.
  - The only path for DAQ data to outside of TDAQ is by transferring data off the online cluster, and that is covered by the data logging information in Mu2e-docdb #1520.

Design Maturity and Path to Completion

- Nearly all hardware is commercial “off-the-shelf”.
- Design is 90% complete.
- Packet protocol is well documented.
- Remaining work is mostly finishing the firmware and software.
- Advantage that FPGAs are reprogrammable.

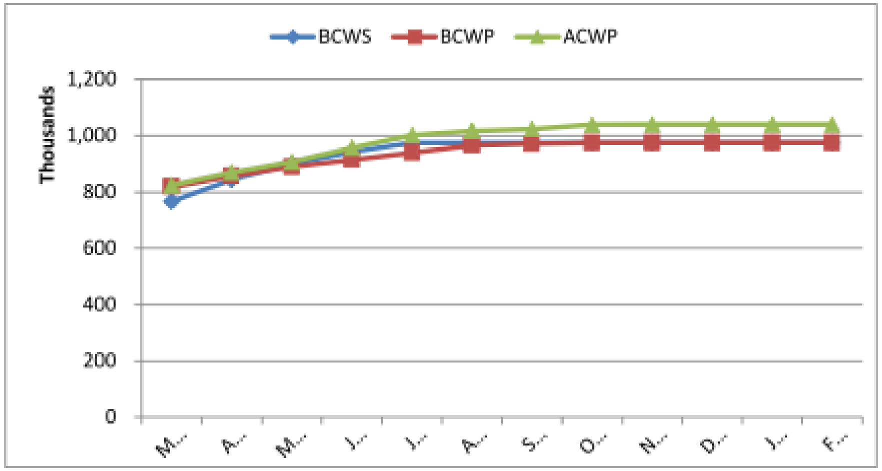
Quality

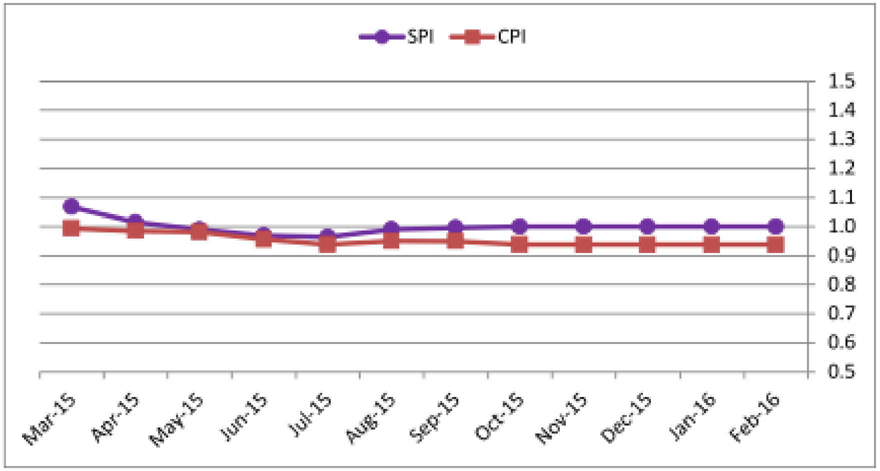
- DAQ included in Mu2e Quality Planning Document (DocDB 6005)

Deliverable	QA or QC Step?	QA or QC Process Documentation (DocDB #)	Inspection or Acceptance Criteria/Plan	Verification
DAQ DTC and CFO Hardware	Acceptance tests, burn-in tests	Meet or exceed manufacturer's specifications	Incoming inspection, basic power-up functional test	72 hour continuous burn-in test (self-test firmware)
DAQ Optical Links Hardware	Acceptance tests, burn-in tests	Meet or exceed manufacturer's specifications	Incoming inspection, basic power-up functional test	72 hour continuous burn-in test (loopback bit-error rate, power level monitoring firmware)
DAQ Timing System Hardware	Acceptance tests, burn-in tests	Meet or exceed manufacturer's specifications	Incoming inspection, basic power-up functional test	Test timing system synchronization and alignment (Oscilloscope, Jitter Analyzer)
DAQ Event Building Hardware	Acceptance tests, burn-in tests	Meet or exceed manufacturer's specifications	Incoming inspection, basic power-up functional test	72 hour continuous burn-in test (full rate in six groups of six ports, 12 hours per group, using iperf)
DAQ Software	Test with pattern and simulated data	Final Design Report Chapter DocDB #6377	NA	Incremental release testing

Cost and Schedule Performance

475.09.03 Data Acquisition





- No significant variances.

Cost and Schedule Performance

Report: **Mu2e_Earned Value** - Project Stoplight metrics - Control Account

Project: **Mu2e** - Mu2e Project
Status Date: 02/29/2016

Mu2e Project
February 29, 2016
Currency in: $K

Control Account, Work Package.CTC	Current Period							Cumulative to Date						
	Budget	Earned	Actuals	SV ($)	SV (%)	CV ($)	CV (%)	Budget	Earned	Actuals	SV ($)	SV (%)	CV ($)	CV (%)
475.09.03 Data Acquisition	0	0	0	0	0%	0	0%	975	975	1,040	0	0%	-65	-7%
475.492 475.09.03.01 Data Acquisition Prototype (PED)	0	0	0	0	0%	0	0%	462	462	462	0	0%	-0	0%
475.493 475.09.03.02 Data Acquisition Pilot System (Line Item: PED)	0	0	0	0	0%	0	0%	513	513	578	0	0%	-65	-13%
475.494 475.09.03.03 Data Acquisition Production System (Line Item: Co	0	0	0	0	0%	0	0%	0	0	0	0	0%	0	0%

Control Account, Work Package.CTC	BAC	EAC	VAC	% Spent	% Complete
475.09.03 Data Acquisition	2,023	2,089	-67	50%	48%
475.492 475.09.03.01 Data Acquisition Prototype (PED)	462	462	-0	100%	100%
475.493 475.09.03.02 Data Acquisition Pilot System (Line Item: PED)	513	578	-65	100%	100%
475.494 475.09.03.03 Data Acquisition Production System (Line Item: Co	1,048	1,049	-1	0%	0%

- No significant variances.

Change Control

							Values		
Control Account	CR #	CR Description	Prior Start	Revised Start	Prior Finish	Revised Finish	BAC Before	BAC After	Cost Increase / (Decrease)
475.09.03	**2**	Establish internal baseline and incorporate recommendations from Director's Review.	-	-			1,840,980.05	1,831,537.75	(9,442.30)
	6	Corrections made to CR002	-	-			1,831,537.76	1,831,537.50	(0.25)
	3	New rate adjustments for labor fringe and overhead.	-	-			1,831,537.50	1,824,844.83	(6,692.67)
	4	Cost leveling; new CD-3c strategy	-	-			1,824,844.83	1,830,656.09	5,811.25
	8	FY15 Rate changes	-	-			1,830,656.09	1,891,900.21	61,244.12
	12	Solenoids PS and DS Contract terms and Accelerator design reviews	**1/30/2013**	1/30/2013	**1/21/2020**	4/28/2020	1,891,900.21	1,903,313.21	11,413.01
	15	Establish CD-2 Baseline	**1/30/2013**	1/30/2013	**4/28/2020**	6/29/2020	1,903,313.21	1,937,377.00	34,063.78
	17	PS/DS Vendor Pay Milestones; Remote Handling Design	**1/30/2013**	1/30/2013	**6/29/2020**	6/29/2020	1,937,377.00	1,938,627.52	1,250.53
	18	Detector Bldg Constr Change Order; Argonne Support	**1/30/2013**	1/30/2013	**6/29/2020**	6/9/2020	1,938,627.52	1,937,906.85	(720.67)
	19	Reduced Constr oversight, FFP ECPs, and TS Module fab delay	**1/30/2013**	1/30/2013	**6/9/2020**	6/9/2020	1,937,906.85	1,937,906.85	0.00
	21	Test Cryostat mods; Upstream pbar window transfer; CRV staff change	**1/30/2013**	1/30/2013	**6/9/2020**	6/24/2020	1,937,906.85	1,938,475.14	568.29
	22	Detector Bldg. changes; Award TS Module fab; Test Cryostat mods and move	**1/30/2013**	1/30/2013	**6/24/2020**	6/30/2020	1,938,475.14	1,939,606.68	1,131.54
	24	FY16 Rate Update	**1/30/2013**	1/30/2013	**6/30/2020**	6/30/2020	1,939,606.68	1,939,826.39	219.71
	27	Constr. Changes, CD3 Review Prep	**1/30/2013**	1/30/2013	**6/30/2020**	6/30/2020	1,939,826.39	1,947,614.82	7,788.43
	28	Increase Project Office Support, Constr Rev 13, Racks & Rack Monitor	**1/30/2013**	1/30/2013	**7/9/2020**	7/9/2020	1,947,614.82	2,022,618.48	75,003.66
475.09.03 Total									**448,349.99**

- BCR 27 added timing distribution prototyping
- BCR 28 changed from 7 racks to 22 racks
- The other changes listed above have been a consequence of changes in schedules and labor rates outside of TDAQ.

TDAQ Interfaces

- Internal and external interfaces identified and described in DAQ Interface document (docdb #1520).
- Internal interfaces between servers, timing system and general-purpose networking.
- External interfaces such as power and cooling needs and the network connection to offline storage.
- Participation in Electronics and Detector integration meetings.

Interfaces are understood and under control

Integration

- Participate at the weekly Electronics Integration meeting.
- Internal bi-weekly TDAQ meeting often includes invitees from other subsystems.

Environment, Safety, & Health

- ESH is integrated into all phases of the Project
  - Design, Construction, Installation
- ESH requirements are clearly defined within the Project
  - FESHM, FRCM
- L2 hazards & mitigations are captured in the Project HAR
  - High voltage (208 VAC, no exposed connections)
  - Electronic racks
  - Class 1 lasers (eye safe)
- Design & installation review process includes an ESH component
- Utilize Fermilab's work planning requirements & processes
  - Hazard analysis

Summary

- The TDAQ Data Acquisition design is 90% complete. The risks associated with the remaining design are understood and will be tested in the Pilot system.
  - Simulated ROCs will be used along side of prototype ROCs in the Pilot system to refine and validate firmware and software.
  - Interfaces, risks, ES&H issues identified and under control.
  - QA/QC plans in place.
- Current design **meets** TDAQ requirements.
- TDAQ Data Processing is ready for CD-3 approval.