Fermilab

Mu2e CD3c Review
WBS 7.7 FEE & Power

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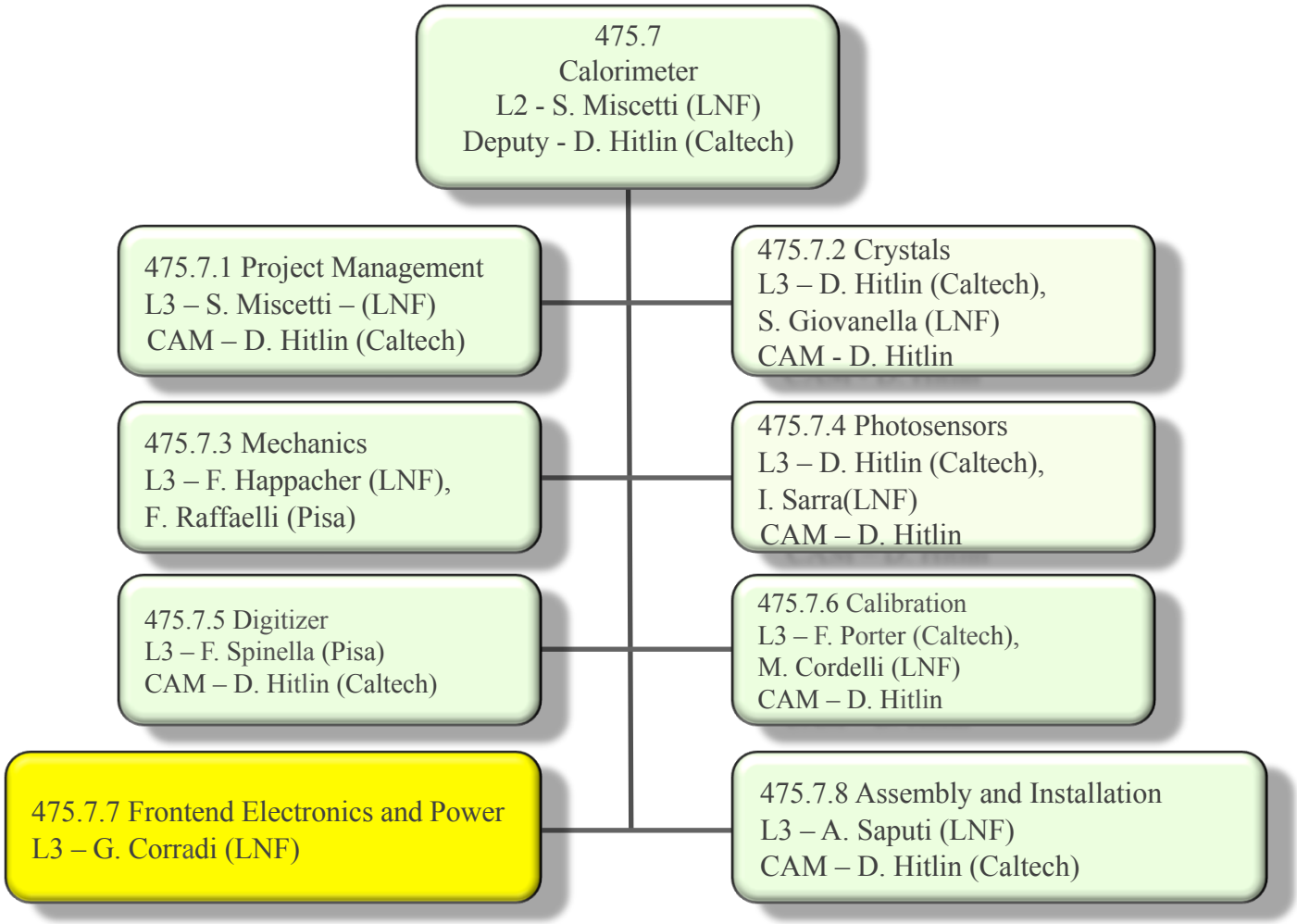
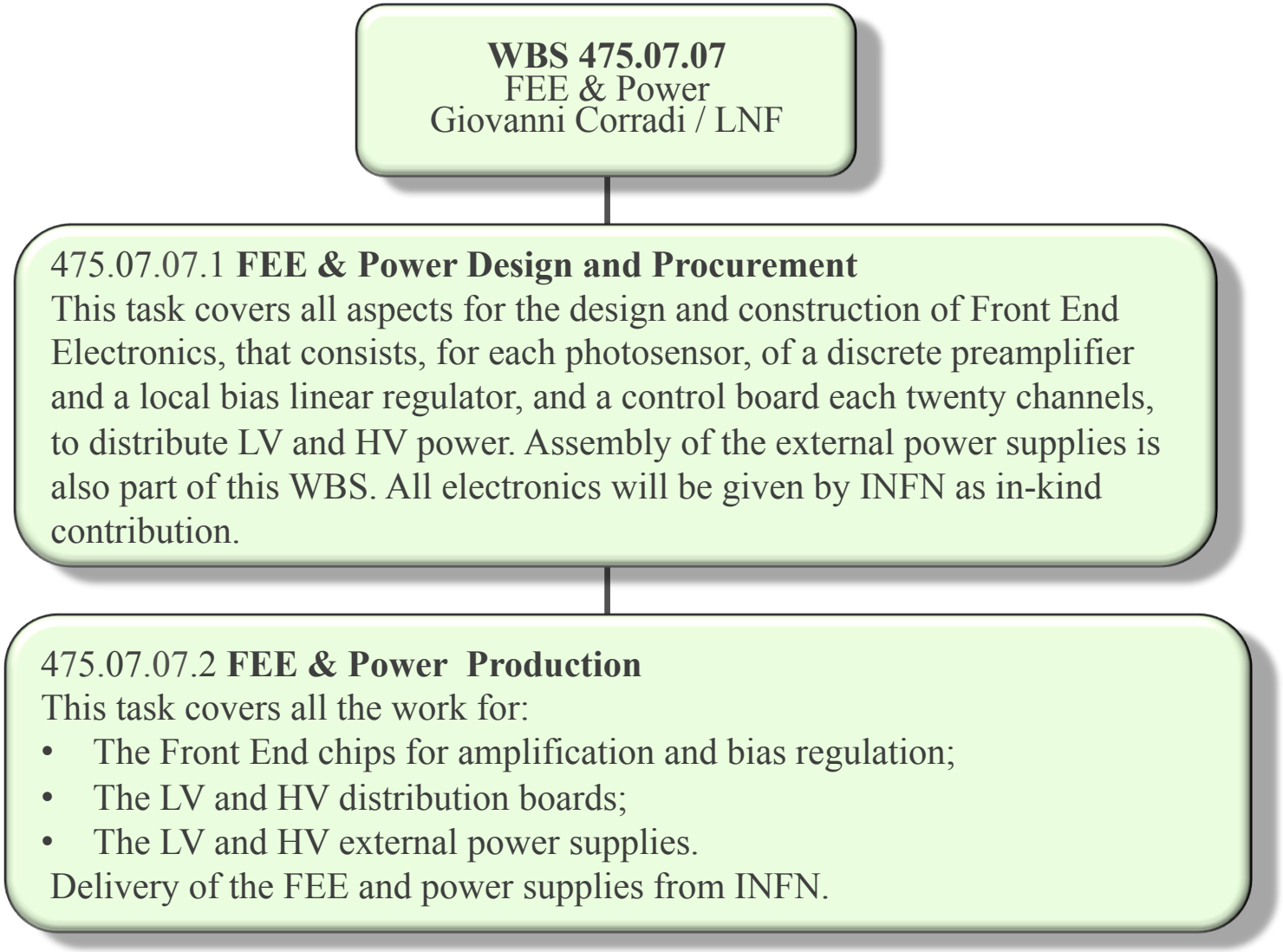
G. Corradi, Mu2e Calorimeter Frontend Electronics and Power L3 Manager

18 April 2016

Mu2e Calorimeter Organization



Scope

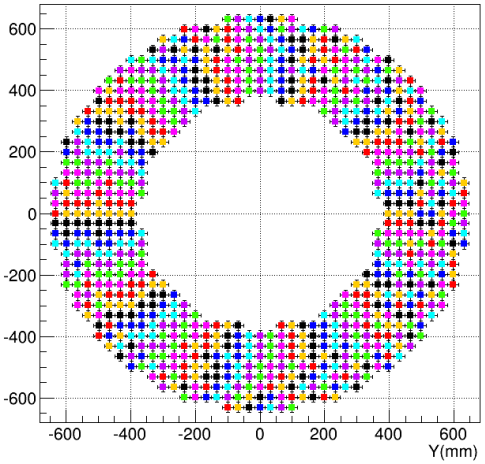

WBS 475.07.07
FEE & Power
Giovanni Corradi / LNF
475.07.07.1 FEE & Power Design and Procurement
This task covers all aspects for the design and construction of Front End Electronics, that consists, for each photosensor, of a discrete preamplifier and a local bias linear regulator, and a control board each twenty channels, to distribute LV and HV power. Assembly of the external power supplies is also part of this WBS. All electronics will be given by INFN as in-kind contribution.
475.07.07.2 FEE & Power Production
This task covers all the work for:
• The Front End chips for amplification and bias regulation;
• The LV and HV distribution boards;
• The LV and HV external power supplies.
Delivery of the FEE and power supplies from INFN.

Calorimeter Electronics Scheme

- Overview of the calorimeter readout electronics: each disk (~ 680 crystals per disk) is subdivided into 34 groups of 20 crystals.

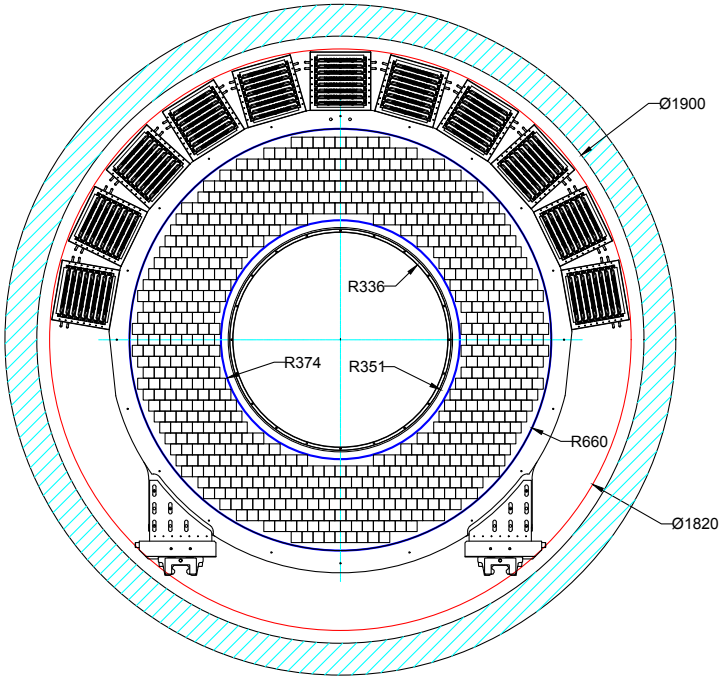
– Groups of 20 left (right) Amp-HV chips, controlled by a dedicated mezzanine board that distributes the LV and the HV reference value, while setting and reading back the locally regulated voltage

– Groups of 20 amplified signals are sent to a digitizer module where they are sampled and processed before being optically transferred to the DAQ system.

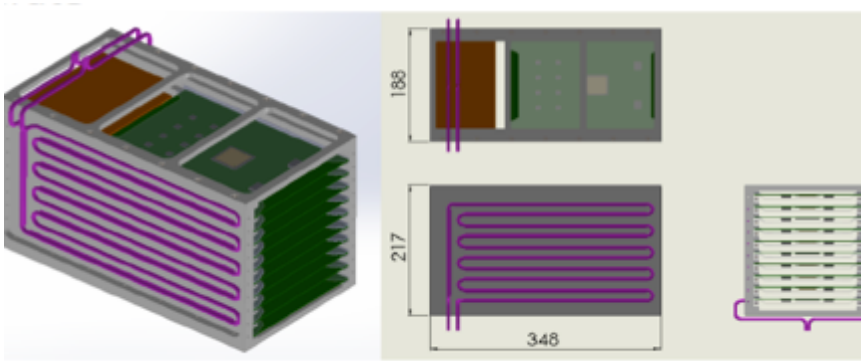


Calorimeter FEE Layout

- There are therefore 11 crates per disk, hosting 6/7 sets of AMP-HV and WFD boards;
- The crates are placed in the outermost region of each disk;
- The crates are designed to provide heat dissipation for the electronics boards (see presentation on cooling).

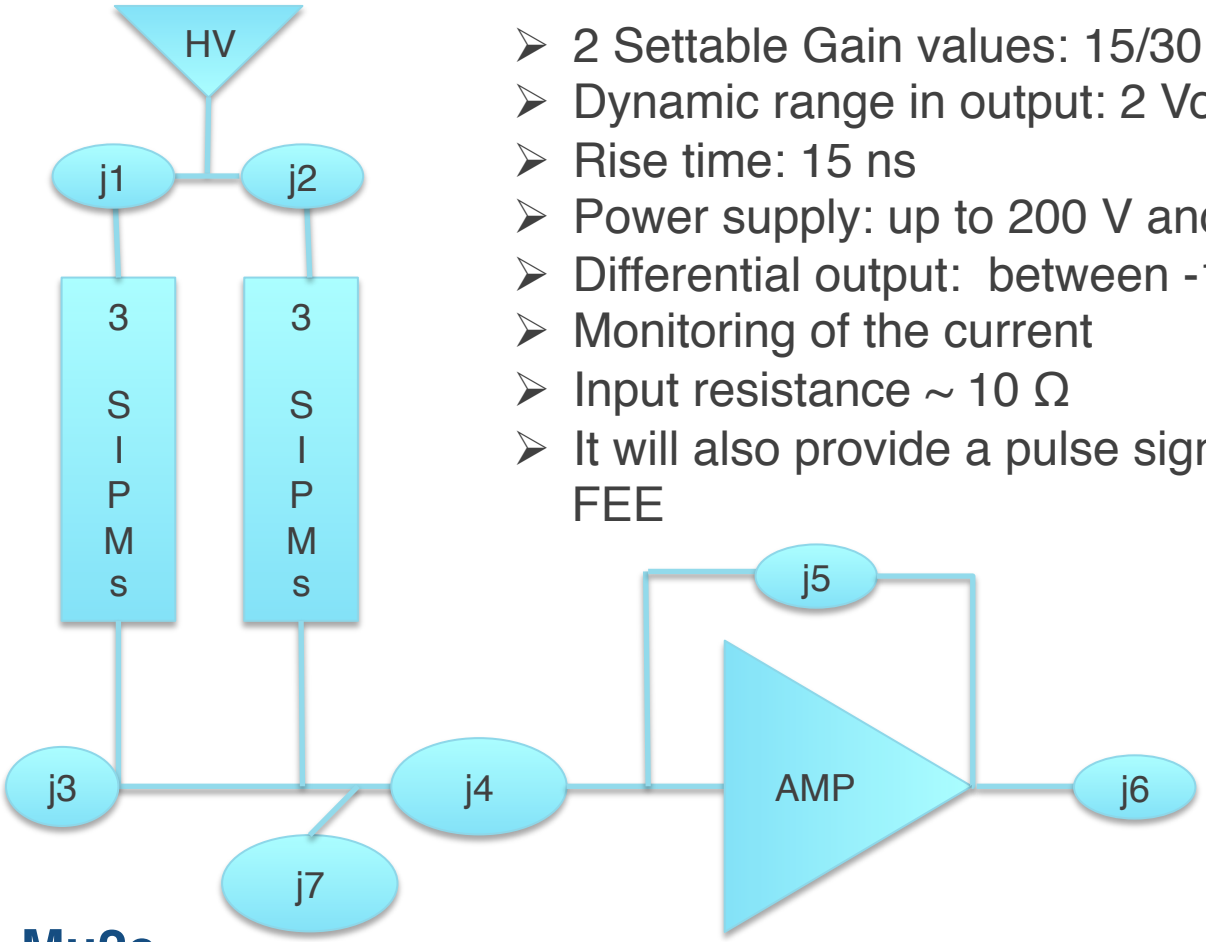


Crystal 34.3 mm x 34.3 mm (including wrapping 0,15 mm)
(34 mm + 0.15 mm + 0.15 mm) x (34 mm + 0,15 mm + 0.15 mm)
674 crystals



Requirements I – Calorimeter FEE

- Provide both the amplification stage and a local linear regulation for the Silicon photosensor bias voltage

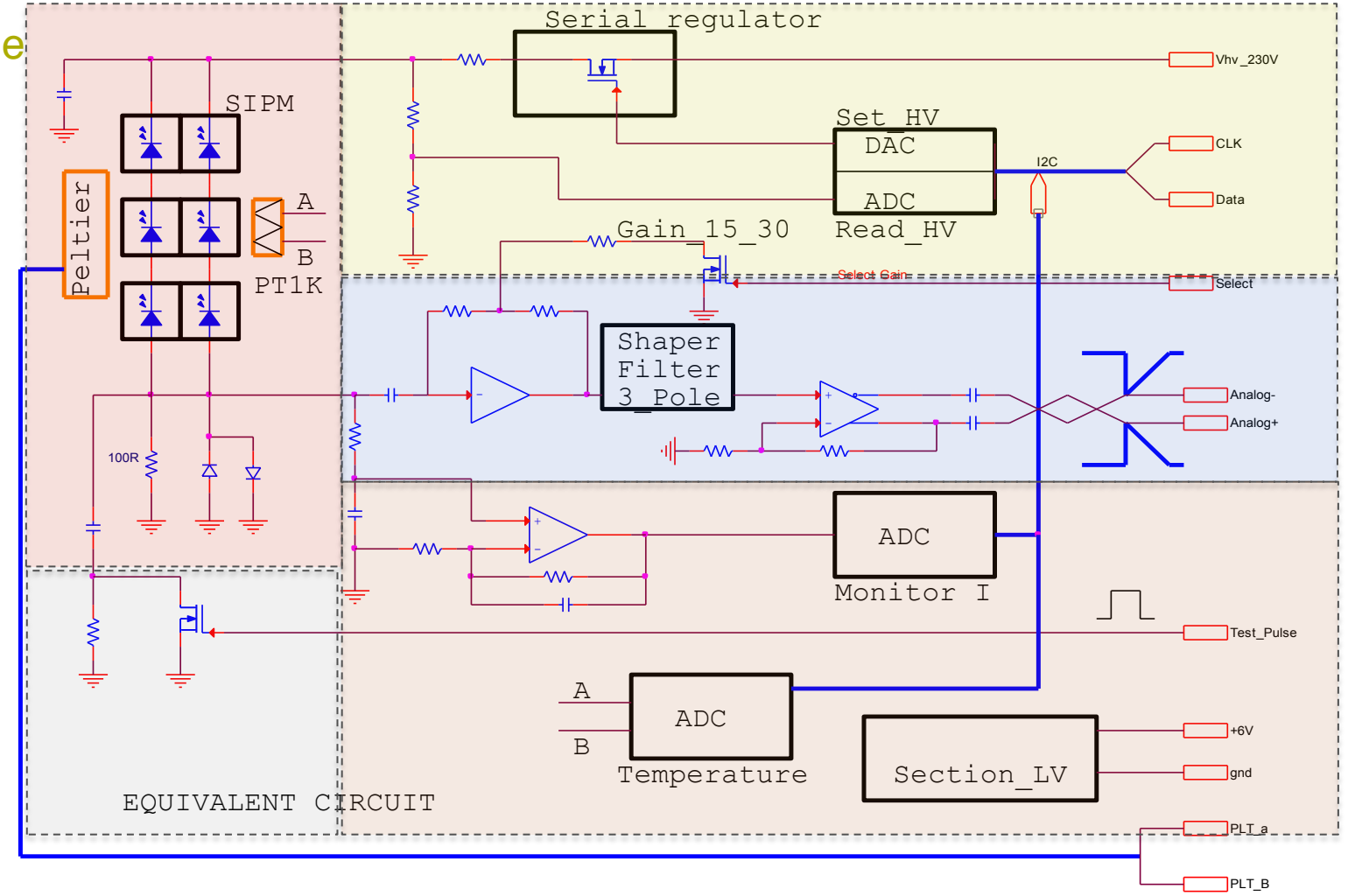


- 2 Settable Gain values: 15/30
- Dynamic range in output: 2 Volt
- Rise time: 15 ns
- Power supply: up to 200 V and 3 mA
- Differential output: between -1 and +1 Volt
- Monitoring of the current
- Input resistance ~ 10 Ω
- It will also provide a pulse signal to test the FEE

j1 and j2: Possibility to disconnect each series
j3: Monitoring of the temperature
j4: Monitoring of the current
j5: Settable Gains
j6: Differential output
j7: Pulse Signal

Architecture of Front-end

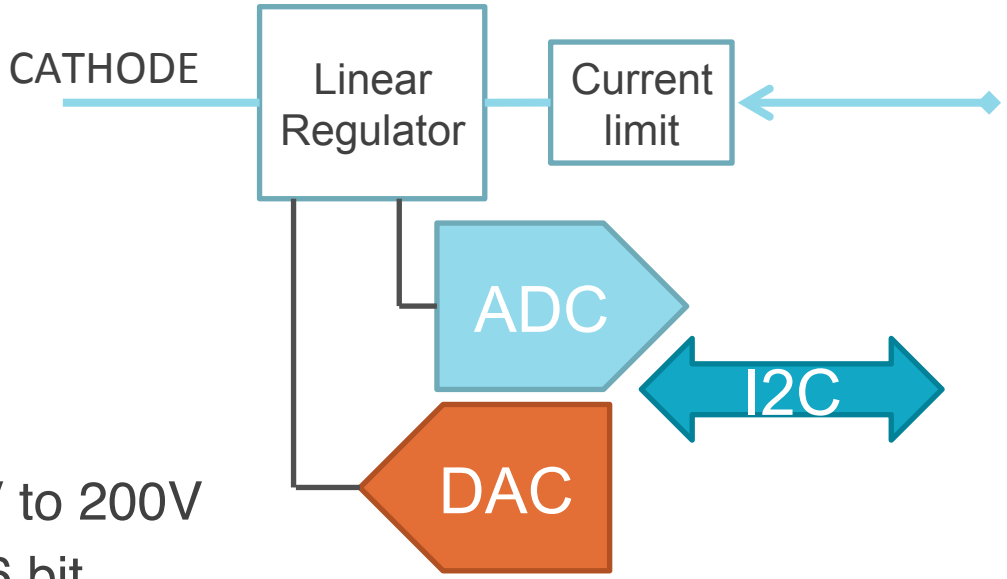
- ✓ Series voltage regulator
- ✓ SiPMs polarization
- ✓ Amplifier
- ✓ Pulse signal
- ✓ Temperature and current monitoring



Transimpedance Preamplifier

- Trans-impedance 750Ω to 1.5KΩ
- Dynamic differential 2V
- Bandwidth 35 Mhz
- Rise time 15ns
- Polarity Differential
- Output impedance 100 Ω
- Coupling output end source AC
- Filter Shaper 3-pole
- Noise, with source capacity 1pf must be evaluated
- Power dissipation 20mW
- Power supply 6V
- Input Protector over-Voltage 10mJ

Linear Regulator shunt architecture.



- Adjustment range Vout 20V to 200V
- Accuracy, reading and writing, 16 bit
- Current limiter can be adjusted max. 3mA
- Noise tot. 2mVpp
- Long-term stability 100ppm
- Settling Time "local feedback" < 500 us ρ< 1
- Double filter high Voltage, attenuation 56db
- Temperature measurement -20 to 40°C

AMP-HV Prototyping

Since 2014 2 different production of preamplifiers have been carried out, together with their control boards in ARM technology, following the long story of our technology choice :

→ Amp-HV for LYSO (Gain 300, Vbias ~ 500 V)

→ Amp-HV for SL APD (Gain 300, Vbias ~ 2 kV)

A lot of experience gained with these prototyping phase

✓ Prototypes have been designed and produced also for the MPPC option for the used SPL/MicroFilm arrays of 16 3x3 mm^2 SIPMs.

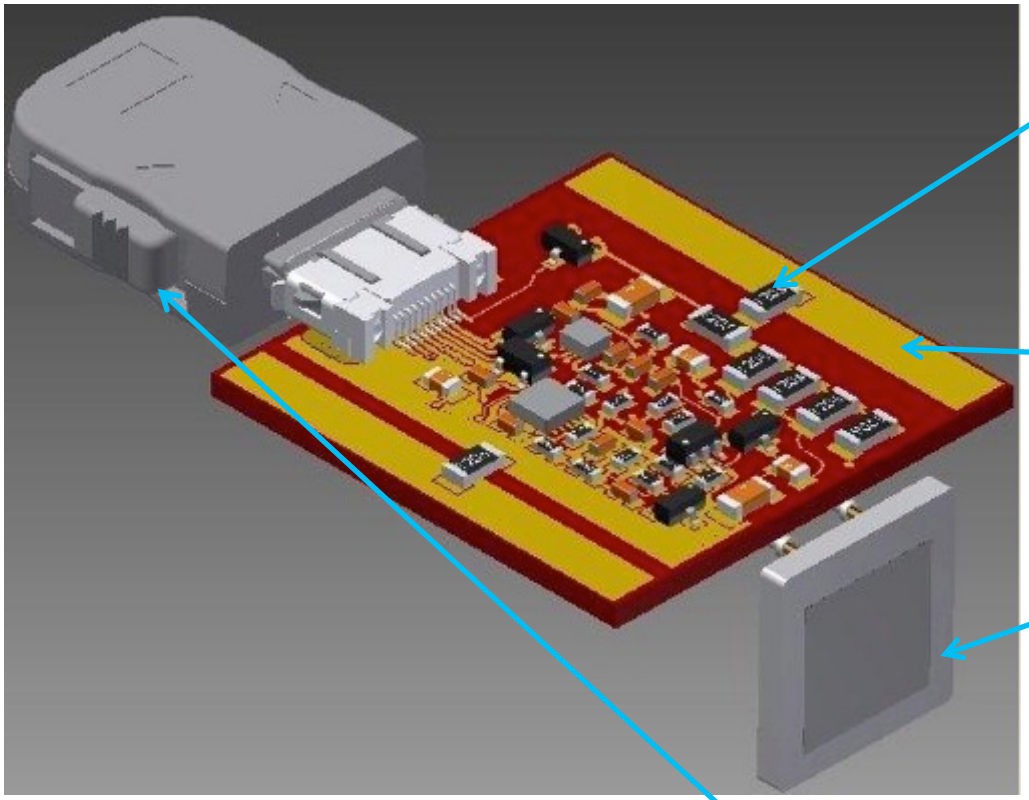
✓ Test beam carried out successfully in April 2015

→ Amp-HV and analog adder for 16 channels MPPC at 60 V bias used.

➢ The design of the new electronics for the final selected SIPM packaging is starting from this last experience.

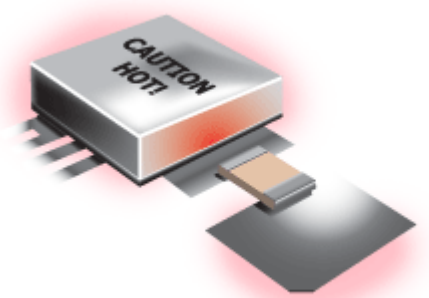
Therma-bridge Resistor

Power to dissipate 150mW



Cooling problem for Amp-HV

- We solve the problem of cooling in Vacuum by transferring the heat from the Amp-HV to the mechanical support, through a therma-Bridge
- An example is shown in the side view.
- The heat transfer must take place in isolation from common ground.

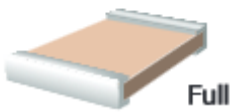


Therma-Bridge™ Electrically Isolated AlN Thermal Management Device

The ims Aluminum Nitride (AlN) **Therma-Bridge™** is a simple, cost effective device which aids in thermal management. Bridges are available in standard sizes and thicknesses. Custom sizes are also available on request. The **Therma-Bridge™** is designed to transport heat from one location to another. Simply attach one terminal to the heat source, and the other terminal to a thermal plane or heat sink. Popular application configurations are shown on the reverse side. The **Therma-Bridge™** has the following features:

- Electrically Isolated AlN substrate material
- Multiple sizes and thicknesses
- RoHS PtAg or Solder coated PtAg terminals for easy attachment

Terminal style:



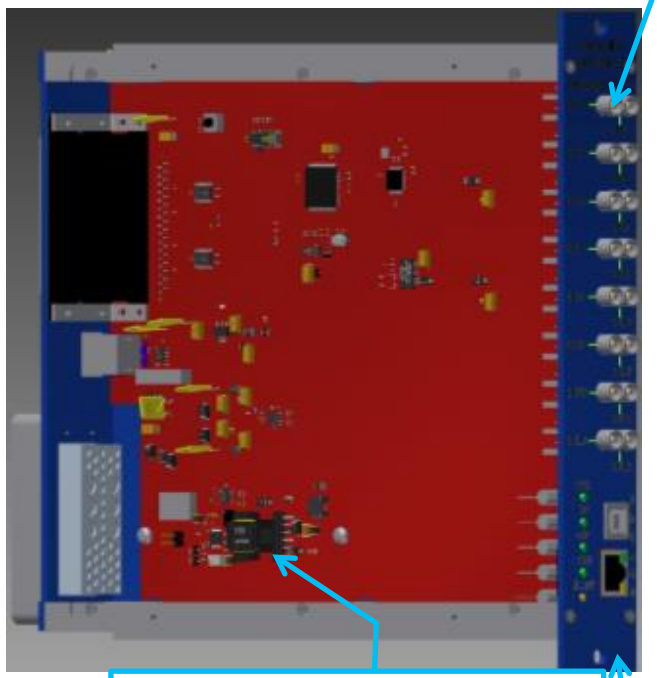
Full wraparound

Terminal materials:

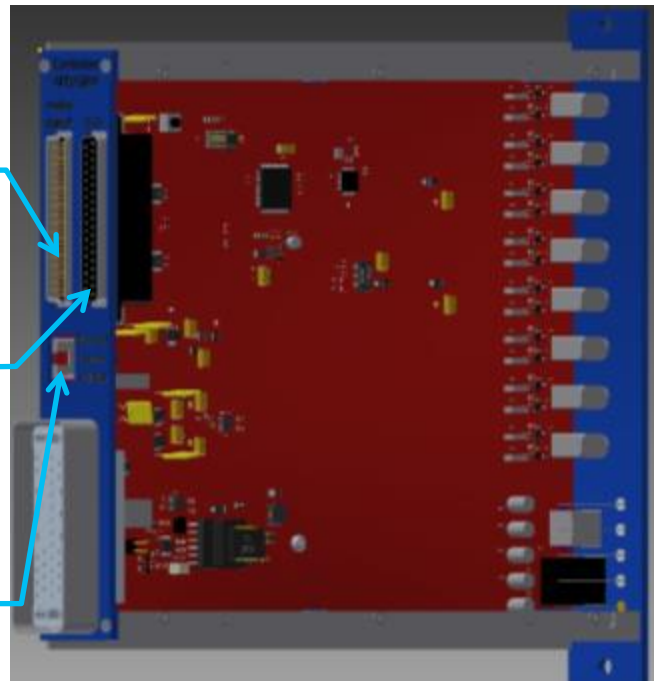
-3 ✓	PtAg (platinum silver) for epoxy or solder attachment
-C	Solder coated PtAg for solder attachment

Controller- ARM used for Test Beam

Front Panel NIM-1U



Rear Panel NIM-1U



16 Analog Signal Output

16 Analog Signal Input

16 line I2C. Slow Control

1-Ware protocol for external sensor:
- Temperature.
- Humidity.

USB & Ethernet Connection

Primary Generator High Voltage.
Frequency: 250kHz.
Stability: 0,5%
Selectable Voltage range:
- 50V - 100V - 550V

ON BOARD:

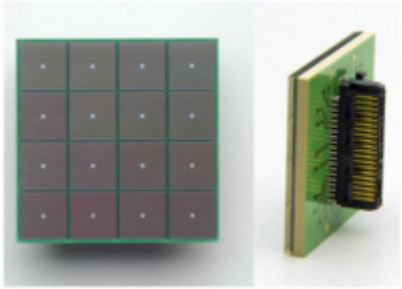
- CPU (LPC1768FBD100)
- HV and LV for 16 Channels of Front-end.

MPPC amplifier

- The Amp-HV is a multi-layer double-sided discrete component board that carries out the two tasks of amplifying the signal and providing a locally regulated bias voltage, thus significantly reducing the noise loop-area.

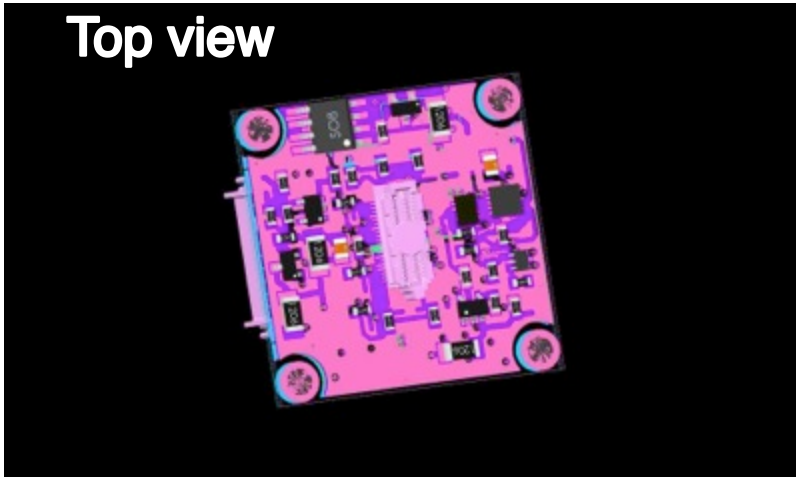
Adder Amplifier

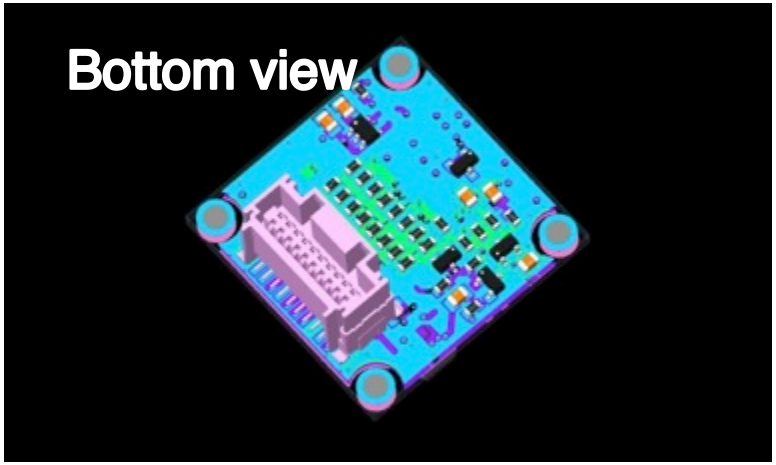
- Gain 4
- BW 200 MHz
- Rate up to 100 kHz



HV regulator

- regulation steps 10 mV up to 90 V
- Stability better than 10 mV





Design Maturity

Calorimeter Subsystem	Design Completion	Remaining Work/Risks
Crystals	90%	Specification of CsI slow component - Low risk.
Photosensors	85%	SiPM packaging. Have one packaged SiPM from Hamamatsu but want to qualify other vendors - Low risk.
Mechanical Infrastructure	65%	Finalize cooling design. Optimizing tradeoffs between noise, radiation damage and operating temperature. x2 headroom - Low Risk
Front End Electronics And Digitizer (WFD)	60%	• New pre-amp design for CsI/SiPM - Low Risk. • **WFD board design with 20 channels.** Moderate risk that we may have to back off to 18 channel boards. Adds a small amount of complexity.
Calibration	90%	Integration of source pipes. Finalize laser optics. – Low Risk
Overall Design	**80%**	

Quality

- FEE' plans included in Mu2e Quality Planning Document
  - Available on web page (docdb 6005)

Deliverable	QA or QC Step?	QA or QC Process Documentation (DocDB #)	Inspection or Acceptance Criteria/Plan	Verification
FEE	QA: Calibration of Voltage scale	in progress	The regulation voltage part of each FEE chip will be tested on a bench in a semi-automatic manner by varying the setting in steps of 100 mV around the operation bias.	Each step of setting will be controlled by means of an external voltmeter with digital readout
FEE	QA: Gain	in progress	For the preamplification part, both the signal shape and the amplification gain will be tested when sending in input a narrow analog signal.	The linearity in response will be determined by sending 20 different values of input signal in mV to test both the amplification value and its linearity. Dinamic range up to 2 V, Gain = 10. We will use input signals from 10 to 190 mV
FEE	QA: Calibration of mezzanine board	in progress	The mezzanine boards will be tested both for evaluating the ADC/DAC part to set and read the voltages.	A reference WFD board will be used to test the connection between the mezzanine and the WFD and allows to communicate via optical fibers to a control desktop. A digital voltmeter will be used to measure the output.

Interfaces

Internal Interfaces			
Item	Interface	Descriptions	Owners
107.04.1.1	SIPM/FEE/Laser system	The disk consists of a self- standing structure built piling-up the single crystal units in a way which allows insertion and extraction of photo-sensors if repair is needed. The SIPMs are mounted in the SIPM/FEE holders attached to the rear support disk. The SIPM are closely connected to the related FEE electronics. The connectors for inserting optical fibers will be placed in the rear face in a dedicated spot in the SIPM holder. Interference between calibration services and FEE cabling have to be considered in the cabling layout at CAD level and tested in a dedicated full size mockup and in a larger size prototype (Module- 0).	475.07.04 475.07.05 475.07.06
External Interfaces			
107.07.2.1	AC Power Distribution	AC power is required for the power supplies of the calorimeter, for and the general distribution will be supplied by WBS475.03	475.07.07 475.03

Interfaces are understood and under control

Milestones

- **Short term:**
  - → Pre-production for the module-0 in June 2016
  - → QA of pre-production July 2016
  - → Module 0 in fall 2016

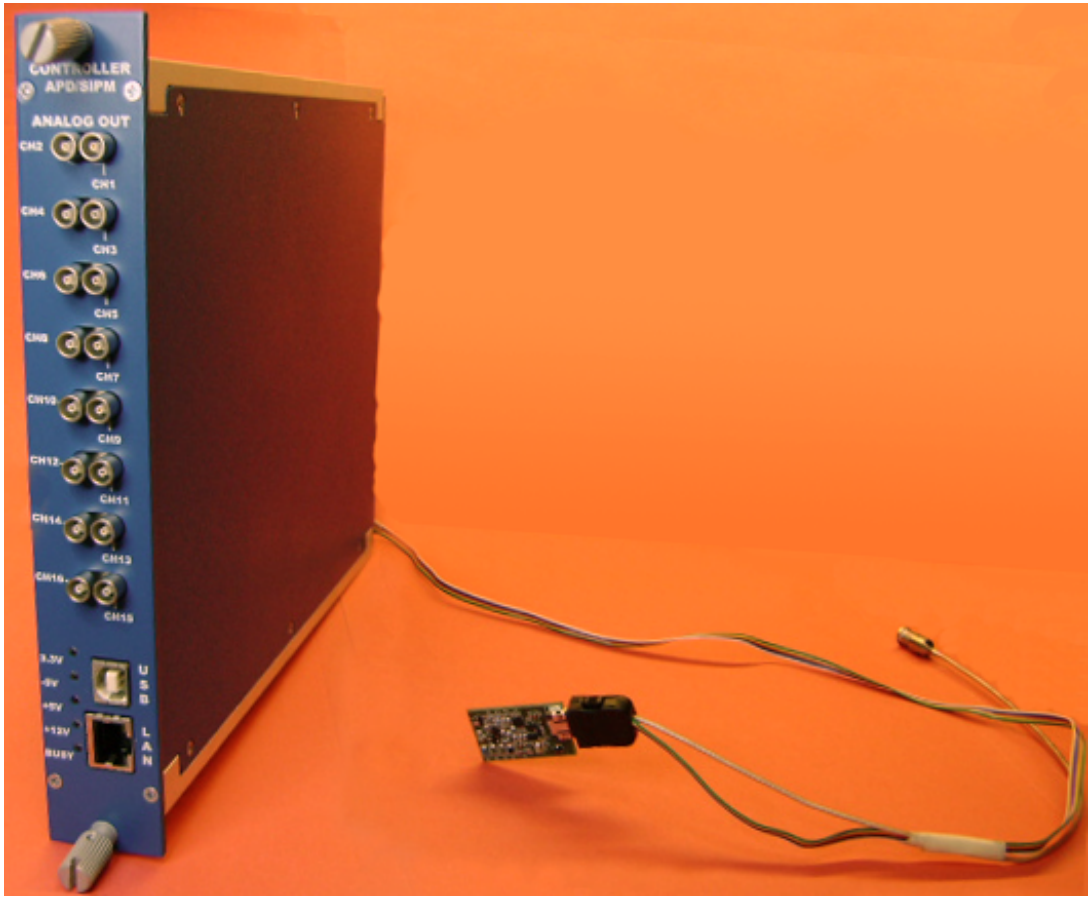
- **Long Term:**

PO issued for production FEE and Power	**April 2017**
QC of all FEE and Power complete	**August 2018**

Conclusions

- The front-end system can handle the SiPM photosensor, in a Voltage range regulation between the 20-230 Volt.
- In the preamplifier, the gain can be adjusted at two different values in case of needs for the innermost region after irradiation.
- The connection cables, between preamp and controller card, should have lengths smaller than two meters. This is in agreement with the cabling layout we are designing for the final calorimeter geometry.
- **We are now developing another version of this system, that will be adapted to the new SiPM packaging layout with readout in series:**
  - → Conceptual design ready;
  - → Technical design will be released **end of May 2016**;
  - → 120 prototypes will be assembled for test beam of the module 0, end of June 2016.

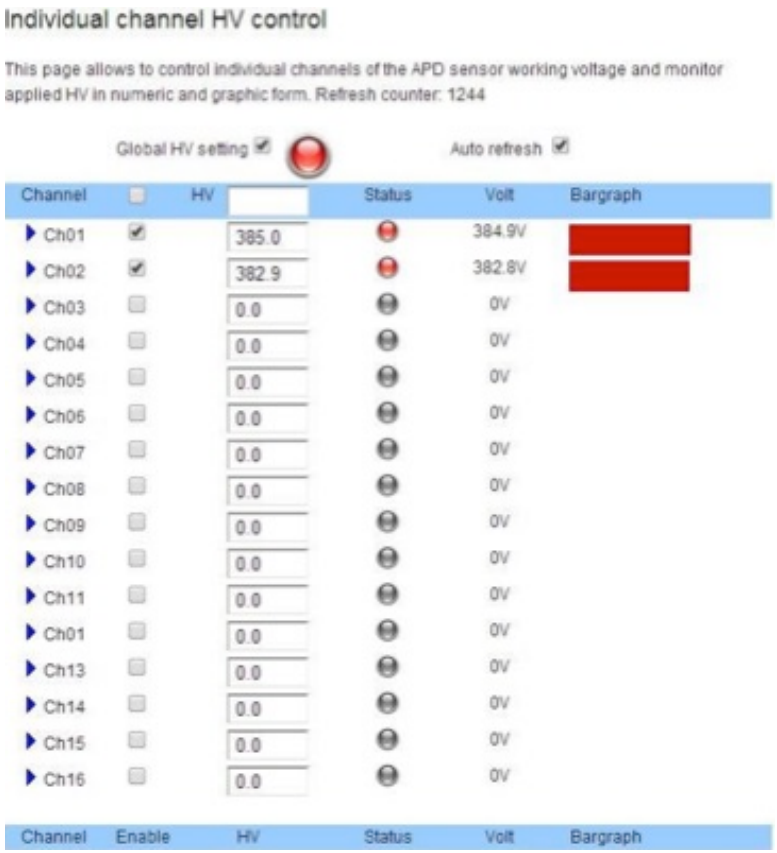
Controller_ARM MPPC



Front view

Back view

Control Panel



Control panel via network

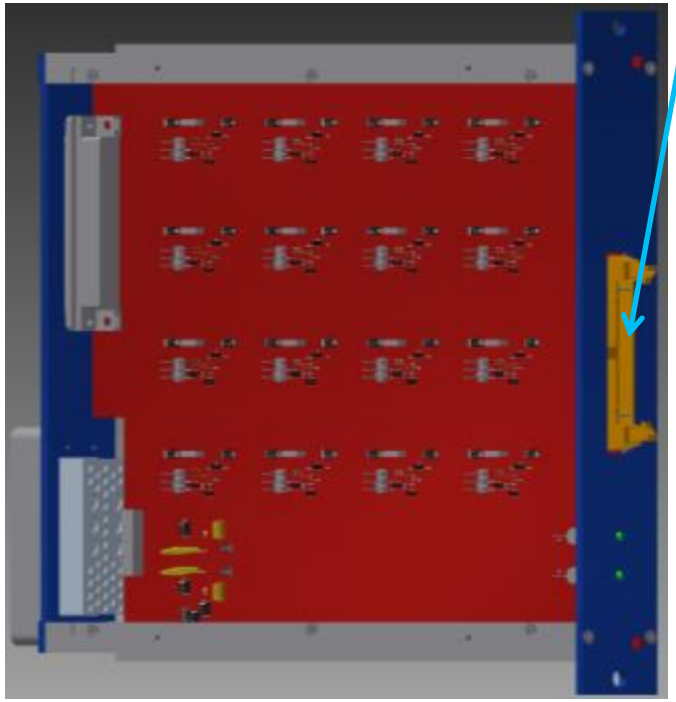
→ Control the Front-End cards.

→ Setting and reading the output voltage.

→ Measurement of Temperature and supply voltages.

Card shifter coax to differential.

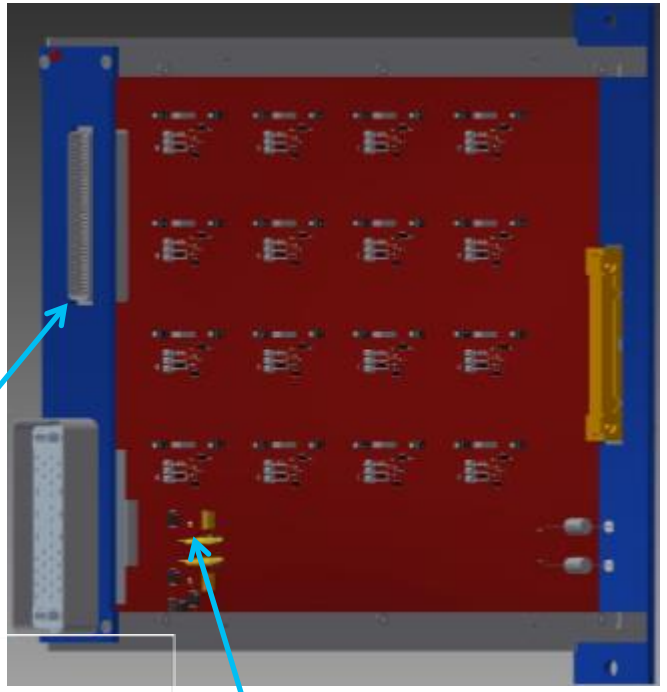
Front Panel NIM-1U



16 Analog Signal Output

16 Analog Signal Input

Rear Panel NIM-1U



16 Jumpers, for Inverting Signal output.

On the board we have:

- 16 channels level translator.
- Reverse polarity by jumper.
- Nim standard mechanics.