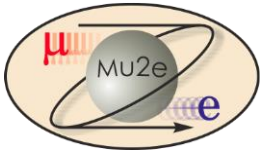
Fermilab



Mu2e CD3c Review
WBS 475.07.05 Calorimeter Digitizer

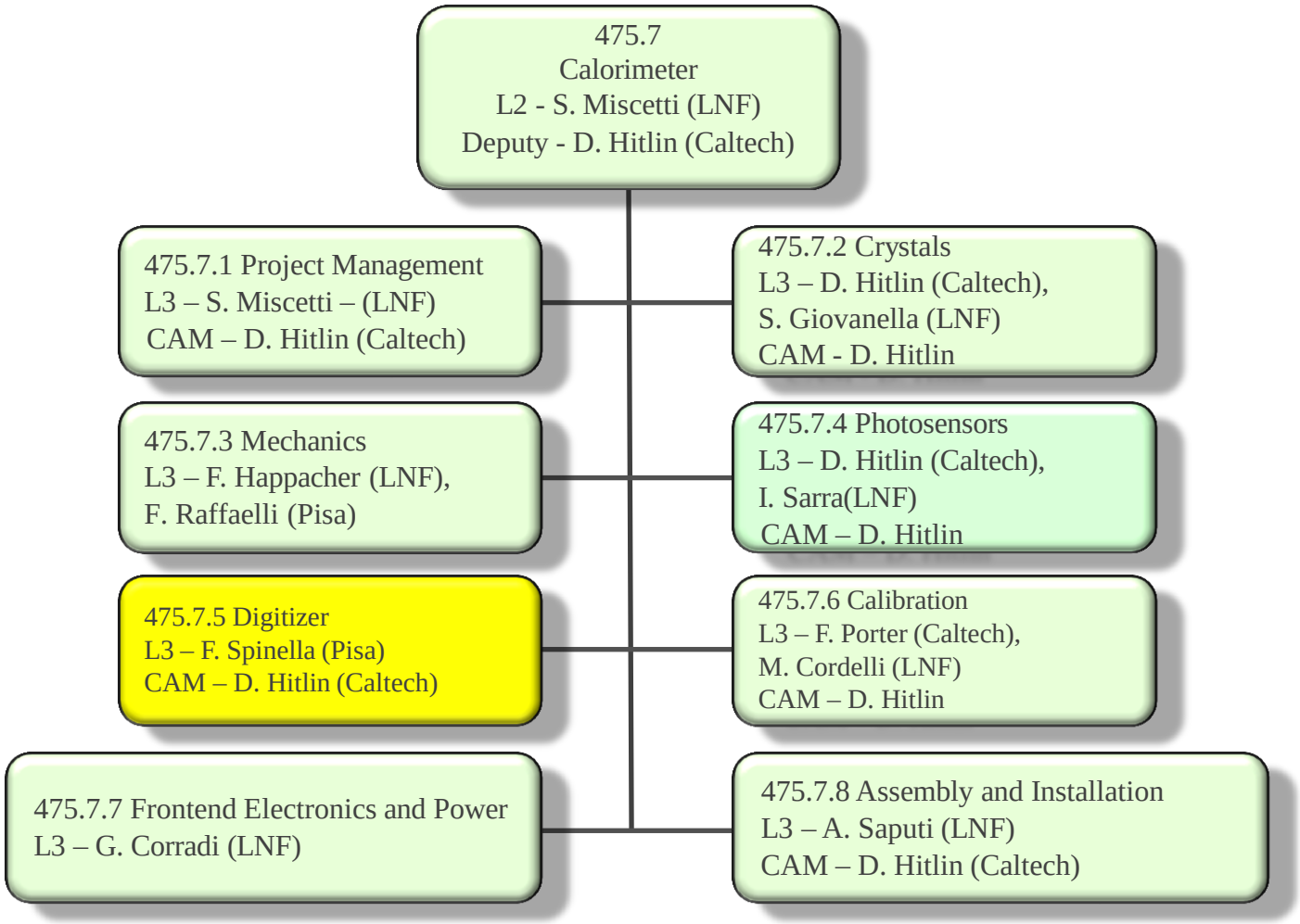
F. Spinella
Mu2e Calorimeter Digitizer L3 Manager
4/19/16
(presented by S. Di Falco)

Calorimeter Digitizer Team

Designed digital electronics for CDF, AMS-02, NA62...

- Franco Spinella:
  - Calorimeter Digitizer L3 Manager
- Luca Morescalchi:
  - FPGA firmware design
- Giani Pezzullo and Stefano Di Falco:
  - Simulation and performance test

Mu2e Calorimeter Organization



Scope

WBS 475.07.05
Digitizers
Franco Spinella / PISA

475.07.05 **Delivery of the calorimeter digitizer boards from INFN.**

Technical Objective
This WBS covers all aspects of the design and construction of prototype and production digitizer boards for the calorimeter system. The design of the board will be done by INFN. Construction of all digitizer boards will be provided by INFN as an in-kind contribution.

Scope of Work Statement
The scope of work includes:

- The calorimeter prototype digitizer board;
- The construction of all digitizer boards for the calorimeter;
- Test of the full readout chain.

Requirements 1

•The Calorimeter requirements are described in Docdb 864

•Calorimeter Digitizer system must meet the following requirements as in Docdb 6770 & Docdb 6782:

1) Sample the SiPM signal (after FEE) to achieve a good energy resolution O(5%) and an optimal time resolution < 500 ps

2) Provide 2700 ADC channels (each crystal is readout through 2 SiPM)

3) To be located inside the cryostat to limit the number of pass-through connectors

Requirements 2

(1) Sample the signal with an ADC with 200 Msps - 12 bits

(2) Stand a radiation environment of $5x10^{10}$ n/cm^2
@ 1 MeV_{eq} (Si)/y and 0.5 krad/y of TID (Total Ionizing Dose)

(3) Work in presence of high magnetic field (1T)

(4) Operate in vacuum:

- Low power
- large reliability to allow to operate for 1 year w.o. interruption

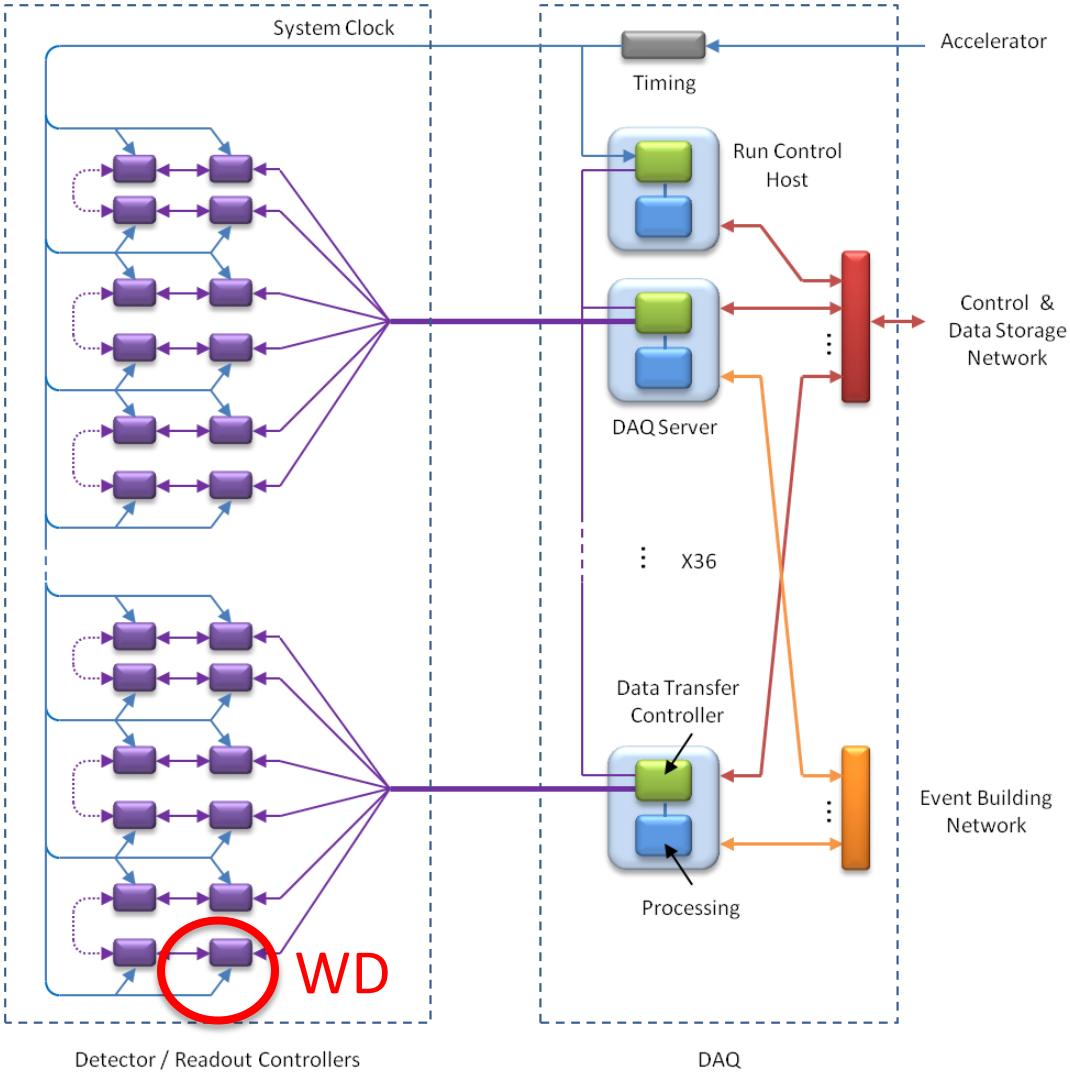
(5) Host 20 channels/board (mechanical constrains & BW limit)
Consider backup solution at 18 channels/board.

Design choice – progress since CD-2 (2014)

• At the CD-2 we presented the architecture of the calorimeter DAQ and the conceptual design of the WD (docdb 4323,5412,6782)

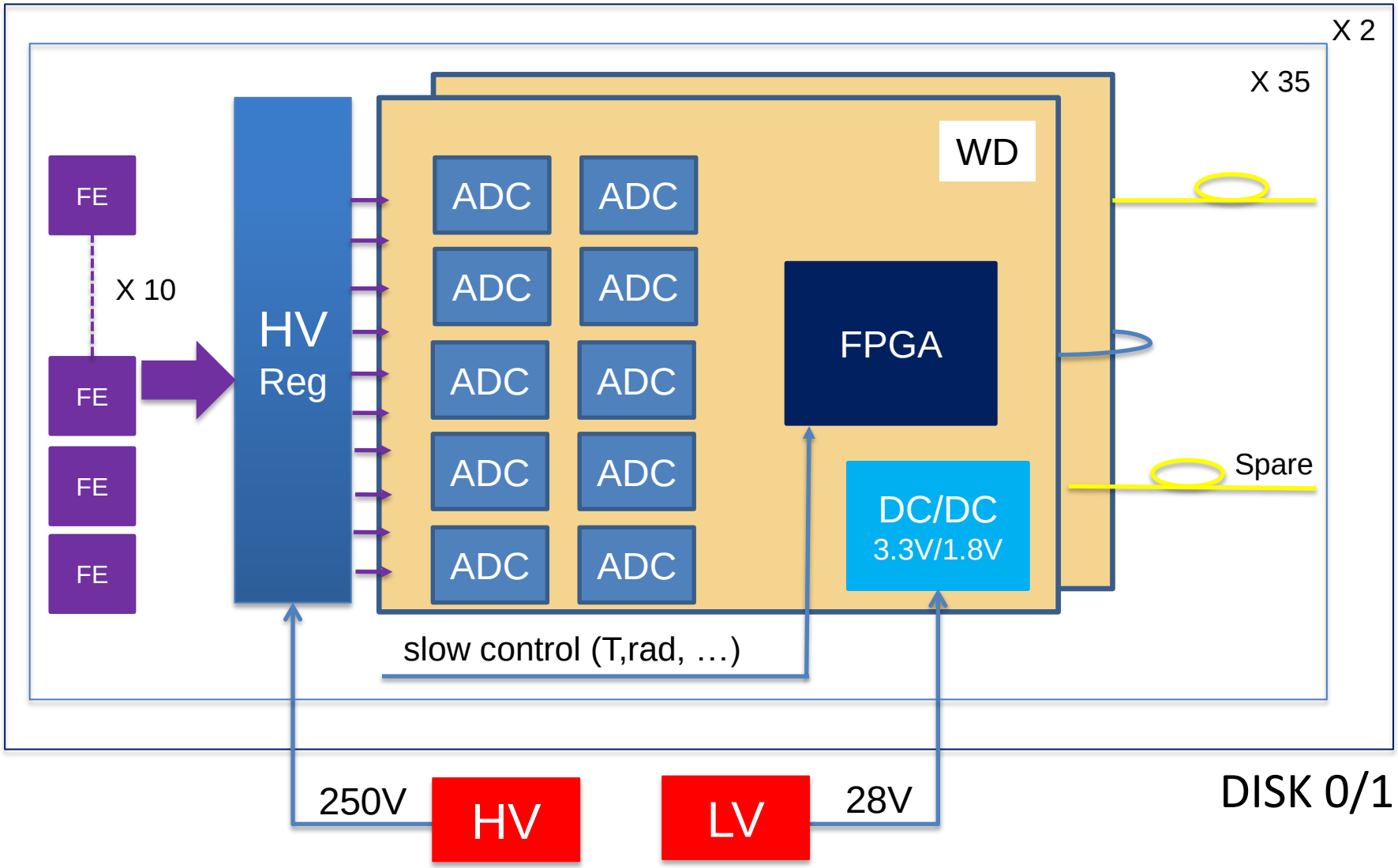
• This is basically unchanged at the high level, while a new design based on the final choice of the components has been developed at this stage.

MU2E DAQ

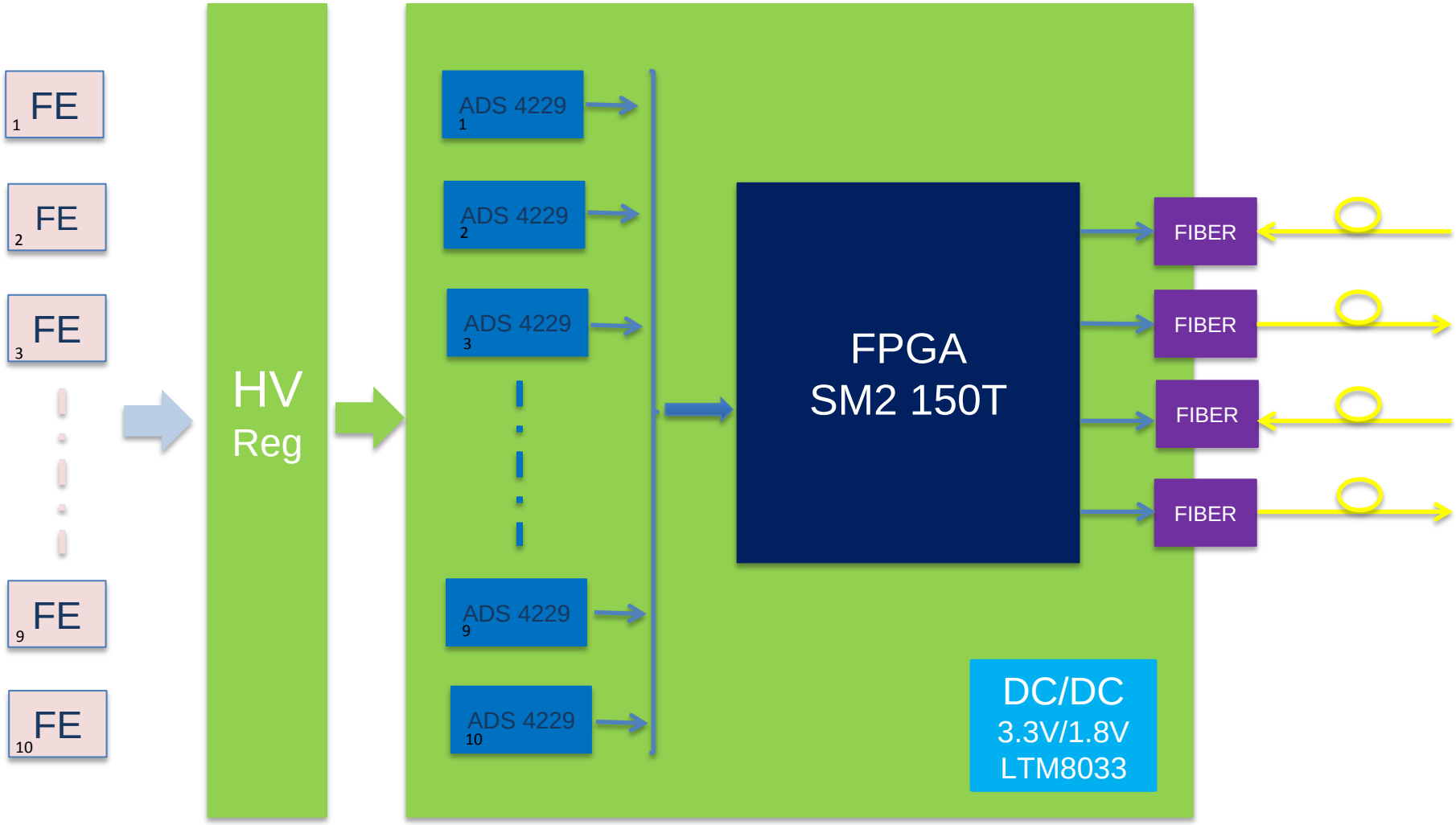


- WD are readout in chains (2-4 boards/chain)
- Chains are redundated
- Each chain is connected to the DAQ servers through optical fibers

DAQ for the calorimeter



WD block diagram



Design Maturity and Path to Completion

- WD design components have already been selected and tested for radiation and high magnetic field immunity (docdb 6782)
  - FPGA: Smartfusion II SM2150T (qualified by producer)
  - ADC : ADS4229
  - DCDC : LTM 8033

- A first pre-prototype has been designed assembling demo boards and custom interconnecting boards. The obtained prototype is functionally identical to a single channel WD

- The design of the final WD is almost complete and the PCB is being laid out

- The first prototype of the 20 channels board is foreseen for end of July

Performance: FPGA

- The choice is almost unique (at moment)
- Microsemi SmartFusion2 family (SoC: FPGA + CPU)
  - –Specs:
    - Flash (and not RAM) based
    - SEL free (see tables)
    - Configuration Flash SEU free(up to 90 MeV ions)
    - Data SEU low
    - Very low power

- We will use the largest and fastest one
- SM2150T-1 (1152 pins)

- In principle we do not need to qualify this part as a single element

$5x10^{10}$ n/cm^2/y
5 Mbits RAM

1 SEU/board/hour
1 each 200000 events
(pessimistic)

Table 1: Single Event Latch-Up Summary

Run	Device Tested	Number of Parts Tested	Test Facility	Test Temperature	Total Test Fluence	Number of SEL Events LET <= 20	Number of SEL Events LET > 20
1	M2S050	3	LBNL	Room Temperature	2.20×10^8	0	0
2	M2S050	3	LBNL	Room Temperature	4.09×10^8	0	0
3	M2S050	8	TAMU	100°C	4.41×10^8	0	2
Total		14			1.07×10^9	0	2

Table 4: Configuration Single Event Upset Boundary of FIT rates

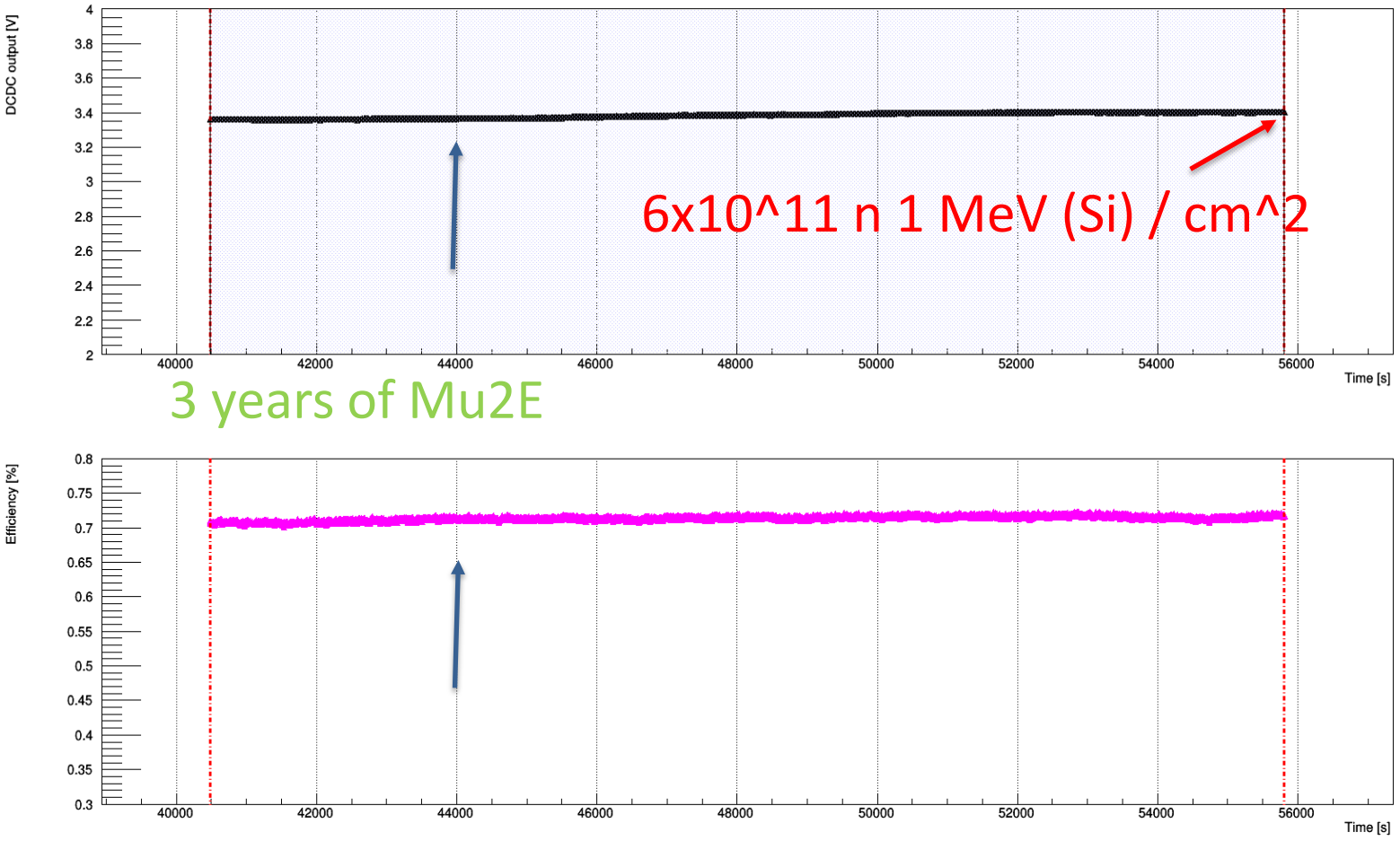
Environment	Upper Boundary of Configuration SEU FIT Rates
Ground Level (Sea Level, New York City)	Immune
Aviation (40,000 feet, New York City)	Immune
Space (Low Earth Orbit, 800 km circular, 85° inclination)	Immune

Table 5: Data SEU Summary (Single Bit Upsets)

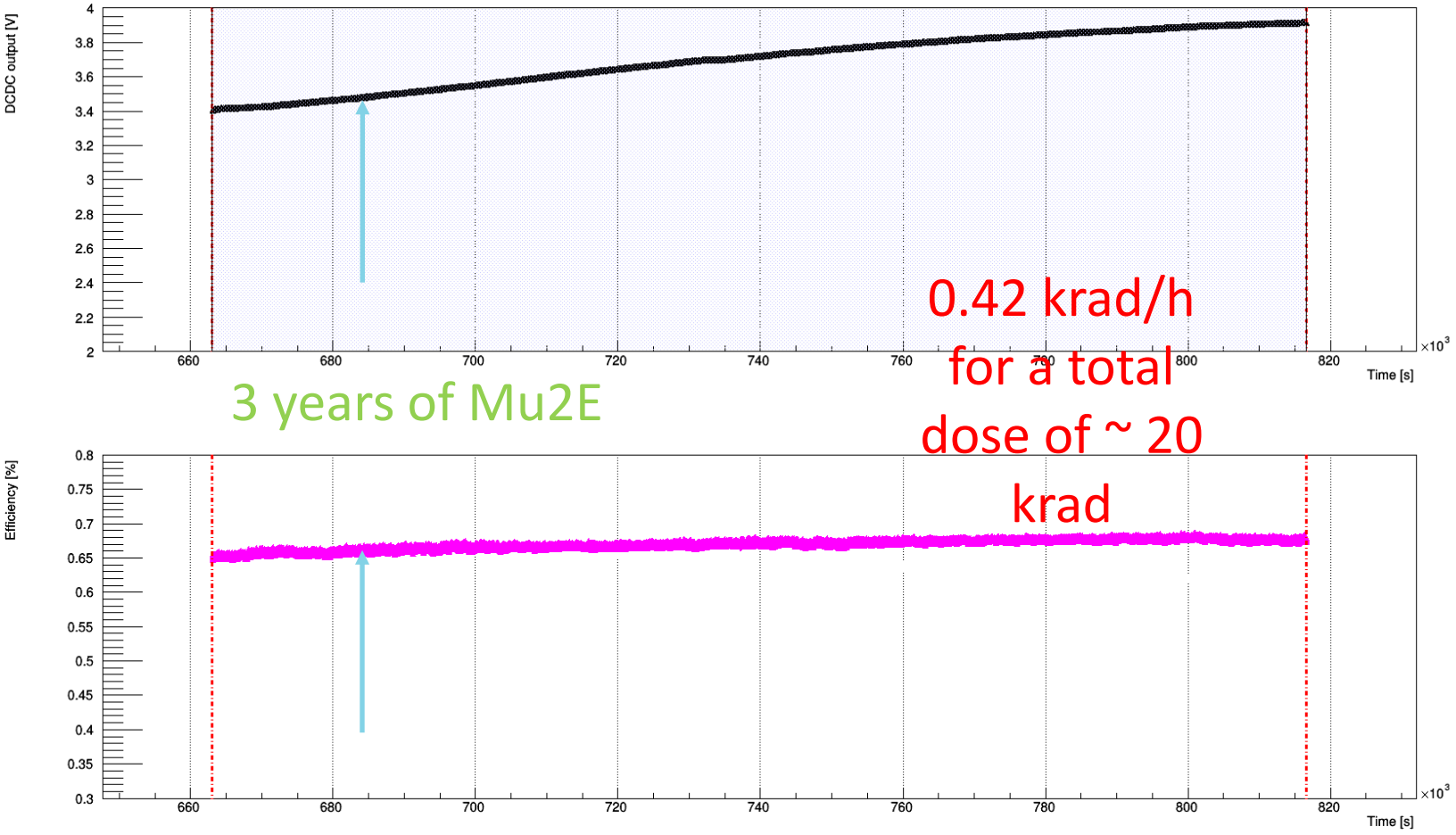
Feature	Test Fluence (Neutrons/cm^2)	Error Rate Ground Level (Sea Level, NYC, FIT)	Error Rate Aviation (40,000', NYC, FIT)
Flip-flop	4.35×10^{11}	218.3 FIT / million flip-flops	1.13×10^5 FIT / million flip-flops
LSRAM	1.7×10^{11}	340.6 FIT / million bits	1.75×10^5 FIT / million bits
uSRAM	1.7×10^{11}	175.3 FIT / million bits	9.04×10^4 FIT / million bits

http://www.microsemi.com/document-portal/doc_view/134103-igloo2-and-smartfusion2-fpgas-interim-radiation-report

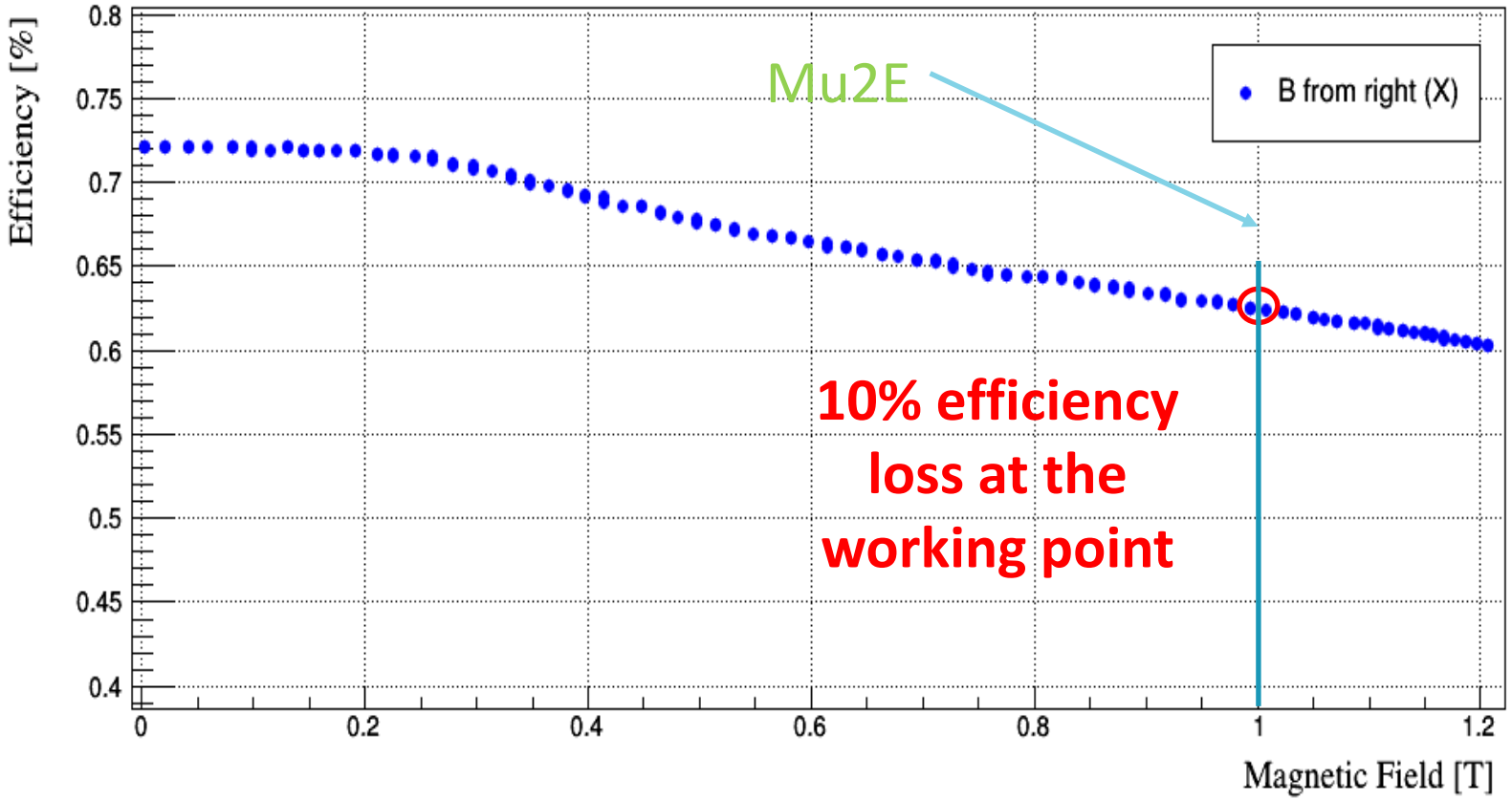
Performance: DCDC converter neutron irradiation



Performance: DCDC converter gamma irradiation

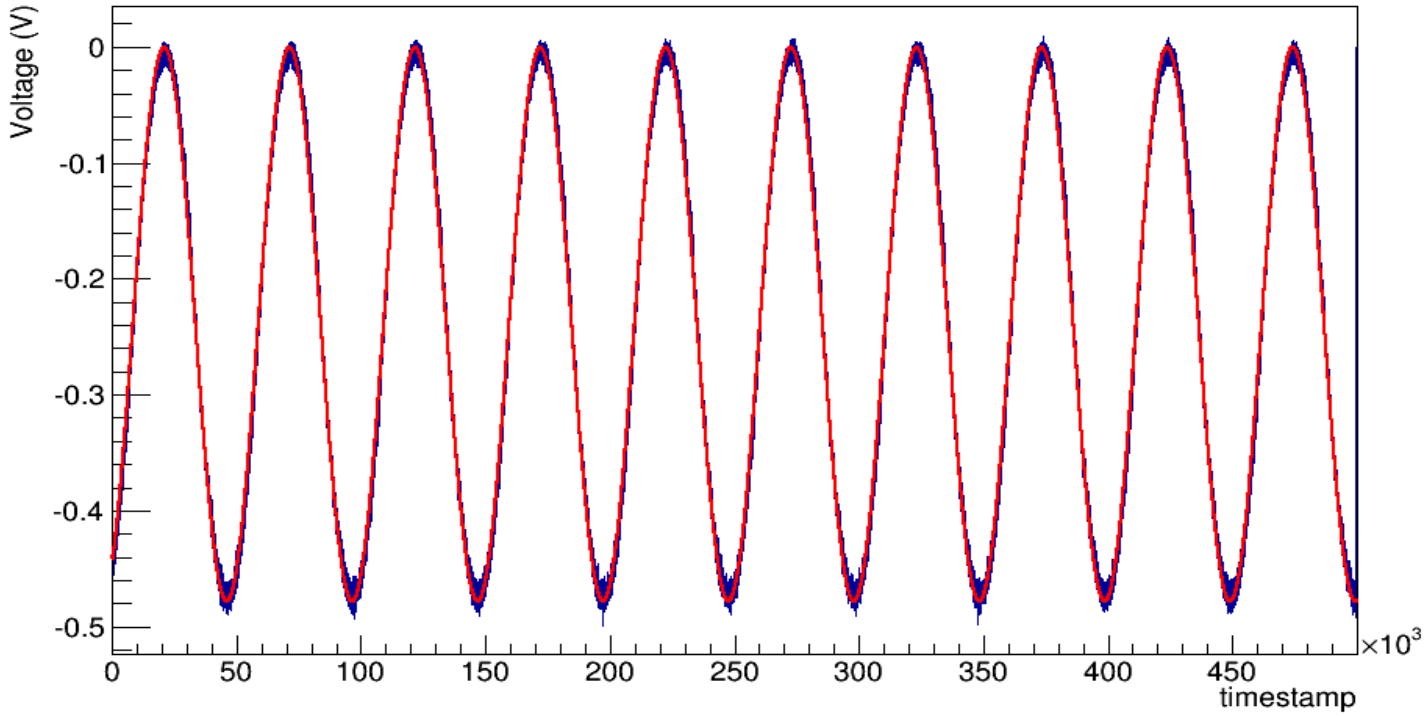


Performance: DCDC converter in magnetic field



Performance: ADC neutron and gamma irradiation

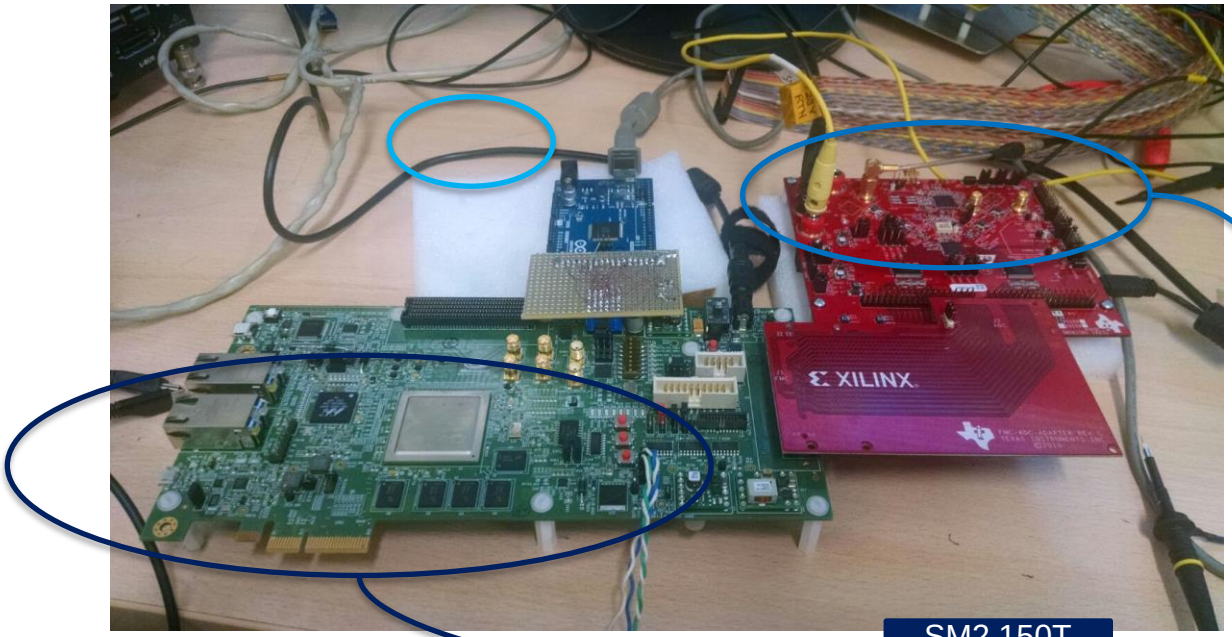
Neutron test 6x10^11 n 1 MeV (Si) / cm^2
Gamma ray Total Ionizing Dose: 20 krad TID



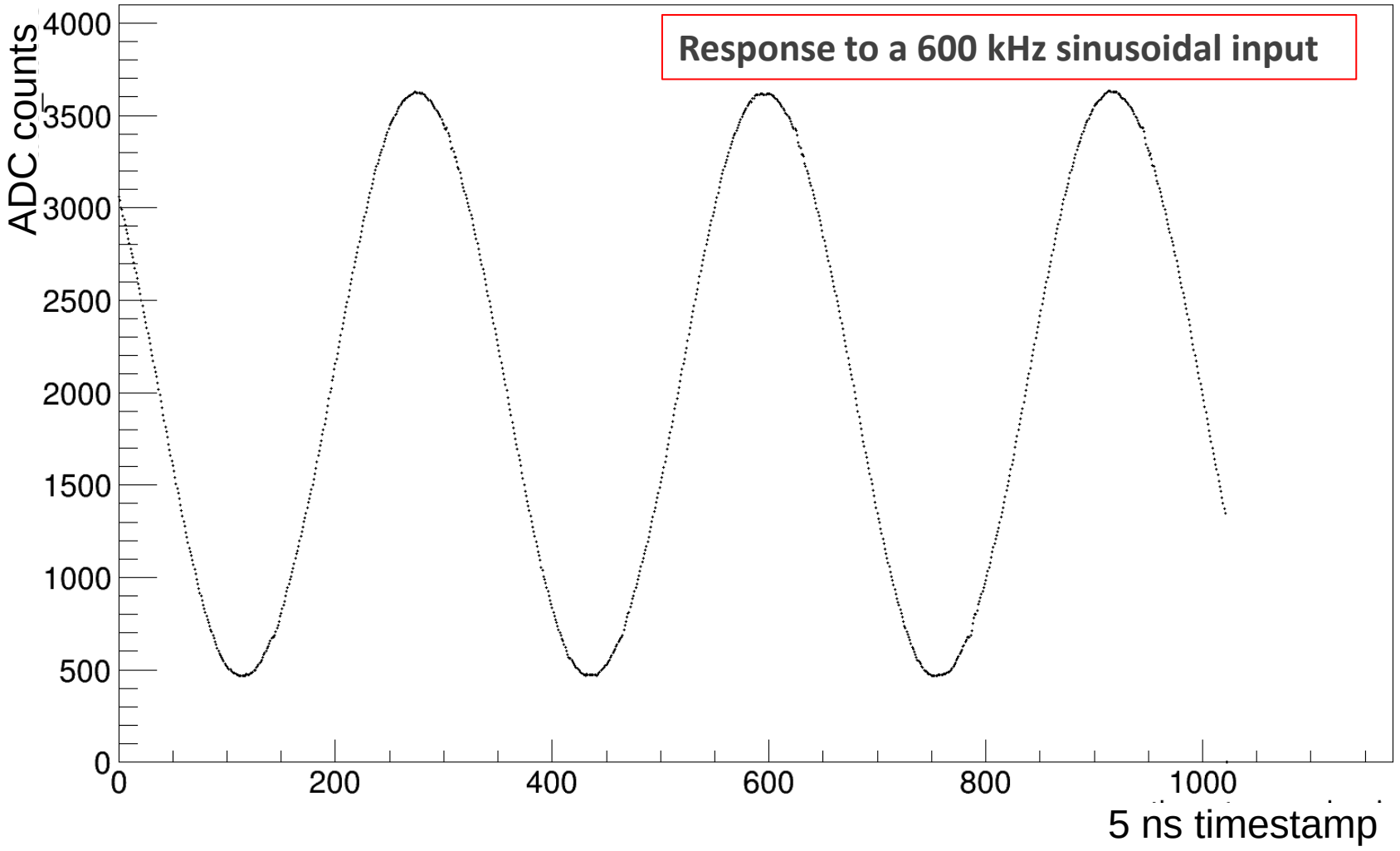
We acquired more than 300 GB of data in both neutron and gamma-ray tests, with no evidence of bit flips or waveforms shape variation.

Performance: pre-prototype

- Performance tests on the single channel pre-prototype has shown that the components choice is capable of digitizing the incoming signal and also to substain the data flow (docdb 6782, 6770)



Performance: 1 ADC at 200 MHz DDR



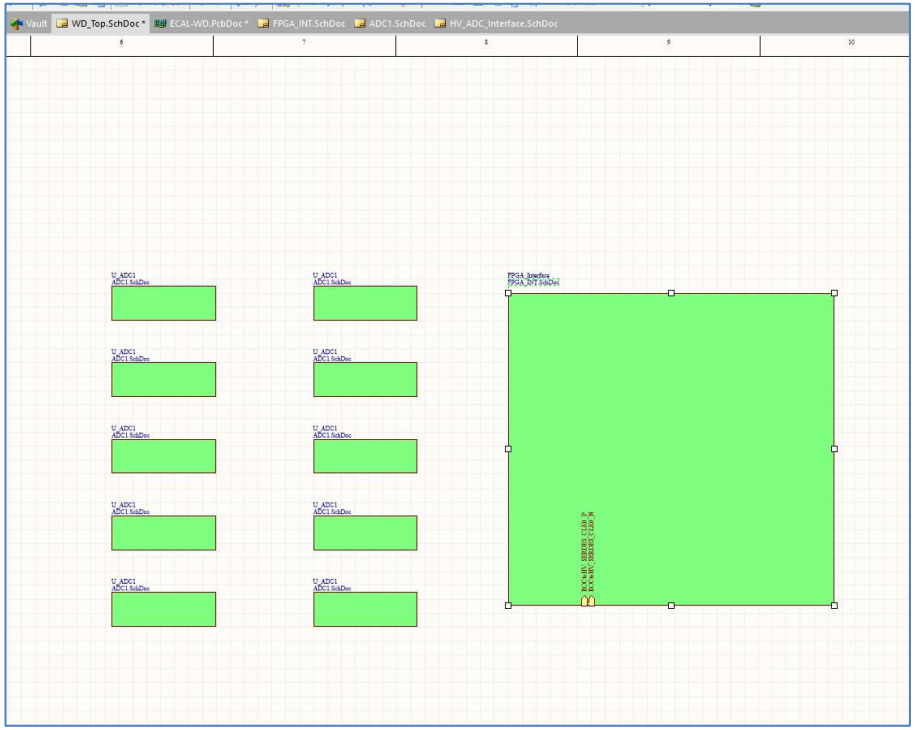
No evidence of bit flips (some noise due to pulse generator)

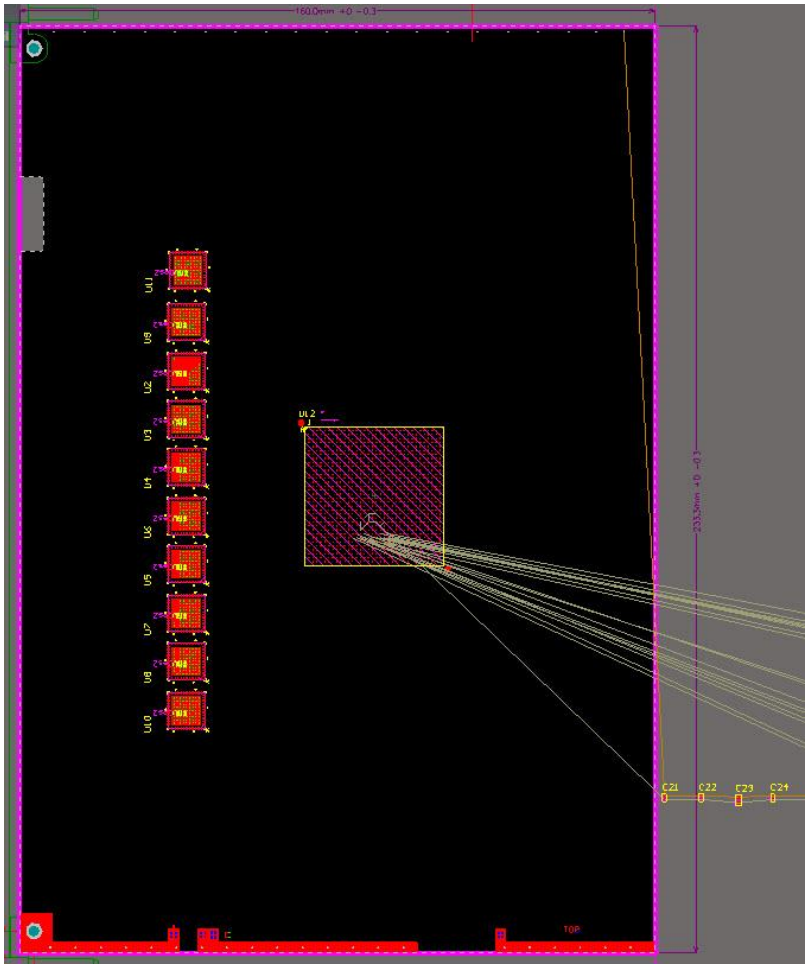
`Design maturity

docdb 6972.

Calorimeter Subsystem	Design Completion	Remaining Work/Risks
Crystals	90%	Specification of CsI slow component - Low risk.
Photosensors	85%	SiPM packaging. Have one packaged SiPM from Hamamatsu but want to qualify other vendors - Low risk.
Mechanical Infrastructure	65%	Finalize cooling design. Optimizing tradeoffs between noise, radiation damage and operating temperature. x2 headroom - Low Risk
Front End Electronics And Digitizer (WFD)	60%	• New pre-amp design for CsI/SiPM - Low Risk. • WFD board design with 20 channels. Moderate risk that we may have to back off to 18 channel boards. Adds a small amount of complexity.
Calibration	90%	Integration of source pipes. Finalize laser optics. – Low Risk
Overall Design	**80%**	

Design completed





Fabrication Plan

•Digitizers will be paid by INFN and fabricated from qualified companies

• A bid will be called to assign the production contract

Quality Control / Quality Assurance

•QC: the relevant procedures will be detailed at the end of the prototype testing and before the production

•QA:

- Each board will be optically inspected and electrically checked for power shorts
- After the first power-on all the electrical parameters will be measured and checked toward the reference prototype board
- Each ADC channel will be checked for linearity digitizing a known sinusoidal waveform (standard test for digitizer)
- A minimum one month burn-in test at working temperature will be performed on each card before the installation

• Document QA process (facility PC and Mu2e Hardware DB)

<u>Configuration Management:</u>

•Use labels with barcodes for each board

•Correlate labels with QC/QA and shipping data

Quality

- Digitizer plans included in Mu2e Quality Planning Document

Sub-Project	QA or QC Step?	Inspection or Acceptance Criteria/Plan	Verification	Records (DocDB# or Database Reference)
Waveform Digitizers	QC: Inspection and certification	Each board will be optically inspected and electrically checked for power shorts.	Inspection by certified personnel. All the electrical parameters will be measured and checked toward the reference prototype board	A database of digitizer QC will be kept on docdb.
Waveform Digitizers	QA: functionality test	Each ADC channel will be checked for linearity digitizing a known sinusoidal waveform. A minimum one month burn-in test at working temperature will be performed on each card before the installation	Check for missing ADC bits. Fourier analysis of the waveform	A database of digitizer QA will be kept on docdb.

Internal Interfaces (docdb 2195)

Item	Interface	Descriptions	Owners	
107.05.1	FEE/Waveform Digitizer	Digitizer boards will receive analog channels through a mezzanine board, frontally connected to the WD through a high density connector. DC power will arrive to the WD through a terminal block screwed to the back of the crate. Clock will be distributed through differential links coming from a clock fan-out board also hosted on the crate	475.07.05 475.07.07	
107.05.2	Mechanics/ Waveform Digitizer	Digitizer boards and crates will match the geometry, the thermal and electrical insulation constraints for the calorimeter disks	475.07.03 475.07.05	

Interfaces are understood and under control

External Interfaces (docdb 2195)

Item	Interface	Descriptions	Owners	
107.05.1.1	Cooling System	A dedicated cooling system should remove the heat from the electronics. Dimensioning of the electronics and overall power dissipation will constrain the overall cooling system and has to respect the mechanical constraints of the disk structure and of the DS.	475.07.05 475.07.07 475.06	
107.05.1.2	DAQ System	Waveform digitizers are hosted in custom crates. Each crate will host 8 boards plus a clock distributor. All the boards will receive DC power (+28 V) from a terminal block installed on the side of the crate. Boards will be daisy chained through a couple of bi-directional fibers for redundancy while the extreme boards will be connected to the external servers with fibers through a vacuum pass through connector The streaming readout assumes that all data above zero will be transferred by optical fibers to the DAQ and the overall throughput has to be recorded.	475.07.05 475.09	
107.05.1.3	Readout System and Monitoring	Uniformity in readout systems and monitoring is likely similar to that of the tracker.	475.07.05 475.06	
107.05.1.4	Low Voltage	Number, capacity and voltage of low voltage lines has to be defined for the digitizers and FEE and vacuum penetration provided in the DS bulkhead.	475.07.05 475.07.07 475.05	

Interfaces are understood and under control

Integration

- Strict cooperation with:
  - TDAQ group to discuss the data links and protocols
  - Tracker group to optimize the FPGA firmware

- Integration meetings:
  - Attend weekly Calorimeter meetings
  - Attend weekly Electrical Integration meeting

Environmental, Safety & Health

- Digitizers follow established safety procedures at Fermilab as specified by FESHM
- No special hazards are expected given the low operating voltage

Risk 1: CAL-212 number of channels/board (docdb 7038)

Title: Cannot integrate 20 channels/board in the Waveform Digitizers

Description: Due to the limited space for positioning the boards inside the DS, we have organized the readout in electronics board composed by a mezzanine-board (for HV setting) and a digitization board where 20 calorimeter channels are digitized at 200 Msps. The preliminary estimate with 1 channel prototype and simulation demonstrates that the selected FPGA (Smart Fusion II) is able to handle such a readout but we have not yet a full demonstration of a 20 channel prototype working.

Cause: We have not yet a 20 channels prototype built.

Effect: We cannot readout all calorimeter channels.

Start Date: FY16 **Finish Date:** FY17

Initial Analysis: This risk has a medium probability but no cost impact

Upper bound of cost impact: It is all in-kind from INFN

Exposure: To build boards with a more performing FPGA to readout 20 channels.

Initial Mitigation Plan: We have 3 mitigations in progress:

a) speeding up the construction and test of the 20 channels prototype,
b) investigate channels and boards organization within mechanical and integration constraints to see if we can fit more boards with 18 channels prototypes
c) investigate the new Smart Fusion III release.

Risk 2: Cal-210 DAQ ring organization (docdb 7036)

Title: Reliability of DAQ ring organization in 4 WFD boards

Description: In the current scheme, 4 Waveform Digitizer Boards (WFD) are connected in a ring: if one board is lost it can take out other boards in the ring as well.

Cause: The bi-directional link for the WFD boards works up to the point of loosing connection from 2 out of 4 boards. If it happens the entire ring (i.e. 4 boards, 80 channels) will be lost.

Effect: We can lose a large fraction of the Calorimeter readout channels inside the DS.

Start Date: FY16 **Finish Date:** FY16

Initial Analysis: This risk has a low probability and a low impact on schedule.

Upper bound of cost impact: 30000 $ if needed (for penetrations, server will be Procured during operations)

Exposure: 30 days of lost running time to access, fix and re-establish operations.

Initial Mitigation Plan: We are still developing the mitigation plan that considers only 2 WFD boards per DAQ ring. This comes at the cost of:

a) increasing the number of penetrations in the DS bulkhead from 12 to 27
b) increasing the number of DAQ servers by one.

We are studying the organization of penetrations in the bulkhead and the additional outgassing associated with doubling the number of readout fibers.

Summary

- All critical components have been qualified:

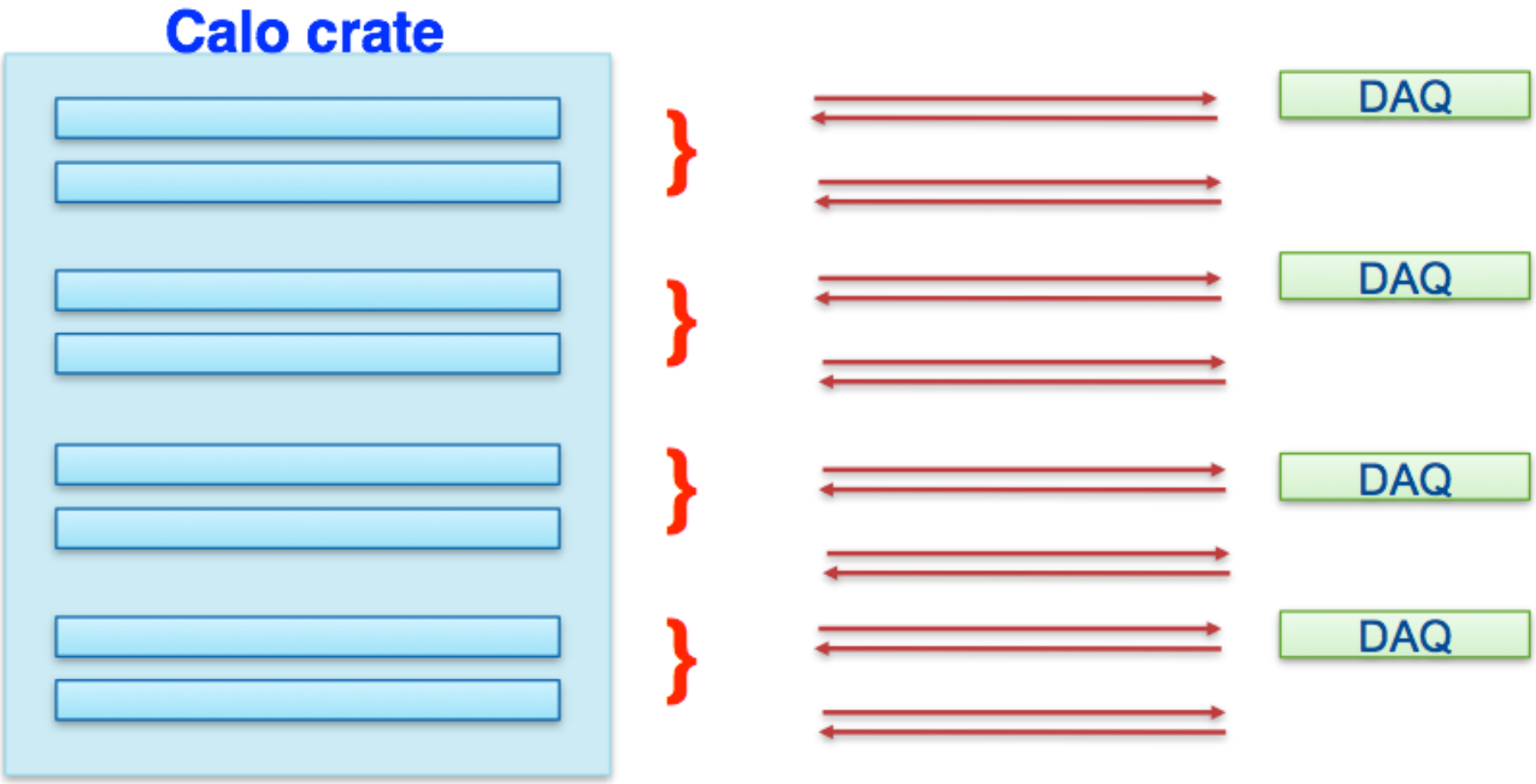
 - the FPGA is the same in use for all the mu2e electronics and qualified by the producer

 - DCDC converter and ADC have been qualified to operate in high magnetic field and to survive to the expected ionization dose and neutron flux

- Schematic design is completed, PCB is being laid out
- A pre-prototype with 1 FPGA reading 1 ADC is functional
- We will build 2 prototypes and use them in the test beam of calorimeter prototype in fall 2016
- The calorimeter digitizers are ready for CD3-c approval.

Backup

Proposed DAQ scheme



- 2 bidir-fibers each 2 boards: only 1 connected to the DAQ

Risk evaluation of proposed DAQ scheme

With a daisy chain of **2** boards there are 3 failure modes:

1. **1 bidir-fiber lost**
2. **1 transmitting board lost**
3. **link between boards lost**

Failure recovery

- **Case (1)** -> use the other fiber=> **NO DATA LOSS**
- **Case (2)** -> use the other fiber=> **1 BOARD LOST**
- **Case (3)** - > use both fibers => **NO DATA LOSS**