Timing system and other possible requirements (or desires) for the WIB from the DAQ group

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Timing system proposal – docdb-1203

- So far, this is not a proposal, because we have not obtained a firm agreement from groups interested in doing this.
- Document is a useful start - A team has made a note (now docdb-1203) and iterated based on four extensive discussions in the group
  - Requirements
  - The two most likely possible implementations
- Focused on the needs for the far detector – so that whatever we build for ProtoDUNE is a real prototype of that.
- There is still time to do the main timing system, however it was realized recently that it will impact on the warm interface board, which is why working all this out is accelerated.

Requirements

- Independent in 4 caverns
- Cold chip clocks: (a) 50MHz clock, (b) 2MHz digitize 'command' clock, (c) 30.5Hz sync command (=2MHz/65536),
- Long term clock, e.g. 1-PPS or per 10s, 5mins etc.
- Jitter on 2MHz digitize clock must be below 5% of one 2MHz cycle (=25ns).
- 50MHz must be in phase with 2 MHz
- 50MHz frequency and 2MHz frequency specified specifically.
- Phase of 50MHz must not change abruptly (internal PLLs in cold chip circuitry), i.e. change frequency by no more than 0.25% to realign phase.
- SSP clocks: Can be made to work with 50MHz frequency, try to operate with something consistent with 2MHz clock (to be discussed)
- Do we need to reconcile with DP 2.5MHz clock? Likely not if they will never be in the same cavern.
- 'Time stamping constraints' – the counters must be related to seconds/etc so that external events such as spill triggers can be associated.
- Inject signals such as calibration triggers etc.
- Monitoring of timing stability
- Not a requirement: Software trigger delivery – latency on Ethernet network is sufficient.

Implementations

- Easy - Getting the time from GPS and/or beam spills – reserve two fiber pairs per 10kt in shaft.
- More tricky – Fan-out timing signals from central point in each cavern to the 75 rack locations, and then to the individual boards.
- Two solutions:
  - NOvA-like timing: Clock is distributed at correct frequency (50MHz) and simply fanned out. 'Automatic' cable length correction.
  - White Rabbit: Used by dual-phase, clock distributed at 125MHz, we generate 50MHz from it at each location.

Possible WIB considerations (timing)

- If timing is controlled by the RCE and just passes through the WIB, all these considerations are for the RCE, not the WIB.

- Need a state machine in the warm to regenerate the 50MHz clock, 2MHz digitize command and 30.5ms (=2MHz/65536) sync command from the timing system.
  - straightforward for the NOvA timing
  - still working on understanding the complexity for the white rabbit.

- Need monitoring reports sent to slow control over Ethernet to report if errors are detected (e.g. non-zero counter on sync pulse reception) – this should also be in the data, but the data packets may be removed by the trigger.

- Data have only the 16-bit 2MHz counter on labeling it (rolls over after 30.5ms). Need to know which 30.5ms epoch this is. Computer clocks (xntp) are not accurate enough to do this, needs another layer of hardware to go to 1-sec epochs (or 10-sec epochs), then add h:m:s with software. Question: Is the 1-sec epoch labeling hardware in the WIB or RCE?

- Awkward that a round number of 30.5ms epochs don't make up a 1 second period. Several suggestions are made in docdb-1203 to fix this.
  - It is imperative that the decoding of time stamps is not complicated as it will need to be done many times in the software trigger
  - Also imperative we do not need to carry round the start time of the run to interpret the data.

(Non-timing possible considerations for WIB)

- The cold electronics interface as seen by the DAQ is very simple, which is great.

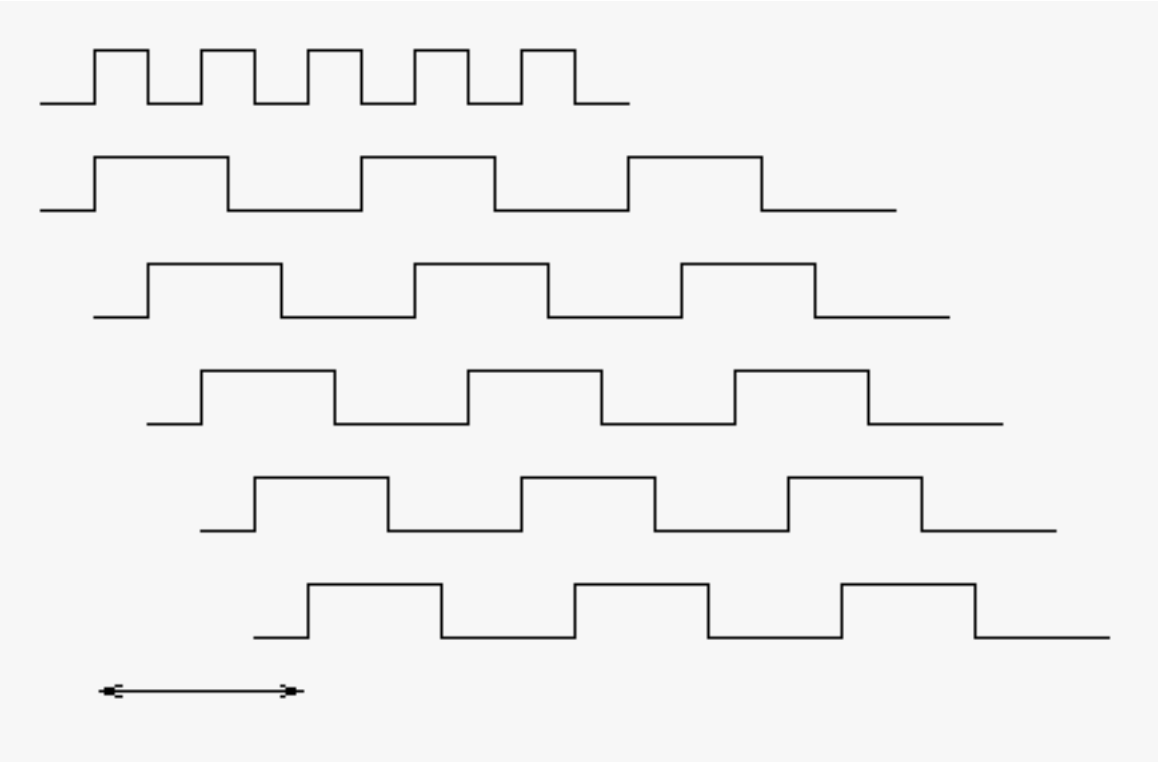
- If the WIB multiplexes the fibers from 1.2GB/sec to something else, what additional complication is added – are there resets that need applying at the start of the run? How is such a reset delivered? Over the link from the RCE, or via Ethernet? Can stale data be left in any FIFOs after a crash? How do we read the status to verify it is clear?

- If the WIB multiplexes, does this reduce the flexibility of how many cold board links we can assign to a single RCE. We should have the option of having 8 links per RCE (so 10 RCEs= 1 APA) which is the default, but also 10 links per RCE (so 8 RCEs = 1 COB = 1 APA) and 4 links per RCE (this is a test scenario where we can read data continuously even if the compression ratio is not so great.

Backup

125MHz to 50MHz

- Novices at White Rabbit, so not sure how straightforward this is.
- Multiply by 2, divide by 5. Five separate ambiguities in phase.
  - How to resolve this with White Rabbit functions?
  - Do we have to resolve it, it produces a 16ns/sqrt(12) jitter that is below our requirements.



Backup: from rates document (rate estimate with extra rows shown)

	1a RCE triggered High rate/energy			1a RCE triggered Goldilocks			1b RCE Continuous		
	Data	Cap-acity	Head-room	Data	Cap-acity	Head-room	Data	Cap-acity	Head-room
Trigger rate (Hz)	50			10			500		
Readout time (ms)	5			2			2		
#APA active/event	6			3			6		
Spill time (sec)	4.8			4.8			4.8		
Cycle time (sec)	16.8			16.8			16.8		
#Channels/APA	2560			2560			2560		
Digi rate (MHz)	2			2			2		
Sample size (bytes)	1.5			1.5			1.5		
Readout size (MB/evt)	230.4			46.08			92.16		
Lossless compession	2			2			2		
Instant total data rate (GB/s)	5.8			0.2			23.0		
Average total data rate (GB/s)	1.6			0.1			6.6		
Channels/FEMB-link	32			32			32		
Cold Links/APA	80			80			80		
WIB link combination function	1			1			1		
Cold links/RCE	8			8			8		
Input data rate/Link (Gbit/s)	0.768	1.0	0.768	0.768	1.0	0.768	0.768	1.0	0.768
Input data rate/RCE (Gbit/s)	6.144			6.144			6.144		
Untrig comp RCE data/spill (GB)	1.843			1.843			1.843		
Triggered RCE data/spill (GB)	0.461	0.8	0.576	0.037	0.8	0.046	1.843	0.8	2.304
#RCE/COB	8			8			8		
Trig data/spill/COB (MB/s)	768	1250	0.614	61.44	1250	0.049	3072	1250	2.458
Trig data/cycle/COB (MB/s)	307.2	1250	0.246	24.58	1250	0.02	1229	1250	0.983
#Event builders	12			12			12		
Input data/cycle/EVB (MB/s)	153.6	1250	0.123	6.144	1250	0.005	614.4	1250	0.492
Data rate to storage total (MB/s)	1843			73.73			7373		
#HDD needed	36.86			1.475			147.5		