WARM INTERFACE IMPLICATIONS FOR FELIX

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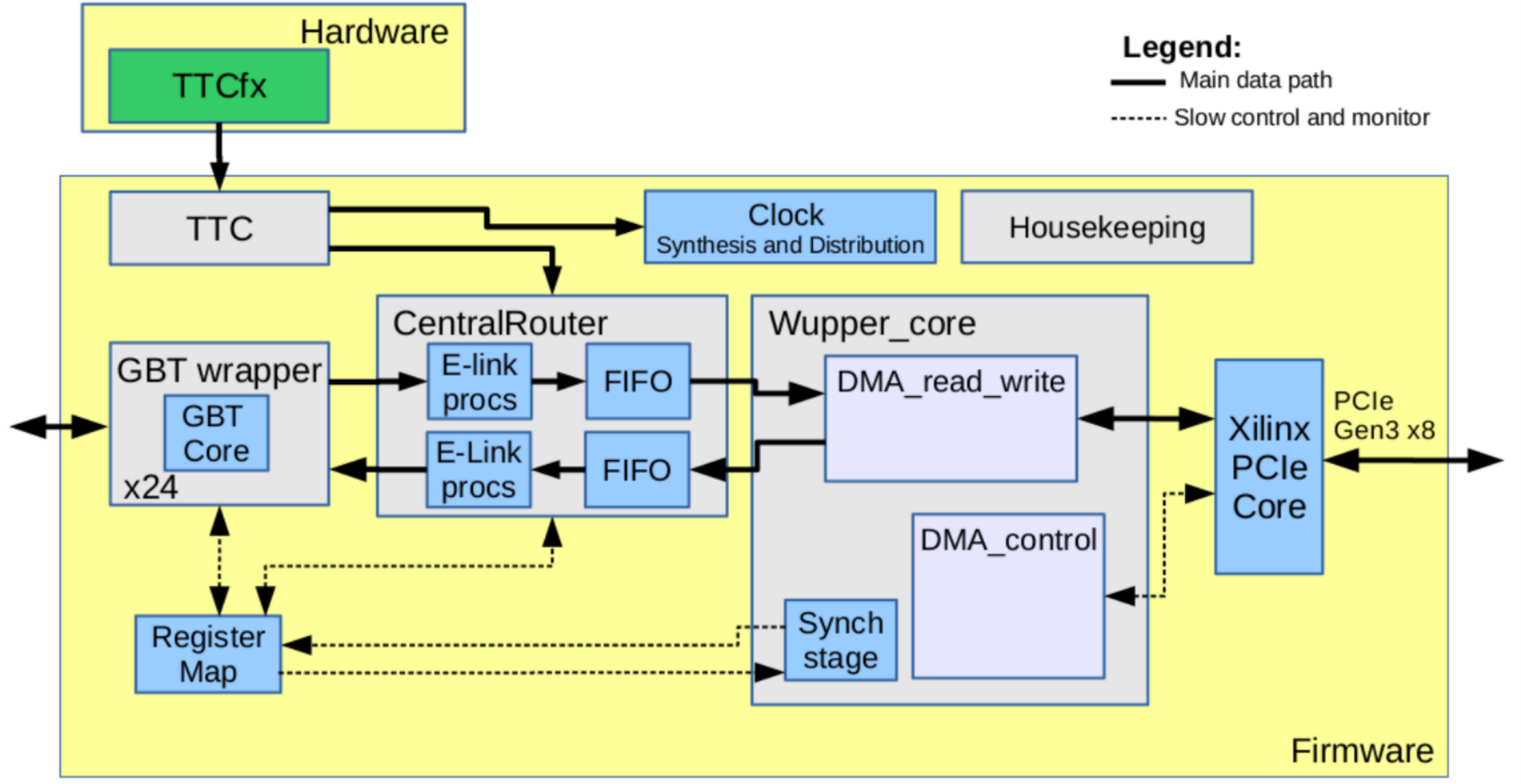
FELIX GOALS

- Read out 1 APA of ProtoDUNE
- interface with rest of electonics and DAQ
- *without* major disturbance to DAQ developments
- Part of a general DAQ R&D plan for ProtoDUNE

FELIX HARDWARE

- FLX-709,710,711
- up to 48 duplex optical links
- PCIe Gen3 x16 lanes (≈ 100 Gb/s)
- Onboard DDR4 up to 16 GB
- **GBT for front-end communication**
- **TTC receiver**

FELIX FIRMWARE



GBT PROTOCOL

- 4.8 Gb/s line rate
- 3.28 Gb/s with Forward Error Correction
- 4.48 Gb/s data rate without FEC
- Requires a GBT-capable chip on the WIB
  - most likely an FPGA
  - example firmwares exist but may require some modification
- To use another protocol would require significant changes to FELIX FW code
- Future line rates expected ~10 Gb/s
- FELIX requires optical input

TIMING/TRIGGERING

- Protocols
  - FELIX is designed to use TTC (CERN)
  - White Rabbit is under development
    - Therefore FW is already modular
  - Another simple protocol with clock and trigger is likely feasible in a relatively short timeframe (months) (à la Nova).
    - possibly requires a new FMC input
    - requires agreement with FELIX developers
- Distribution
  - For 35 t, RCEs distributed clock to Front-End
  - FELIX could perhaps do the same
  - What if distribution is separate?
    - sent to both WIB/FE and FELIX

DATA FORMATS

- Does the data from the WIB need to be modified by FELIX for artDAQ?
  - Aggregation?
  - Event building?
- Or does it simply require another artDAQ board reader?
  - Under investigation by PNNL

DETECTOR CONTROL

- FELIX links are bidirectional and can therefore be used for slow control
- How do we expect to configure the WIB?
  - Same WIB FPGA or another board?
- Can FELIX also be used for this?
- Again would require GBT

FELIX LAYOUT

- Ideal case with FELIX
- Used for both DAQ and Slow Control