(Proto-)Dune WiB based on SBND

E. Hazen with content plagiarized at the last-minute from others :)

Overview of SBND-based WI

- Small crate on flange with WiB and PTC
- DC power converted on WiB with bypass option
- Arria-V FPGA handles data from (4) cold FEMB
  - Data multiplexed at least 2:1, up to 8:1
- Slow control handled by same FPGA
- Clock / control on two pairs/fibers distributed in crate
- Substantial local DAQ / diagnostics accessible via GbE

Background from Jack Fried

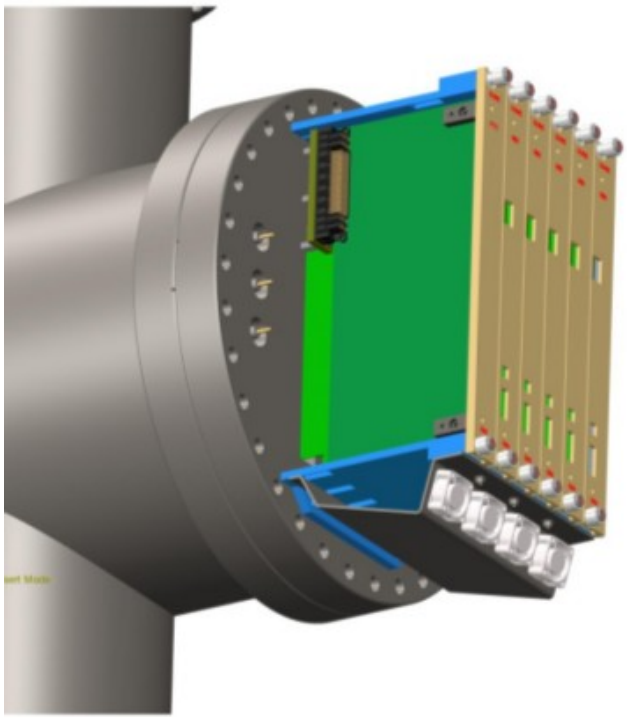
Proposed ProtoDUNE Warm Interface based on SBND

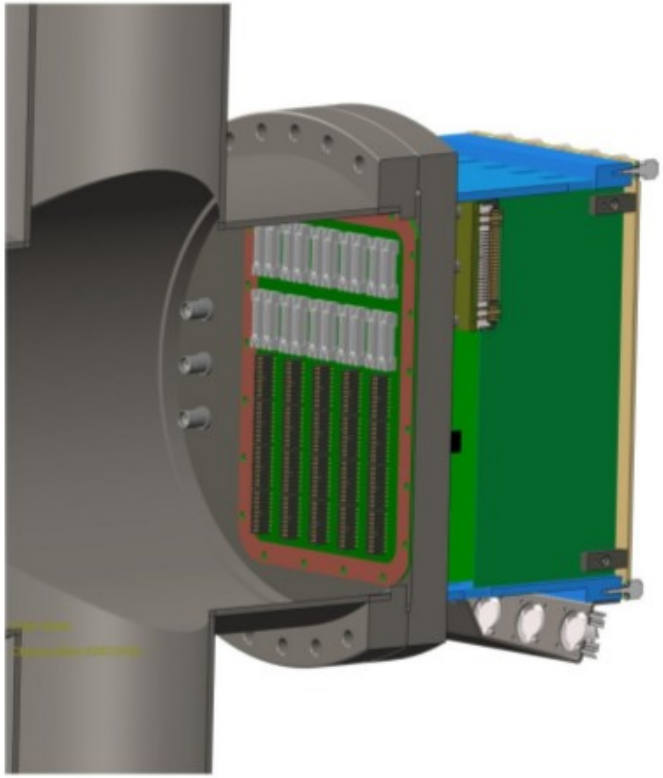
See Jack's talk for further detail:

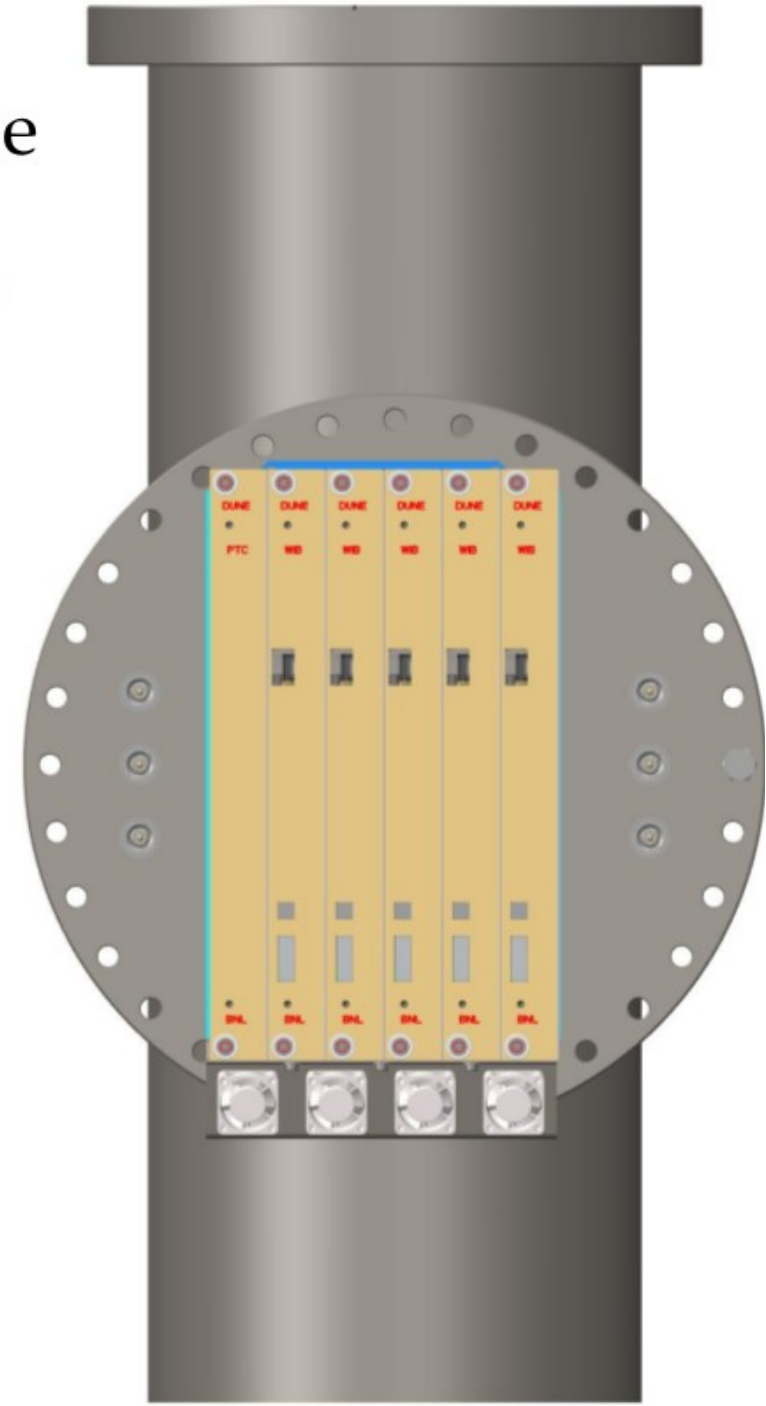
https://indico.fnal.gov/getFile.py/access?contribId=4&resId=0&materialId=slides&confId=11578

ProtoDUNE Warm Interface Electronics

- The 12 inch flange will reduced the size of the Warm Electronics Crate so that only five WIB's will be used per flange
  - SBND has a 14" flange with 6 WIB's

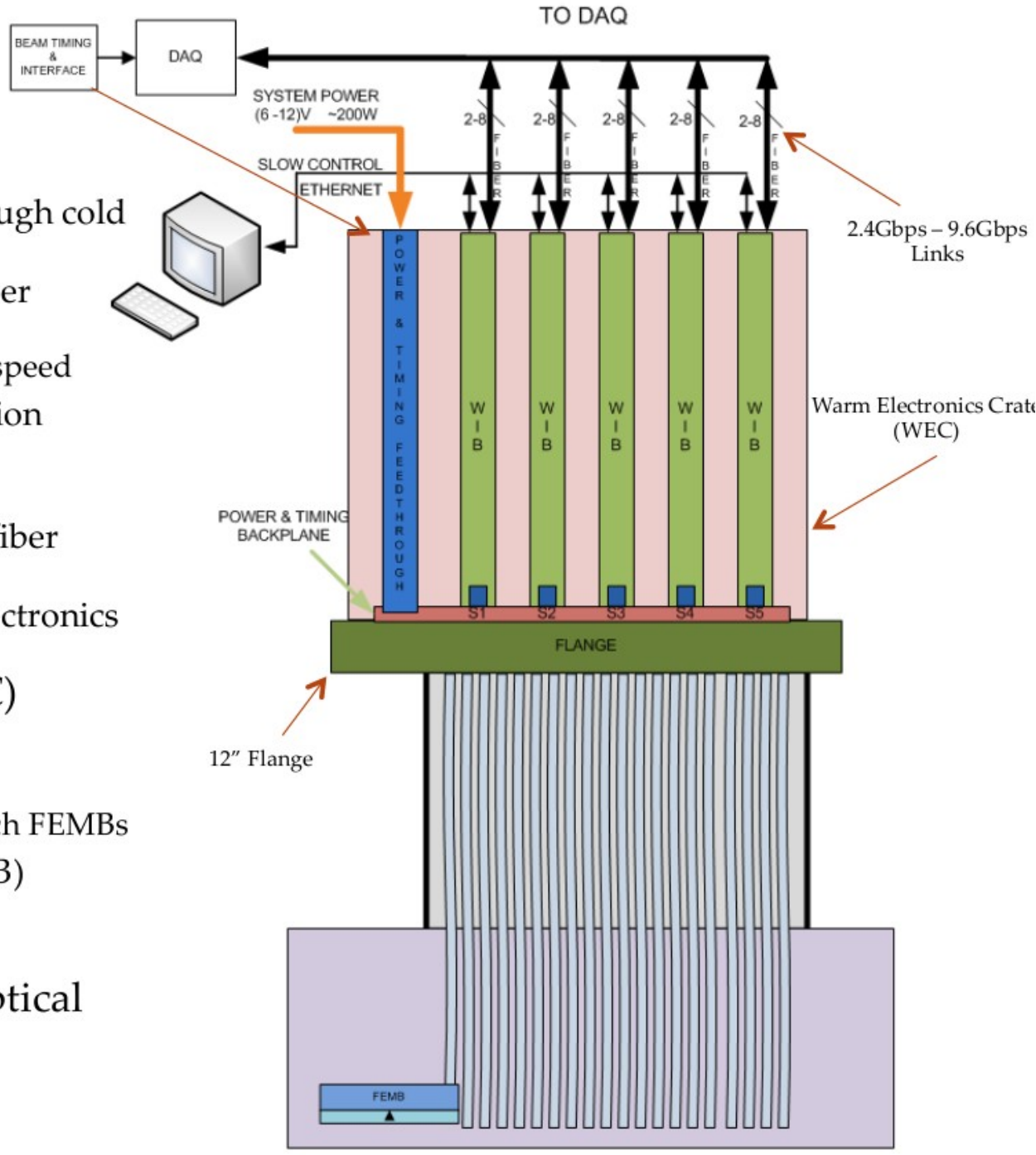






Proposed ProtoDUNE Warm Interface Electronics

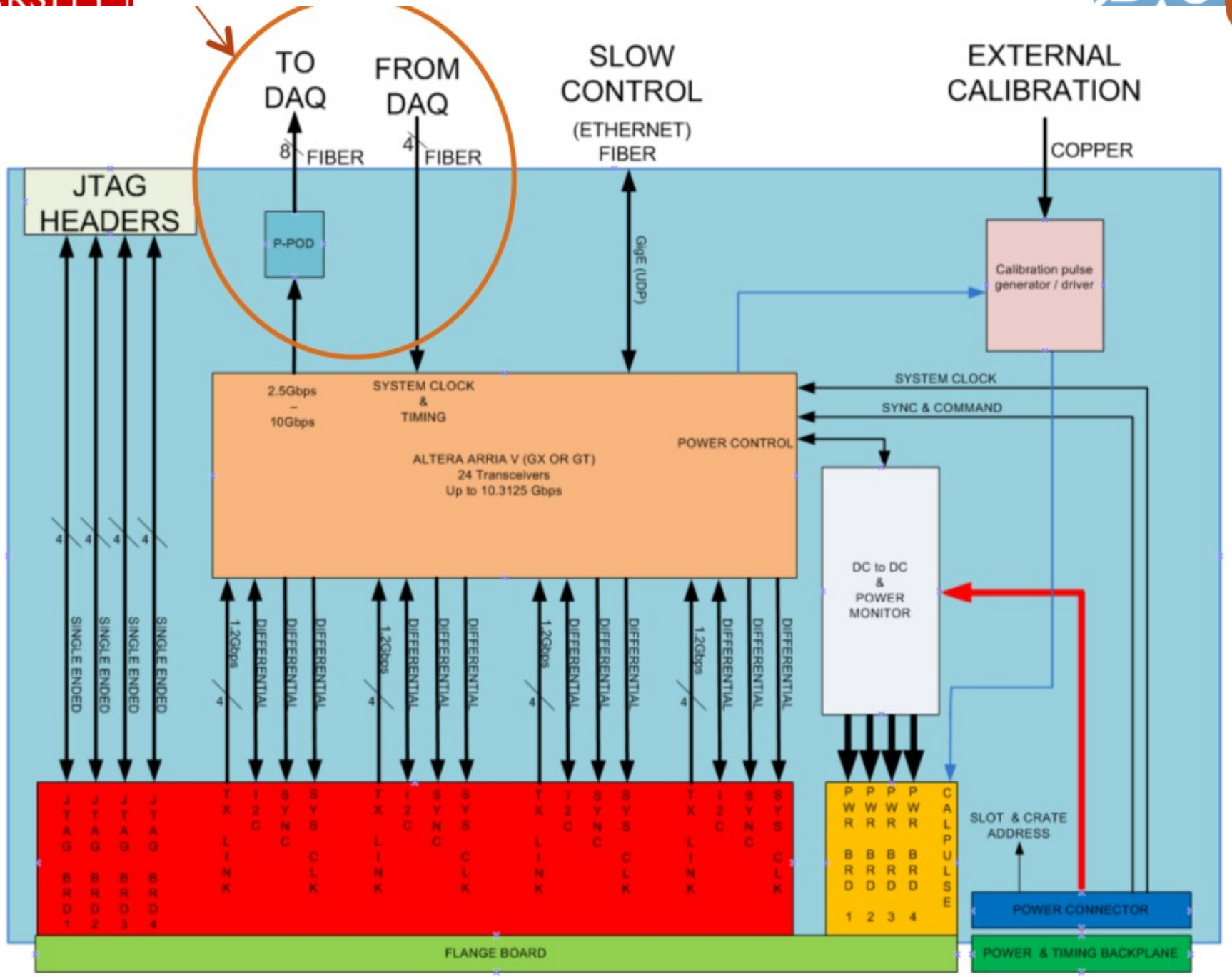
- Warm interface electronics will be installed flange board
  - Receive data from cold electronics through cold cables
  - Send data to ProtoDUNE DAQ over fiber optical links
    - Two to eight links depending on link speed
  - Receive system clock and synchronization signals form DAQ over fiber links
    - (PTC or WIB)
  - Interface to slow control system using fiber GIG-E
  - Manage power and control for cold electronics
- Each Warm Electronics Crate (WEC) contains the following
  - Five Warm Interface Boards (WIB)
    - Each WIB will control up to four 128-ch FEMBs
  - One Power and Timing back plane (PTB)
  - One Power and Timing Card (PTC)
- WEC is a faraday cage with only optical signals going in and out



Warm Interface Board (WIB)

- The WIB can control up to 4 cold FPGA boards, signals for each FEMB include
  - Four 1.20Gbps receiver links
  - One set of differential I2C* links
  - One differential system clock
  - One differential SYNC/CONTROL link
  - One set of FPGA JTAG signals (single ended)
    - FPGA can be reprogrammed for two pairs of differential signals
- Can send data to the DAQ over high speed links with speeds ranging from 2.4Gbps to 10.3125 Gbps
- Can receive up to two high speed serial links and two clock links from DAQ
  - This can serve as communication channels to control system
- Communicates to the control system through a Gigabit Ethernet link using UDP
  - This will be used as the diagnostic tool

Proposed ProtoDUNE WiB Block Diagram



WiB Key Features

- Flexible DAQ output
  - Multiplexed 2:1 (2.4Gb/s), 4:1 (4.8Gb/s), 8:1 (9.6)
  - 10 GbE (UDP)
- Built-in “local DAQ” and diagnostic features
  - Can read out without any additional DAQ
- DC power converted on board
  - Jumper option to bypass for external DC inputs
- Re-use existing SBND engineering
  - as it seems to already meet DUNE requirements

Additional system features

- Clock / controls distribution using point-to-point fanout with COTS clock chips
  - Two inputs for clock, encoded controls using directly the COLDATA protocol
- Power distributed via backplane, DC/DC converters on WiB

Status / Plans

- ProtoDUNE WiB / PTB / PTC adapted from SBND design well underway
- Design being kept very close / identical between SBND and ProtoDUNE
- SBND test stand expected late spring 2016
- Boston U is starting on FPGA design for ProtoDUNE version
  - Intention is to accommodate various DAQ options:
    - RCE
    - FELIX
    - Local DAQ via GbE for diagnostics / testing

Concerns / Open Issues

- Clock system is a moving target
  - Current WiB expects COLDATA clock and control to be delivered on two fibers/pairs, without going through FPGA. Anything more complicated requires some careful thought to avoid adding jitter
- Cable equalization (if needed)
  - Must be treated at the system level as the analog design problem it is. This is not a “management level” decision, but requires some actual engineering.
- If this WiB is to talk to the RCE...
  - We need to get engineers together soon to work out low-level details (FELIX I am less concerned about)