Overview of SLAC/UCD WIB

Hans Berns
for the UC Davis & SLAC groups
April 21, 2016

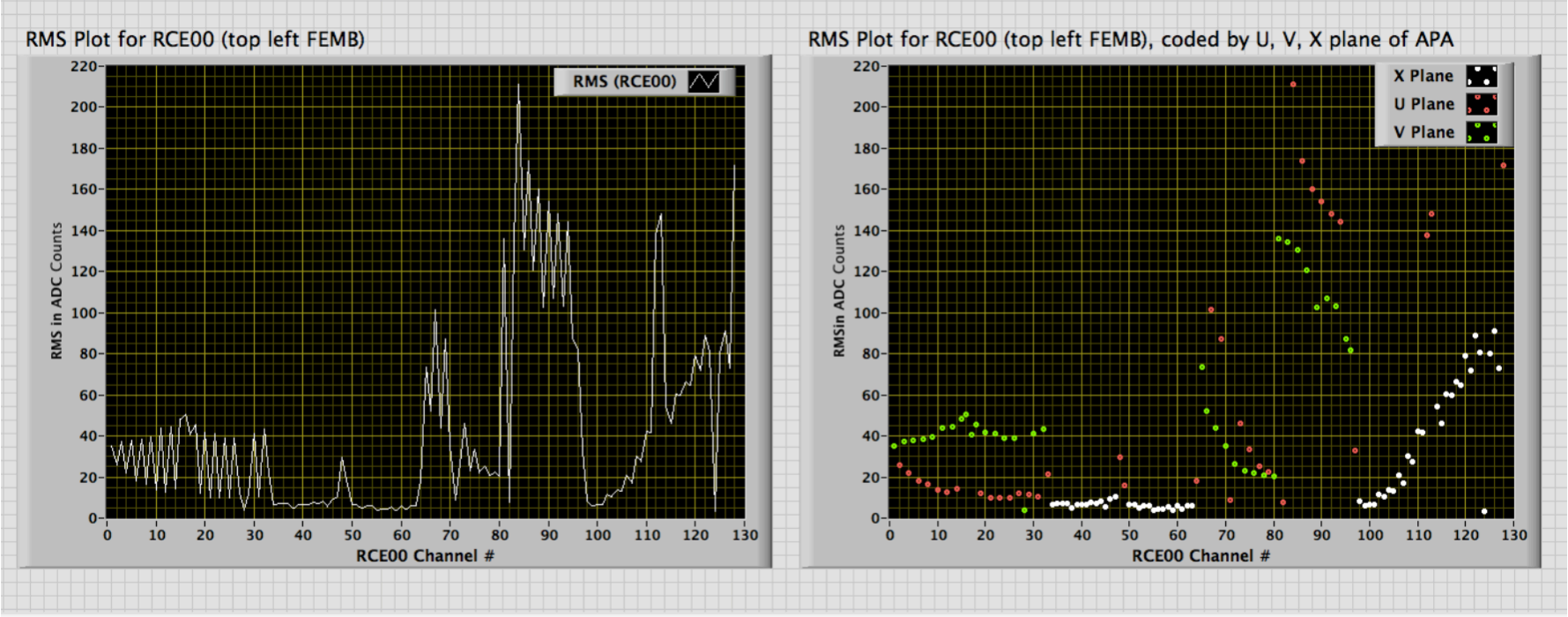
Considerations

- **Noise**: WIB connects the TPC to the potentially nasty outside environment
  - Move potential noise sources such as DC power supplies and FPGAs off of the flange
  - Optimize ground connections for low noise
- **Simplicity**: high MTBF and longevity are important
  - Make use of RCE capabilities to reduce complexity at the flange
  - Reduce power consumption at the flange to allow passive cooling
- **Flexibility**: can support many potential upgrades/changes
  - Make use of powerful RCE firmware/software development environment to enable
- **Support**: groups committed to install, commission, and maintain

Noise

- Noise (especially coherent noise) has been a problem in liquid argon TPC's (certainly true in mini-CAPTAIN and 35-ton)

e.g. see A.Hahn 35-ton talk DUNE Collaboration Meeting 15 April)

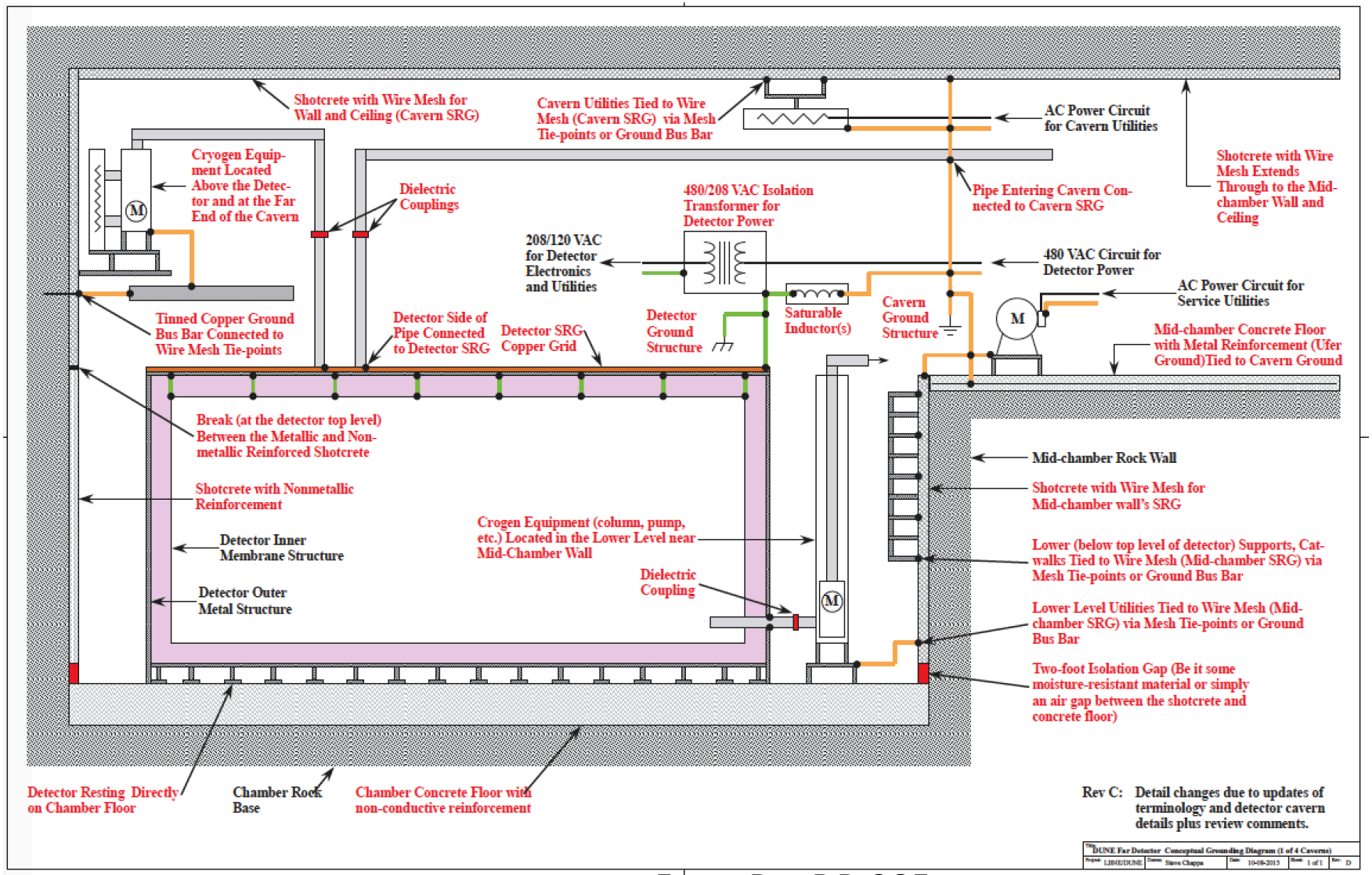


Noise Considerations

- Noise environment difficult to predict or anticipate – need path for flexible response
- *Grounding* is very important for noise reduction. The WIB sits at the interface of the Cold Electronics (CE) and outside environment and thus must be designed with noise in mind from the start. This is especially true for DUNE, where self-triggering is required rather than just triggering on a beam crossing or external signal.
- as much as possible, *isolation* of high-speed digital electronics from sensitive analog lines is good practice.

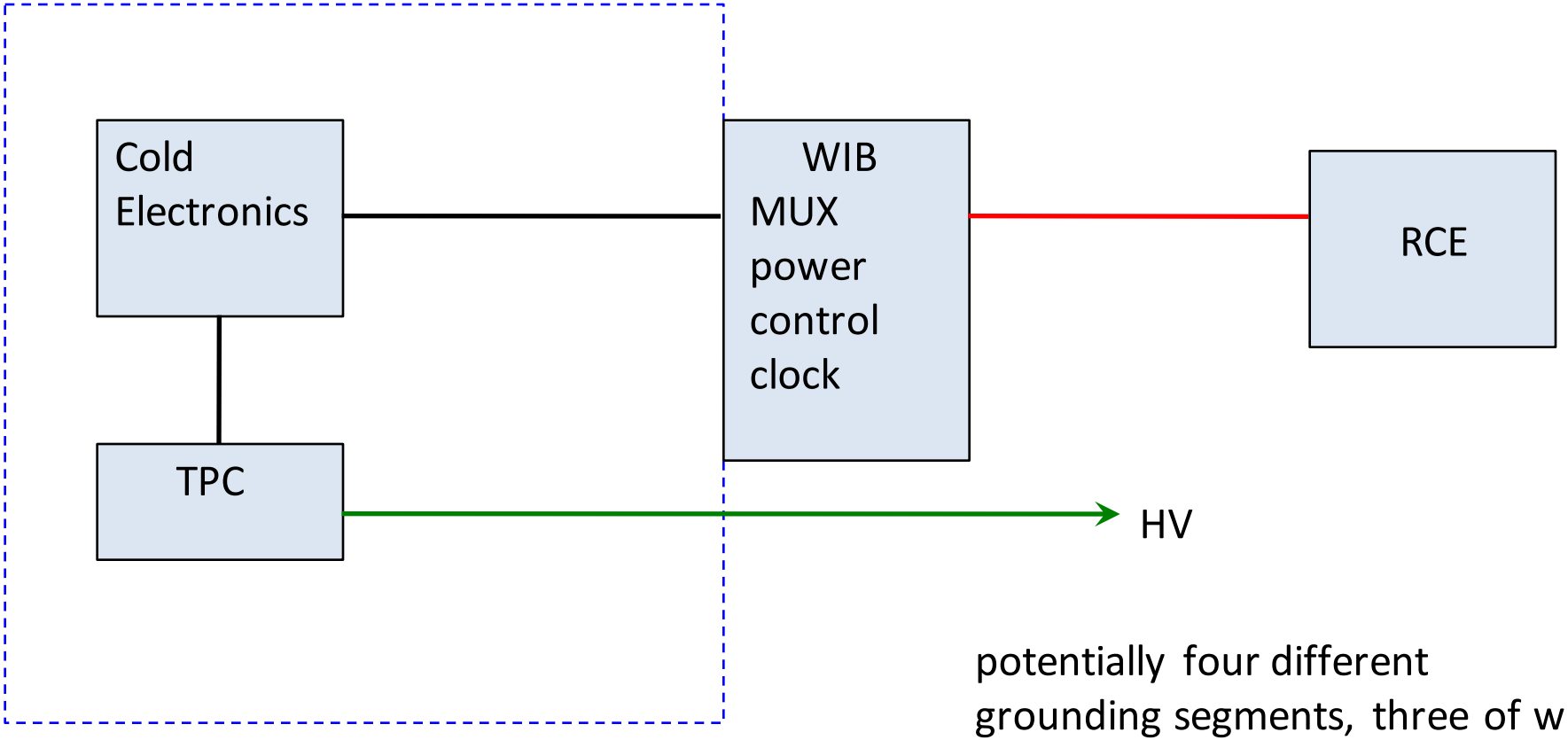
Three separate grounds planned: CAVERN (rock bolts and mesh),
UFER (rebar in concrete floors), DETECTOR (cryostat body) with controlled tie-in points.

What about: internal CE? RCE/FELIX? HV? **WIB is where these all come together**



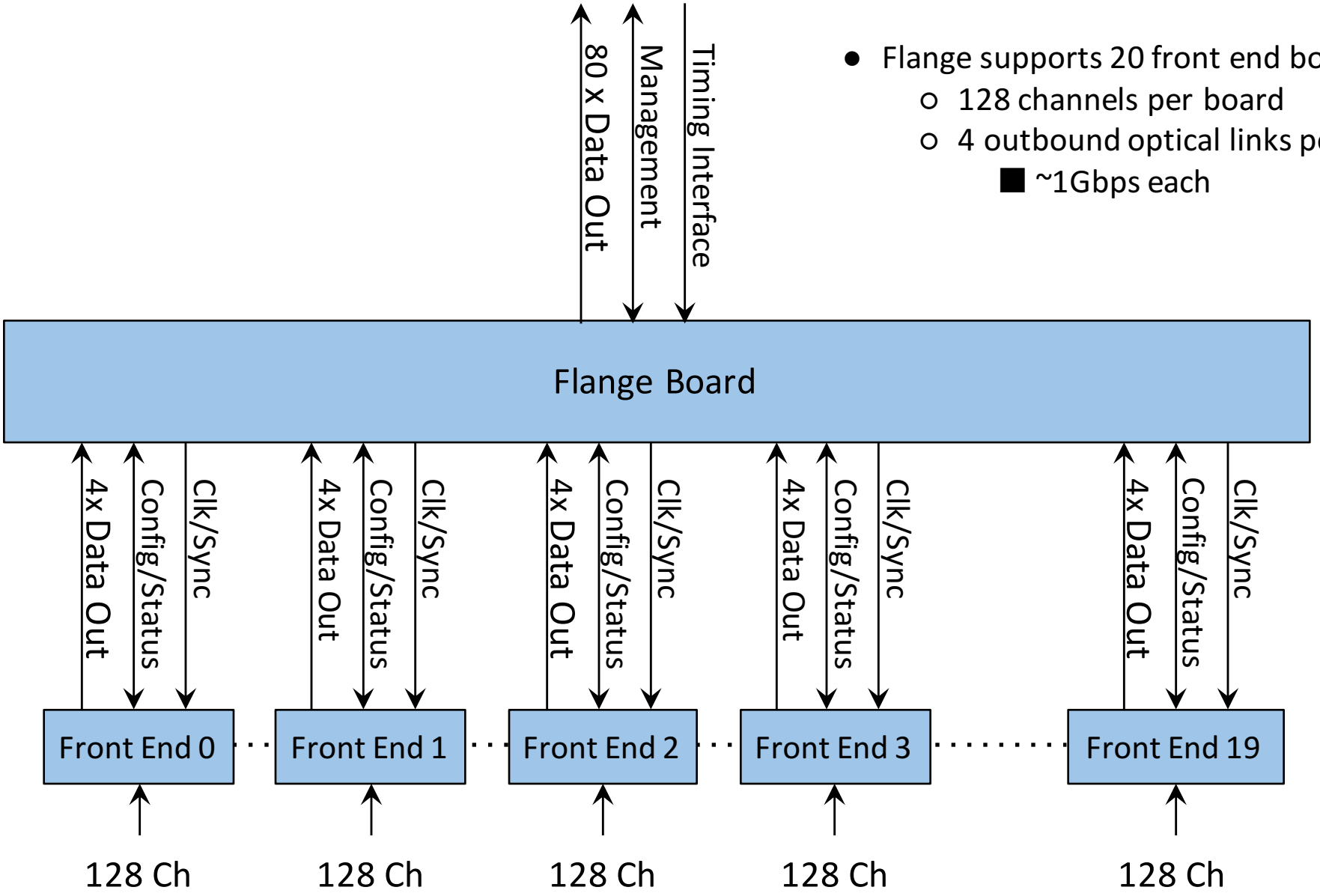
From DocDB-285

WIB/Grounding Concept



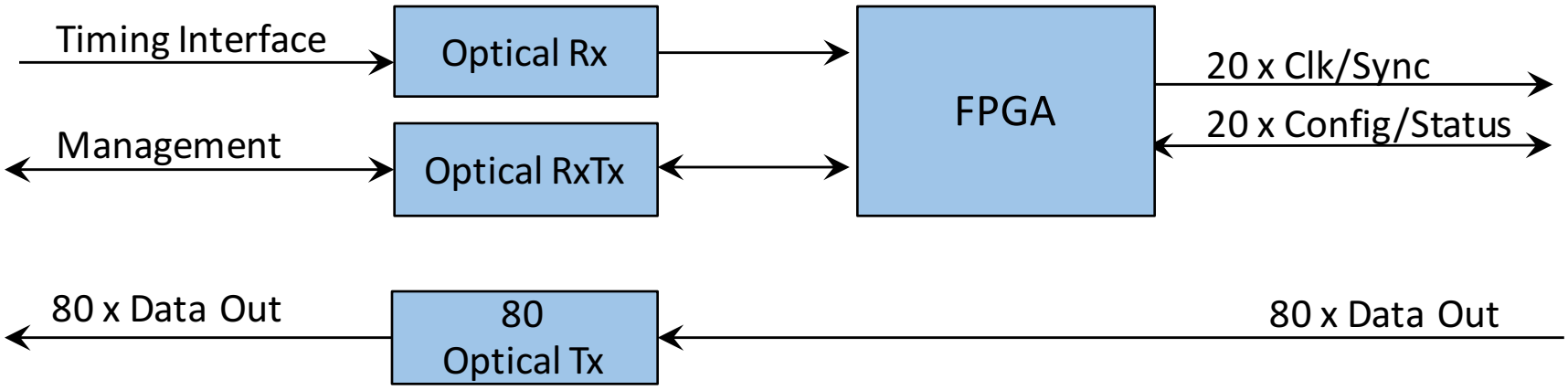
potentially four different grounding segments, three of which will go through WIB. What is the best way to handle this? How to ensure flexible for environments that may be encountered at LBNF?

Flange Block Diagram - High Level



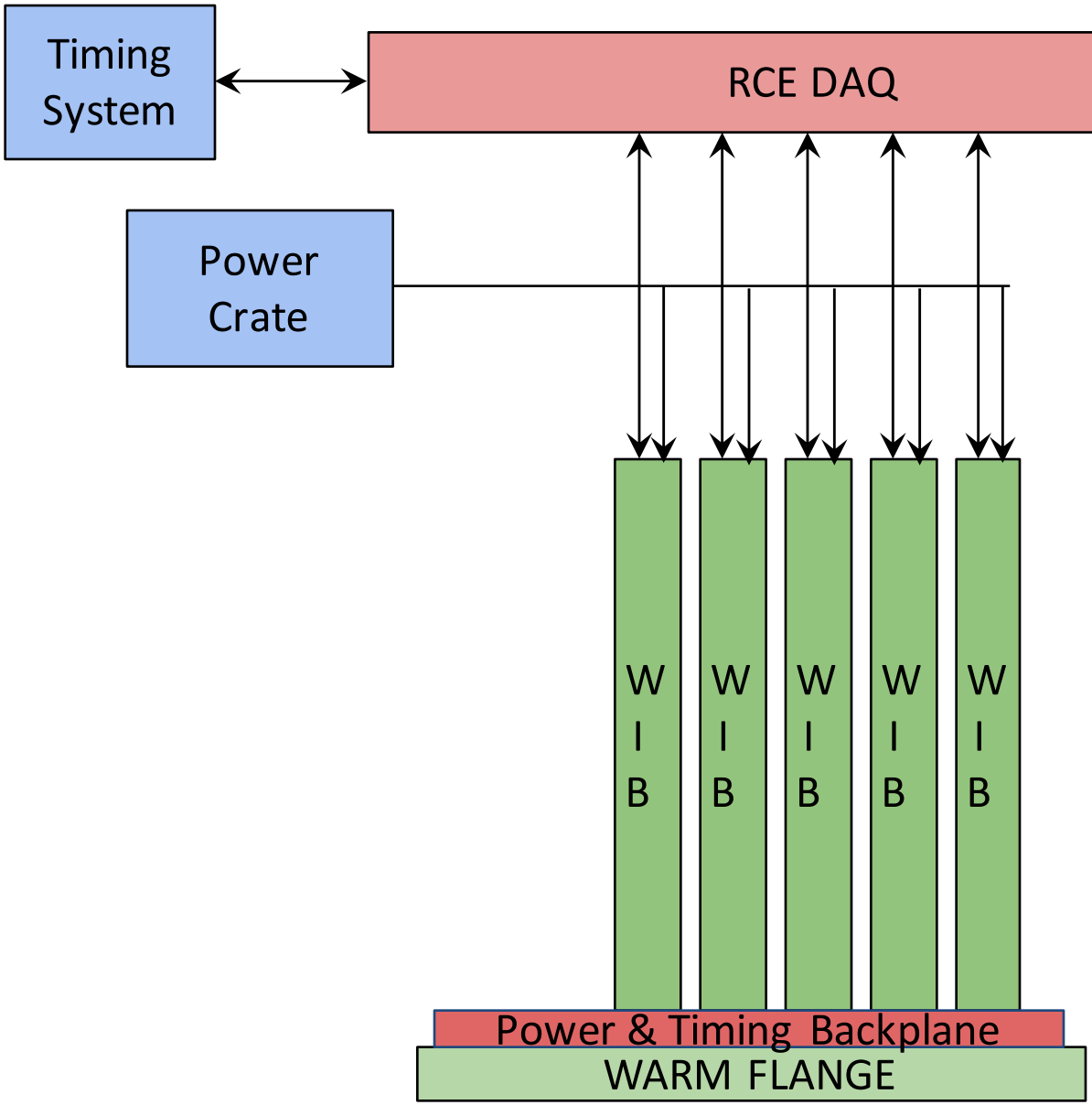
- Flange supports 20 front end boards
  - 128 channels per board
  - 4 outbound optical links per FE
    - ~1Gbps each

Flange Board Block Diagram - Generic



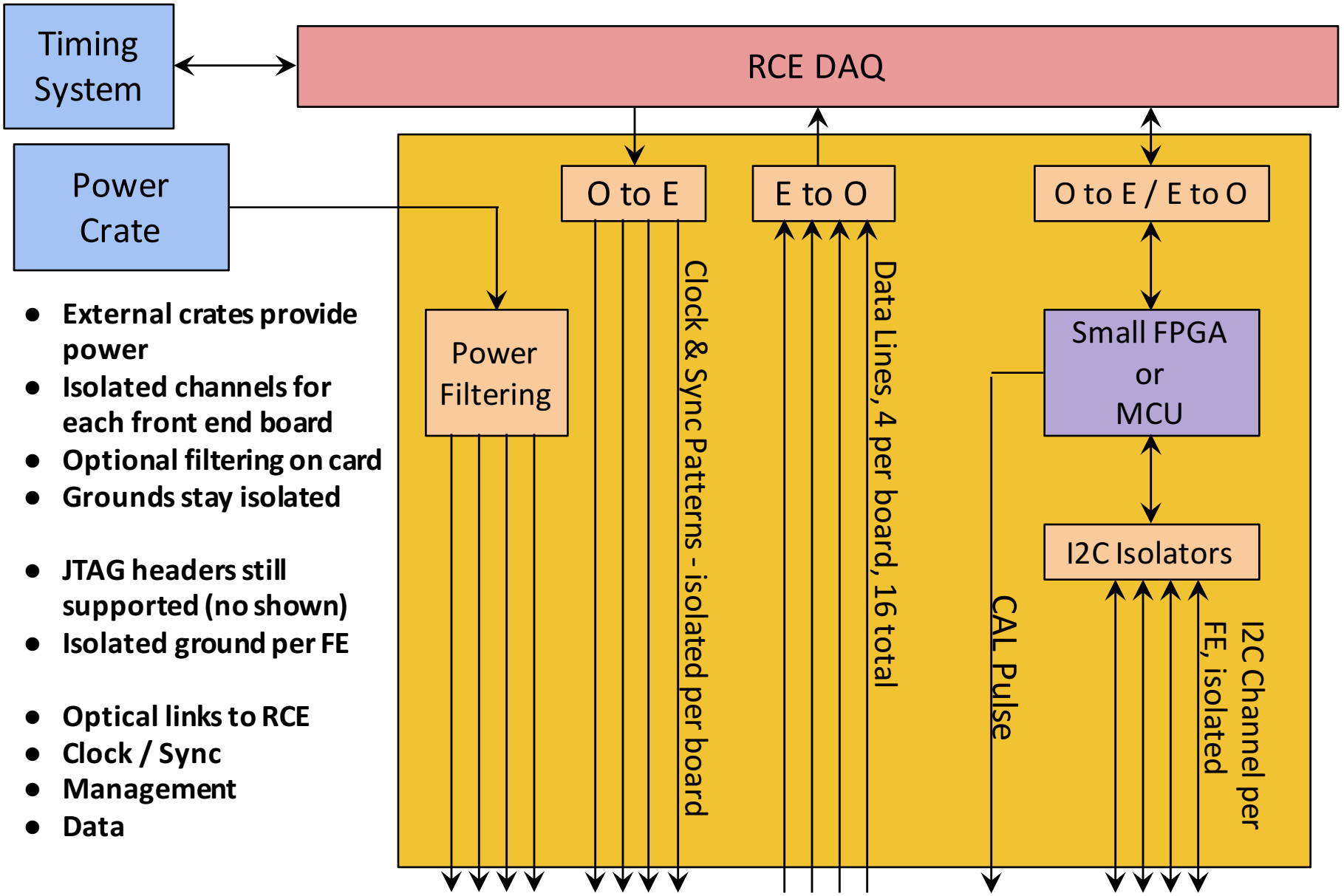
- **Timing interface**
  - Flange FPGA receives timing & sync from external source
  - Can either receive this directly from global timing system or from DAQ nodes
  - FPGA converts this interface to clock, reset & sync signals required by front end ASICs
- **Management Interface**
  - FPGA serves as a bridge between external system management and front end ASICs
  - Can either be connected to external run control layer or to DAQ nodes
    - Ethernet with UDP is a potential protocol
    - Register access and command processing
  - Assume single interface per front end board
    - Most likely I2C
- **Data interface**
  - FPGA is not in the data path
  - Front end ASIC data streams converted to optical and sent to DAQ nodes
    - Low cost 12 channel transmitters can be used (7 total)

Utilizing BNL Crate Based System



- Utilizes the crate design by BNL
- PTC card not needed
- Davis designs WIB

Proposed WIB Board



- **External crates provide power**
- **Isolated channels for each front end board**
- **Optional filtering on card**
- **Grounds stay isolated**

- **JTAG headers still supported (no shown)**
- **Isolated ground per FE**

- **Optical links to RCE**
- **Clock / Sync**
- **Management**
- **Data**

Differences From BNL WIB

- **No local power conversion**
  - External power crate provides isolated power channels which pass through to front end board
  - Ensures ground isolation
  - Optional local filtering to handle penetration into faraday cage (crate)
  - One channel for local devices
- **FPGA function limited to handling I2C and cal pulse**
  - Can be turned off during operation to debug noise
- **Lower power dissipation**
  - Removes need for fans
- **All digital signals to/from front ends should be ground isolated**
  - I2C channels will use isolators
  - All other signals are naturally isolated
  - Assumes backplane and penetration will support this
- **Ability to adjust system grounding on flange will ensure flexibility when debugging noise**
  - Ground loops are tricky
  - Grounding is best left flexible!

Proposal

- UCD will work with SLAC and BNL to design a noise hard WIB according to requirements anticipated for DUNE
- Prototype board to be produced that can be tested at proto-DUNE. Note: beam data not necessary for this commissioning test and this could be done during long shutdown.
- Iterate on this design with consideration of final DUNE DAQ configuration and grounding scheme.

- In addition, UCD will work with SLAC on RCE software for proto-DUNE and commit to having full-time onsite support at CERN for proto-DUNE commissioning and operation, plus testing of WIB when ready