

Upgrade of the ATLAS Monitored Drift Tube Electronics for the HL-LHC

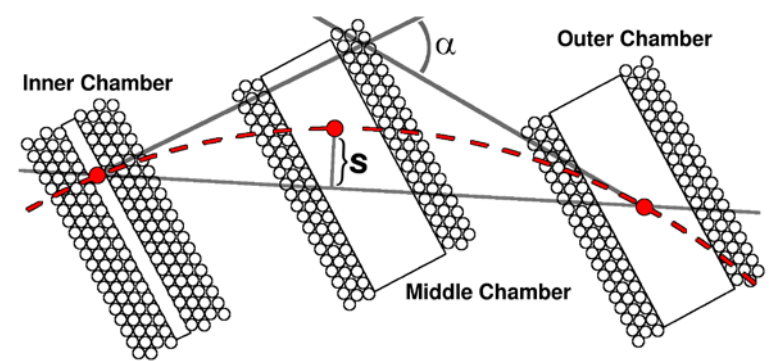
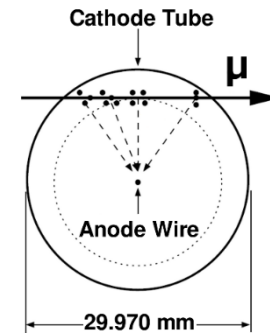
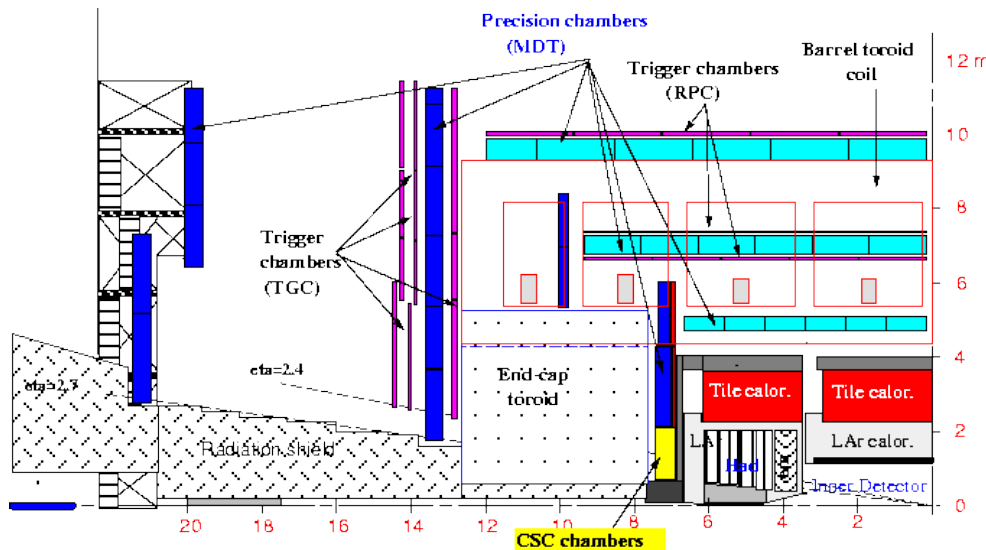
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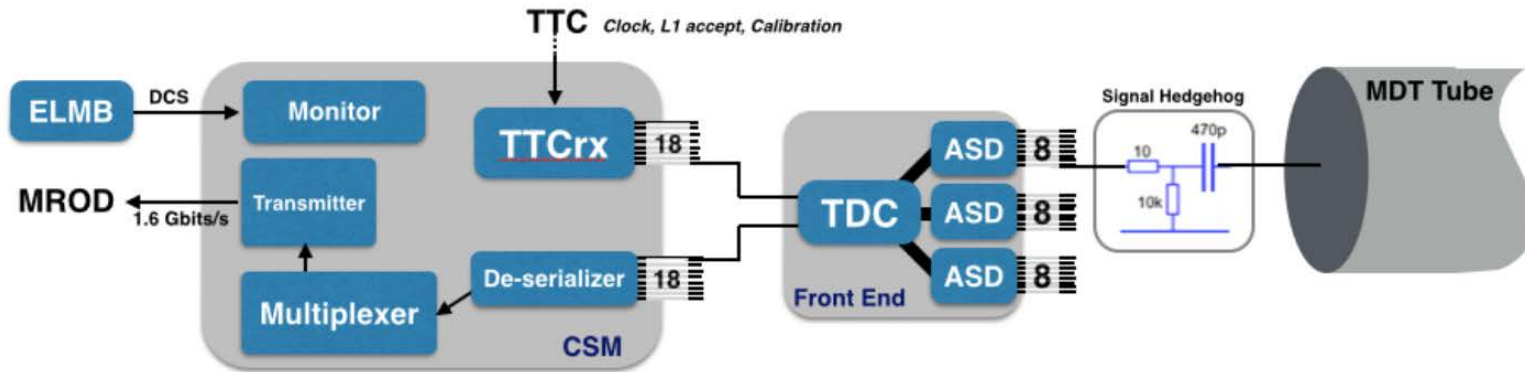
ATLAS MDT detector

- ATLAS muon spectrometer is mainly used for muon triggering, identification and momentum measurement
- Provide a standalone momentum measurement (10% at 1 TeV), mainly by the monitored drift tube (MDT) chambers
- 1150 chambers with 354k tubes covering an area of 5500 m²

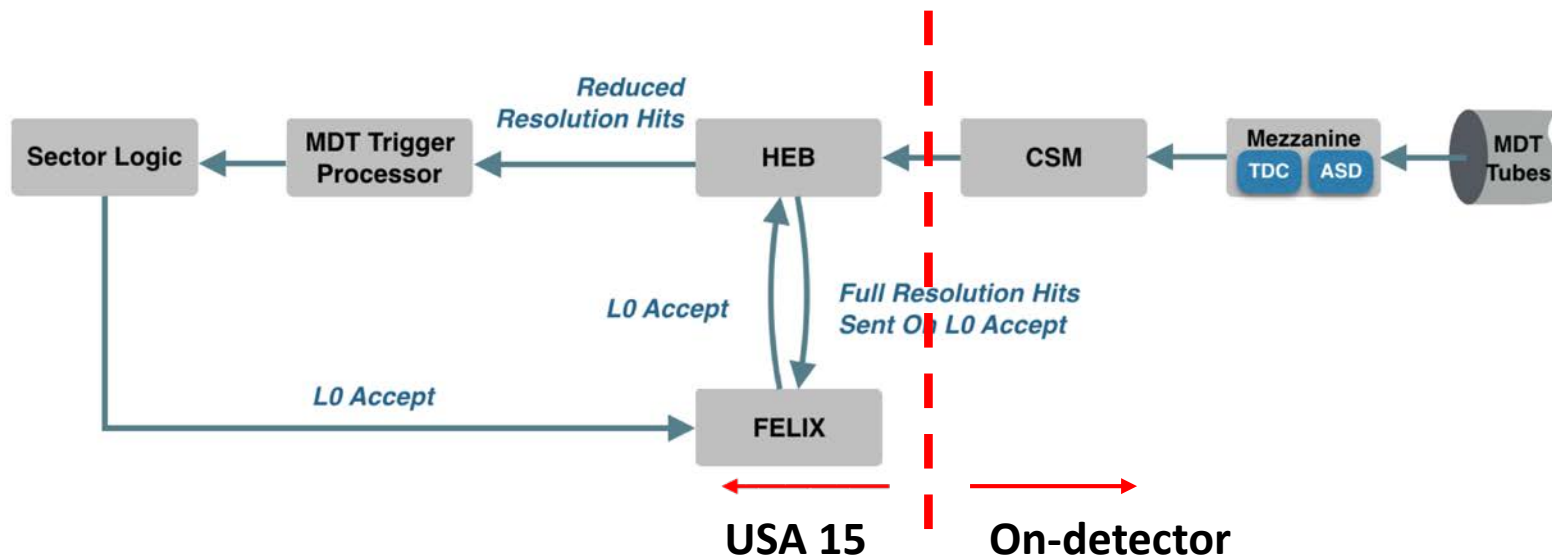


Present and future MDT Frontend Electronics

- MDT is currently only used for precision readout

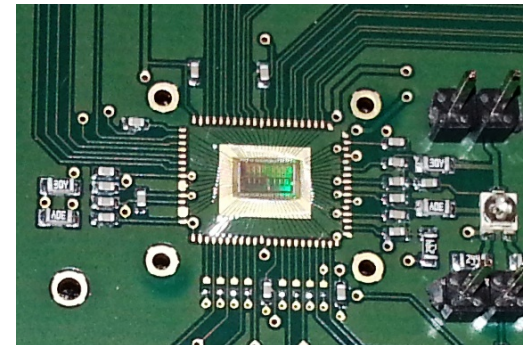
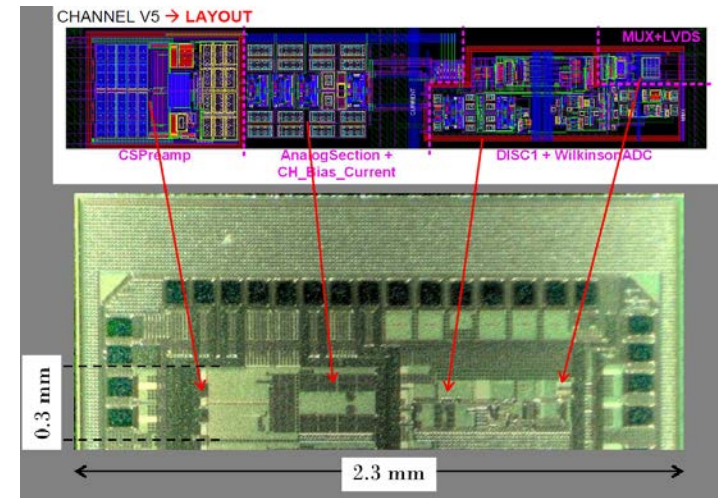
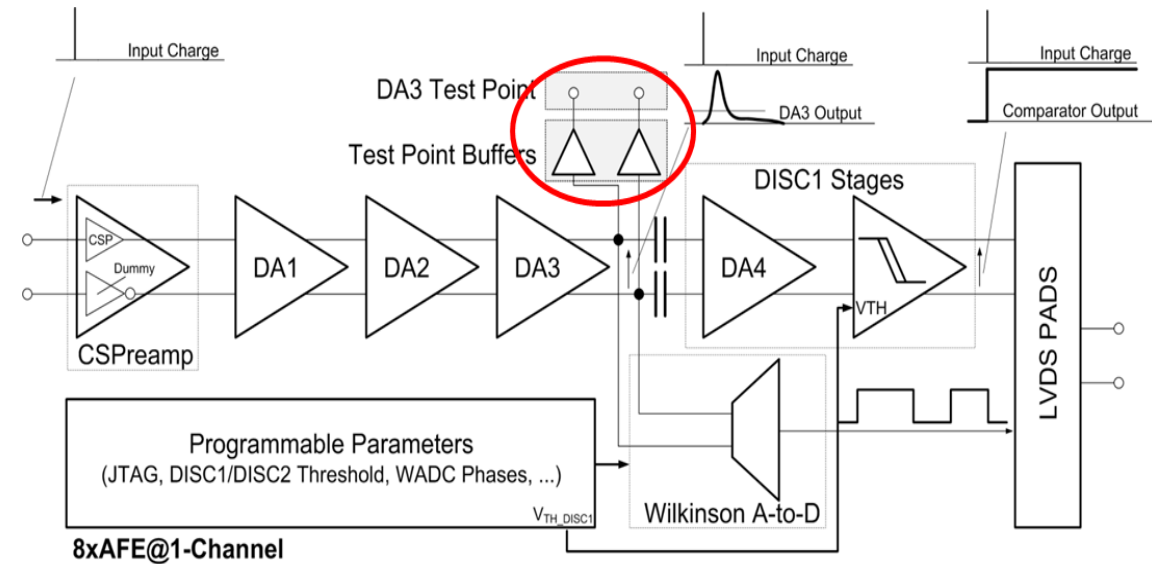


- MDT electronics needs to cope with new proposed ATLAS TDAQ scheme (1 MHz L0 trigger rate with a latency of 10 μ s)
- In addition, MDT will be used at L0 to further sharpen the L0 trigger turn-on curve

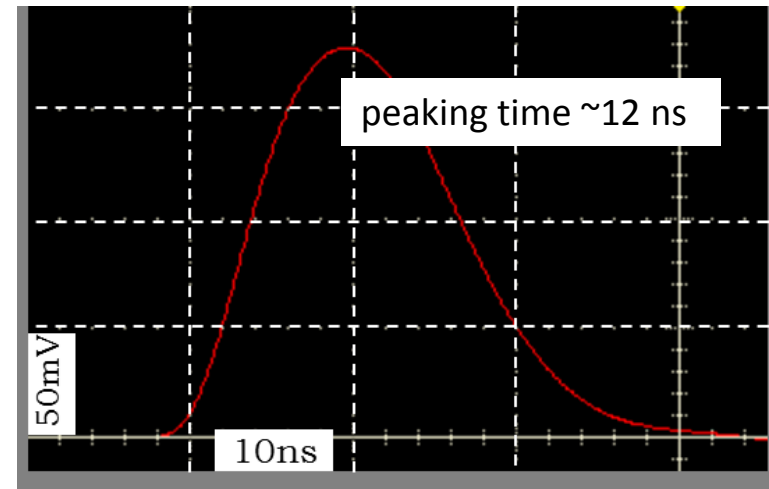
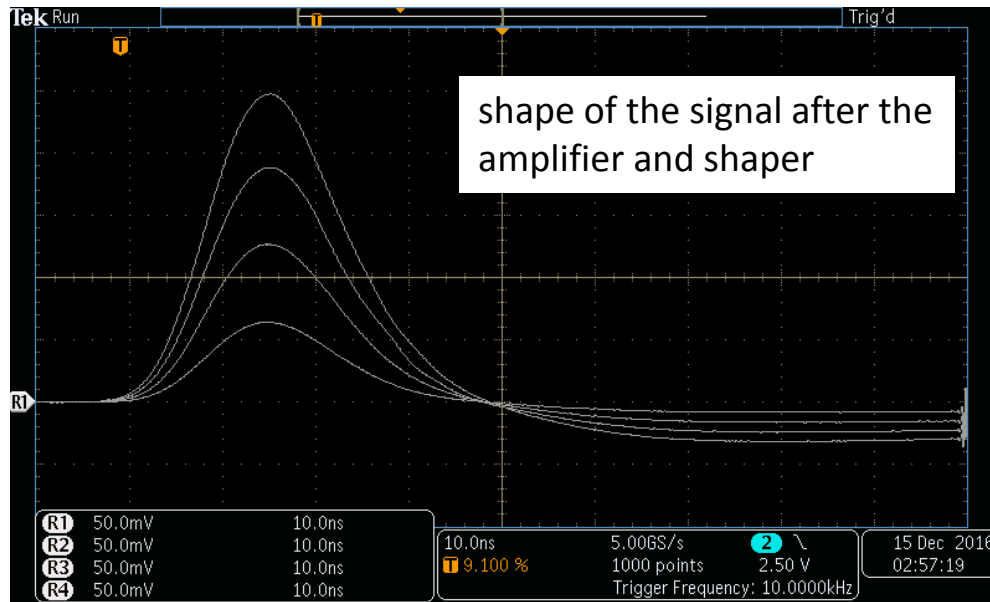


Amplifier-Shaper-Discriminator(ASD)

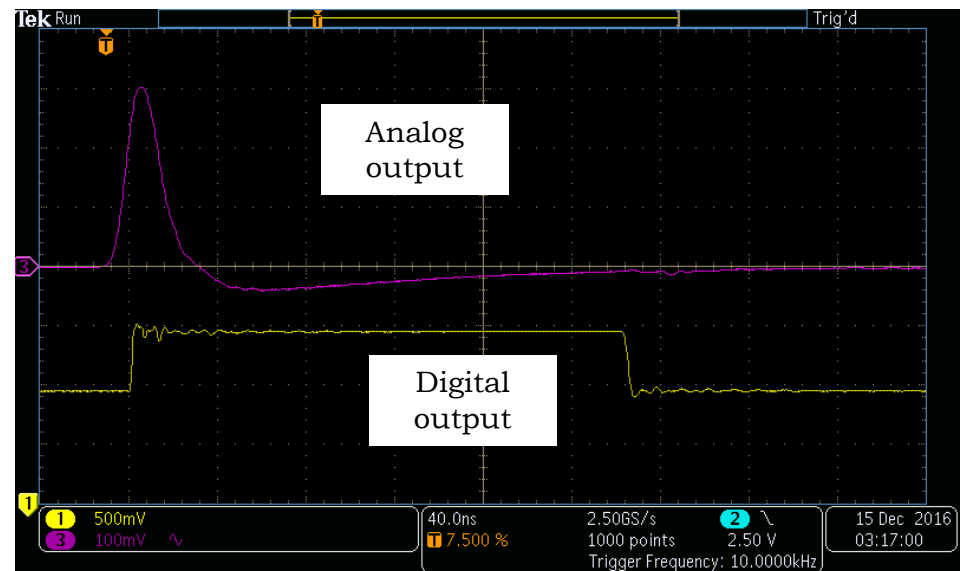
- Similar schematic as the present ASD (500 nm Agilent technology) but using the GF 130 nm CMOS process
- Charge Sensing Preamplifier (CSP) → DA1/DA2/DA3(three shaping stages) → discriminator
- A Wilkinson ADC is used to reduce the dependence of the drift time measurement on the amount of incoming charge
- The silicon area is $2.26 \times 3.38 = 7.6 \text{ mm}^2$



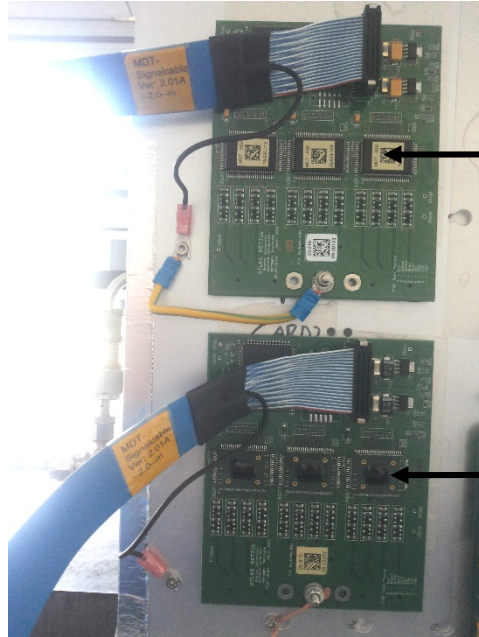
Amplifier-Shaper-Discriminator(ASD)



- Test point waveforms
 - three shaping stages
 - Time and amplitude detail about shaping signal
 - Analog output and reposing digital output



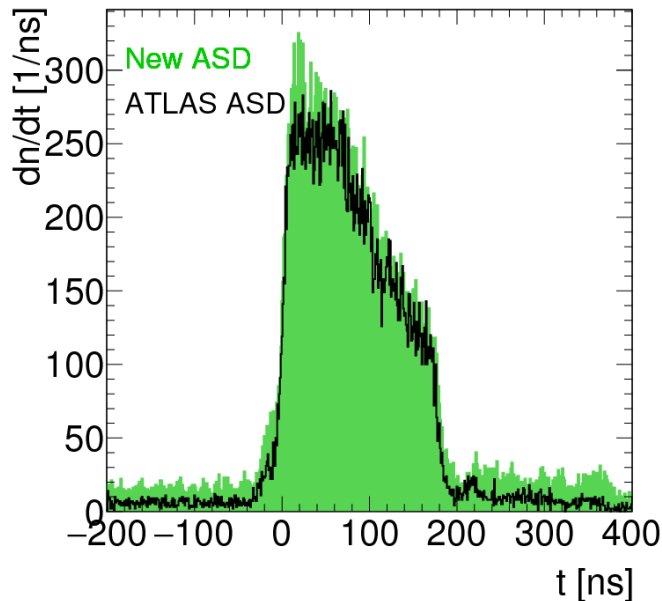
Amplifier-Shaper-Discriminator(ASD)



- Three new ASD chips were put on a mezzanine card for a cosmic-ray test on an sMDT chamber.

ATLAS standard mezzanine card as reference

Mezzanine card with three new ASD chips



- Drift-time spectrum measured with the new ASD chips in excellent agreement with drift-time spectrum measured with ATLAS ASD chips!

A New TDC Design

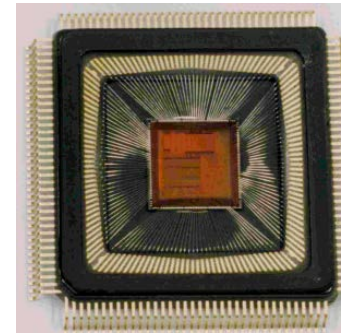
Why a new TDC IS **NEEDED**?

- Previous AMT is no longer available for production
- Output data bandwidth not enough for high rate
- Issues found with the AMT chip

Ref: <https://indico.cern.ch/event/504237/contributions/2138705/>

Develop a new TDC ASIC for the MDT phase II upgrade

- Comparable timing performance (Tubes unchanged)
- Additional features: Triggerless mode + Trigger mode



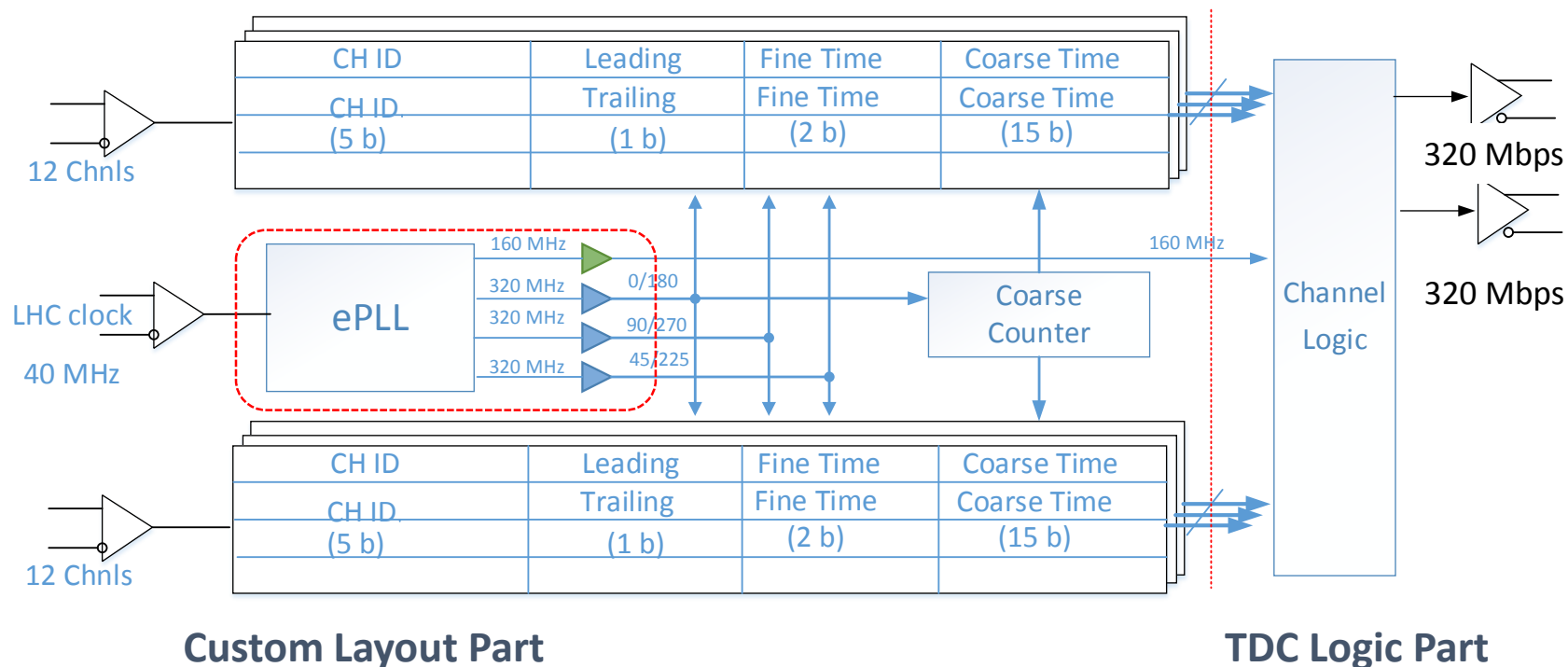
AMT3



UM-TDC v0

Comparison	AMT	MDT-TDC UM
Technology	0.3 μm CMOS Toshiba	0.13 μm CMOS GF
# of channels	24	24
Resolution	0.78 ns	0.78 ns (~ 200 ps)
Dynamic Range	102.4 μs	102.4 μs
Measurement	Rising/falling/TOT	Rising/falling/TOT
Double-hit Resolution	< 10 ns	~ 10 ns
Trigger Mode	Trigger buffer	Triggerless mode + Trigger buffer (early installation)
Output bandwidth	One 80 Mbps line	Two 320 Mbps line

UM TDC v0: Design

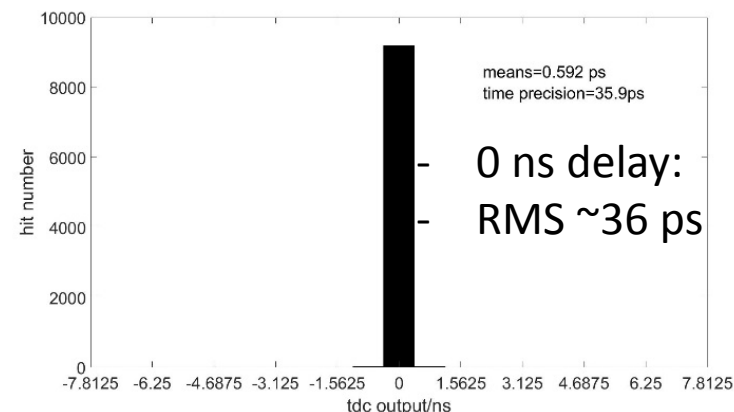
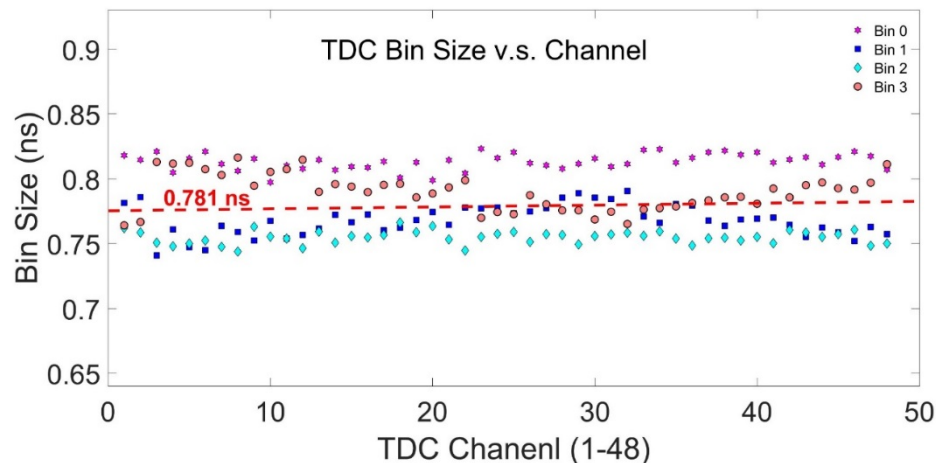
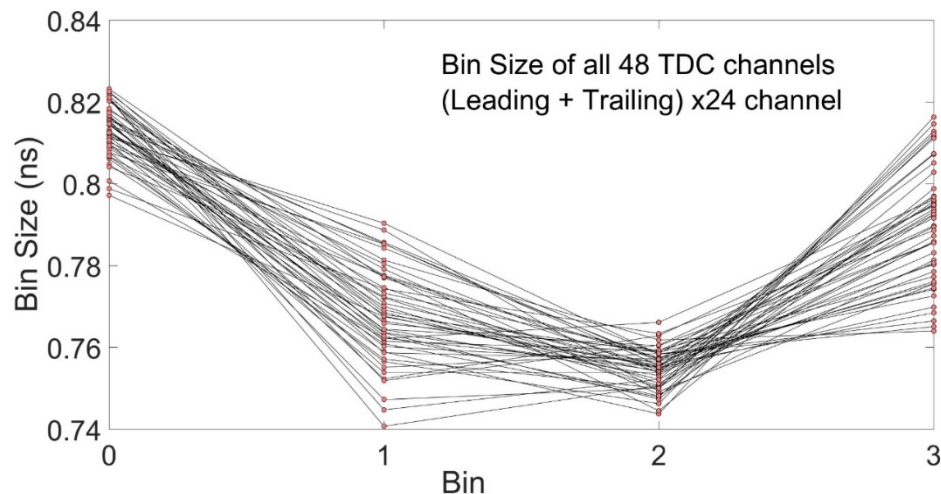


- ❑ It is a demonstration prototype on timing performance, with only triggerless mode.
- ❑ TDC architecture is optimized w.s.t. the timing resolution:
 - Multiple clock phases interpolator** @ 320 MHz: 4 phases of 320 MHz $\Rightarrow 3.125 \text{ ns} / 4 = 0.78 \text{ ns LSB}$
- ❑ Main components:
 - \Rightarrow Generation of multiple clock phases: ePLL (CERN)
 - \Rightarrow Time Digitization: TDC channels (x24 chnl; dual edges)
 - \Rightarrow Time processing/calibration, output serial interface (TDC logic part)

} Custom Layout

Performance of TDC

- Bin sizes for all $24 \times 2 = 48$ channels are within (0.78 ± 0.04) ns
- Integrated and differential non-linearity are less than 5% of the bin size
- Time precision: 0 ns delay, RMS ~ 36 ps;
- Power consumption: ~ 310 mW (TDC fully working).



Chamber Service Module (CSM)

- One Chamber Service Module (CSM) must cover up to 18 new mezzanine boards
- Each new mezzanine boards have two 320Mhz data line
- CSM sends out data to USA-15 using 3 X 4.8Gbps fibers
- CSM get clock, configuration information using a fiber
- CSM sends out the mezzanine boards status like temperature, power supply using a fiber



FPGA-based

Advantages

- Flexibility
- Uniform hardware design
- Can easily handle migration from Phase I triggered mode to phase II trigger-less
- Talk with old mezzanine that cannot be replaced in Phase II

Design Complications

- Uncertainty about FPGA SEU performance in Phase II
- Maintenance needed for firmware

GBTx-based

Advantages

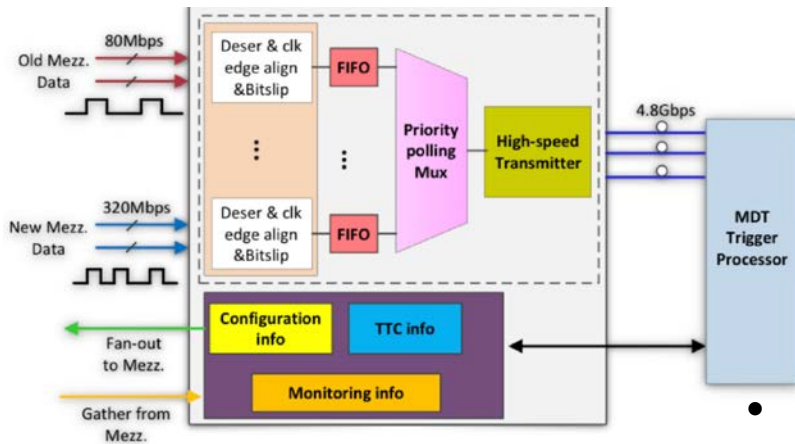
- Low cost, low power
- radiation hard ASIC's from CERN
- No firmware design/maintenance

Design Complications

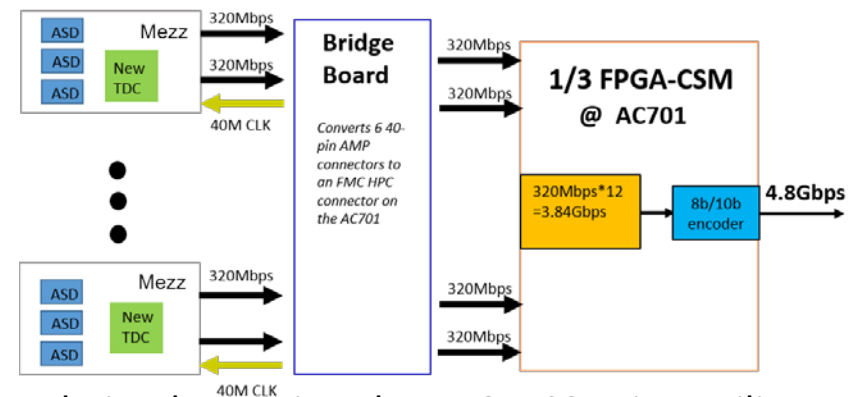
- Functionality fixed by GBTx chipset
- Small additional chip needed for JTAG distribution

FPGA-based CSM Demonstrator

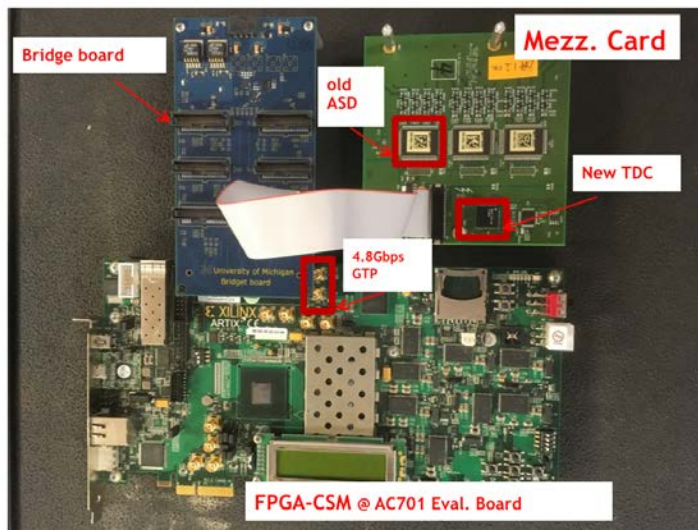
Using priority format fifo



Using multiplexing algorithm based on GBTx wide-frame mode

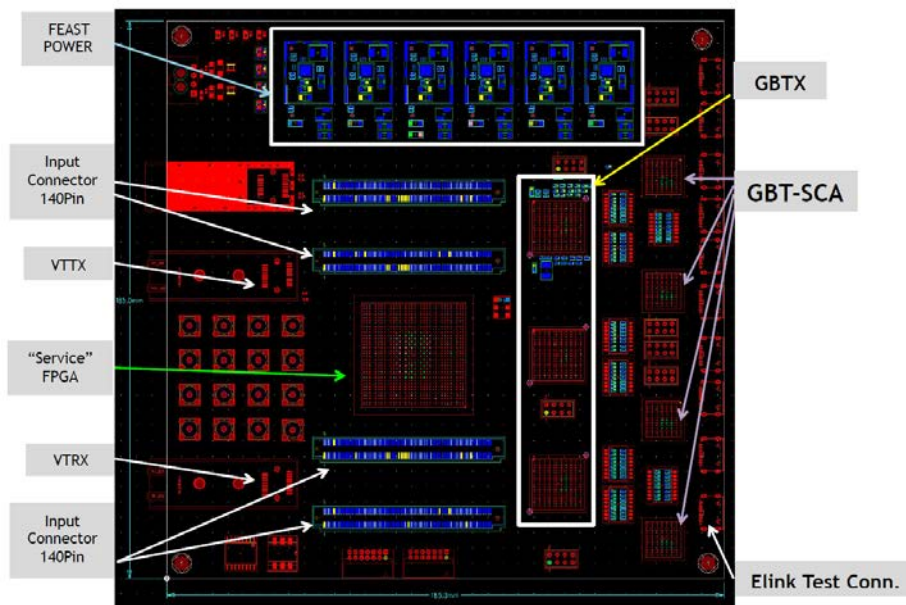


- Currently implementing the FPGA-CSM in a Xilinx AC701 evaluation board with a 4.8Gbps GTP
- Current R&D is focused on interfacing the FPGA-CSM with a new hybrid mezzanine card which pairs the old ASD with the new TDC. The hybrid card was built & tested by Boston University and the University of Arizona.
- One AC701 can handle 6 mezzanine cards - 12 TDC channels @ 320 Mbps. Successfully interfaced three mezzanine with the new TDC to the FPGA-based CSM
- Developing fpga –based CSM using on priority format fifo
- Developing fpga –based CSM using multiplexing algorithm based on GBTx wide-frame mode

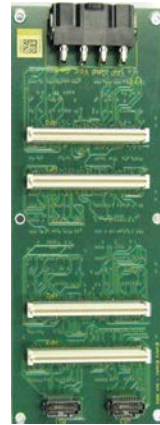


GBTx-based CSM

- Based on three GBTx chips.
- Each GBTx chip:
 - Can utilize a maximum of 14 E-links at 320 Mbps.
 - 4.8 Gbps bi-directional output link.
- Built-in clock manager.
- GBT-SCA will perform configuration and monitoring.
- Small service chip (asic) needed to interface with current mezzanine and fan out JTAG signals from GBT-SCA. Currently prototyping this with an FPGA.

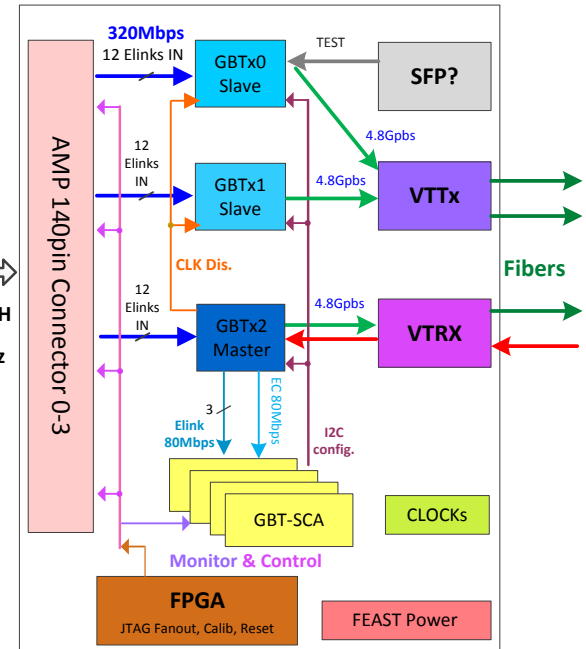


CSM Mother board



Mezz
0-17
320Mbps/CH
2CH/Mezz

GBTx-CSM prototype v1



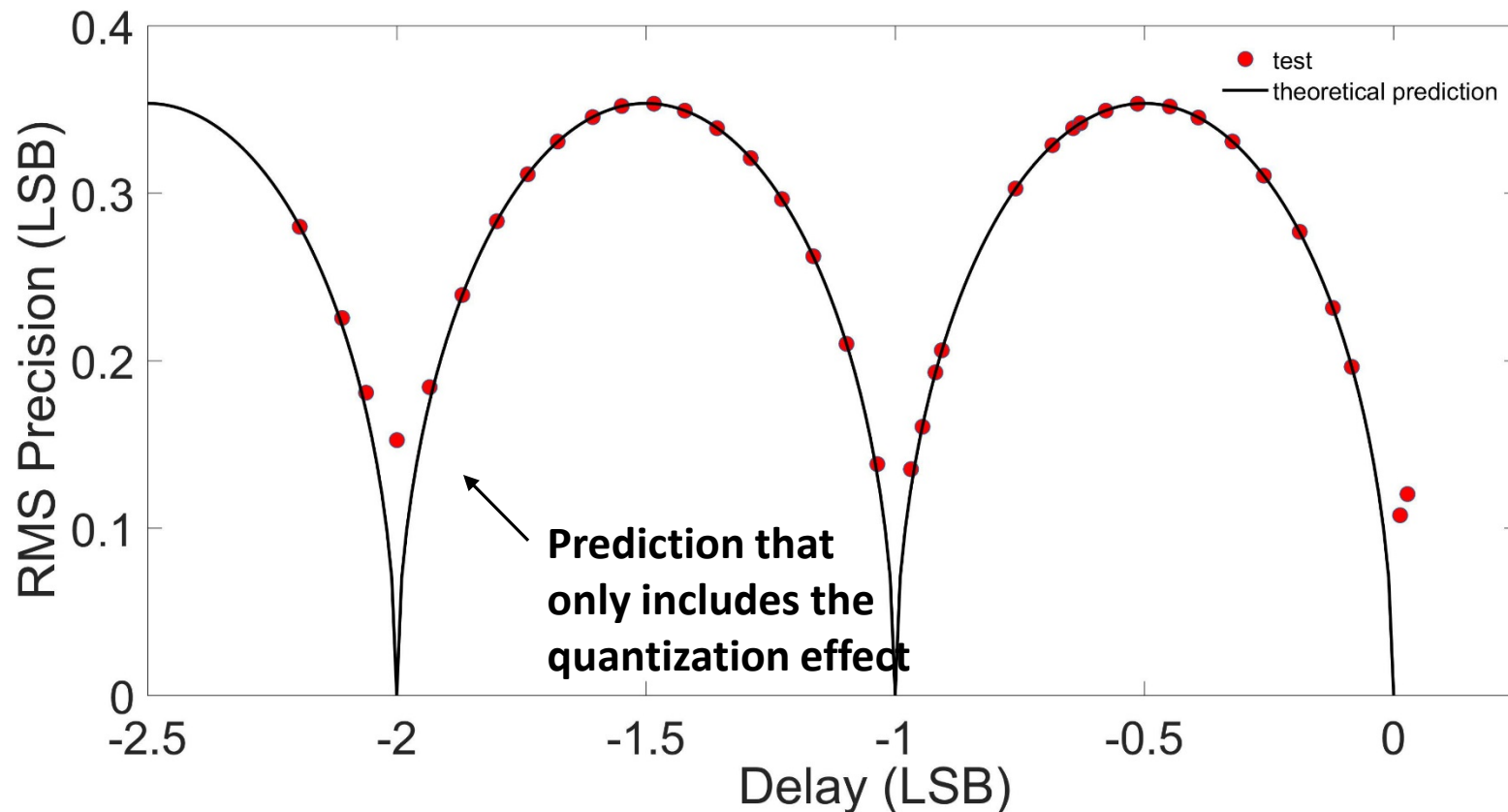
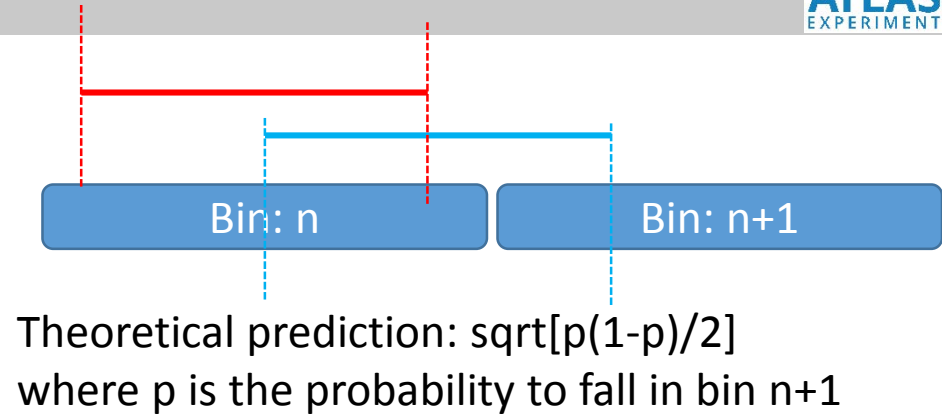
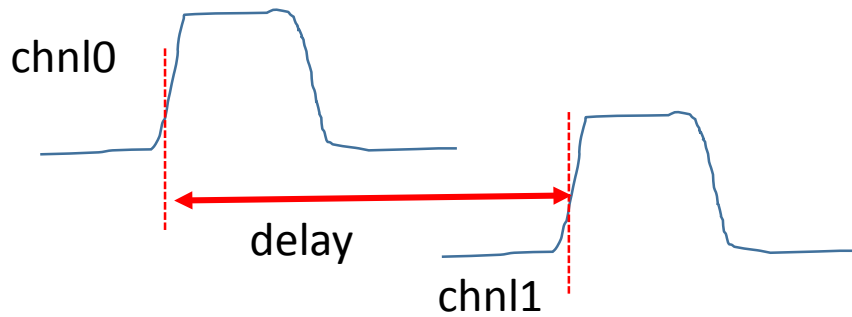
- A 1/3 demonstrator of the GBTx board has successfully shown to be able to pass data between GBTx and FPGA
- Fully prototype board is under development and will be connected to the current CSM motherboard

- ✓ To handle the hit rates expected at high-luminosity LHC runs, new MDT electronics are needed
- ✓ Good progress made on the development of all frontend electronics (ASD, TDC, CSM)
- ✓ Continue the development in the next few years and will be ready for the HL-LHC runs

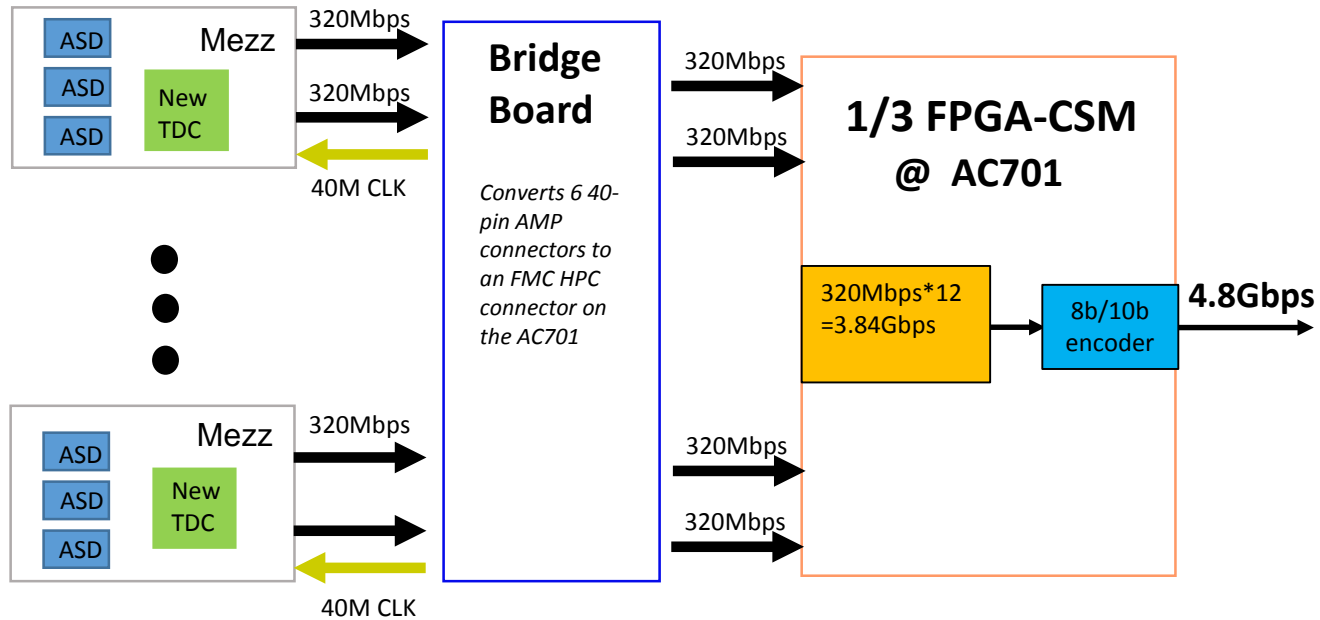
Thank you!

Back up

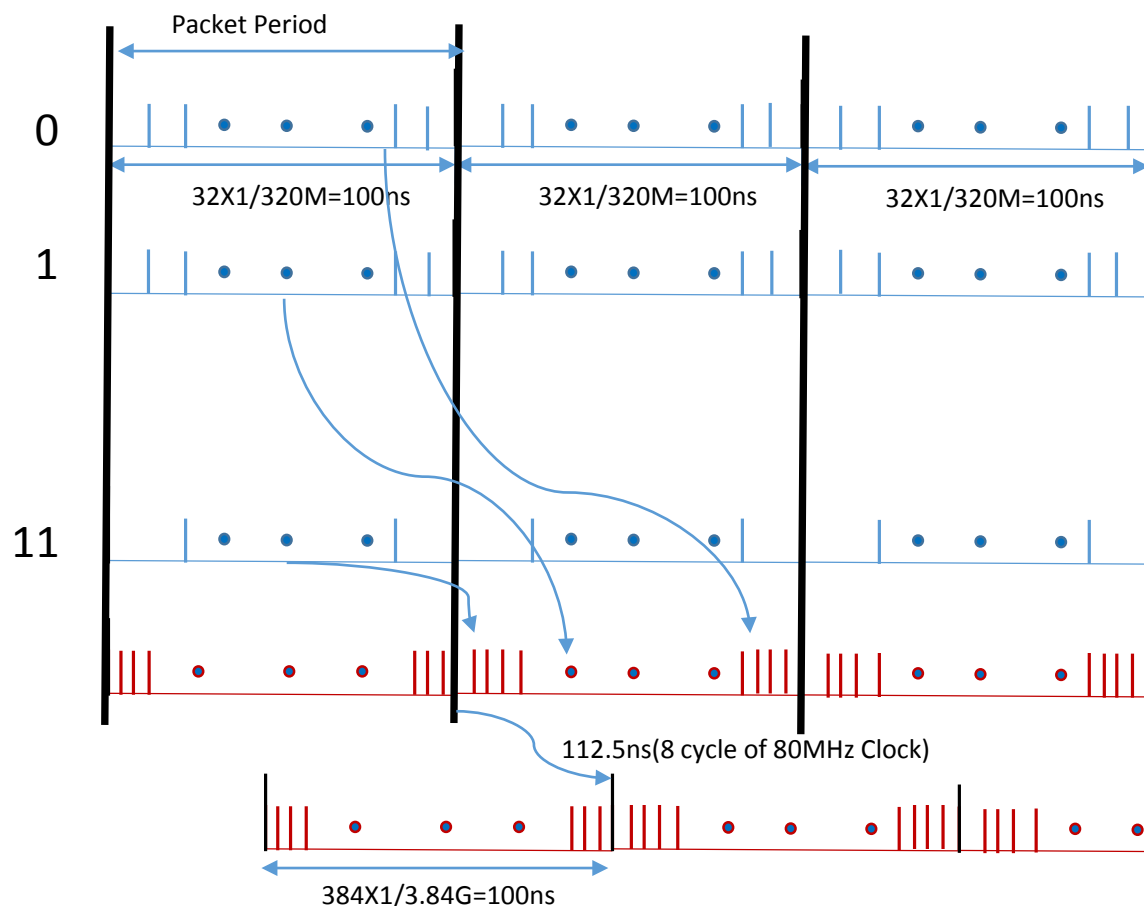
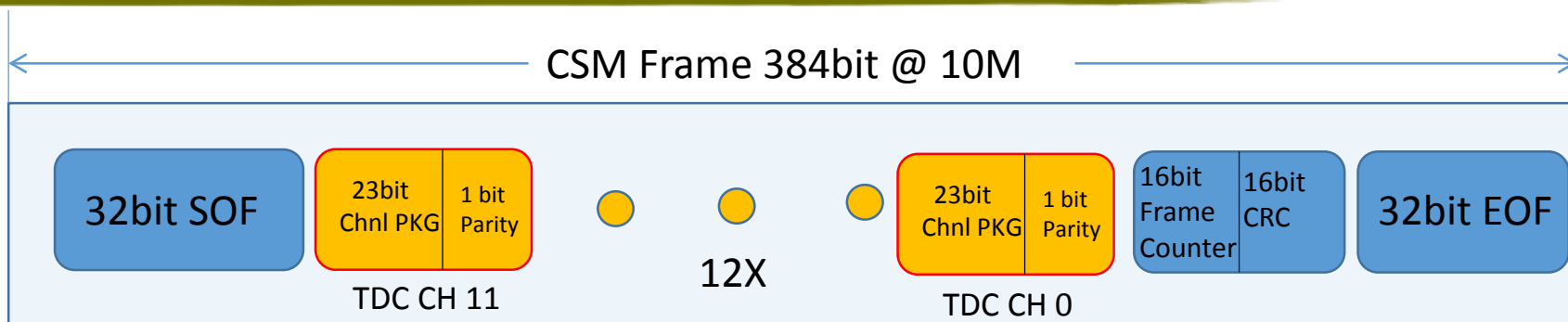
Back up



Back up



Back up



Note:

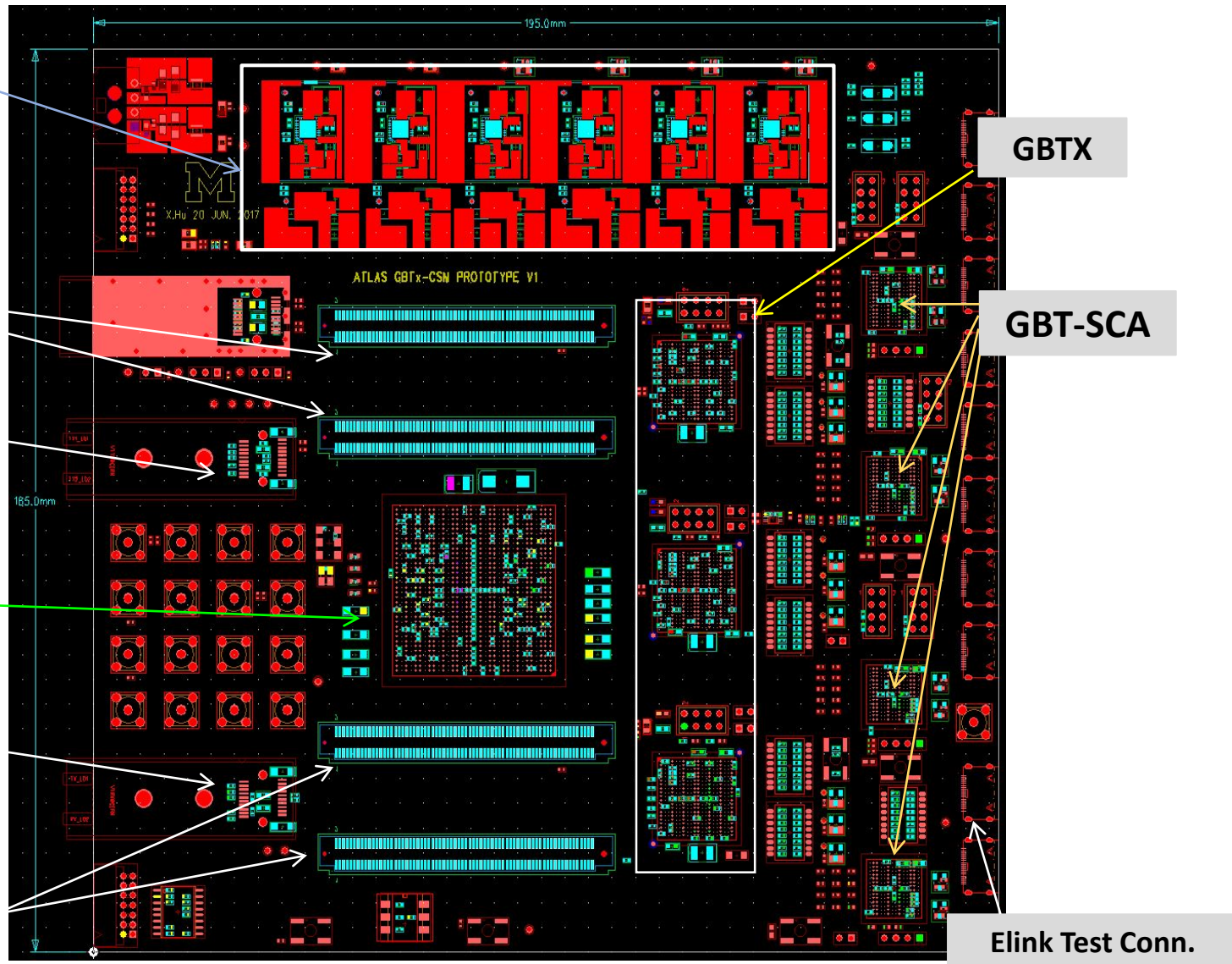
1. Output line rate/fiber: 4.8Gbps, handle 6 TDC modules (12 CHs)
2. Each CSM frame is 384 bit (before 8b/10b encoder)
3. CSM output data field structure is similar to GBTx wide frame mode
32 bit SOF + 24 bit * 12 + 16 bit frame counter + 16 bit CRC + 32bit EOF

Note: 32bit EOF is a place holder

4. Compared to priority FIFO structure
 - Latency (frame to frame) is fixed
 - Avoid packet loss

1/7 Frame to GTX

Back up



- **Functionality**
 - MASTER GBTx: 1
 - Connected with VTRx, responsible for 1 downlink(control), 1 uplink (data readout)
 - Controlled via IC channel (IC[1:0] in GBT frame)
 - EC channel + 80Mbps Elink connected with SCAs
 - Recover clock through downlink & distribute the clock to SLAVE GBTx
 - SLAVE GBTx: 2
 - Connected with VTTx, responsible for 2 uplinks (transmitter mode)
 - Controlled by GBT-SCA I2C master serial bus
 - GBT-SCA: 4
 - Controlled via Master GBTx via 80Mbps Elinks
 - Configure GBTx via I2C channels
 - Monitoring all TEMP, VOLTAGE info from 18 Mezz.
 - Service FPGA: JTAG fanout for Mezz., generate Calibration pulse, encoded reset
 - Power: FEAST ASIC chips
 - Test purpose: SFP, local clocks, SMA connector, Elink connector