High-Speed/Radiation-Hard Optical Engine for HL-LHC

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Outline

- Introduction
- Results from 1st Prototype ASIC
- Results from 2nd Prototype ASIC
- Summary

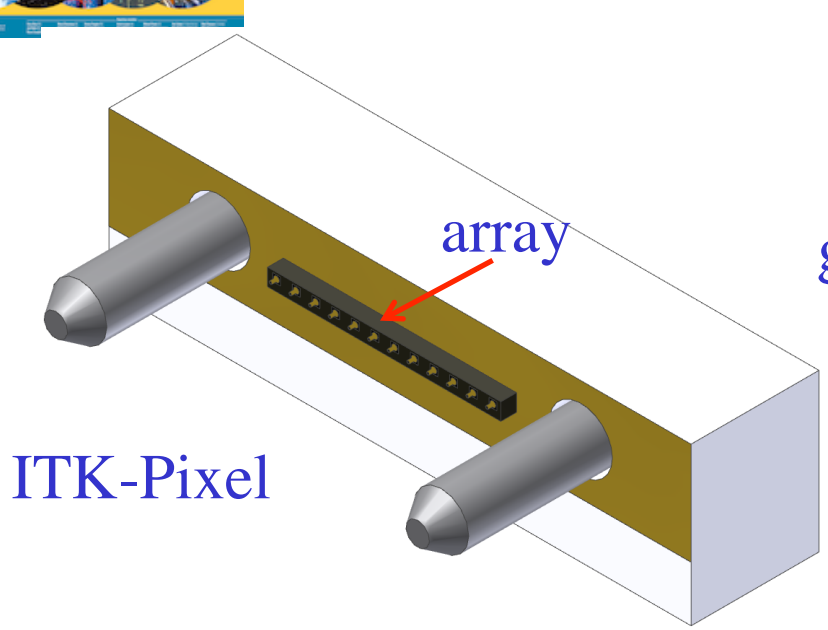
Use of VCSEL Arrays in HEP

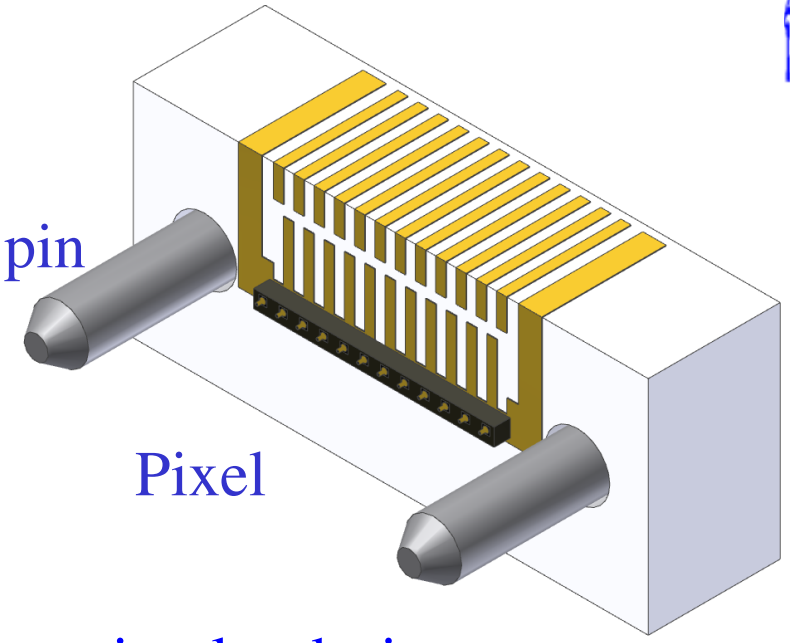
- Widely used in off-detector (no radiation) data transmission
- First on-detector implementation is in pixel detector of ATLAS
  - experience has been positive
    - ⇨ use arrays for the second generation opto-links
    - ⇨ logical for HL-LHC ATLAS pixel detector to use 12-channel arrays as in the 1st and 2nd generation optical modules (opto-boards)

Opto-Board for HL-LHC ATLAS Pixel Detector

- Use experience from building two generations of opto-boards to develop an opto-board capable of operation at 5 Gb/s or higher for HL-LHC ATLAS pixel detector (ITK-Pixel)
- What is required to demonstrate that the opto-board concept is a logical solution?
  - 5 Gb/s per channel VCSEL arrays
  - radiation-hard VCSEL array driver
  - robust high speed array based packaging with thermal management
- A working prototype has been constructed

Opto-Pack for ITK-Pixel



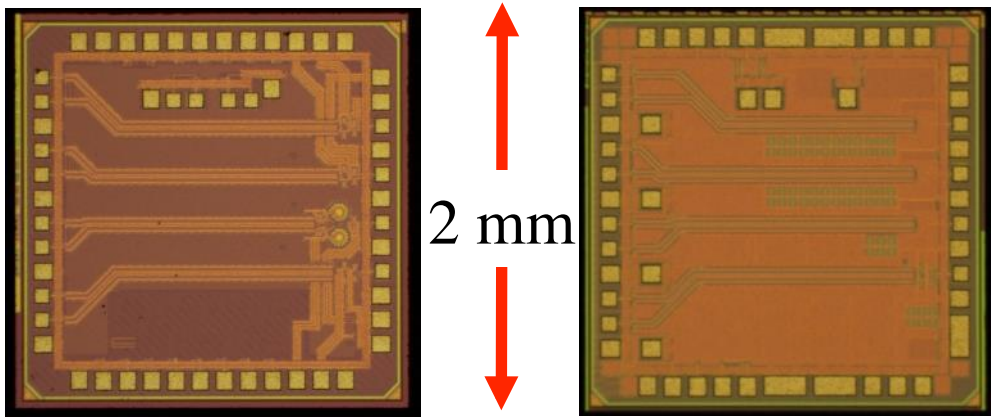


- Proposed opto-pack for ITK-Pixel has simpler design
  - continue to use BeO as substrate for heat management
- experience in building large quantity of opto-packs
  - fabricated 1,200 opto-packs for pixel opto-boards
  - fabricating 300 PIN opto-packs for off-detector opto-receivers
  - equivalent to 18,000 channels

10 Gb/s VCSEL Array Driver

- R&D funded via CDRD program (FY13-15) of DOE (USA)
- Fabricated 4-channel test chips in 65 nm CMOS
  - 2 mm x 2 mm
  - 1st prototype submission: October 2014
  - 2nd prototype submission: March 2016
- Uses only core transistors to achieve maximum radiation-hardness
- 8-bit DACs to set the VCSEL modulation and bias currents
  - DAC settings stored in SEU tolerant registers

Rev. 1

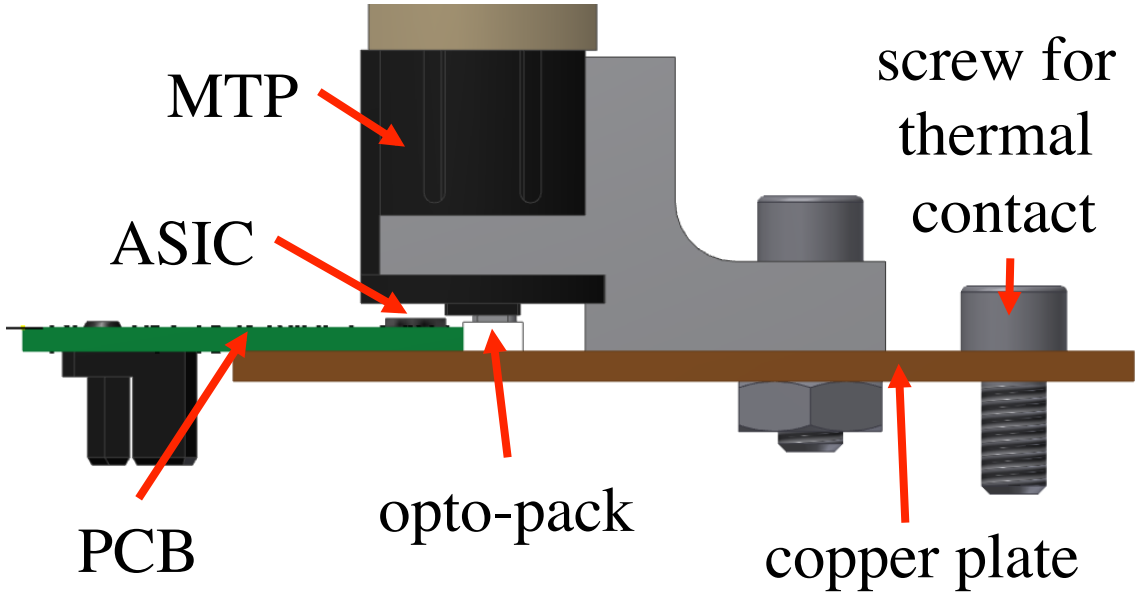


2 mm

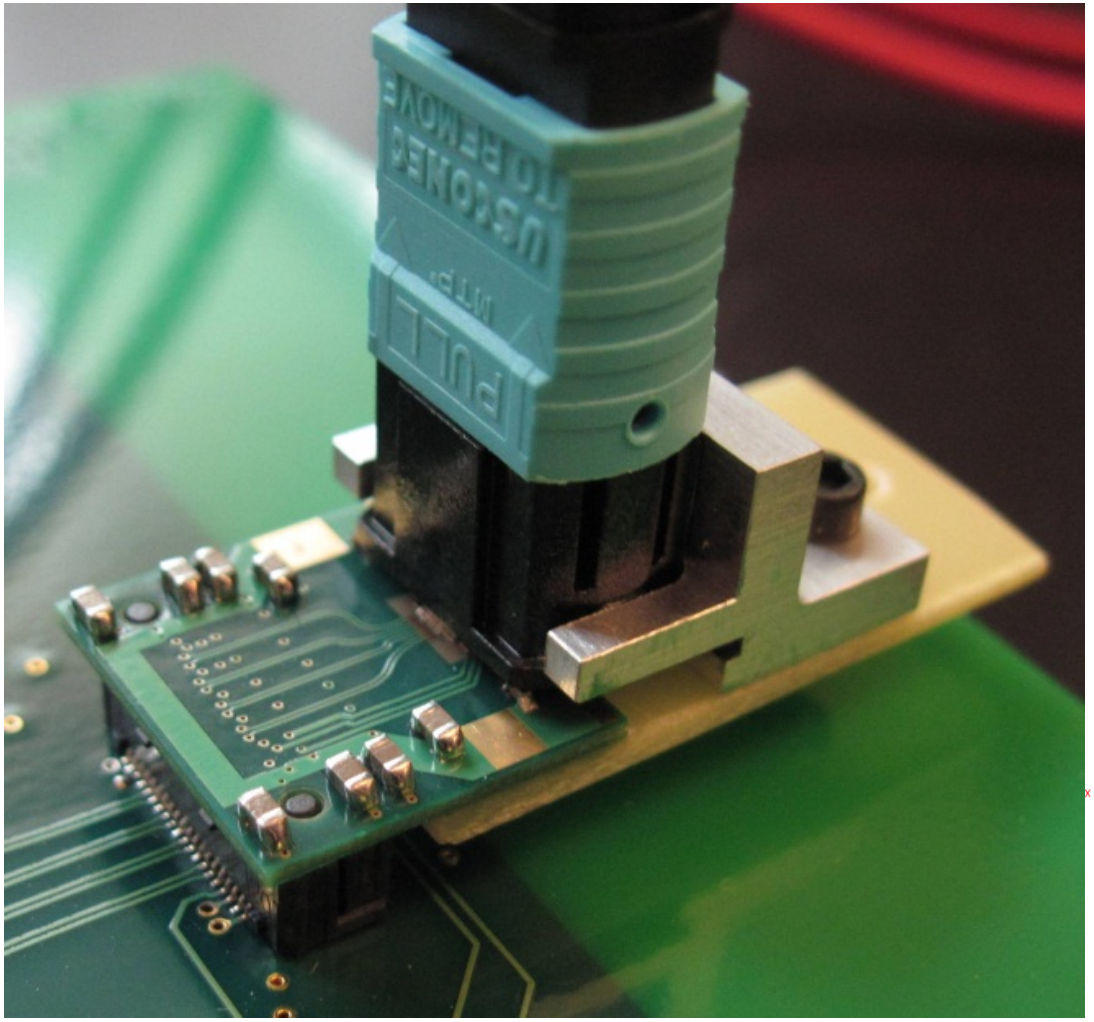
Rev. 2

ITK-Pixel Opto-Board Concept

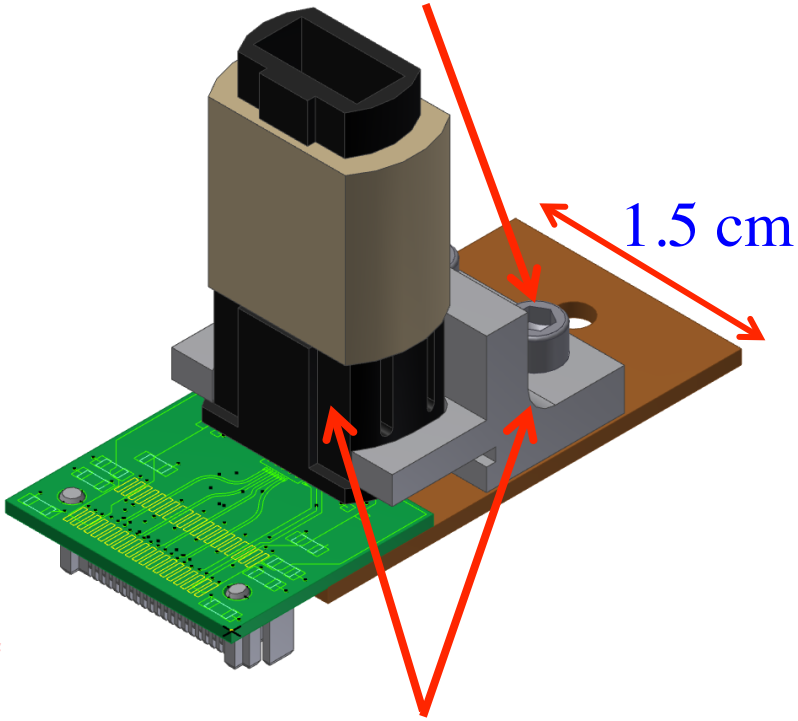
- Keep opto-pack
- Keep copper backed PCB
- Keep MTP connector
- Compatible with an opto-box (opto crate) concept
- No lenses/mirrors used to turn the light



ITK-Pixel Opto-Board



Connector secured to opto-board with screws instead of epoxy in current opto-board



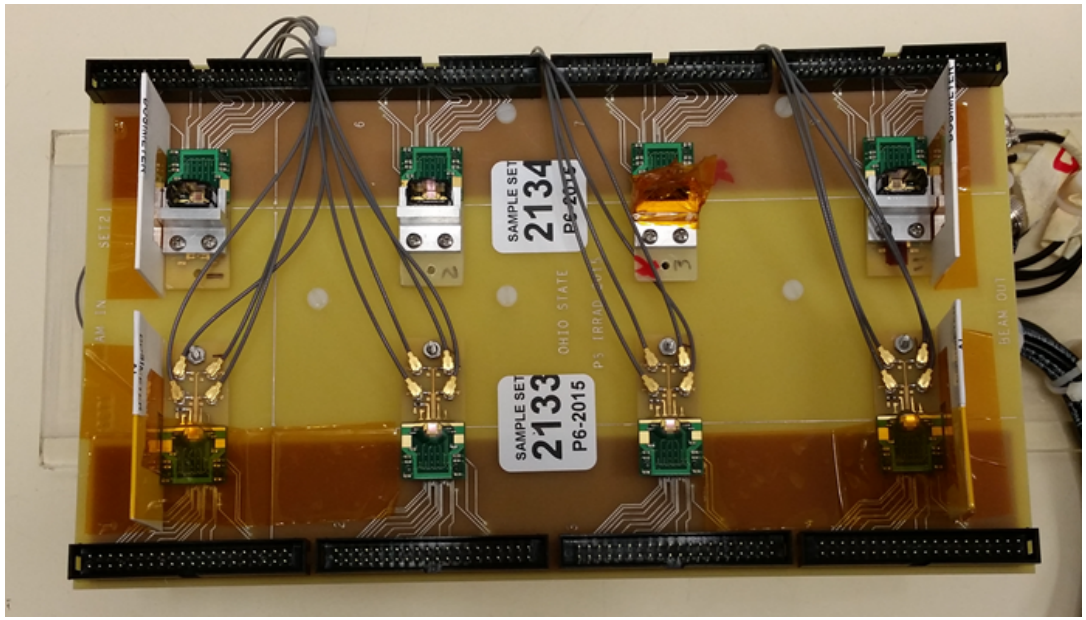
Could be fabricated as one piece with mold injection

New Opto-Board Irradiation

- October 2015: irradiated 8 opto-boards with Rev. 1 array driver using 24 GeV protons at the CERN PS Irradiation facility
- 4 pcs. optical: driving Finisar VCSEL arrays (V850-2174-002)
  - dose: 13 Mrad
- 4 pcs. electrical: driving resistive load
  - dose: 111 Mrad

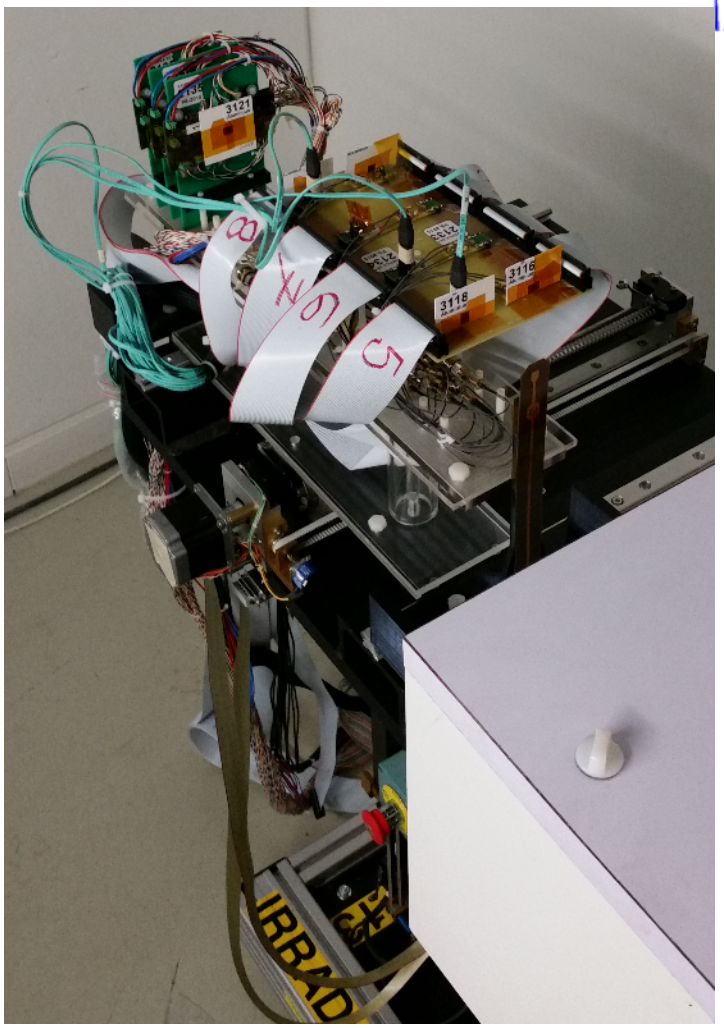
optical

electrical



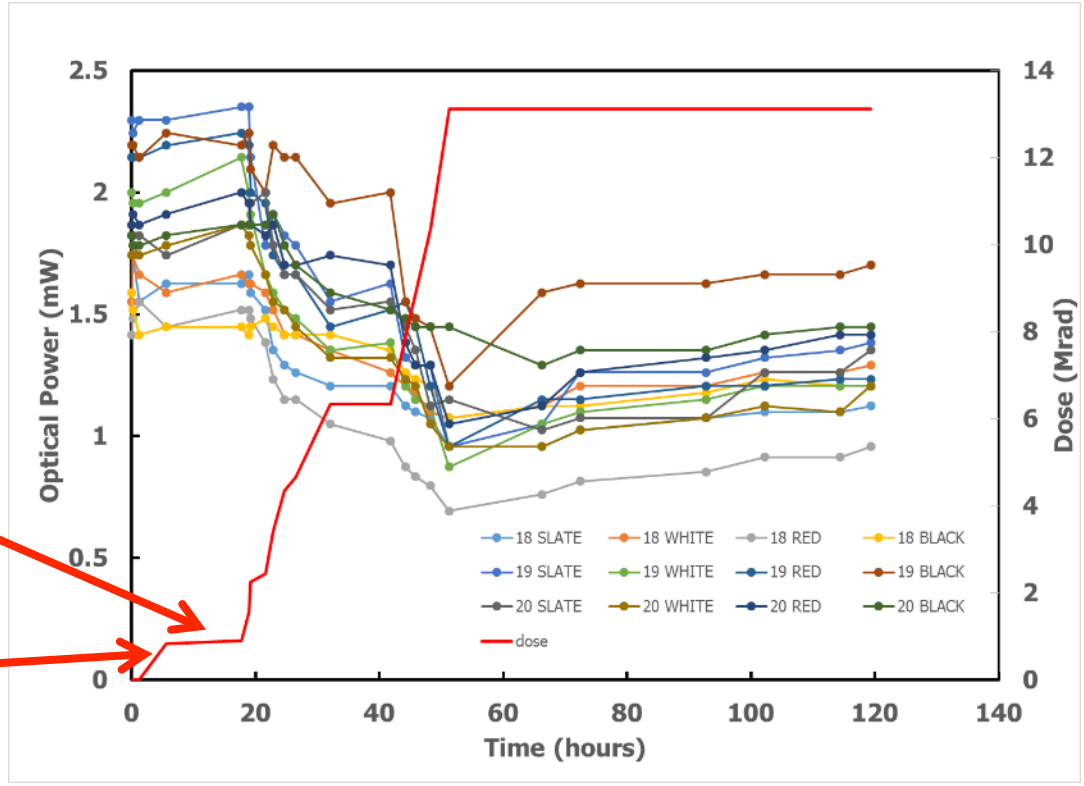
New Opto-Board Irradiation

- Chips were powered and monitored during the irradiation at reduced speeds due to the irradiation facility cabling infrastructure
- All channels survived the irradiation and the cooled down chips have been returned to our lab for a study of their performance at high bit rates



VCSEL Optical Power vs. Dose

- Optical power of irradiated VCSELs decreased with dose as expected
- Annealing occurred (slowly) during times when the VCSELs were removed from the beam
- Monitored 12 out of the 16 VCSEL channels during irradiation due to limited number of fiber connections

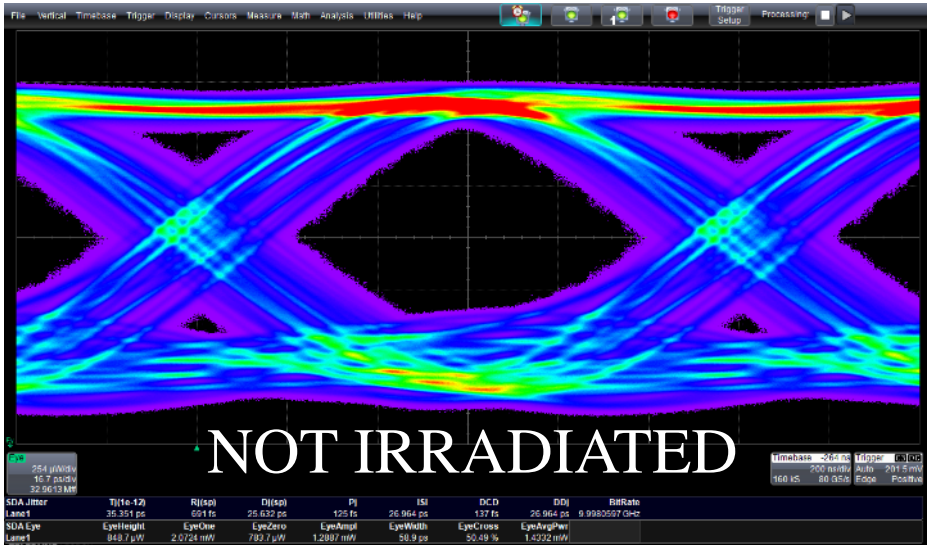


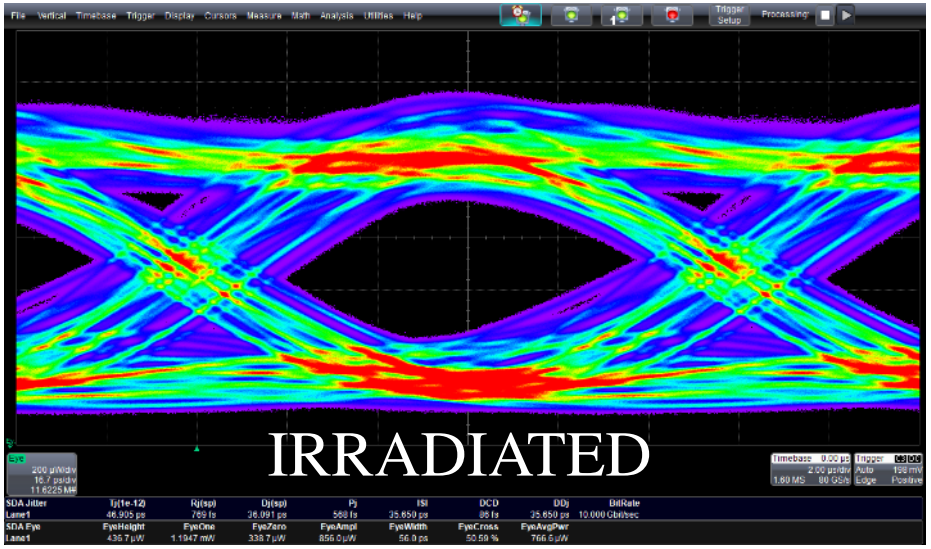
annealing

irradiation

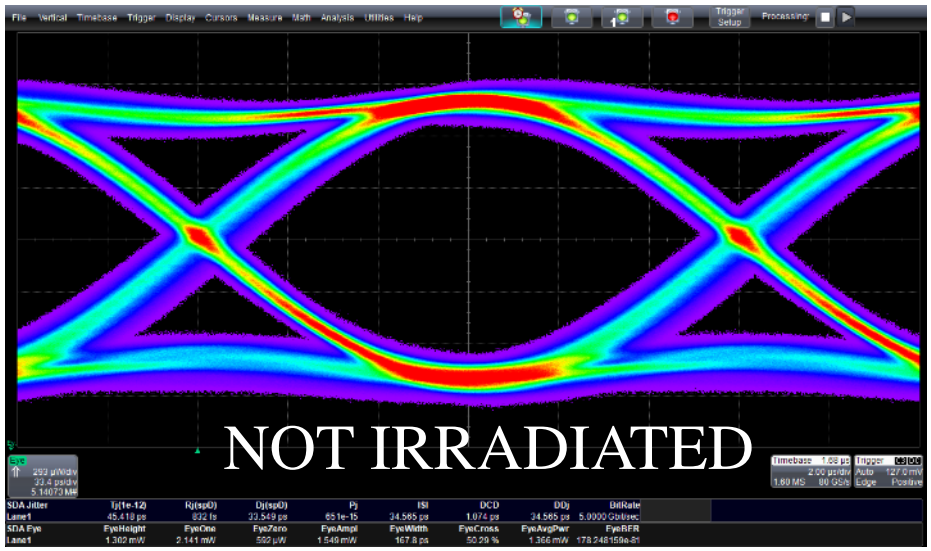
Post Irradiation Results – 10 Gb/s

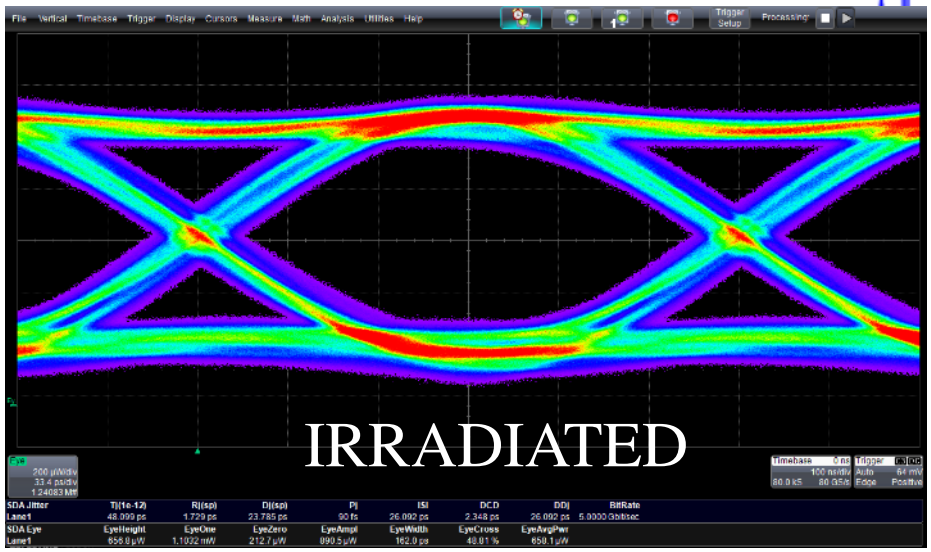
- All channels operational after irradiation
- Optical amplitude reduced from 2.07 mW to 1.19 mW
  - consistent with power loss seen during irradiation
- BER < 5×10^{-14} (run error free for more than 30 minutes)
- First demonstration of radiation hardness of an array driver/VCSEL combination at 10 Gb/s with a dose greater than 10 Mrads!





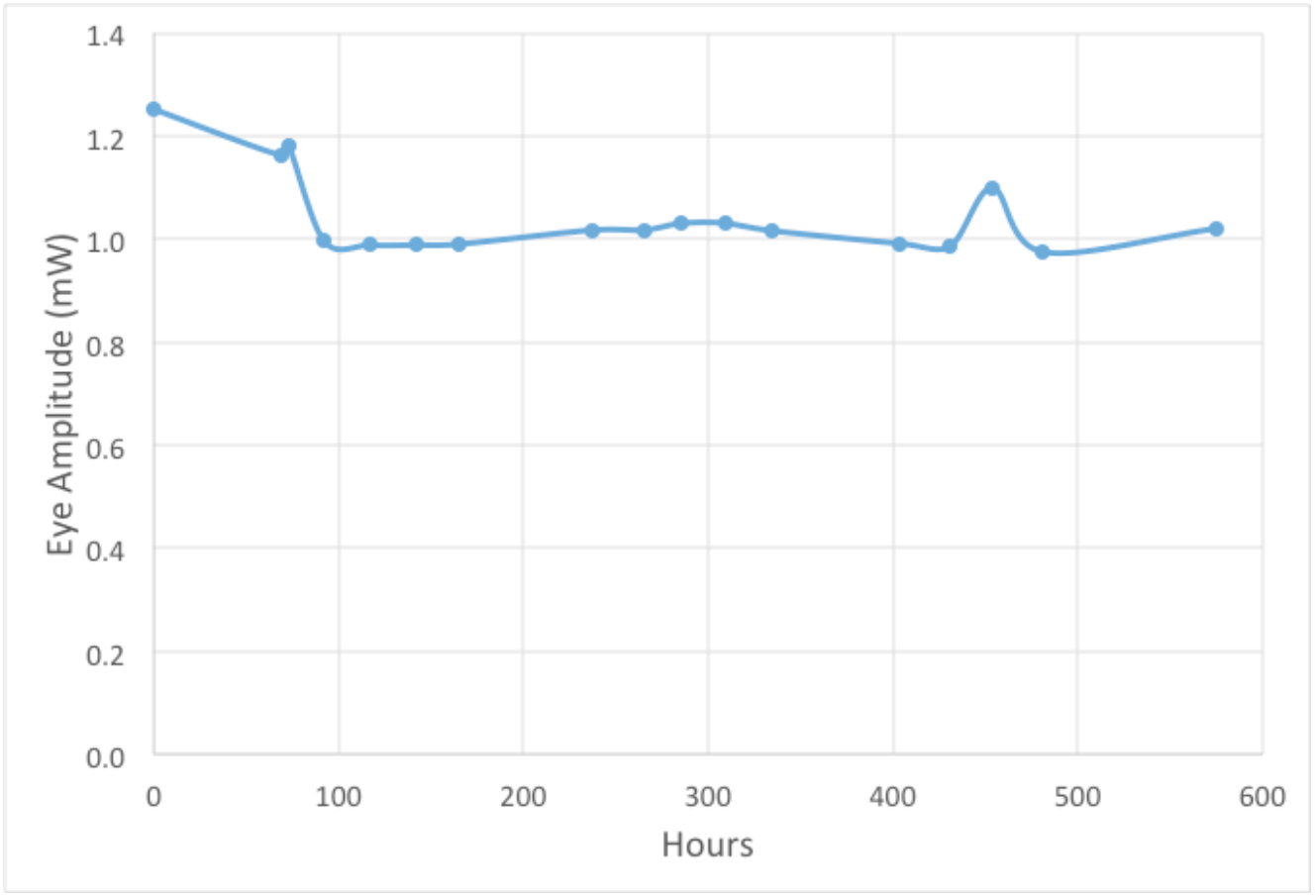
Post Irradiation Results – 5 Gb/s





- performance of the array driver/VCSEL combination at 5 Gb/s is acceptable after irradiation

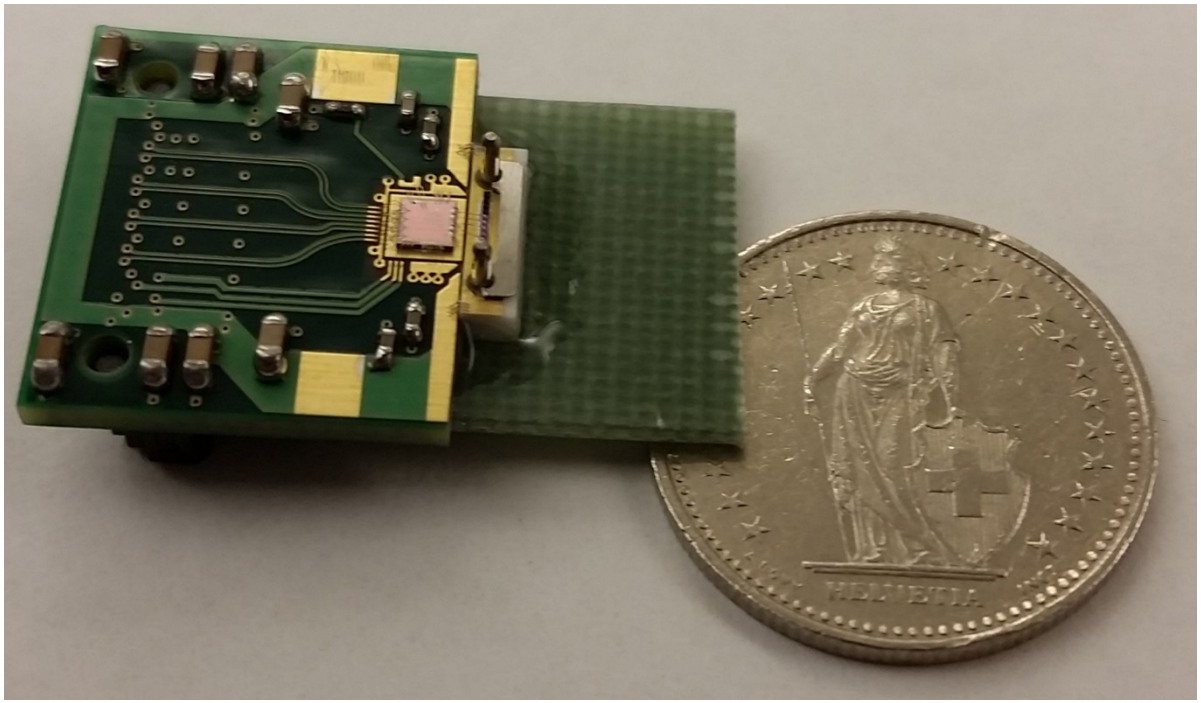
VCSEL Annealing



- Excellent optical power after irradiation
  but no improvement in power in annealing so far

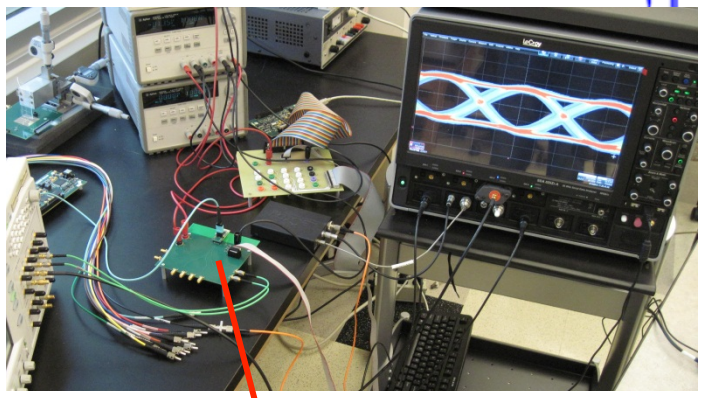
10 Gb/s Array Driver ASIC Rev. 2

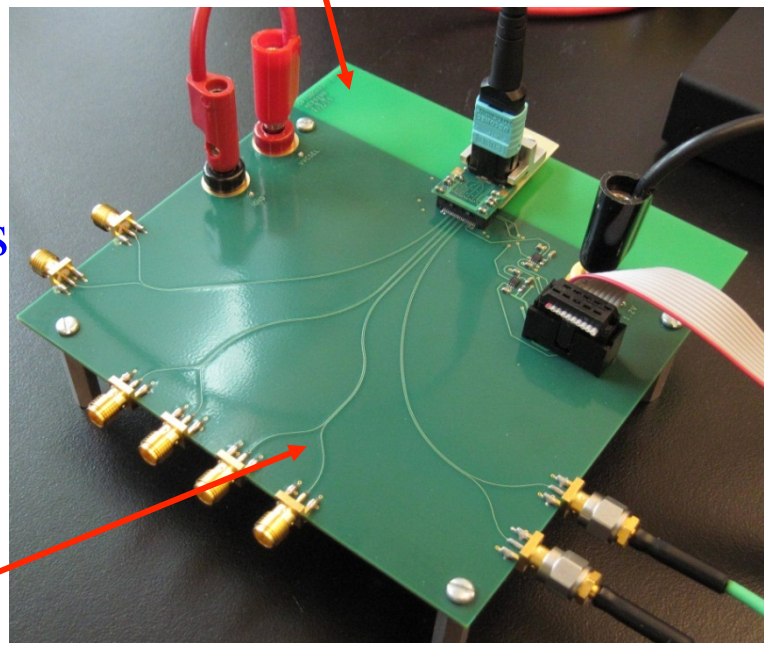
- Rev. 2 has improved architecture for the first three channels, including programmable pre-emphasis current and delay
- One channel was simply a copy of the old design to check for consistency between the versions
- Rev. 2 ASIC is much easier to tune for operation at 10 Gb/s



10 Gb/s Array Driver ASIC Rev. 2

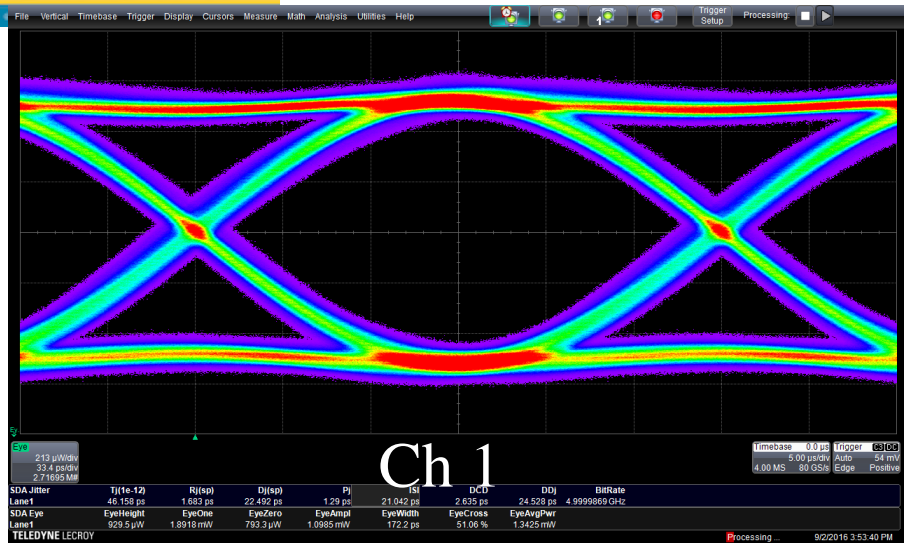
- runs at 1.2 V
  - consumes ~150 mA at 10 Gb/s with all four channels operating
- cathode set to -1.3 V to provide enough headroom to drive the VCSEL
- optical power > 2 mW on all channels
- BER < 5×10^{-14} on all channels at 10 Gb/s with every channel active

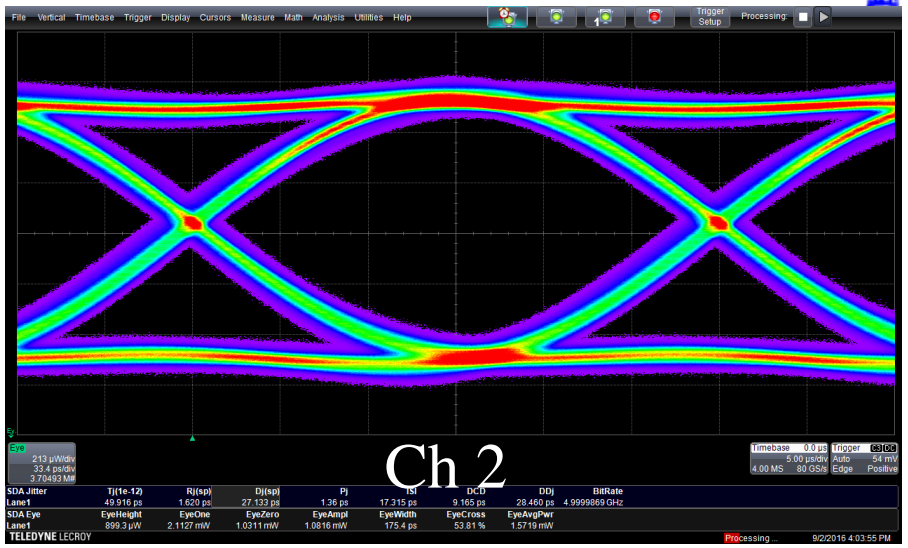


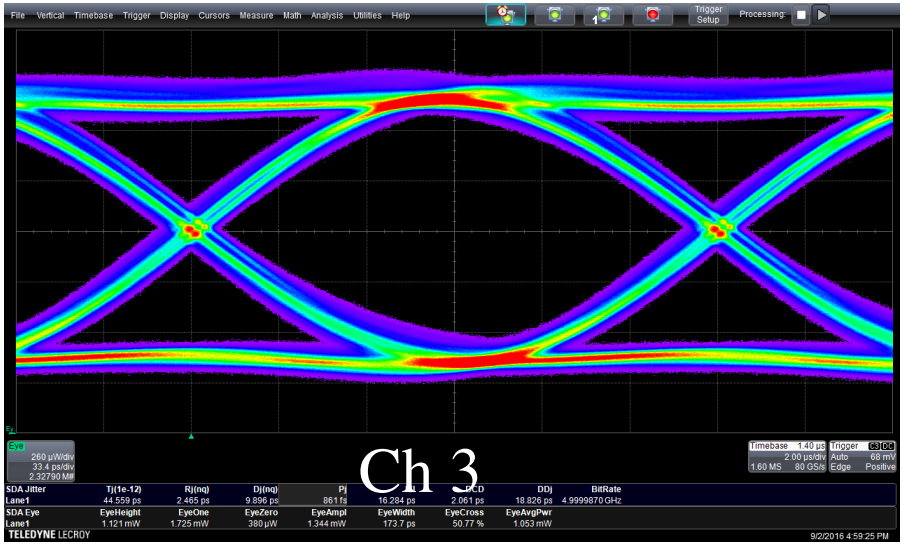


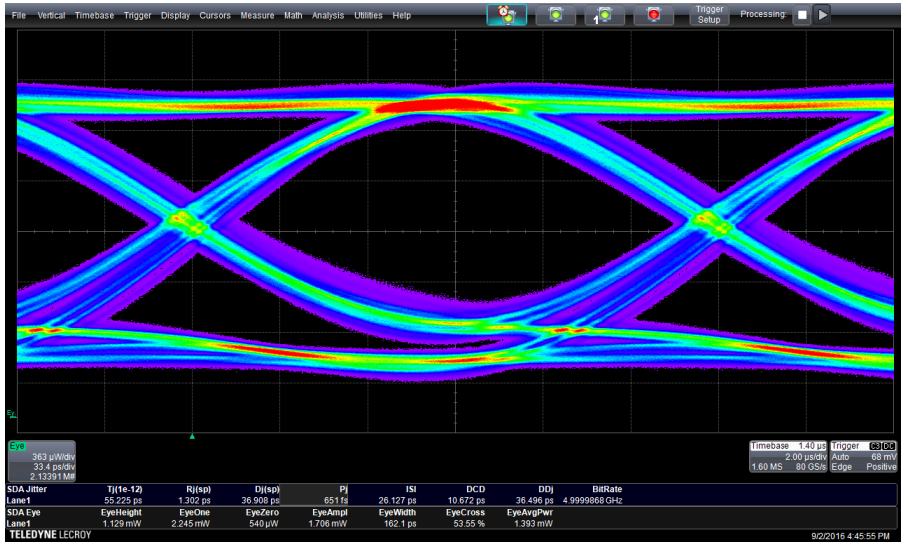
175 μm space/trace controlled impedance transmission lines

Array Driver ASIC Rev. 2: 5 Gb/s

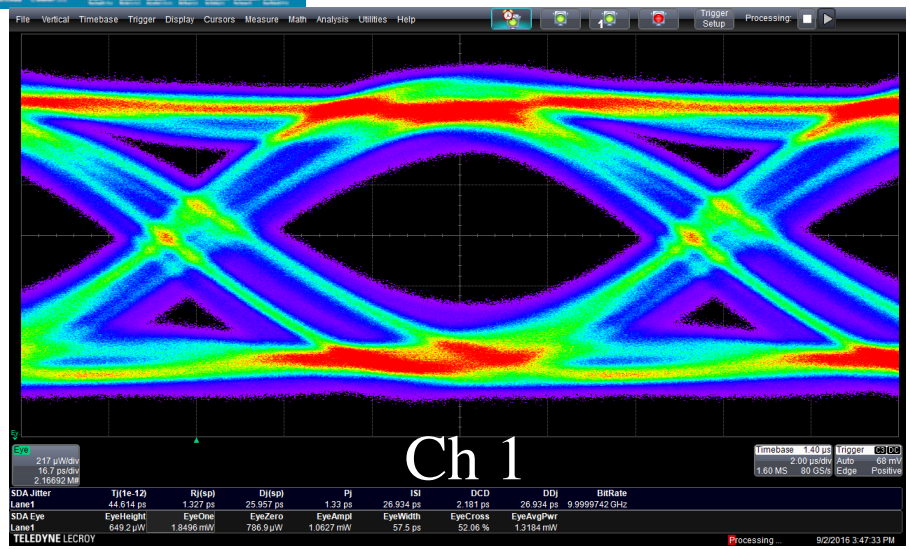


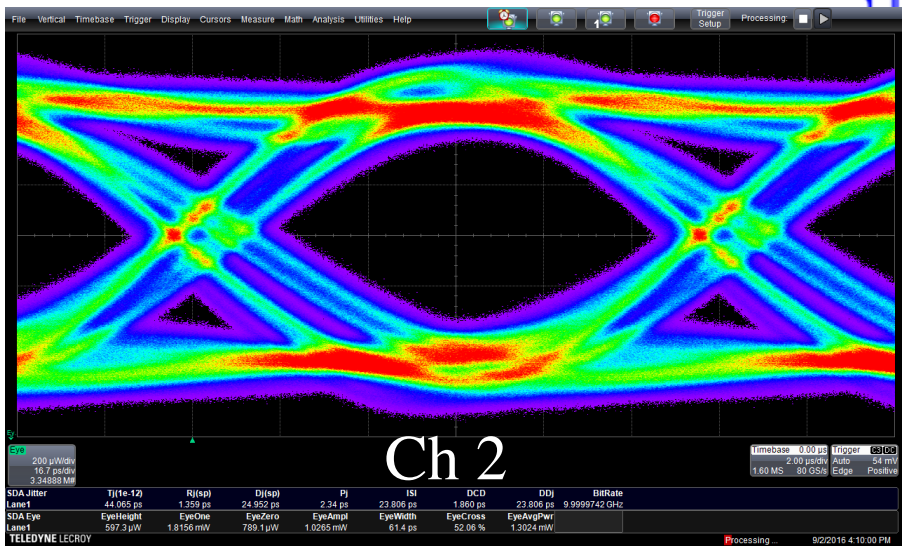


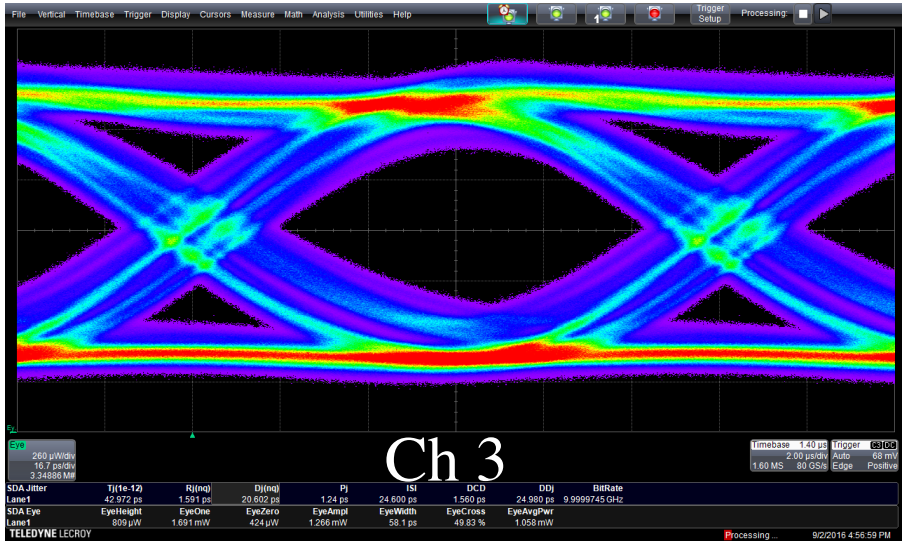


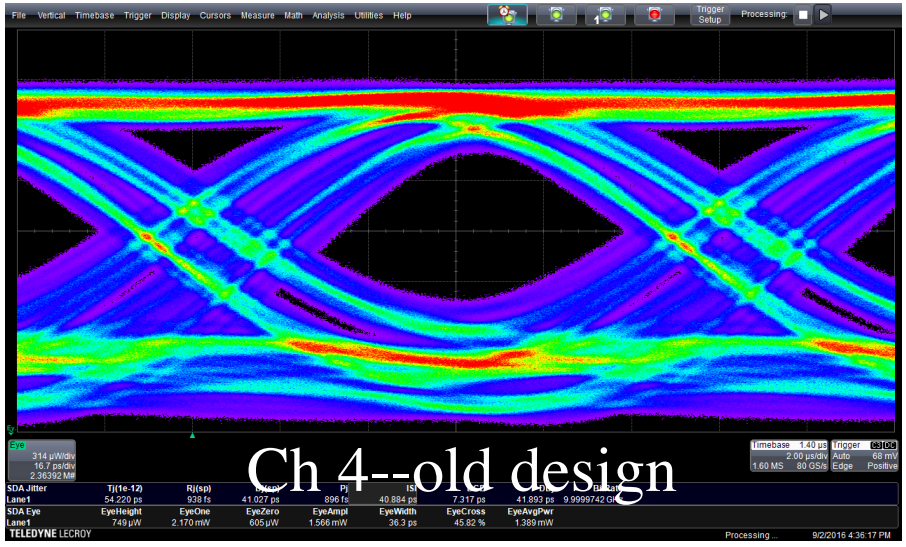


Array Driver ASIC Rev. 2: 10 Gb/s









Summary

- designed and fabricated a new opto-board including
  an array driver ASIC and optical packaging
  to allow 10 Gb/s optical data transmission
- demonstrated the radiation hardness of the combination
  of a new VCSEL array and an array driver ASIC
  with successful 10 Gb/s operation after irradiation (> 10 Mrad)
- improved VCSEL array driver has been fabricated