# TRACK RECONSTRUCTION EFFICIENCIES WITH THE H35DEMO HV-CMOS PIXEL DETECTOR

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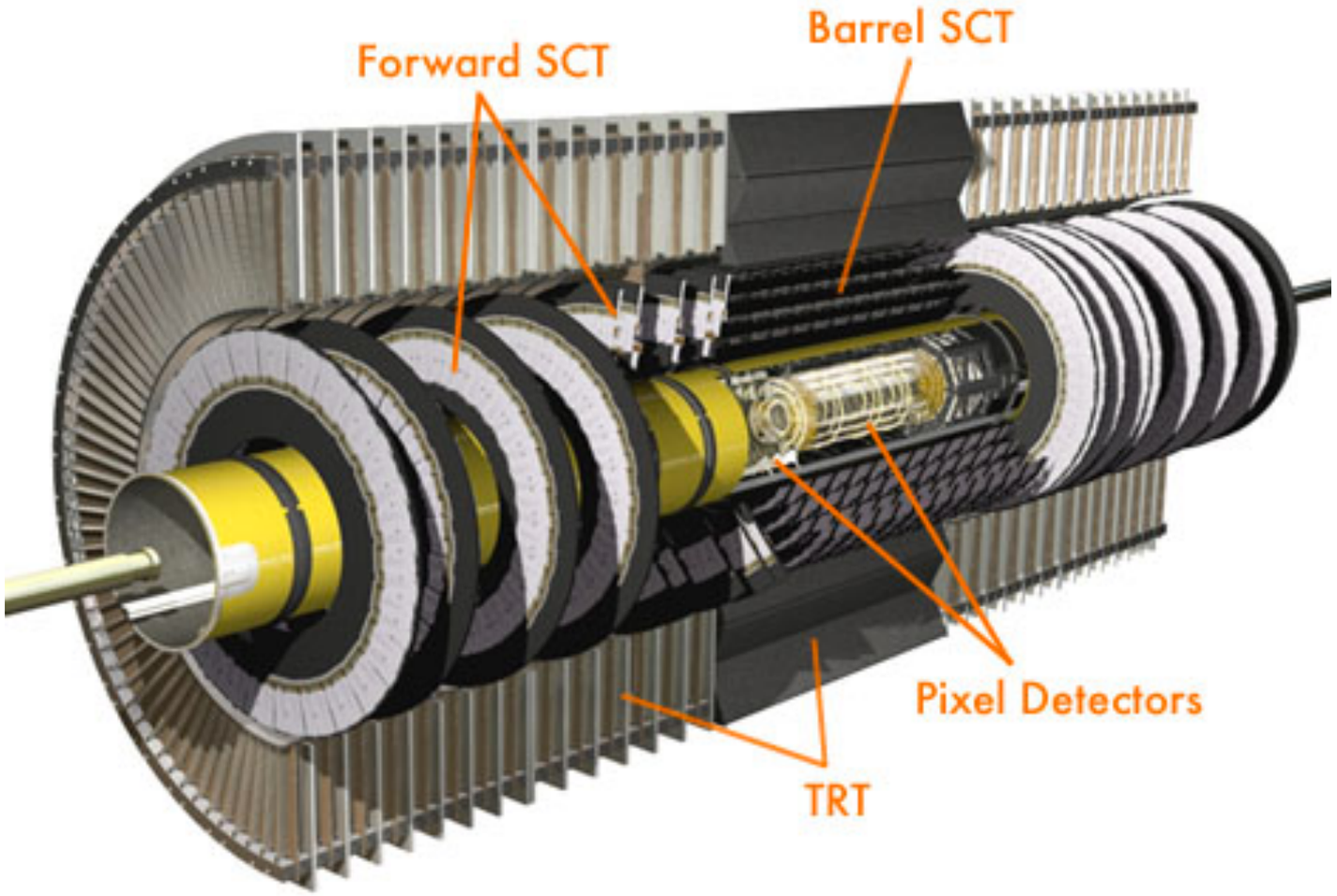
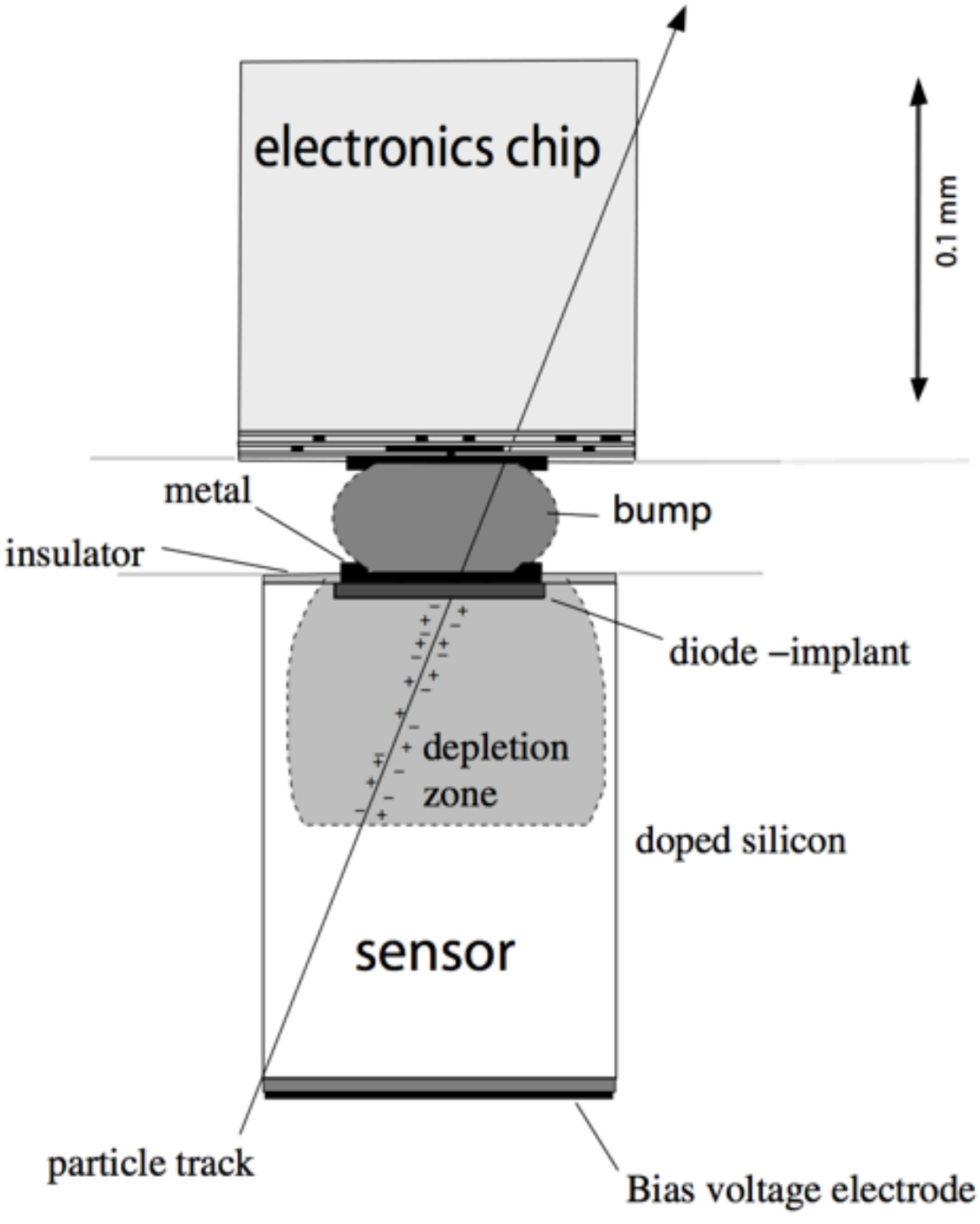
# Contents

- Description and purpose of H35DEMO
- Test beam conditions
- Data analysis method
- Track reconstruction efficiencies
- Results of changing HV, substrate resistivity, and threshold

# Background

- HL-LHC upgrade in 2024
- Entire ATLAS inner detector will be will be replaced (ITK)
- HVCMOS technology is in contention for installation in the fifth layer of the ITK
- Based on commercial processes which are low-cost and scalable
- H35DEMO is a demonstration of the HVCMOS concept



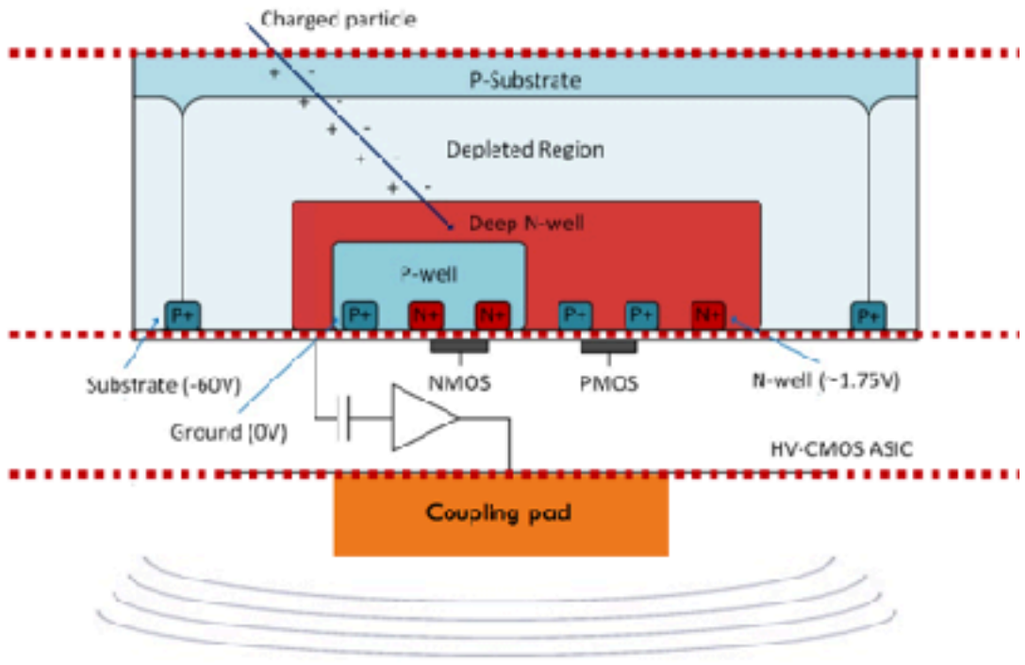



Traditional silicon sensor devices have separate charge collection and readout components, interfaced via bump bonds.

Combining the two components and removing the bump bonds allows us to save money, time, and material thickness.

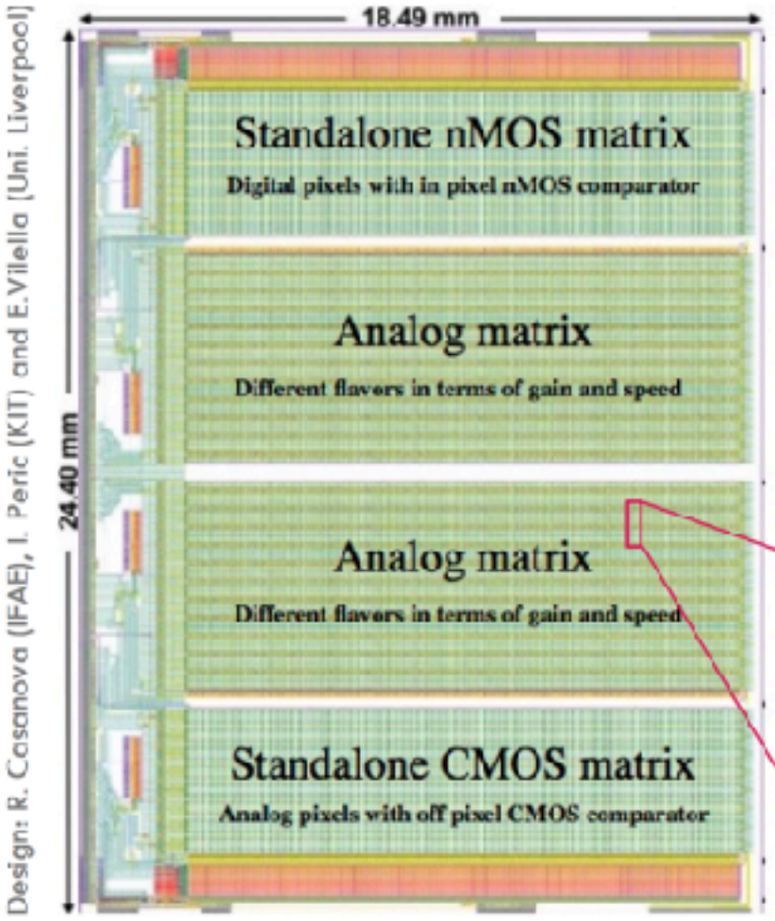
# HVCMOS

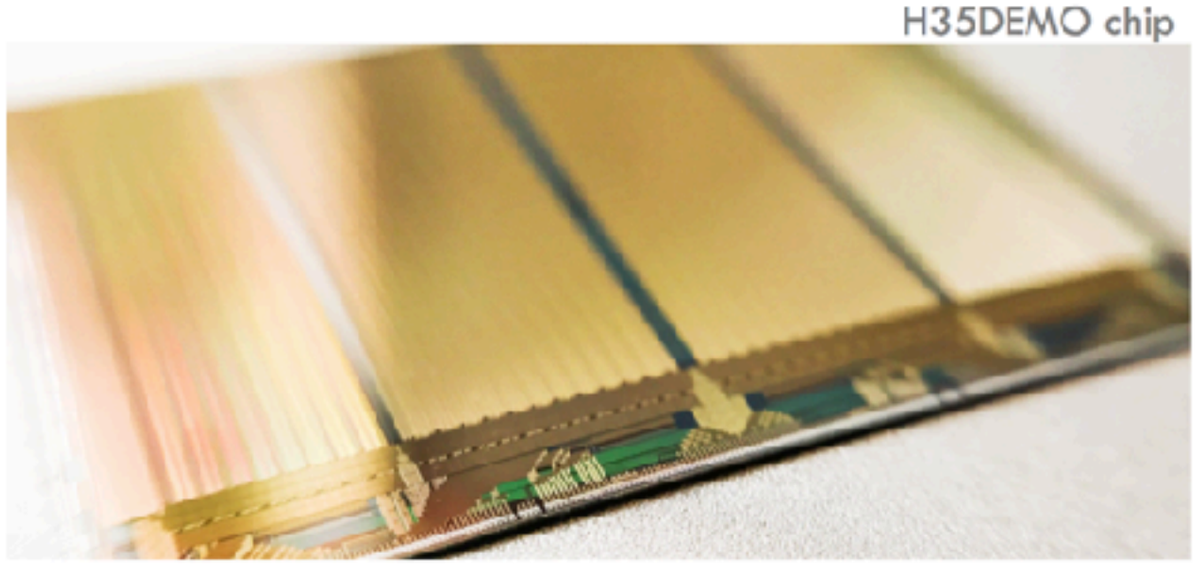
- High voltage (HV) applied to silicon sensor
- CMOS readout circuitry embedded in sensor, and shielded from HV via deep N-well implant
- Bump bonding is not required

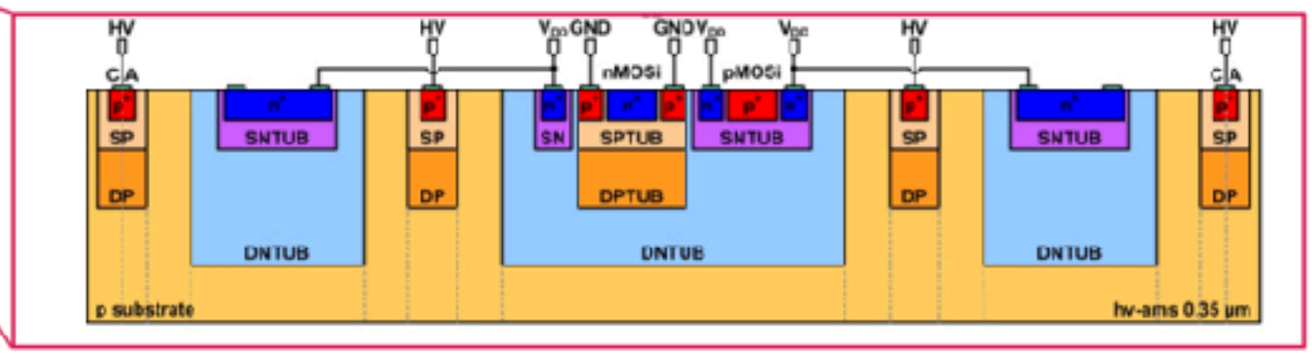


# H35DEMO

- Fabricated using 350nm HVCMOS technology
- 50 x 250μm pixels
- Substrate resistivities available in 20, 80, 200, and 1000 Ωcm

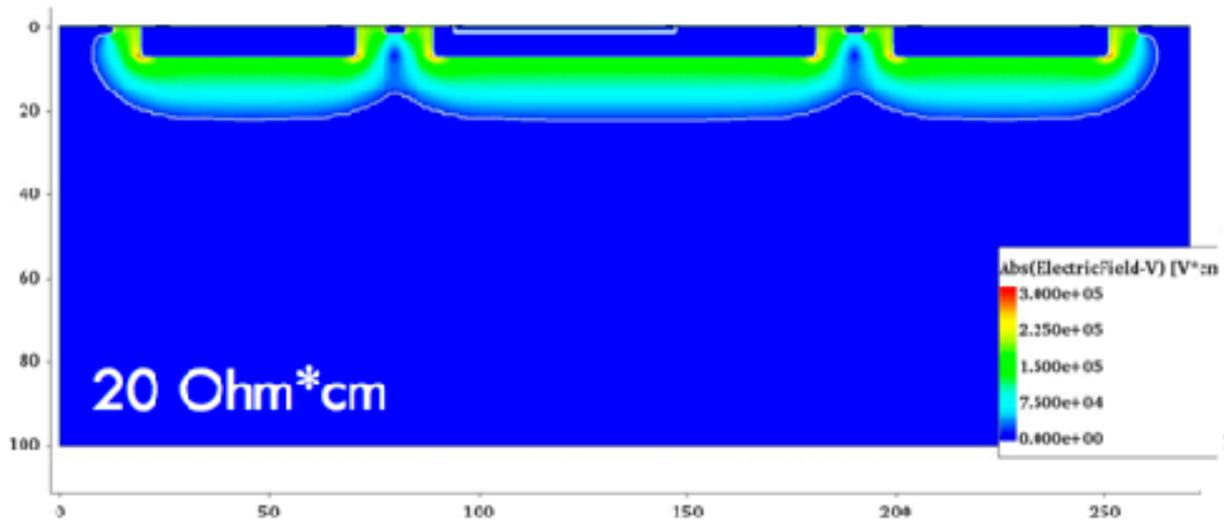


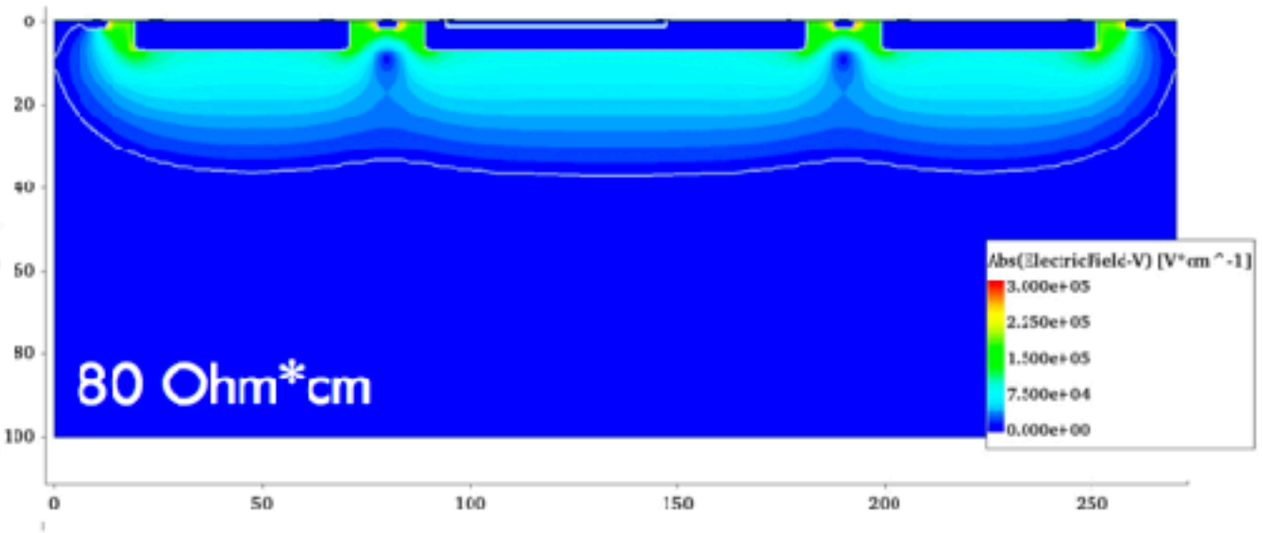



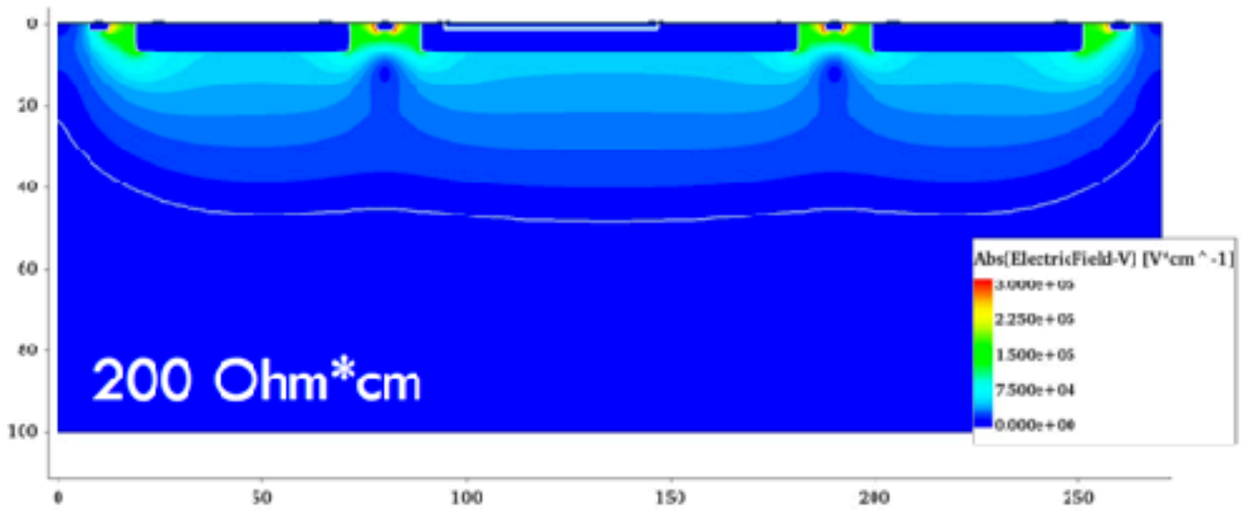



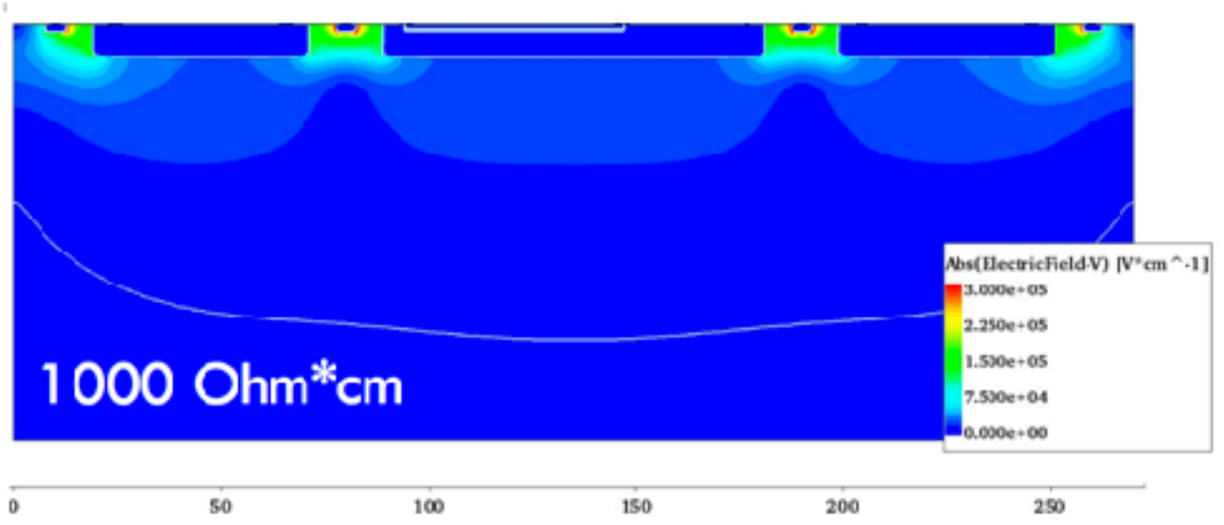
# H35DEMO

Comparison of the electric field between 20, 80, 200 and 1000 Ohm*cm



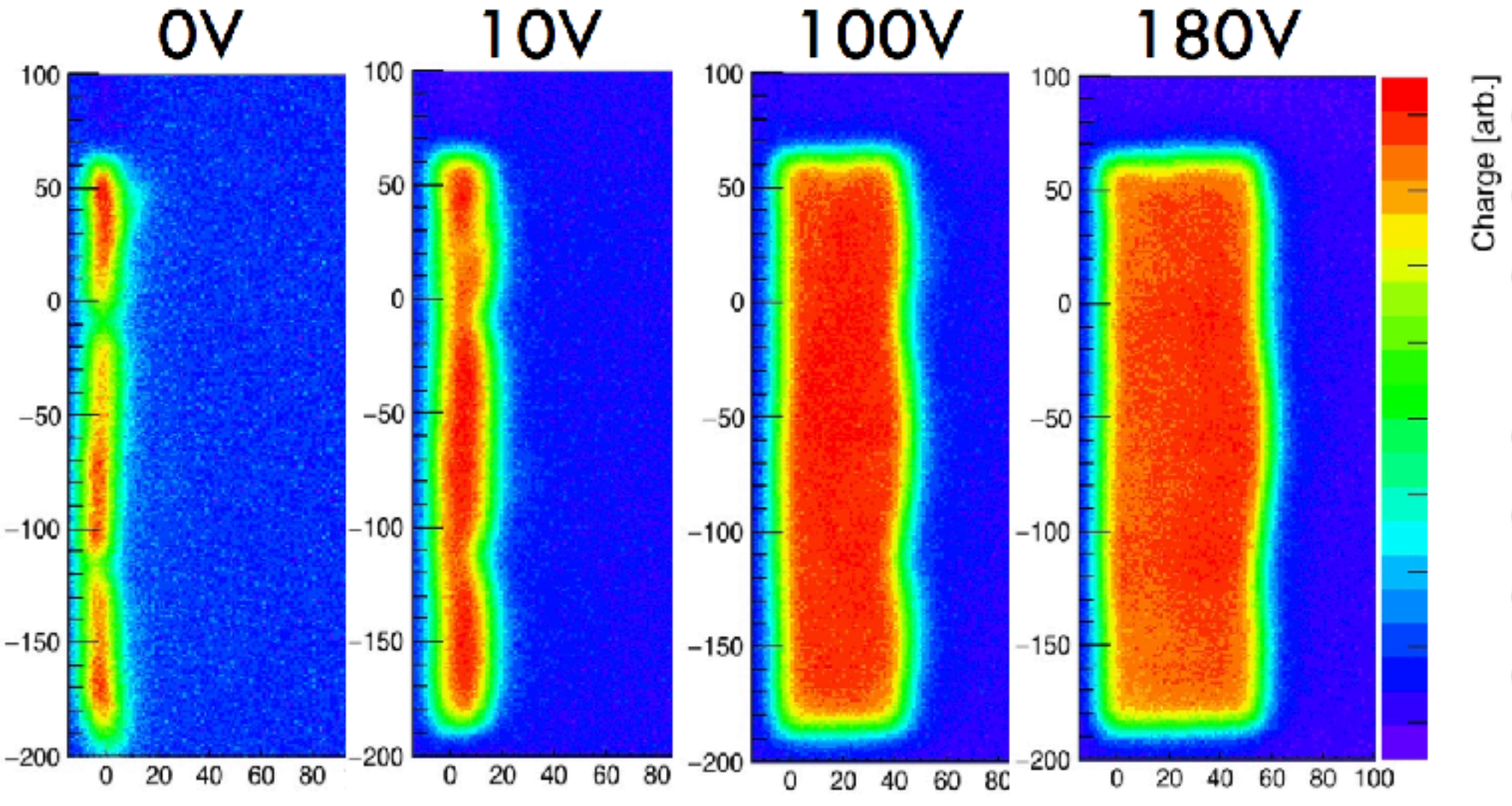



# H35DEMO

Depletion zone as a function of HV



# Test Beam Measurements

- Our team recently conducted test beam measurements at the Fermilab test beam facility, providing the first performance results for the H35DEMO.

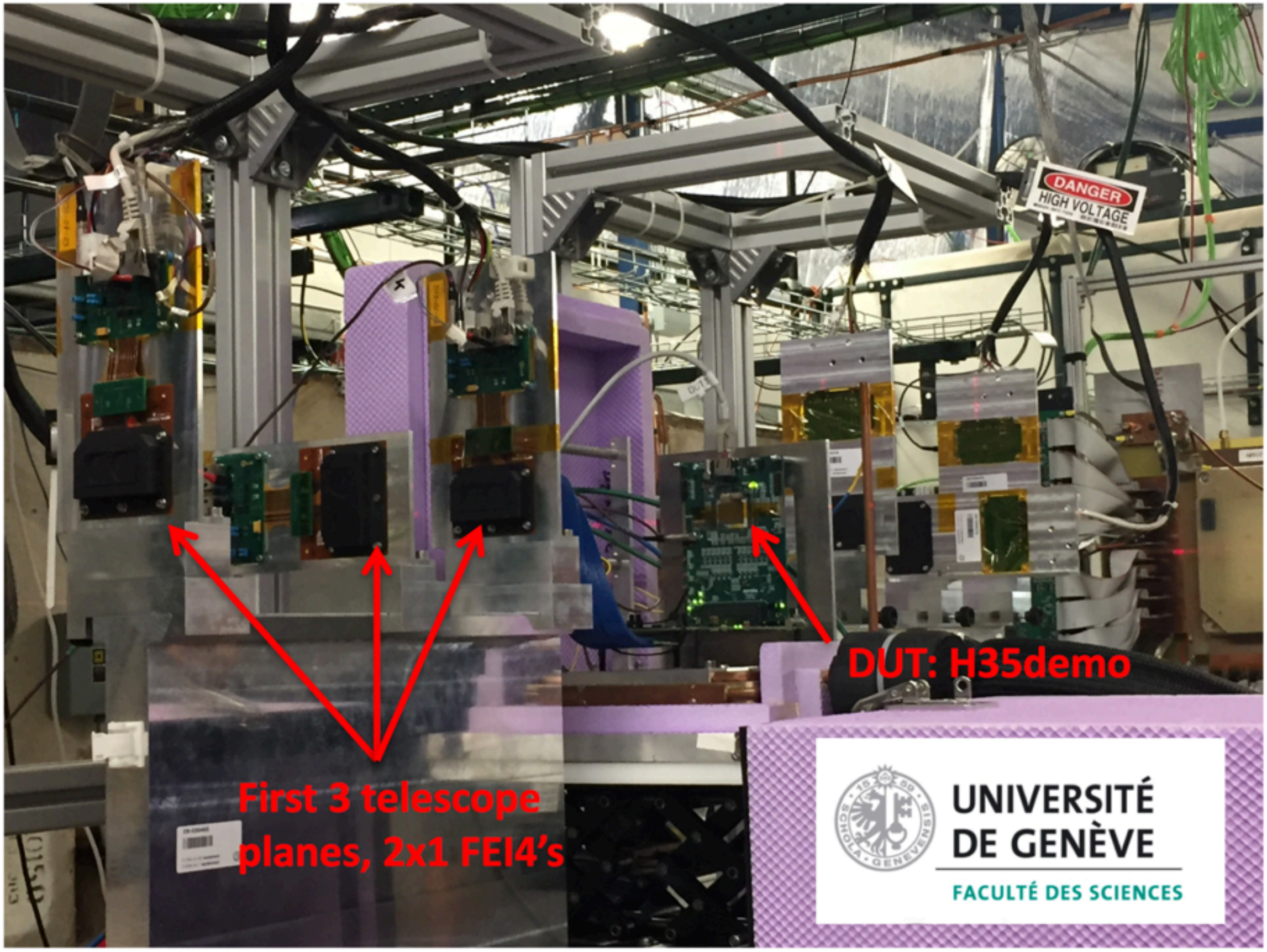
- Measurements were made using the U. Geneva telescope, with six telescope planes based on existing silicon pixel technology, read out via FE-I4 chips.

- DUT held in isolated sample box, cooled via chiller to as low as -30°C. Sample stage is controllable remotely via a motorized stage.

- 120 GeV proton beam, with a ~4.5 second spill per minute, consisting of around 3 million counts per spill.

# Our Test Beam Team

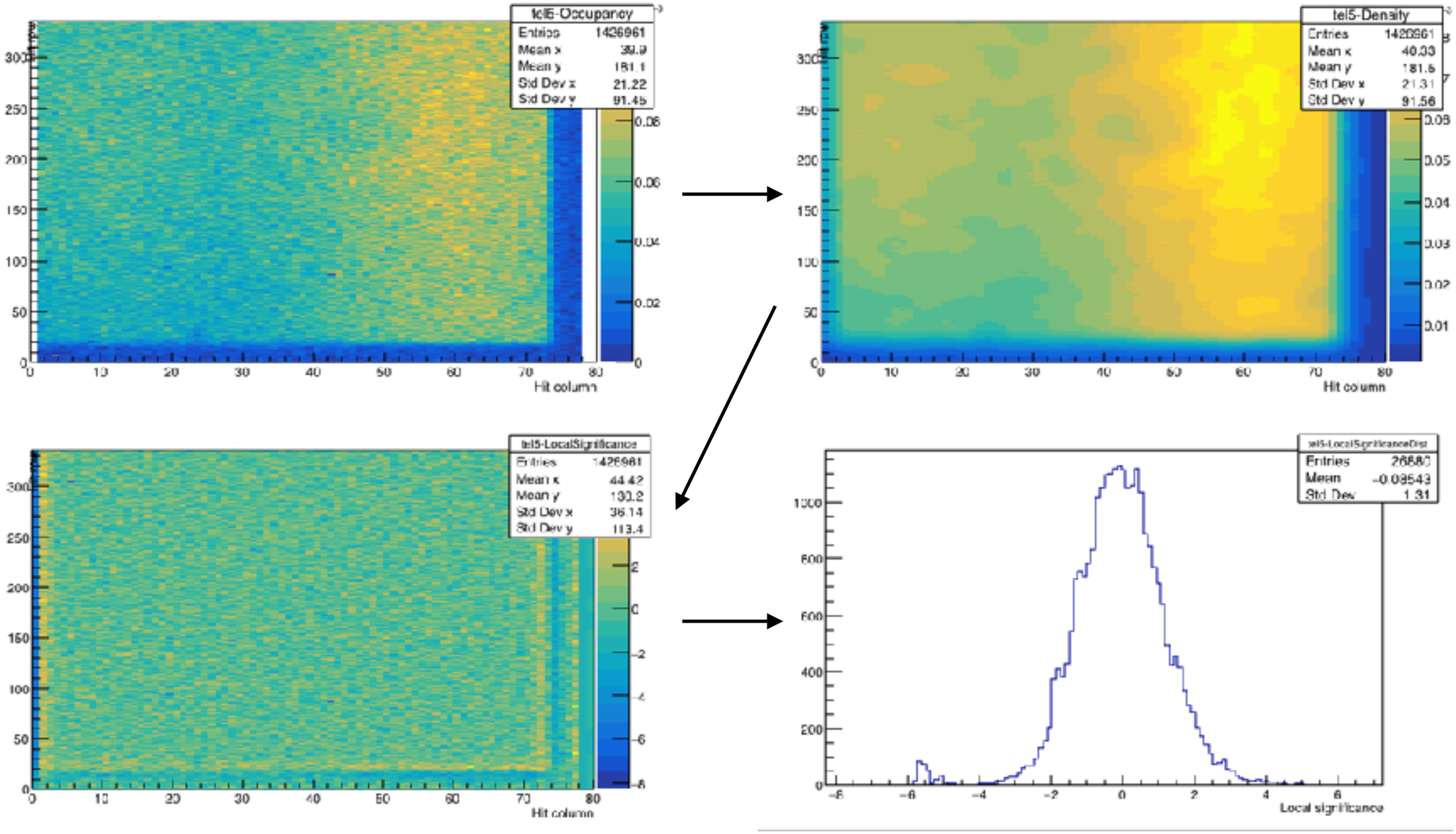
Francesco Armando Di Bello (U. Geneva)
Mathieu Benoit (U. Geneva)
Sergei Chekanov (Argonne)
Dylan Frizzell (University of Oklahoma)
Moritz Kiehn (U. Geneva)
Hongbin Liu (BNL)
Lingxin Meng (U. Geneva)
Jessica Metcalfe (Argonne)
Larry Nodulman (Argonne)
Mateus Vicente Barreto Pinto (U. Geneva)
Rui Wang (Argonne)
Tom Weston (Bern)
Junqi Xie (Argonne)
Ettore Zaffaroni (U. Geneva)
Matt Zhang (University of Illinois Urbana-Champaign)


DANGER
HIGH VOLTAGE
First 3 telescope planes, 2x1 FEI4's
DUT: H35demo
UNIVERSITÉ DE GENÈVE
FACULTÉ DES SCIENCES

# Data Analysis

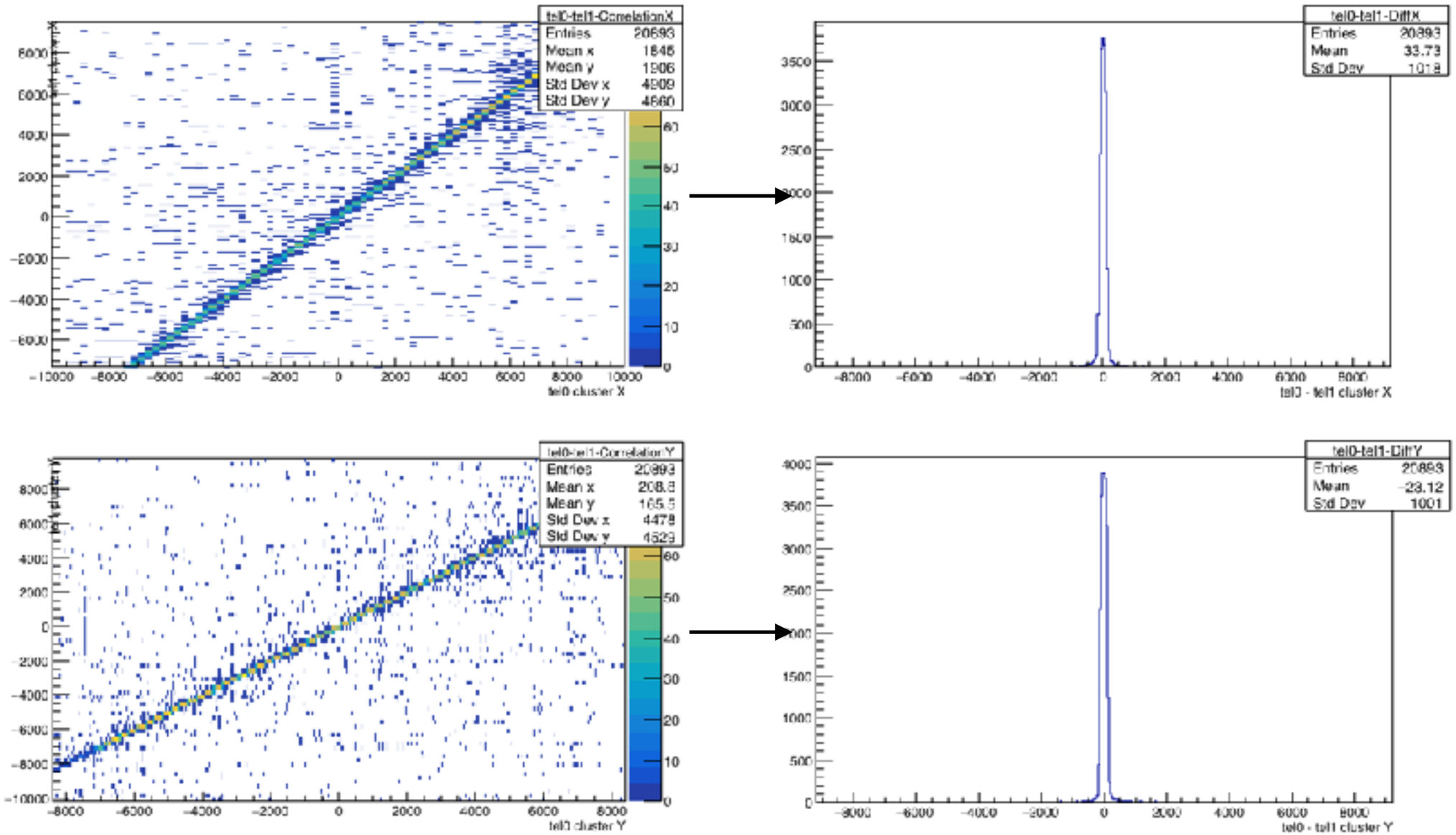
- Analysis consists of the following steps:
    - Noise scans on telescope planes and DUT - mask all pixels with noise 5 sigma above the mean
    - Rough alignment of telescope planes - align positions using pixel correlation, keeping the first plane fixed
    - Fine alignment of telescope planes - find tracks and minimize chi2
    - Rough and fine alignment of DUT - keeping telescope planes fixed, fit the position of the DUT
    - Track reconstruction using the telescope planes, requiring hits on a minimum of five planes (majority of events are one-track events)
    - Track-cluster matching on both telescope and DUT planes
- Following results shown using a sample with a resistivity of 200 Ωcm and a thickness of 725 μm

# Noise Scans




ATLAS Work in Progress

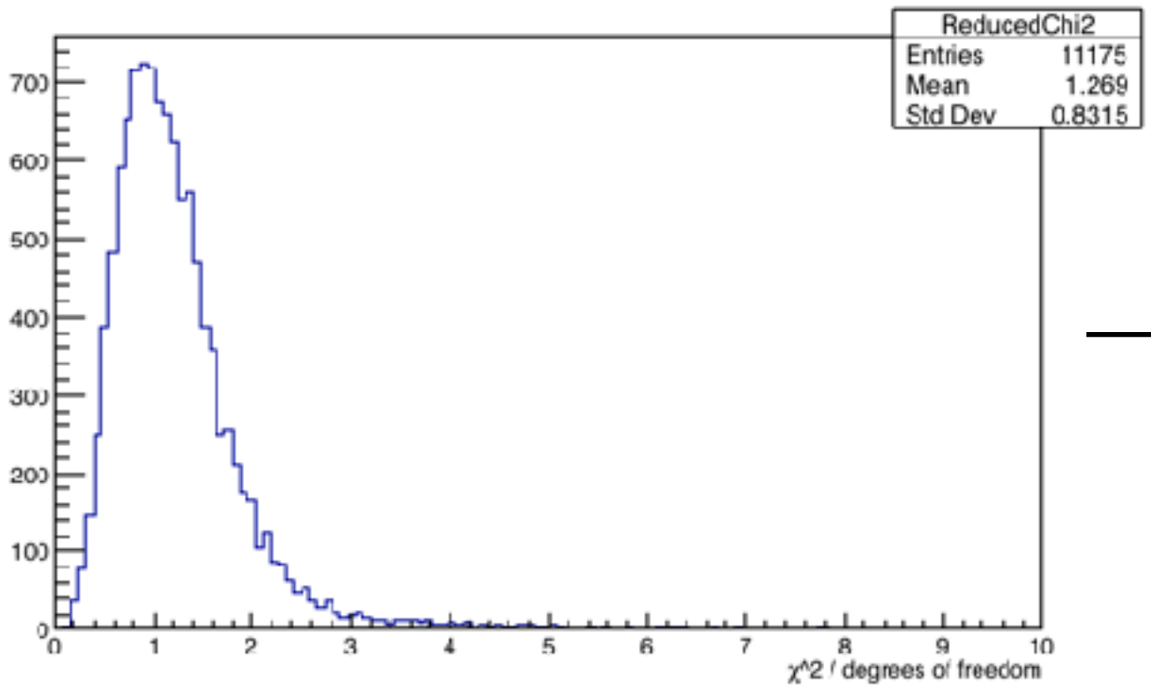
# Rough Alignment



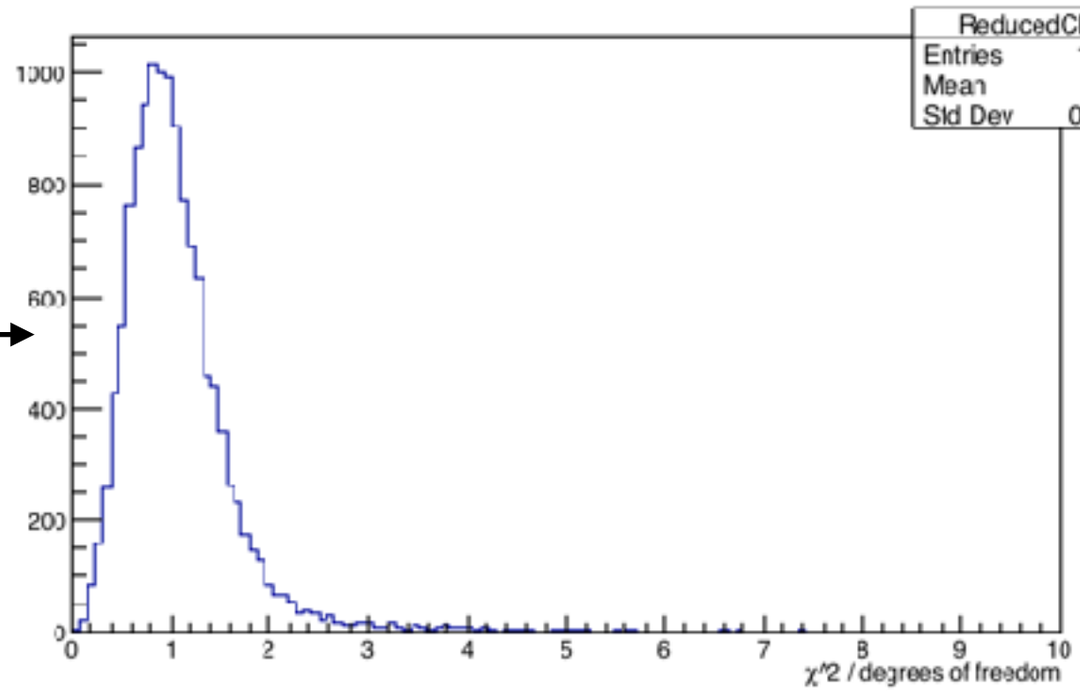

ATLAS Work in Progress

# Fine Alignment

Iteration 1

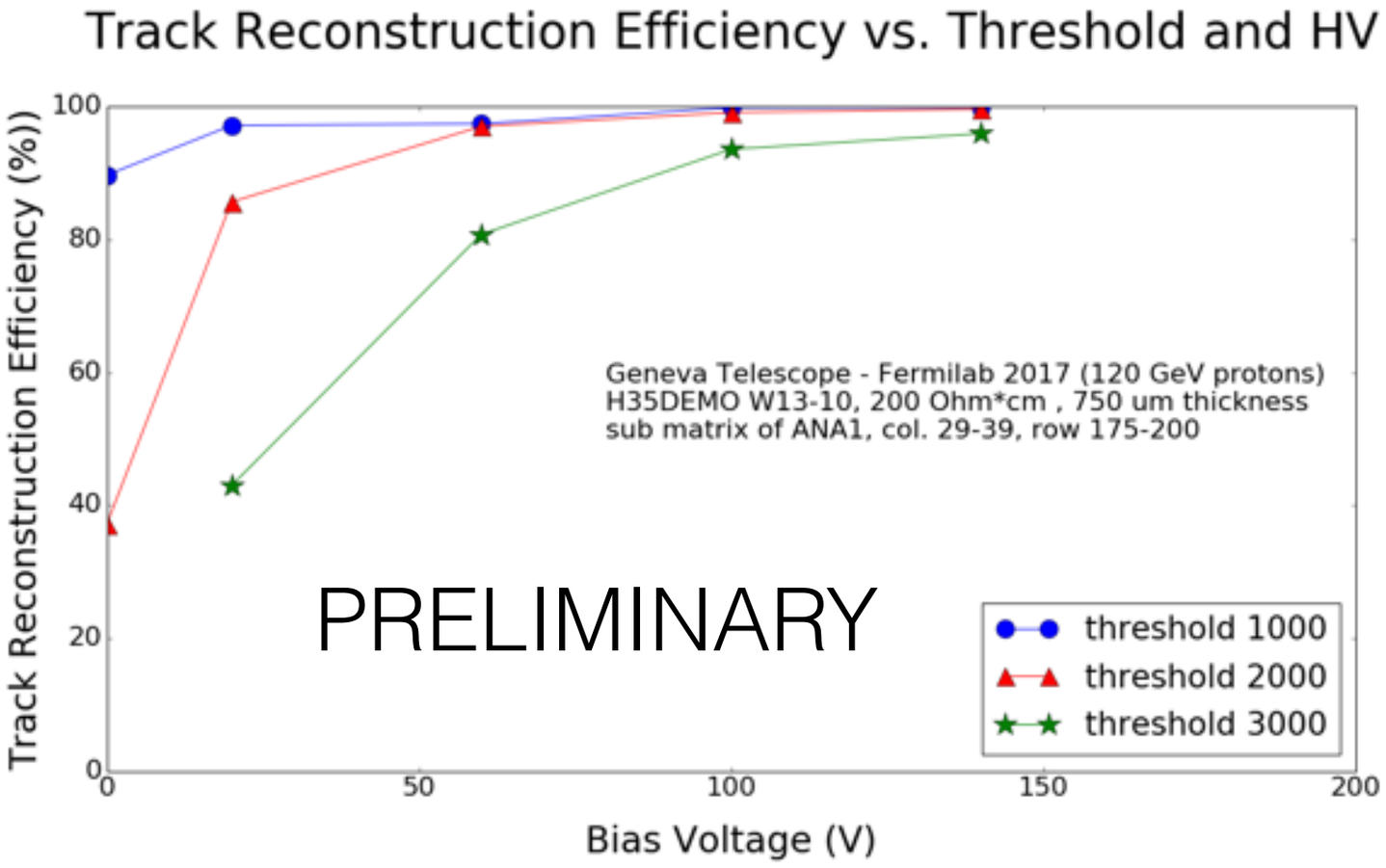



Iteration 20




ATLAS Work in Progress

# Efficiencies




W13-10

| | 0 V | 20 V | 60 V | 100 V | 140 V |
|---|---|---|---|---|---|
| 1000 | 89.71% | 97.22% | 97.46% | 99.90% | 99.93% |
| 2000 | 37.08% | 85.69% | 97.07% | 99.16% | 99.67% |
| 3000 | -% | 42.95% | 80.80% | 93.62% | 95.98% |

# Conclusions

- As expected, track-cluster matching efficiency increases with increased HV and reduced readout threshold

- When HV>=100 V and threshold<=2000 e-, efficiency is above 99%

# Ongoing Work

- First results were promising and we learned a lot from the test beam
- Continued evaluation and development on this technology will be performed
- Test beam ongoing at CERN with new batch of modules
- Lifetime tests being performed using irradiated modules

# Backup

# H35DEMO

**Analog Matrix 1**

CSA uses a folded-cascode with an nMOS transistor as input device without gain boosting
> less noise, better radiation tolerance, increased power consumption

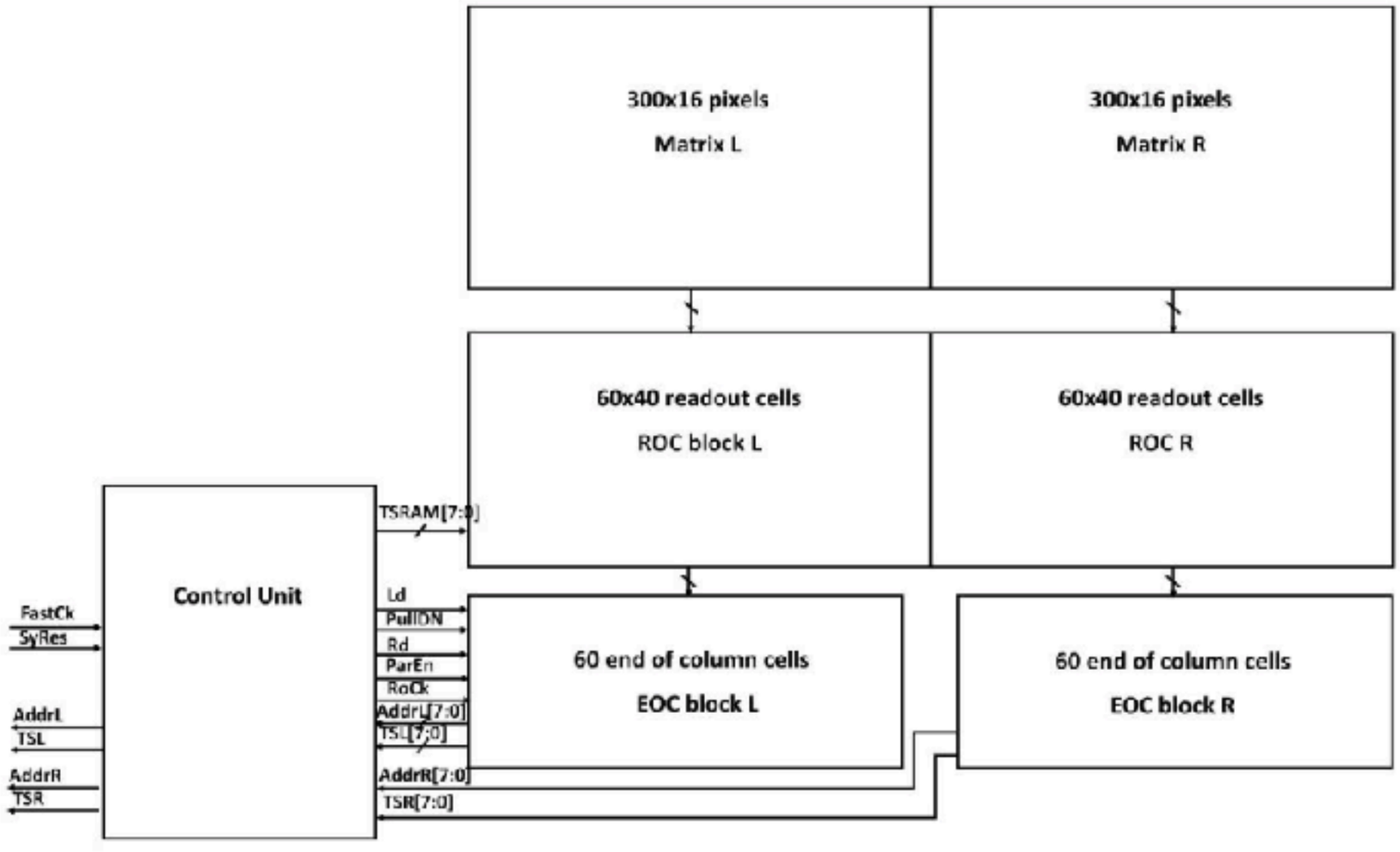
| **Flavour 1** | **Flavour 2** |
|---|---|
| use linear transistors | use enclosed layout transistors |

**Analog Matrix 2**

CSA uses a folded-cascode with a pMOS transistor as input device

| **Flavour 3** | **Flavour 2** | **Flavour 1** |
|---|---|---|
| with DPTUB for HV<br>High Gain | without DPTUB for HV<br>High Gain | without DPTUB for HV<br>Low Gain |

# Pixel Circuitry



# Data Analysis

- Telescope data results analyzed using the Proteus framework.
  - https://gitlab.cern.ch/unige-fei4tel/analysis
- Proteus is based on underlying Judith software, with contributions from authors on the right.

**Authors**

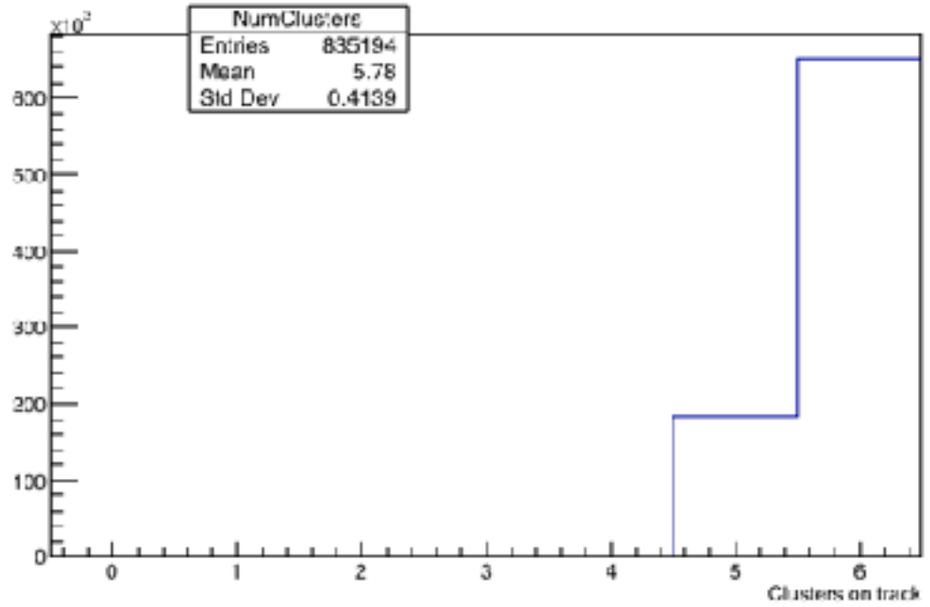
The original Judith software was written by

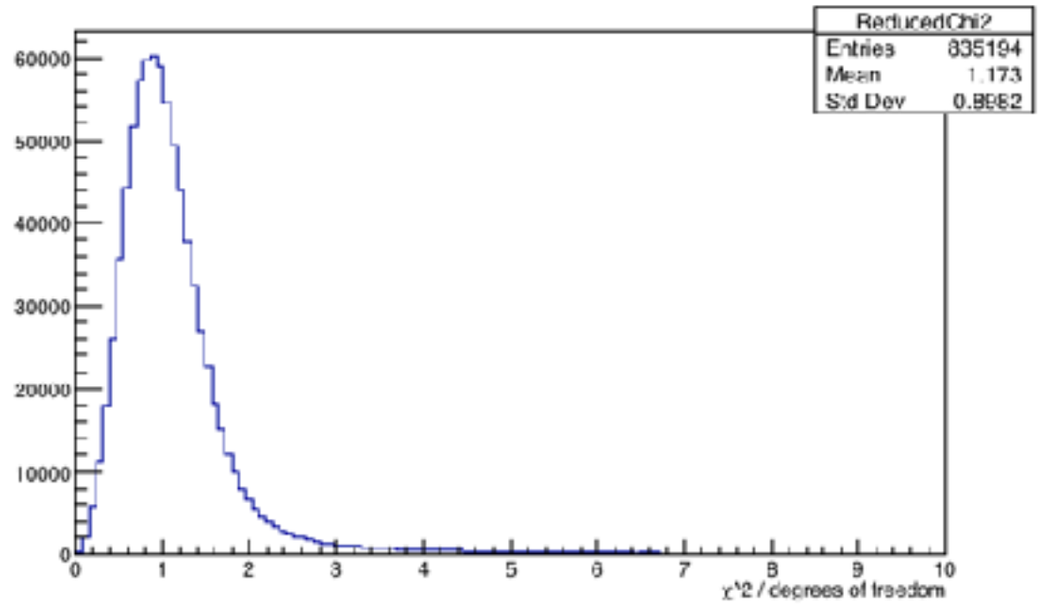
- Garrin McGoldrick
- Matevž Červ
- Andrej Gorišek

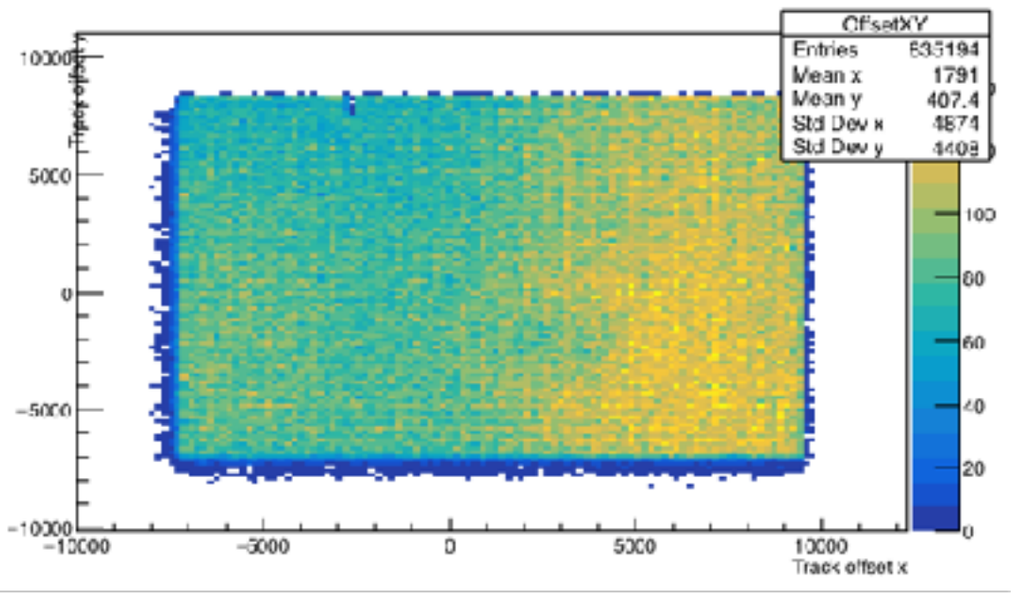
The Proteus fork has seen contributions from (in alphabetical order):

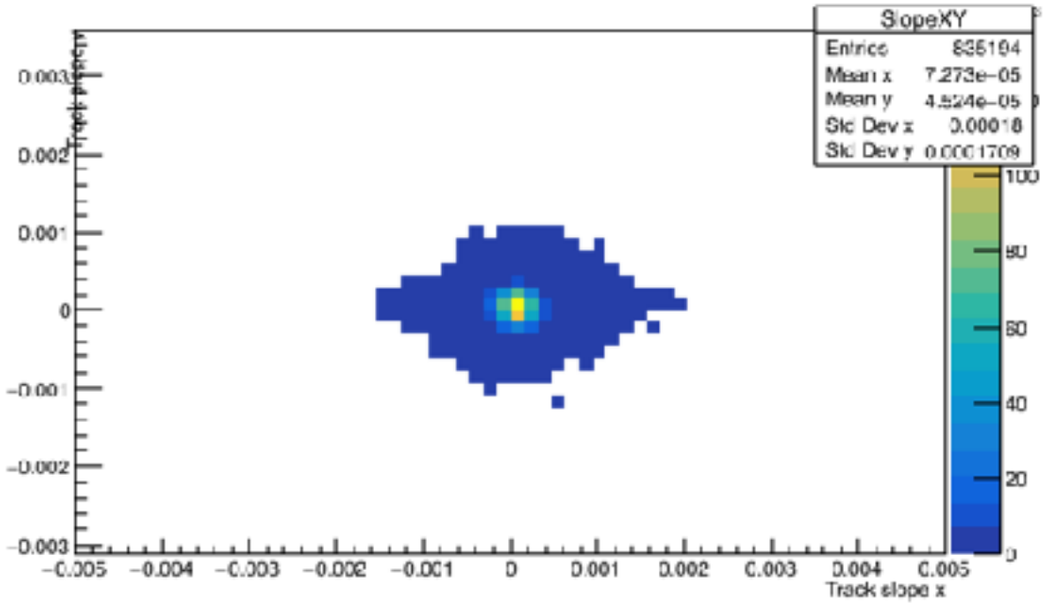
- Javier Bilbao de Mendizabal
- Reina Camacho
- Francesco Di Bello
- Moritz Kiehn
- Lingxin Meng
- Marco Rimoldi
- Branislav Ristic
- Sergio Gonzalez Sevilla

# Track Reconstruction

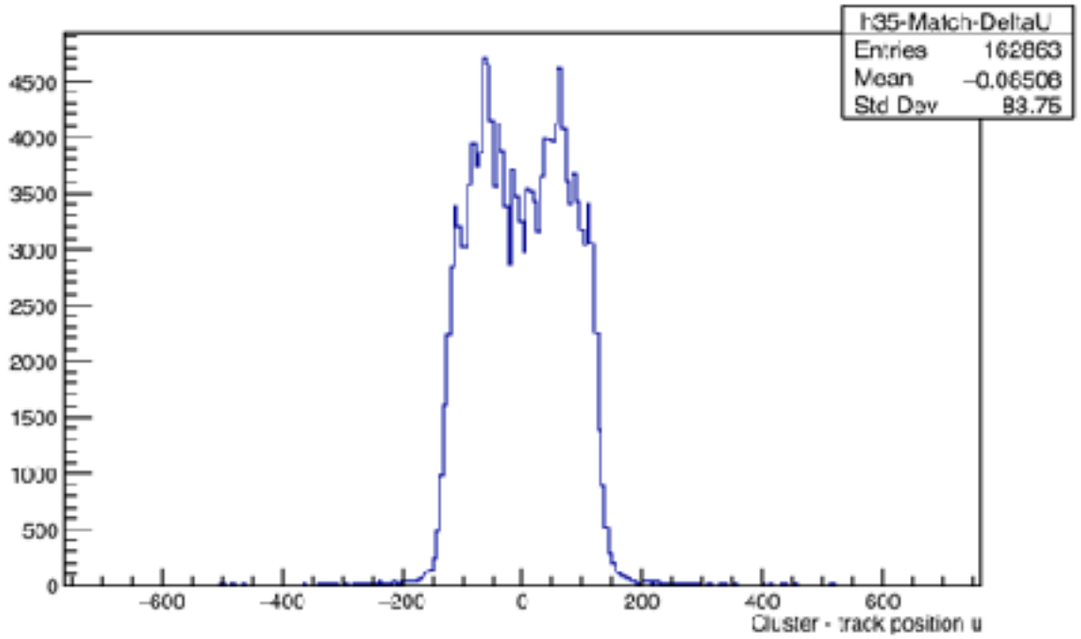


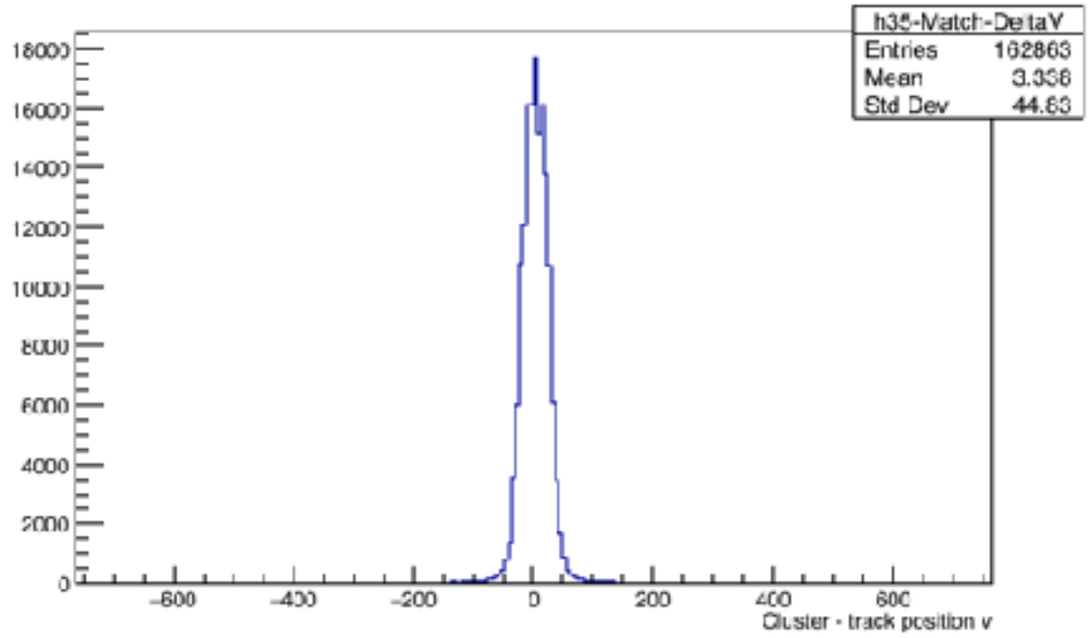



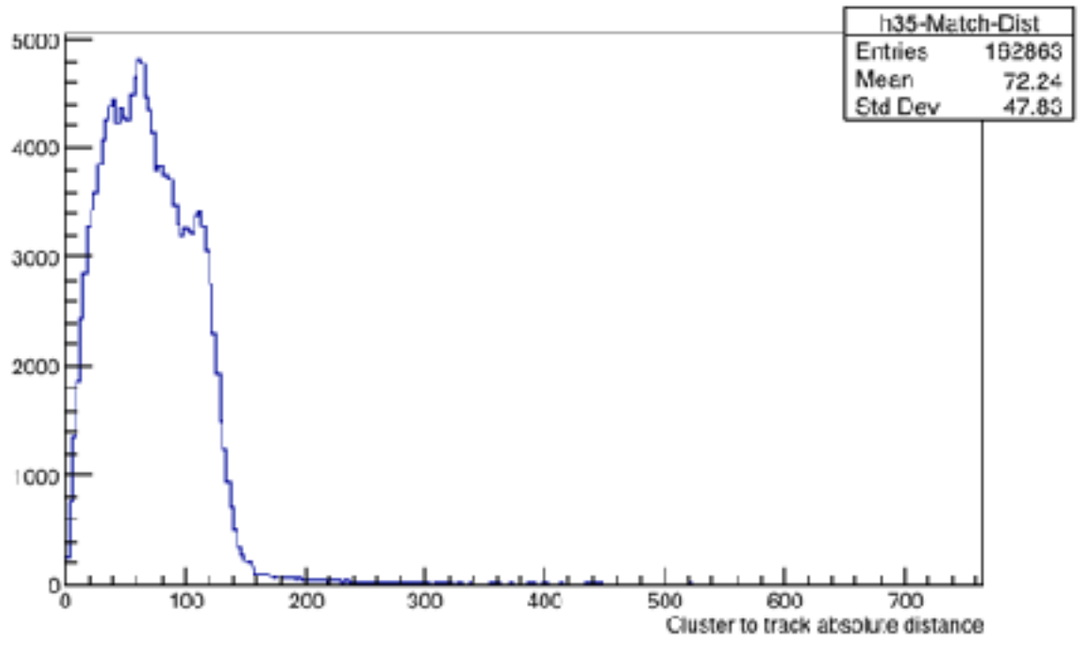



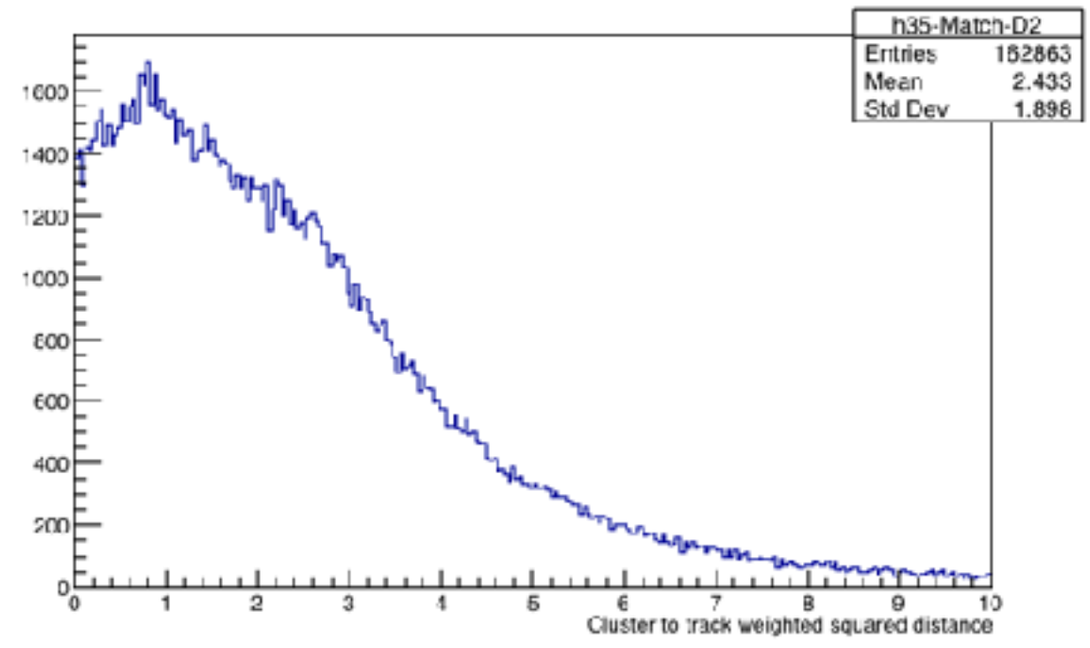



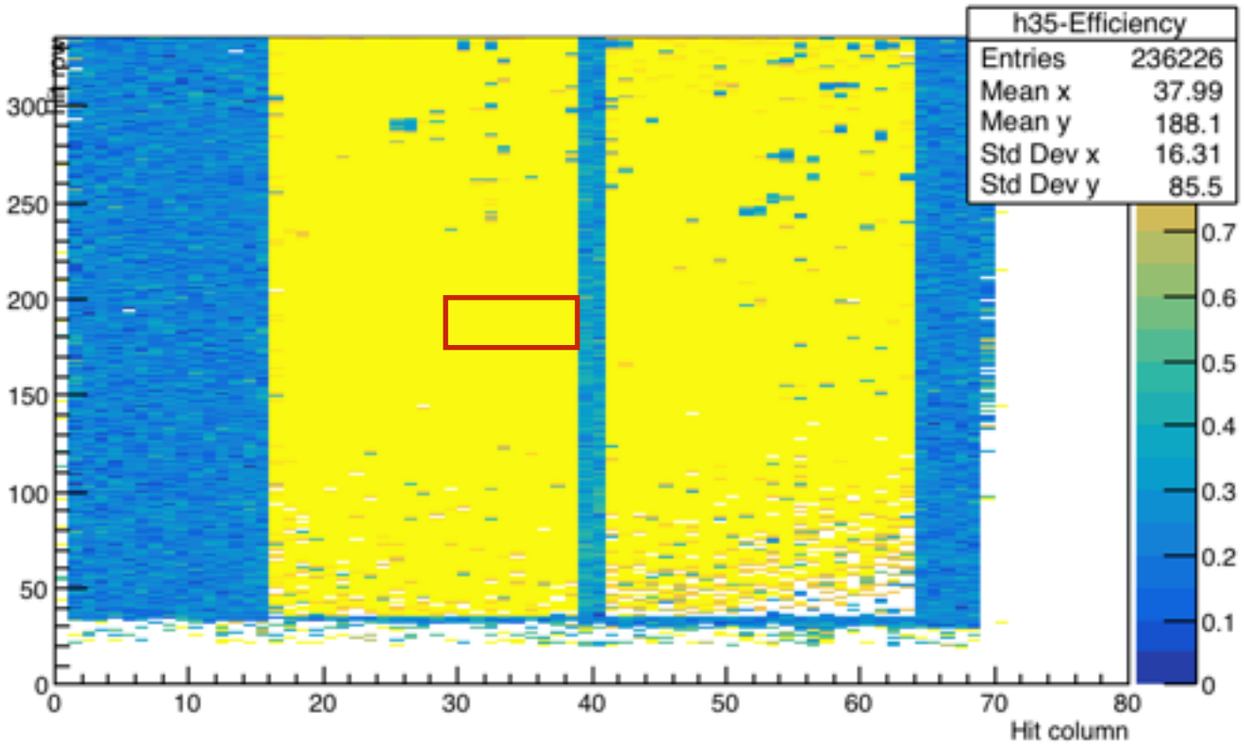
# Track-Cluster Matching






Results are preliminary, and module assembly needs to be tuned.

Currently choosing subsection with good performance to show unimpeded efficiency of technology.