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Track Reconstruction Efficiencies with the H35DEMO HV-CMOS Pixel Detector

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The high-luminosity upgrade of the Large Hadron Collider (LHC) scheduled for 2025 requires an upgrade to the pixel sensor technology in the inner tracker of the ATLAS detector. One candidate is based on commercial high-voltage CMOS (HVCMOS) technology. This design can remove the need for an external readout chip by placing all readout circuitry in the sensor itself, thus providing improved signal sensitivity at a lower cost and reduced material budget. In this talk, we present results using the H35DEMO module, a step towards the fully monolithic HVCMOS detector. This module was created using 350 nm technology, and includes in-chip analog amplification, with discrimination and readout still provided by a capacitatively-coupled external chip. We compare pixel and track reconstruction efficiencies using several variations of the H35DEMO, presenting results with different substrate resistivities, architectures, and applied voltages.

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