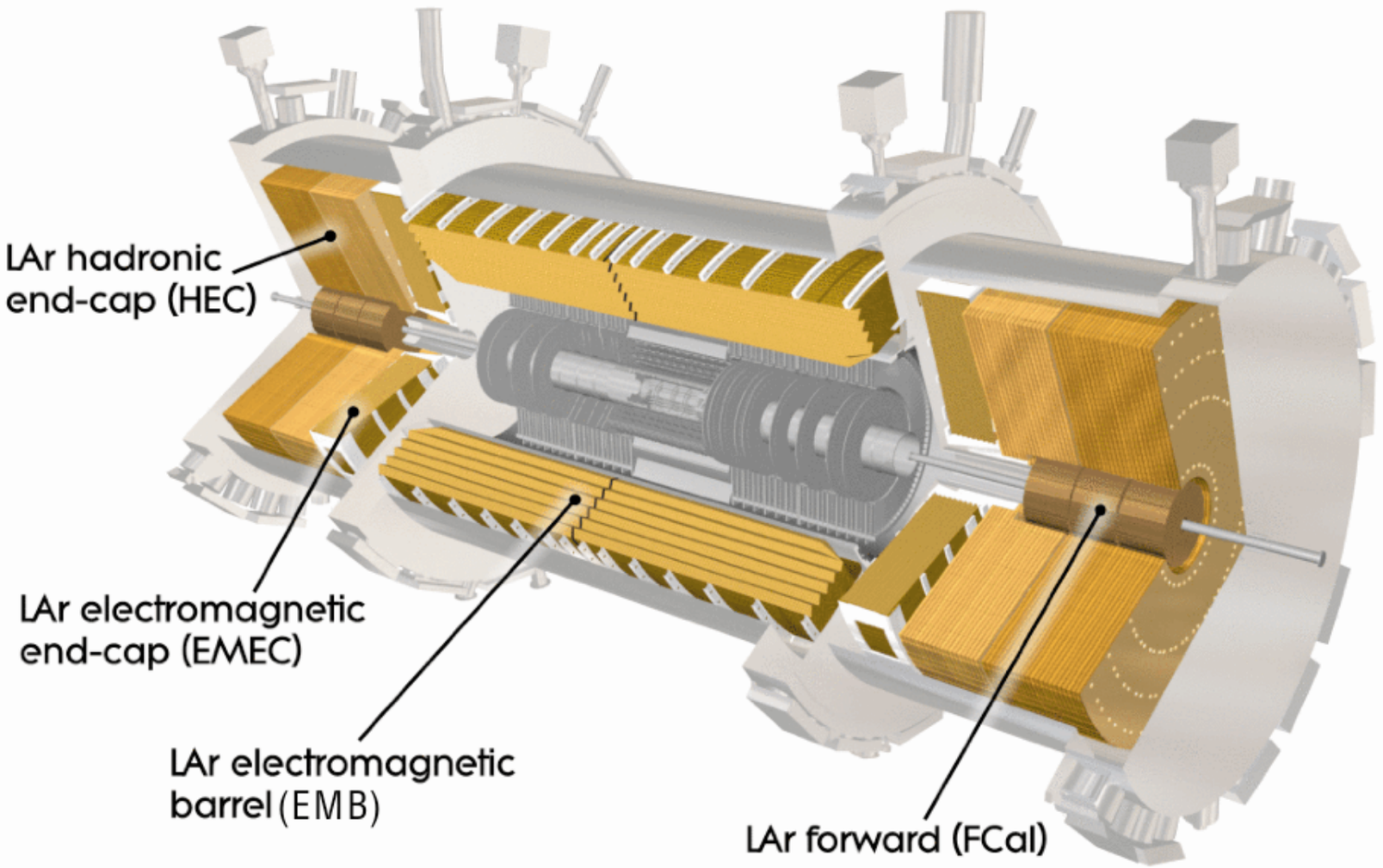
ATLAS Liquid Argon Electronics Upgrade for the HL-LHC

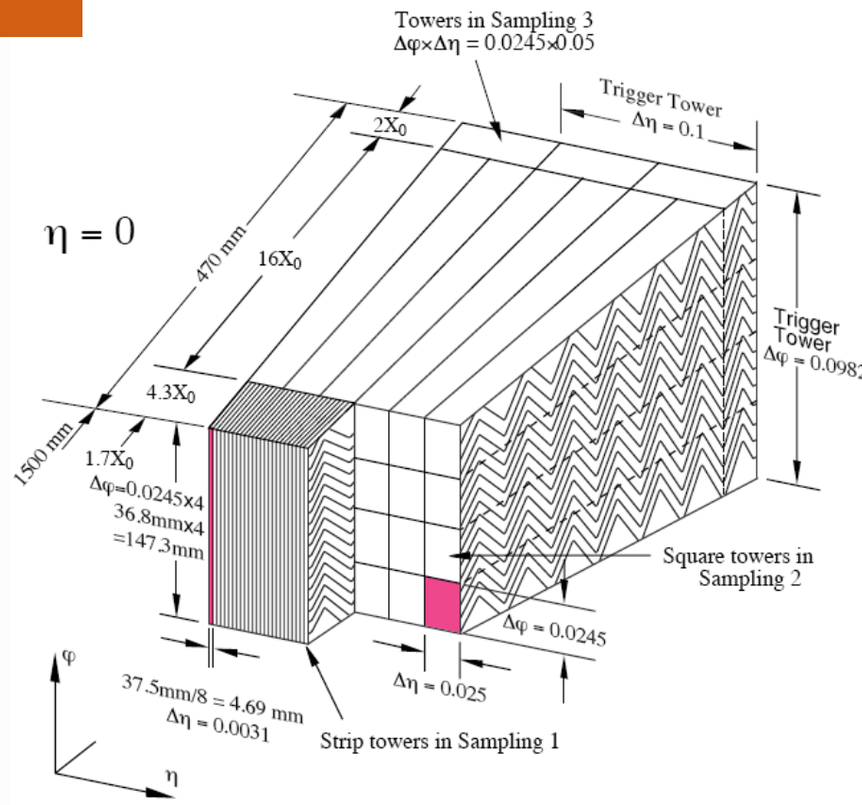
Tim Andeen

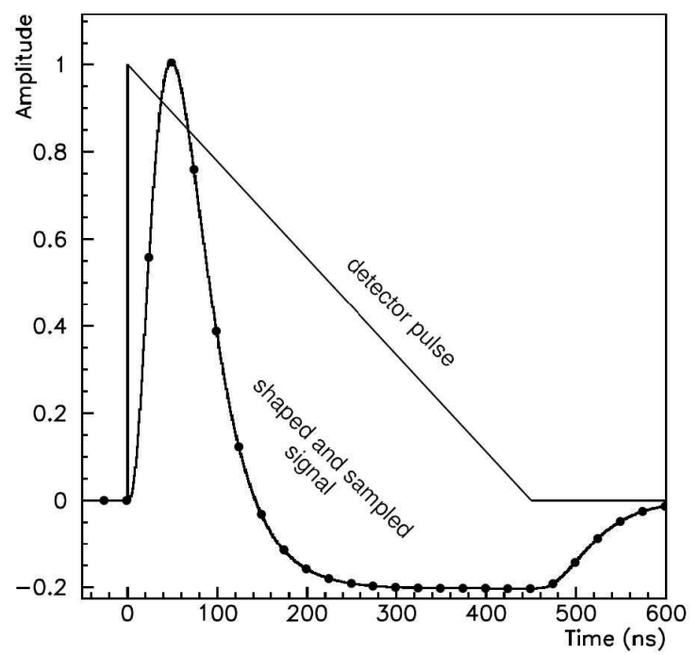
The University of Texas at Austin

APS DPF 2017
August 2

ATLAS Liquid Argon Calorimeter

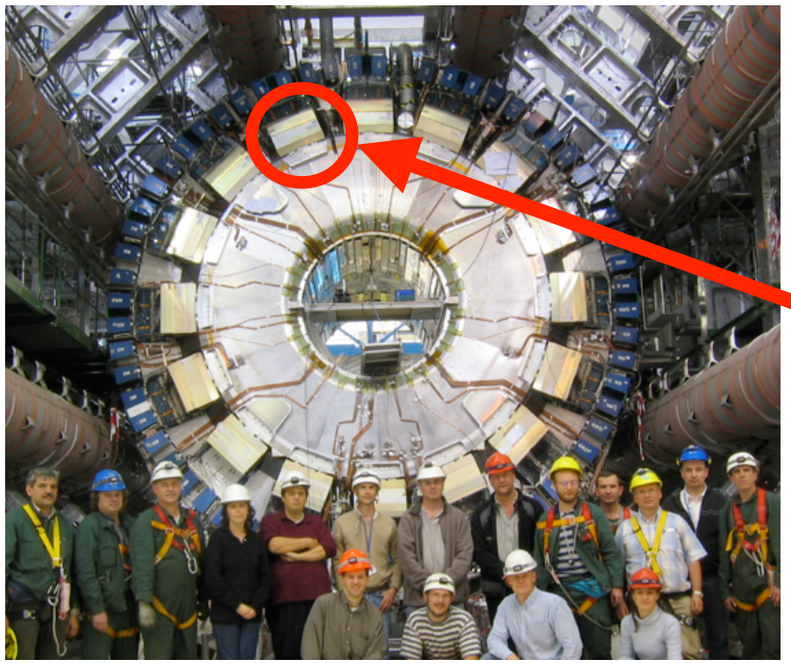


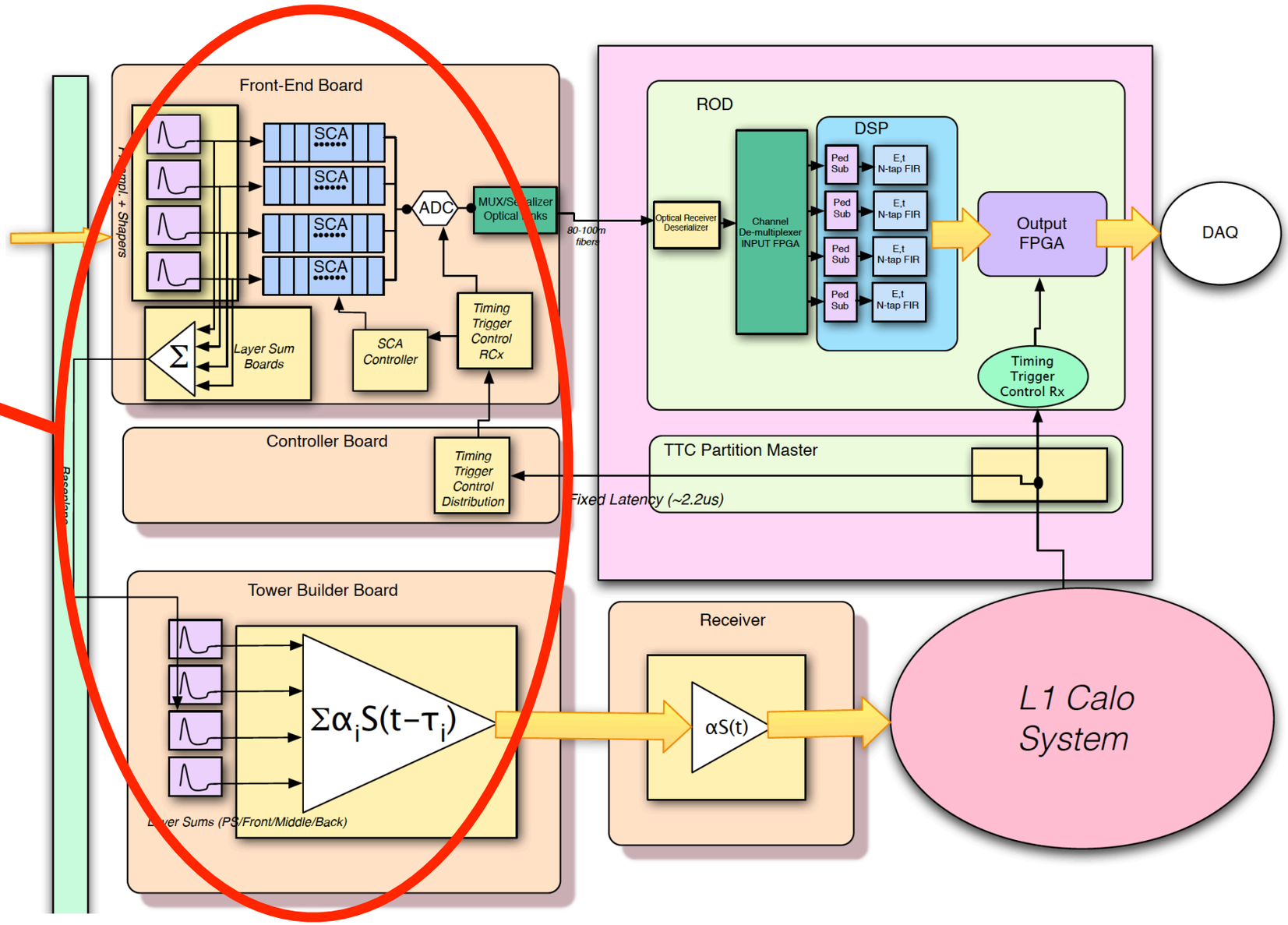




- **Sampling calorimeter**
  - absorber: Pb, Cu, W
  - active: LAr
- 182,468 detector cells
- **Fine granularity**
  - At shower max (middle layer) $\Delta\eta$ x $\Delta\phi$ = 0.025 x 0.025

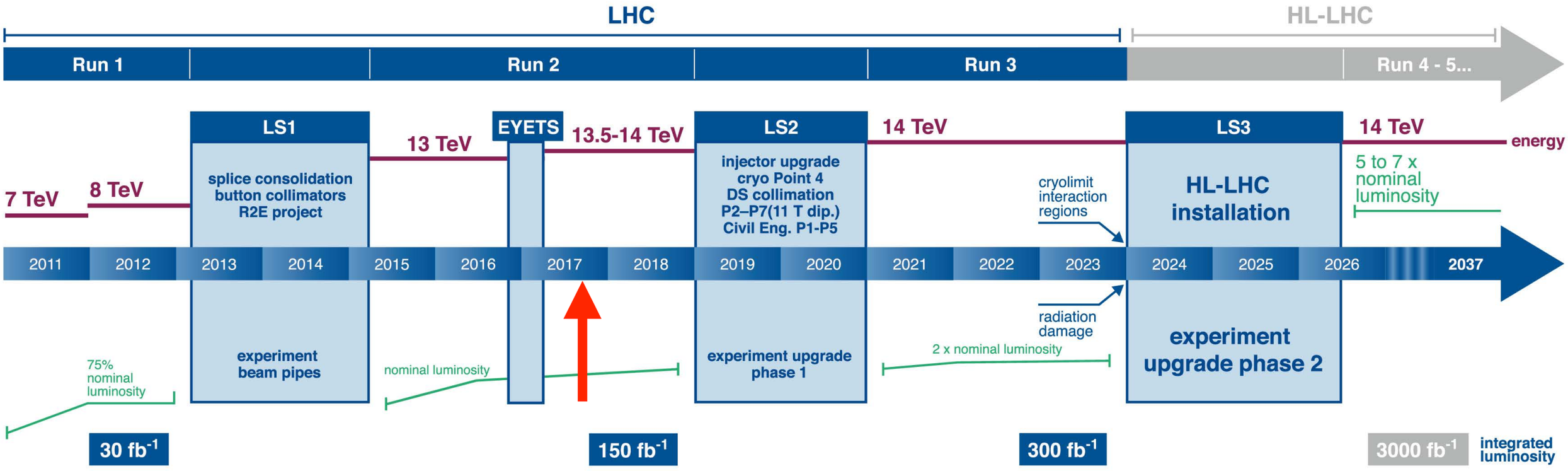
Current Readout





- **Front-end LAr electronics** are located on the cryostat for analog performance.
  - Receives moderate radiation dose.
- Currently we are limited to
  - 2.5 μs latency
  - 100 kHz read-out.

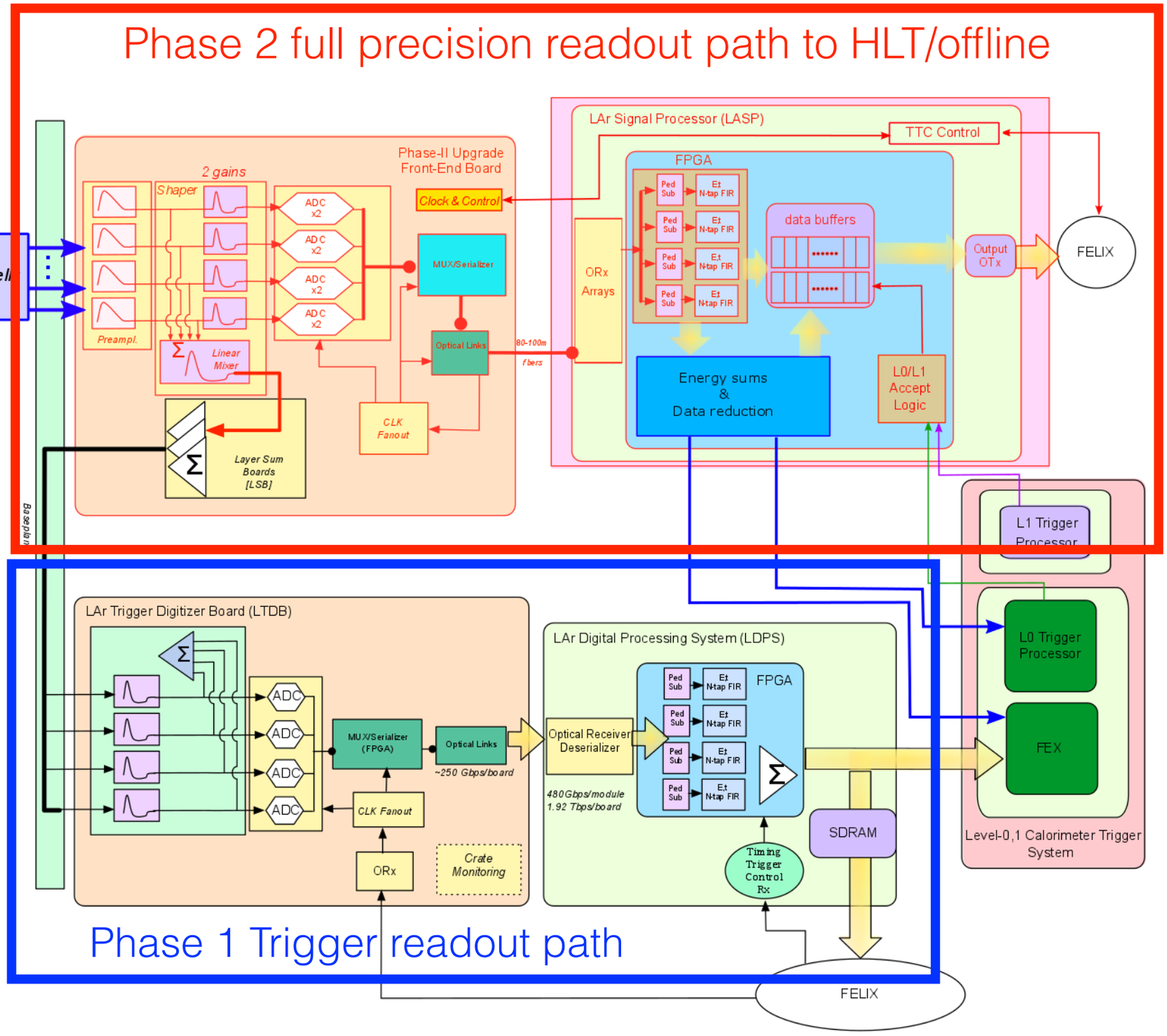
Upgrade for HL-LHC



- **At HL-LHC** (2026) mean number of p-p collisions per bunch crossing of up to 200 (from ~20 today).
- **ATLAS Trigger/DAQ** improvements required to keep pace.
  - ➡ L0-only option: 10 μs, 1 MHz
  - ➡ L0/L1 option: 10 μs, 1 MHz / 35 μs, 800 kHz
- **New LAr electronics architecture**: analog pipeline to “free-running” all-digital design.
- Partial upgrade of LAr electronics is not possible.
  - ➡ Replace all 1524 Front End Boards (FEBs),
  - ➡ and all 120 calibration boards,
  - ➡ and consequently, the off-detector electronics.

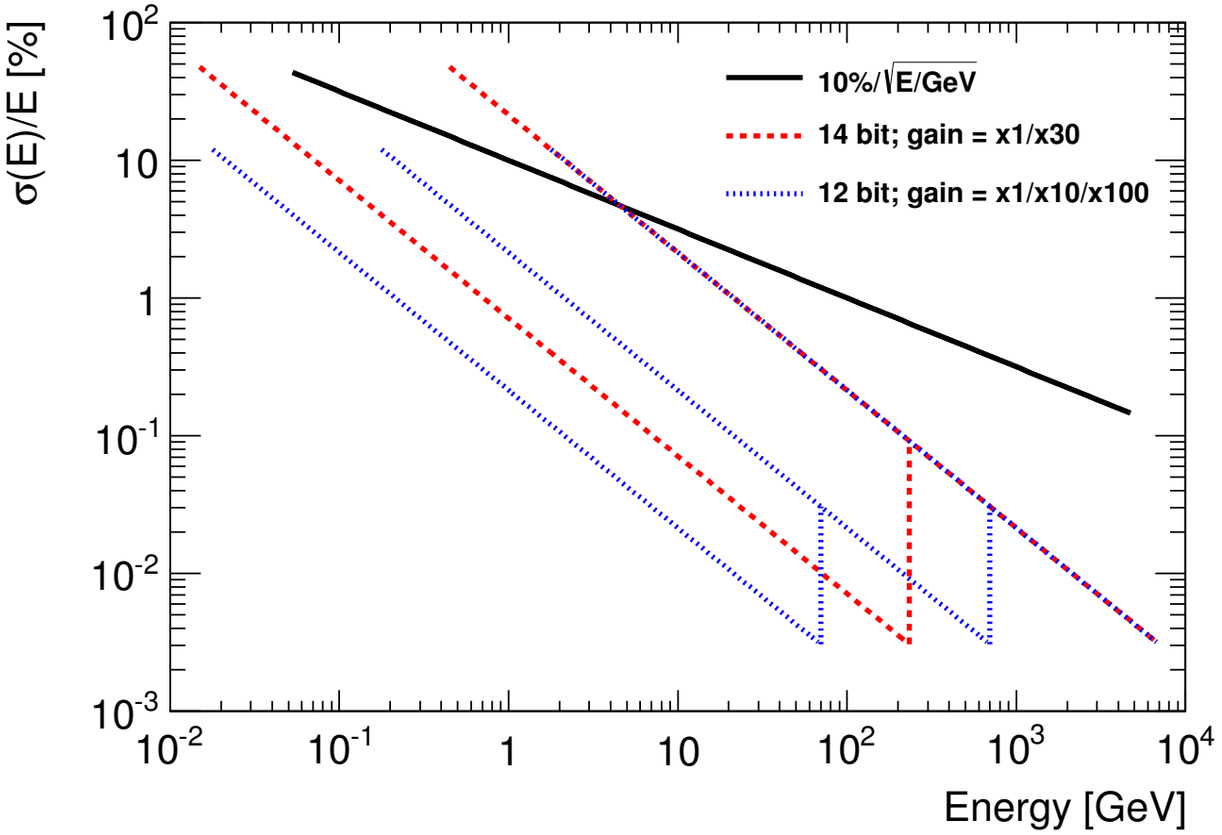
Electronics Requirements

- Cover **full energy range** from electronics noise level to highest possible energy deposited in a single cell: 50 MeV to ~3 TeV.
- **Linearity** of 0.1% up to ~10% of the dynamic range.
- **Low electronics noise**, below intrinsic calorimeter resolution:
  - effectively ~11-bit precision at high energy
  - equivalent precision in analog signal shaping
- **All data sent off-detector**:
  - 1.3 Gbps per channel (two gains)
  - ~180 Gbps per front-end board
  - ~275 Tbps for the full LAr calorimeter.



Simulation and Front-end Requirements

- Major design choices studied in two types of simulation
  - AREUS - electronics simulation design tool
  - Fully simulated Monte Carlo
- **Critical choice of gain selection**. Progress studying dynamic range (DR) in all detector regions:
- Example: **EMB Middle Layer**:

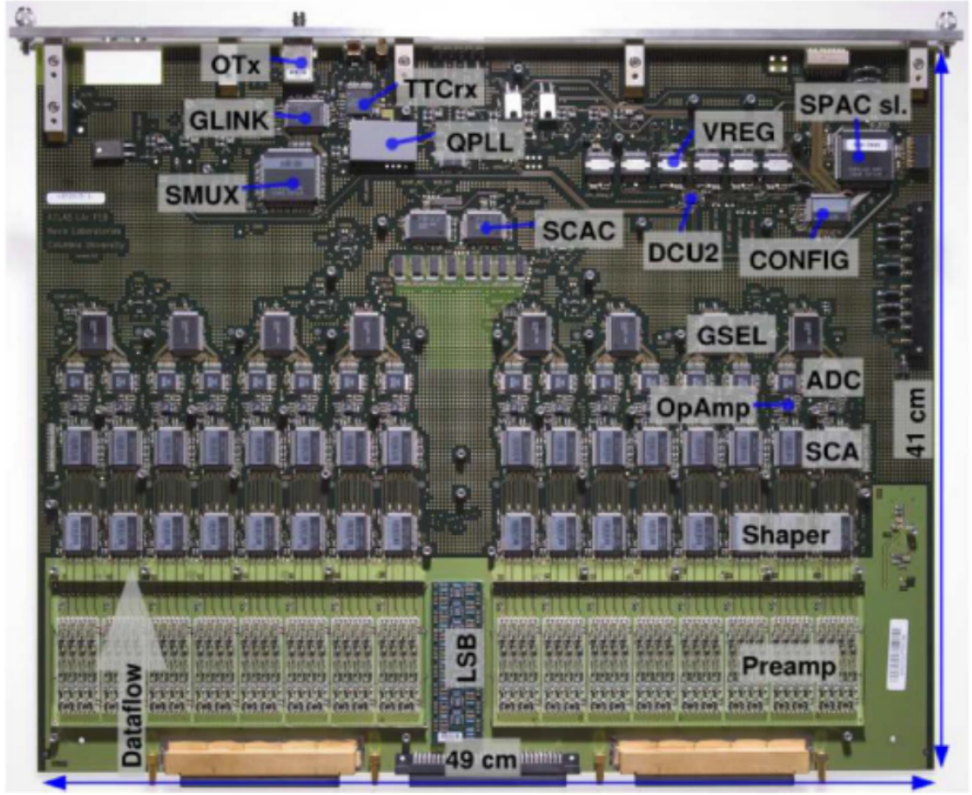


  - In 2 gain system with 1x and 30x gain factor 12b DR and14b DR provide sufficient precision for measuring electronics noise.
  - Gain chosen so both photons from H->$\gamma\gamma$ are (nearly) always in high gain.
  - Measurement of muon MIP can be preserved.

Front-end Board and Calibration Board

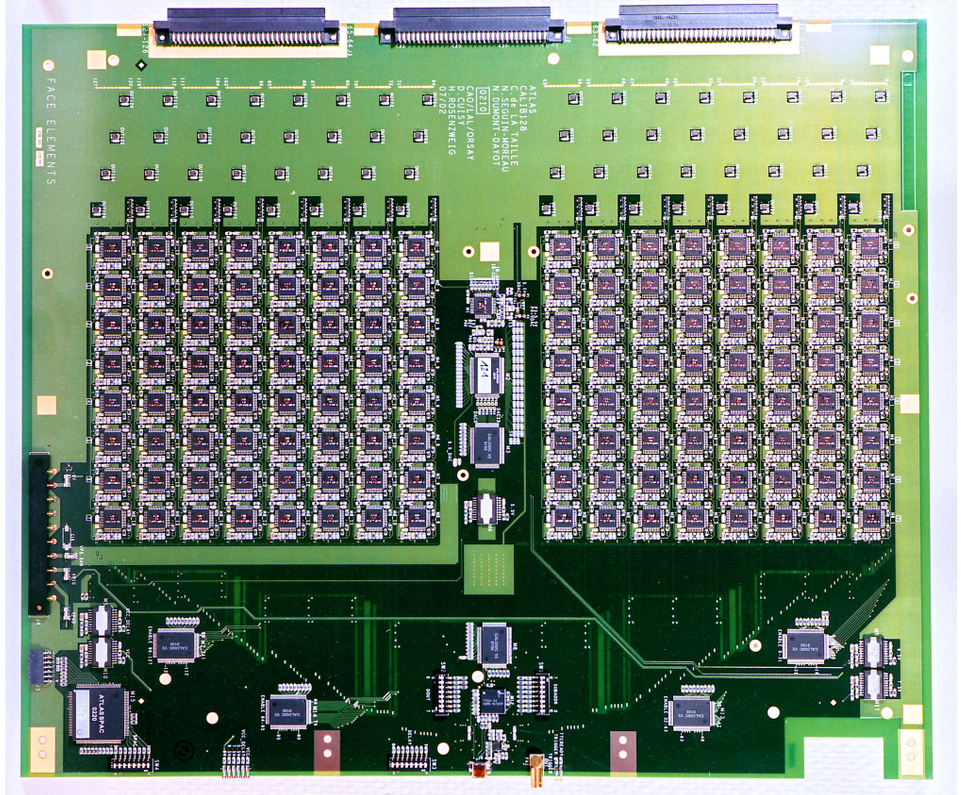
Front-end Board 2 (FEB2)

- Design based on current FEB:
  - Separate analog/digital
  - Well shielded/grounded
  - Shared power (1 - 4 V)
  - Individual control and clock (no control board)
  - 20 data links + 2-4 control links/FEB2 (~35k links for system)

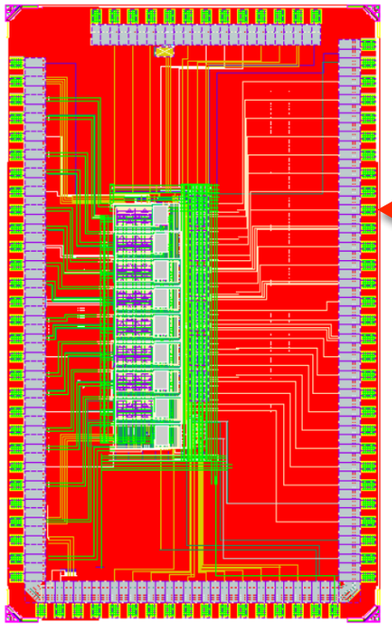


Calibration board

- Sends pulse similar to ionization pulse onto calorimeter cells. Better than 0.25% calibration.
- Studying possible improvements (calibration vs detector position, gain, time) and hardware implications
- Possibility for ramp pulse during bunch train gaps.



Front-end : Pre-Amplifier and Shaper

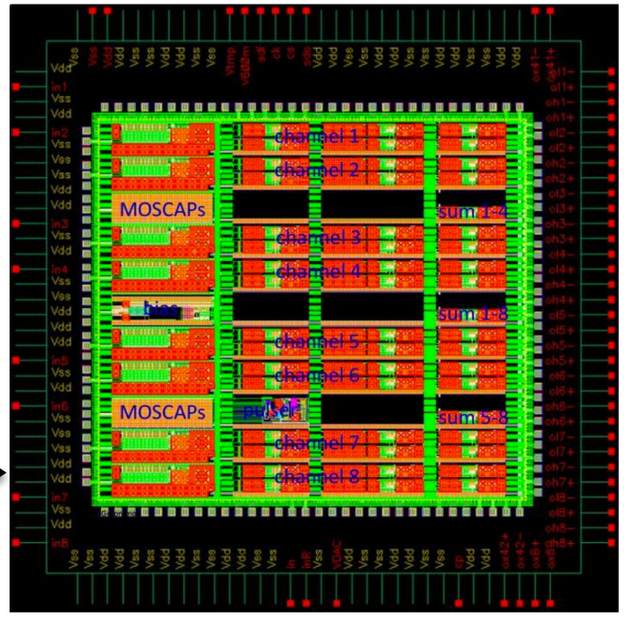


LAUROC: Preamp and shaper ASIC in 130 nm CMOS

- Line-terminating preamp, electrically “cooled” resistor
- 8 channels, various gains
- Testing shows LAUROC meets linearity specification, stable impedance vs input current.

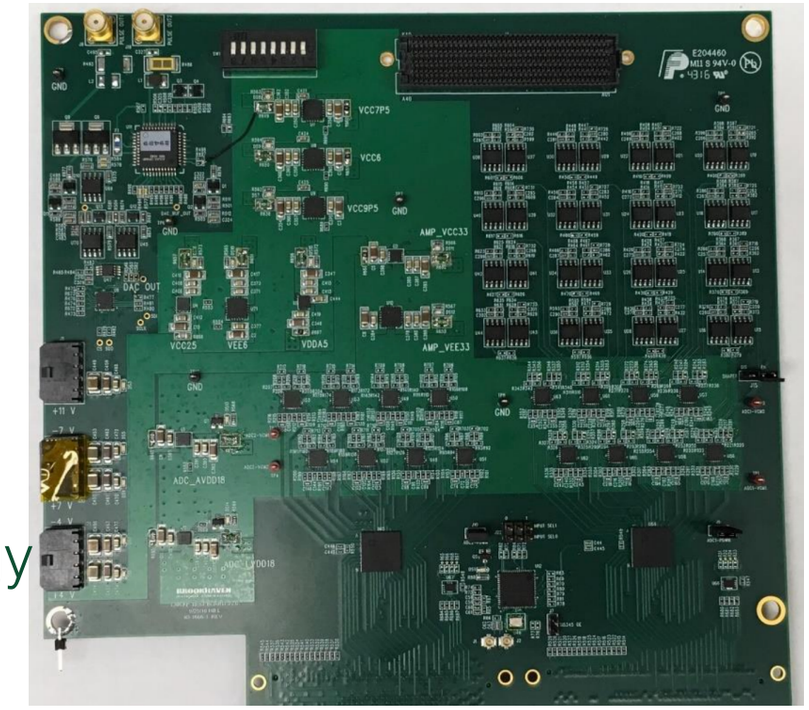
HLC1: Preamp and shaper ASIC in 65 nm CMOS.

- submitted for fabrication
- 8 channels, 2 gains/channel, programmable peaking time, pulse generator.



Front-End Testboard (FETB)

- Common board for both ASICS
- 16x single-ended inputs
- 16x differential inputs
- 2x COTS ADC (16 channels, 14b)
- Calibration pulser, DAQ
- Choosing architecture and technology by end of 2017.



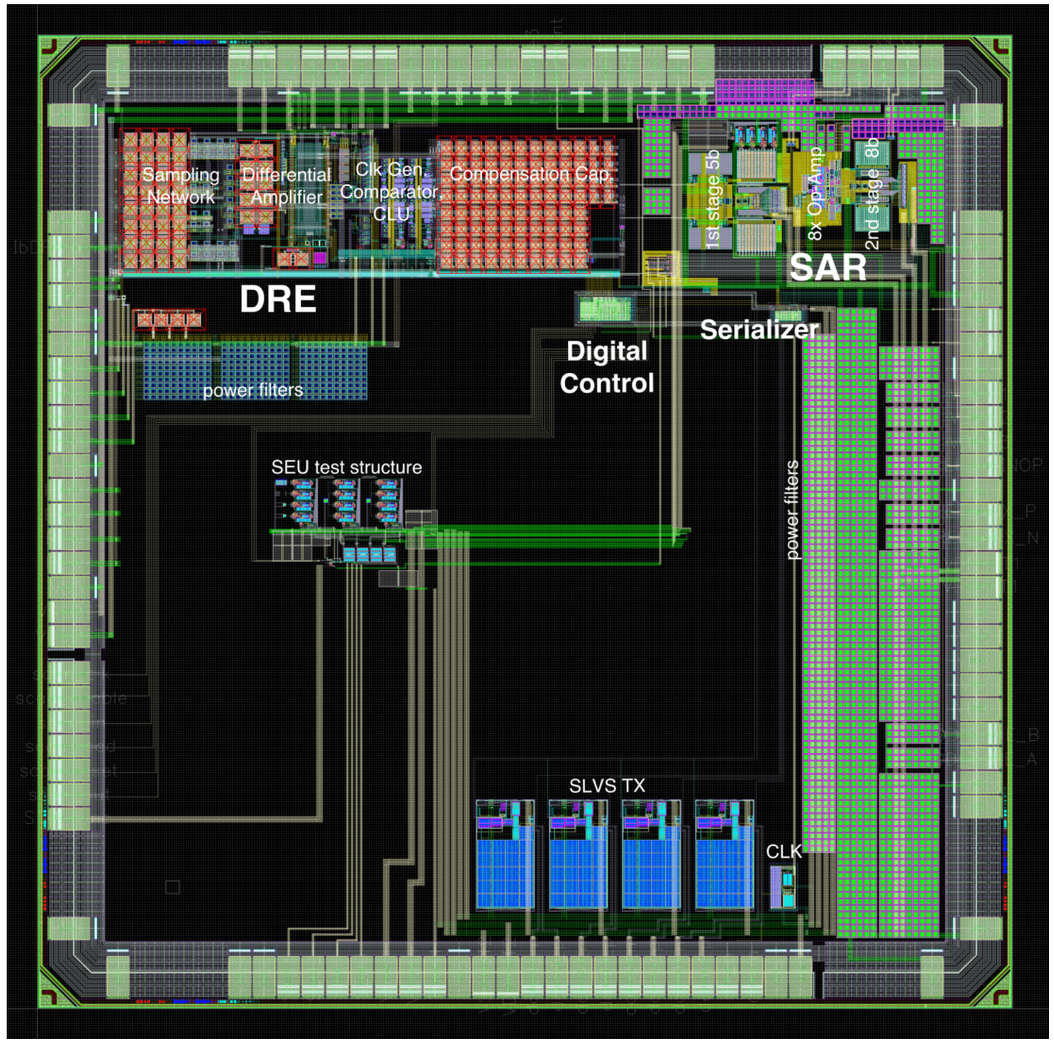
Front-end : Digitization

3 options under consideration:

1. **COTS ADC** - 14b Texas Instruments ADC could be a viable option (of 26 COTS ADC identified).
   - Radiation testing (SEE measurements) studied for Phase 1, more measurements to be done.
   - Requires interface chip.

2. **Purchase ADC IP blocks** - 14b ADC design available in industry.
   - Would be integrated into custom ADC ASIC.

3. **COLUTA ASIC** in 65 nm CMOS.
   - Architecture: Dynamic Range Extender (DRE) + 12-bit pipeline SAR ADC
   - Submitted in May.



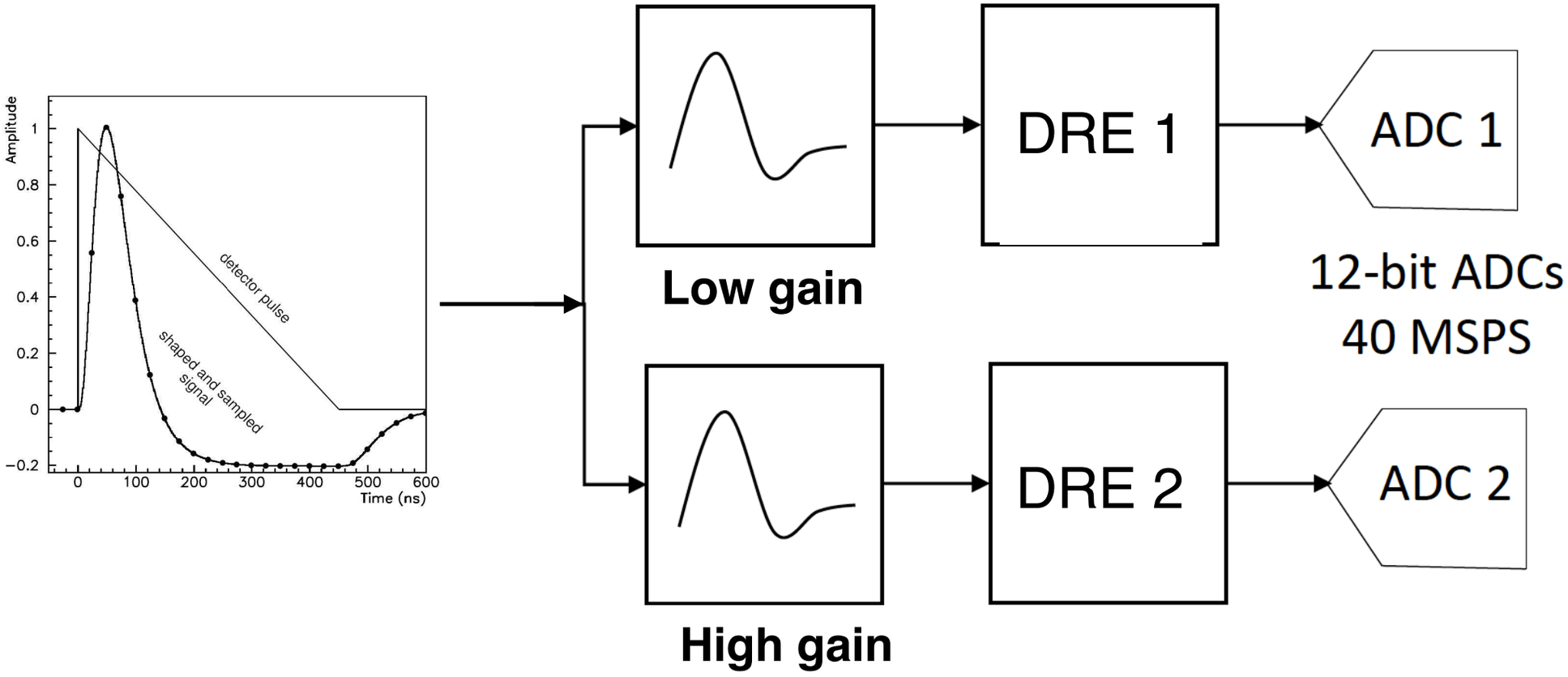
COLUTA ASIC : 65 nm TSMC CMOS

Note: R&D mainly in 65 nm and 130 nm CMOS. Benefits from other HL-LHC work and radiation hard design.

Front-end : ADC ASIC

COLUTA ASIC in 65 nm CMOS.

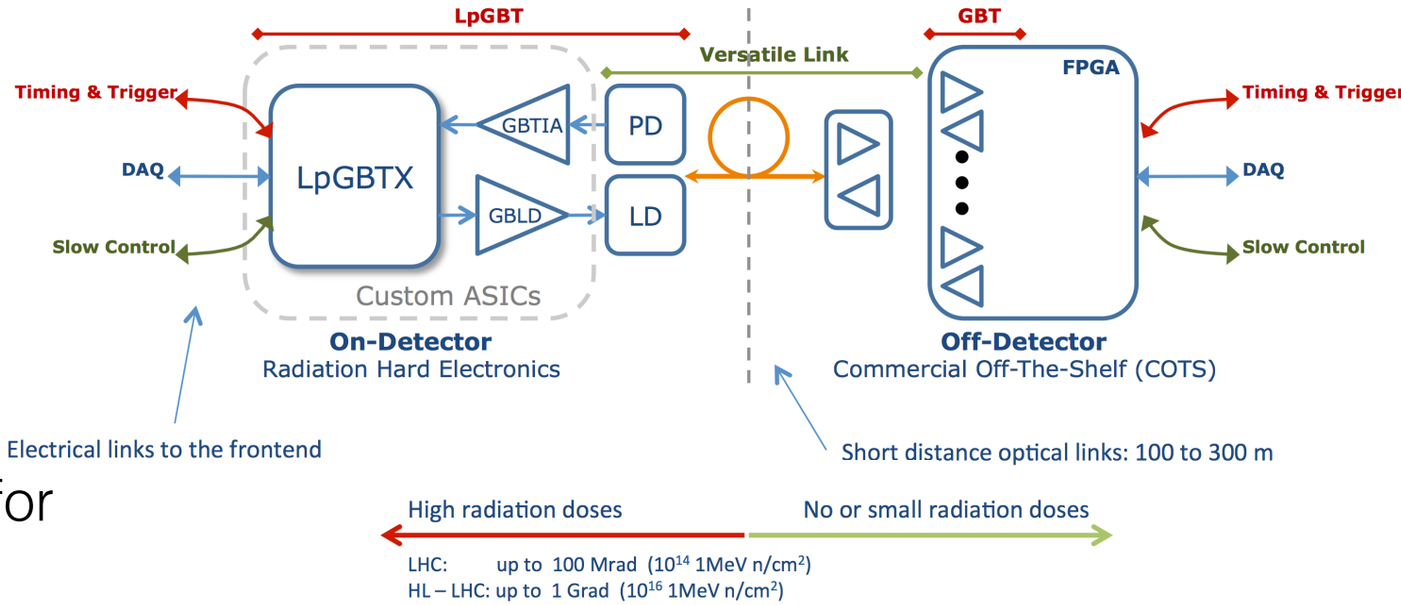
- Dynamic Range Extender (DRE) + 12-bit pipeline SAR ADC
- DRE block is similar to 4x gain amplification, baseline shifted.
- 14b dynamic range, >11b precise SAR in simulation.
- Test chip contains DRE+SAR, rad-hard I/O, bandgap.
- Anticipate approximately yearly submissions to final prototype in ~2020.



Front-end : Optical Links and Power

Links: Each FEB readout by 20 ~9 Gbps, radiation tolerant optical links.

- Use lpGBT and VL+, developed in CERN-based projects
- LAr community is contributing to development.

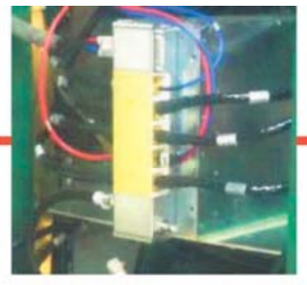


Power distribution: Replacing the LVPS for front-end crates.

- 280 V DC to 1 - 4 V devices with new, intermediate ~24 V step.
- Allows possibility of more accessible locations.
- Rad. qualified converters, long cables identified, under study.
- Investigating fully redundant options for HEC.

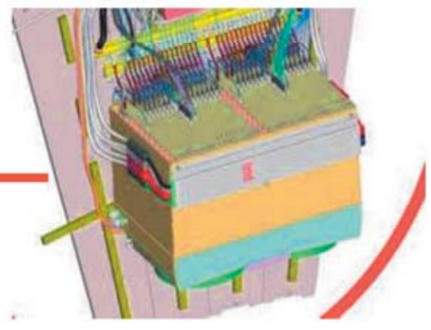
Current power supply, off detector

L = ~60 m
L = ~50 m
L = ~40 m



On detector

L = ~10 m
L = ~20 m
L = ~30 m



Electronics Crate

Off-detector Signal Processor

LAr Signal Processor (LASP) receives fully digitized signals from FE.

- Determines gain selection
- Calculates energy/time per cell
- Digital filtering + shaping to suppress pile-up and noise, based on bunch position.
- Area based pile-up suppression.
- Long latency buffer for L0 (or L1) accept.

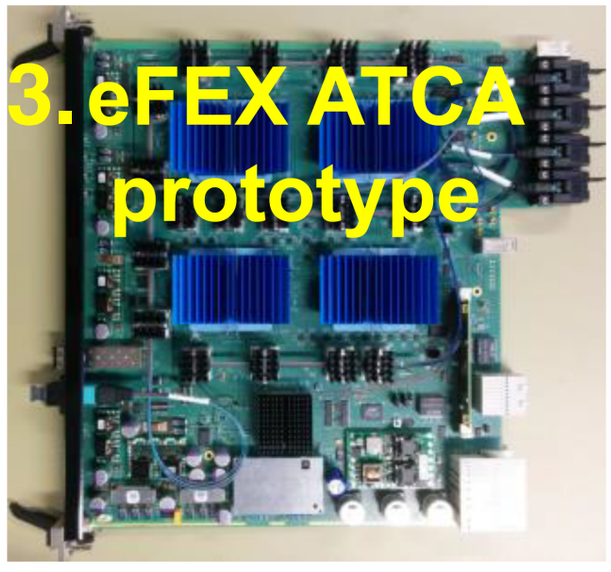
Processing realized in “large” (~4 cm x ~4 cm) FPGA’s (existing FGPA’s meet requirements).

- Each LASP takes data from 4 FEB2 boards
- 20 links/FEB2 (at ~9 Gbps) -> 30,840 total: 100 Tx/Rx transceivers/FPGA.

Studying **3 options**:

1. ATCA + AMC (Phase 1)
2. PCIe + FPGA
3. ATCA main board only

★ **Optimizing fiber count/mapping, memory, processing requirements vs space, power and cost.**



Off-detector Filtering and Trigger Interface

Filtering studies:

- Fully simulated waveforms with pile-up up to $<\mu>$=200 and configurable LHC bunch structure.
- Realistic noise and digital processing.
- Goal is to minimize impact of pile-up on the energy measurement.

Highlights:

- Fully simulated MC samples, optimize filtering for $<\mu>$=200
  - compare to $<\mu>$=0, and to "wrong" filtering determined at $<\mu>$=20.
- Also, AREUS simulation study of filtering in range of pileup conditions from $<\mu>$=0 to $<\mu>$=200.

Trigger Interface:

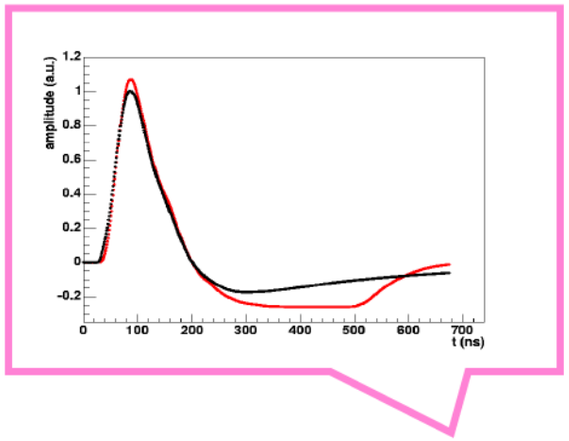
- **LAr electronics sends:** (either L0 or L0/L1 trigger scheme)
  - L0-triggered data to DAQ
  - L0+L1 will scheme buffer on the LASP
  - Potential to send selected cells above energy threshold to trigger processor.

Conclusions

- **All LAr electronics will be replaced for Phase 2 upgrade.**
  - ➡ Current system does not meet rate and latency requirements.
- **Many pieces are coming together now**:
  - ➡ ADC and two preamp/shaper ASICs submitted,
  - ➡ progress on simulation and calibration,
  - ➡ and understanding off-detector processing and trigger interface.
  - ➡ Not discussed: physics performance studies for electrons, photons and jets.
- In parallel, **profit from Phase 1** upgrade experience.
- **It is not so long until 2024!**

Supplementary Slides

Optimal Filtering and Calibration Chain



ADC to DAC (Ramps)

Pulse Samples

$$E_{\text{cell}} = F_{\mu\text{A}\to\text{MeV}} \cdot F_{DAC\to\mu\text{A}} \cdot \frac{1}{\frac{M_{\text{phys}}}{M_{\text{cali}}}} \sum_{i=1}^{M_{\text{ramps}}} R_i \left[\sum_{j=1}^{N_{\text{samples}}} a_j \left(s_j - p \right) \right]^i$$

Cell energy

Sampling fraction

Calibration board

Optimal Filtering Coefficients

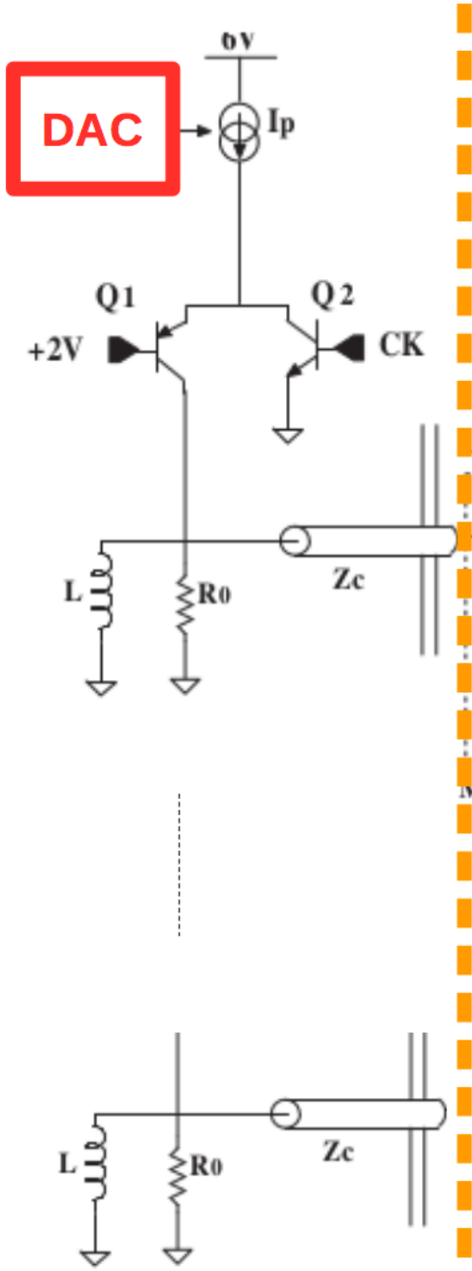
Pedestals

The above formula describes the LAr electronic calibration chain (from the signal ADC samples to the raw energy in the cell. Note that this version of the formula uses the general M_{ramps}-order polynomial fit of the ramps. We use a linear fit as the electronics are very linear, and we only want to apply a linear gain in the DSP in order to be able to undo it offline, and apply a more refined calibration. In this case, the formula is simply:

$$E_{\text{cell}} = F_{\mu\text{A}\to\text{MeV}} \cdot F_{DAC\to\mu\text{A}} \cdot \frac{1}{\frac{M_{\text{phys}}}{M_{\text{cali}}}} \cdot R \left[\sum_{j=1}^{N_{\text{samples}}} a_j \left(s_j - p \right) \right]$$

Calibration

Digital pulse command



128 calibration lines per calibration board

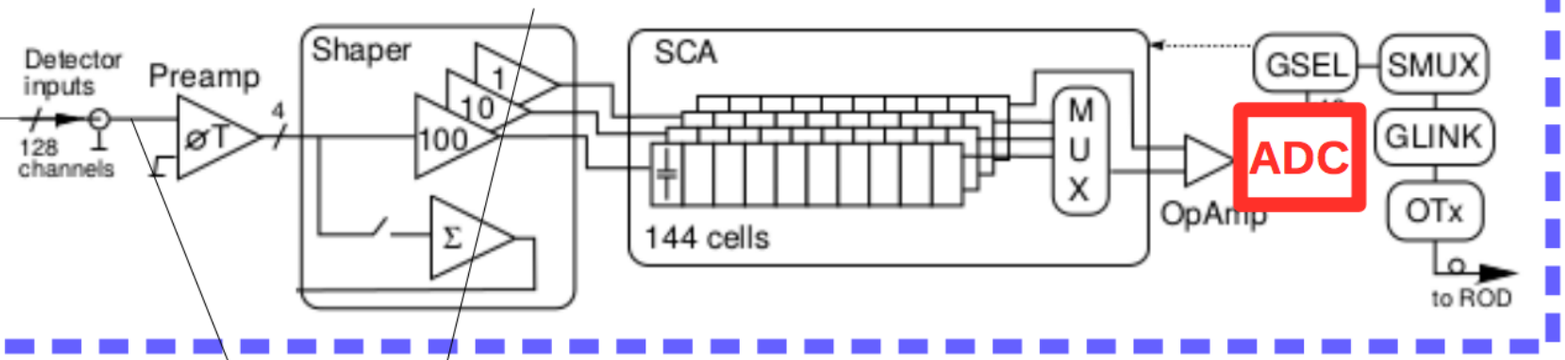
Calibration board

1 calib line is plugged on several cells

8 (resp. 32) cells for back/middle (resp. front) layer

Calorimeter cell

Readout electronics

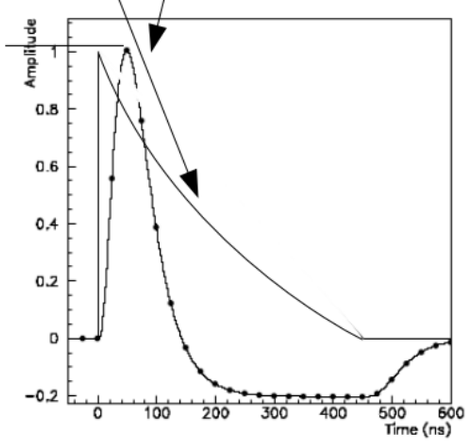


Exponential calibration pulse (**μA**)

Shaped pulse (**ADC**)

Digital pulse samples s_i

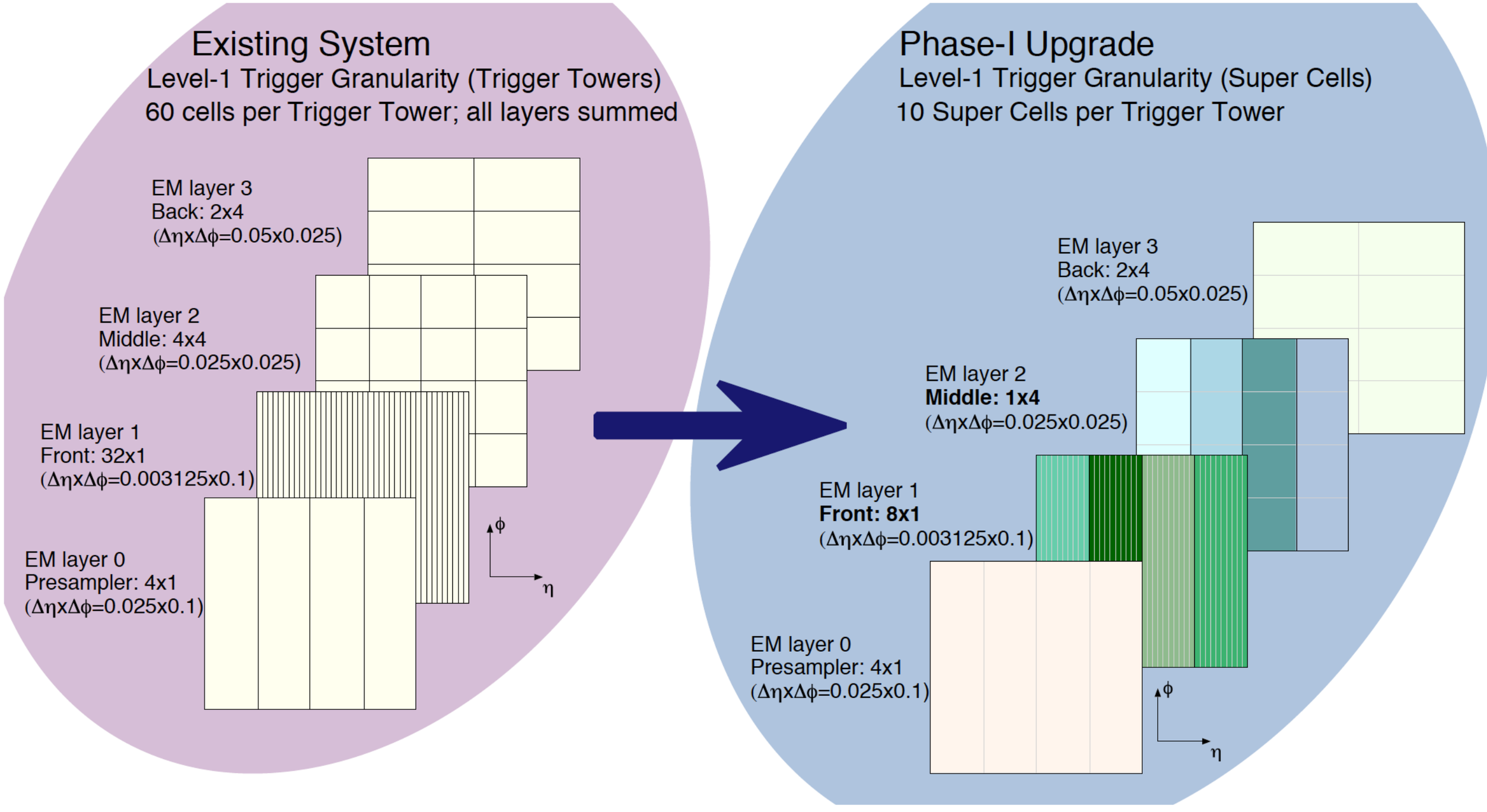
ADC_{max}



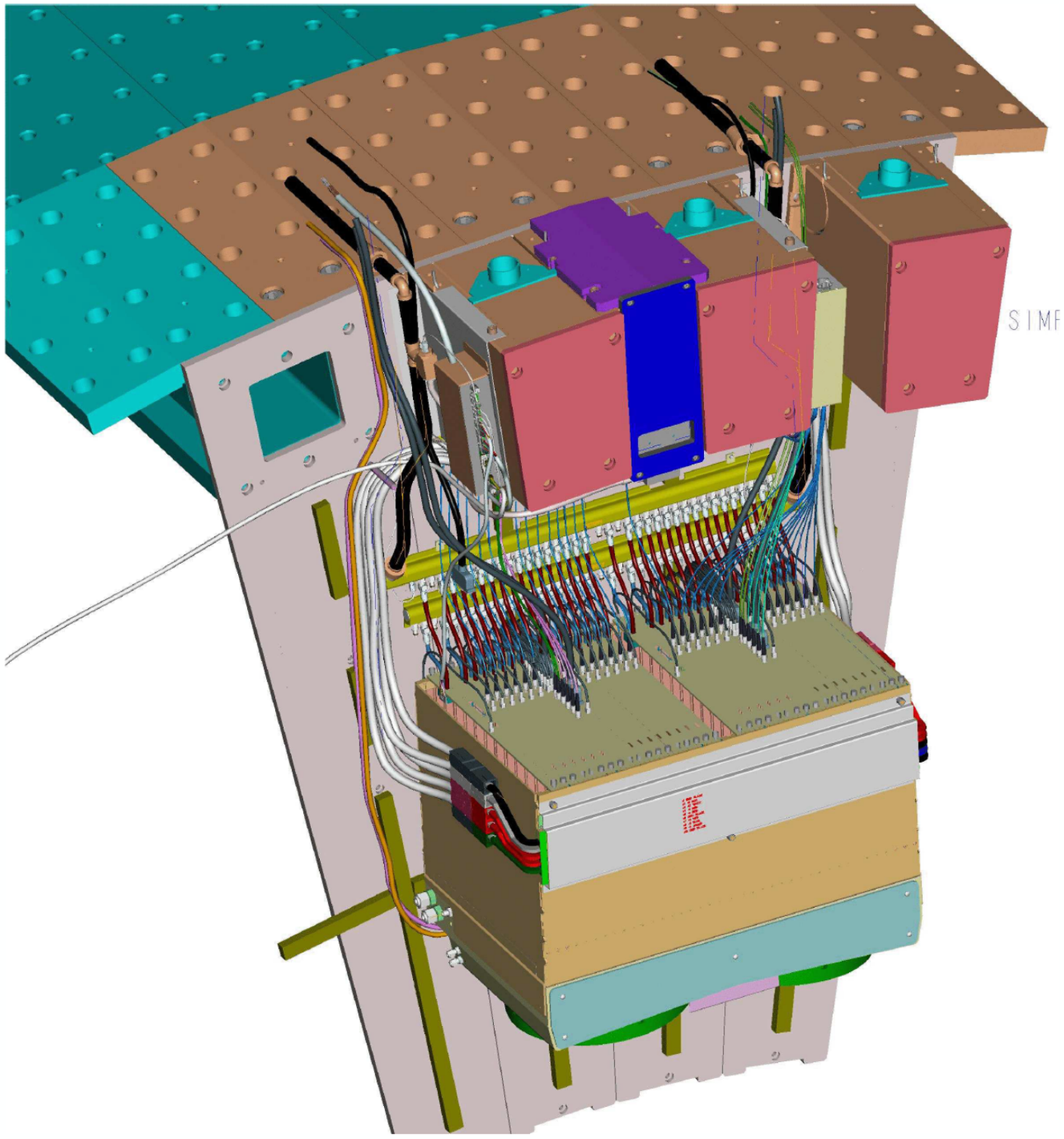
ADC → DAC known from calibration
DAC → μA known from first principle
μA → MeV known from test beam

14/06/2017

Phase 1 Super cells



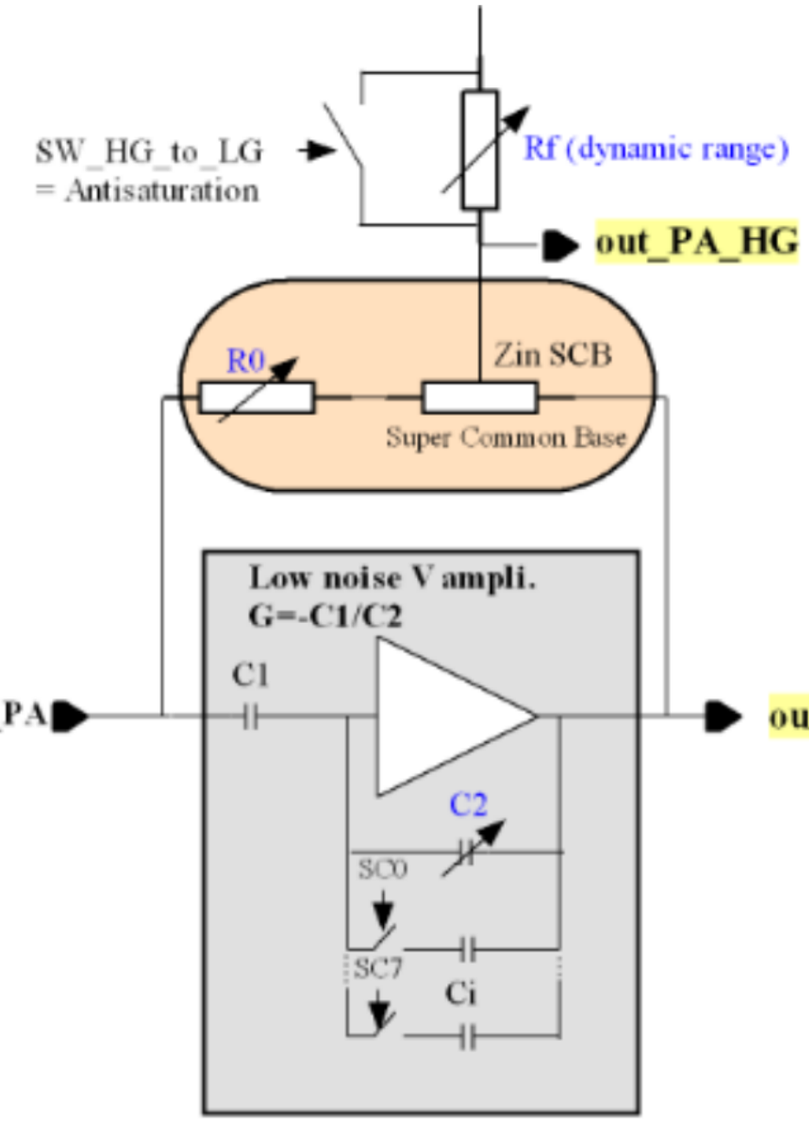
Front-end crate location



$$Z_{in}\,PA = \frac{R_0 + Zin(SCB)}{1 + |G|}$$

"Electronically cooled" resistor

$$\frac{4kTR_0}{(1+|G|)^2}$$



Linearity after shaping