Proto-DUNE single-phase cold electronics Integration test

Guang Yang (Stony Brook)
for the DUNE collaboration

Neutrino Oscillation

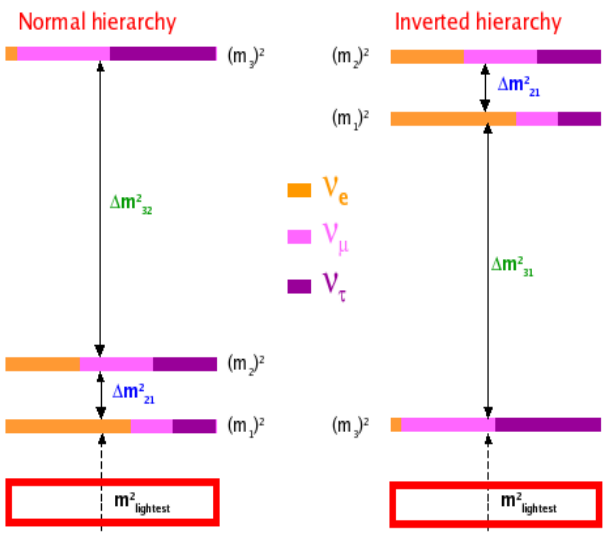
- Neutrino mixing can be parameterized by PMNS matrix.
- PNMS matrix can be broken down into three 3×3 matrices:

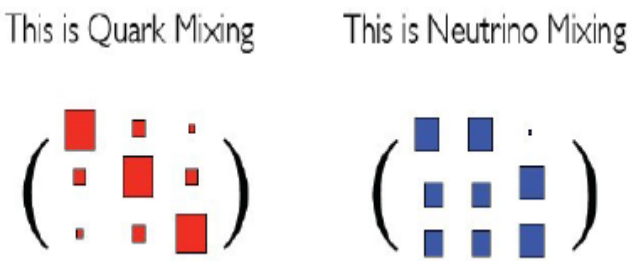
$$(c_{ij} \equiv \cos\theta_{ij}, \quad s_{ij} \equiv \sin\theta_{ij})$$

$$U = \begin{pmatrix} c_{12} & s_{12} & \\ -s_{12} & c_{12} & \\ & & 1 \end{pmatrix} \begin{pmatrix} c_{13} & & s_{13}\cdot e^{i\delta} \\ & 1 & \\ -s_{13}\cdot e^{i\delta} & & c_{13} \end{pmatrix} \begin{pmatrix} 1 & & \\ & c_{23} & s_{23} \\ & -s_{23} & c_{23} \end{pmatrix} \begin{pmatrix} 1 & & \\ & e^{i\alpha} & \\ & & e^{i\beta} \end{pmatrix}$$

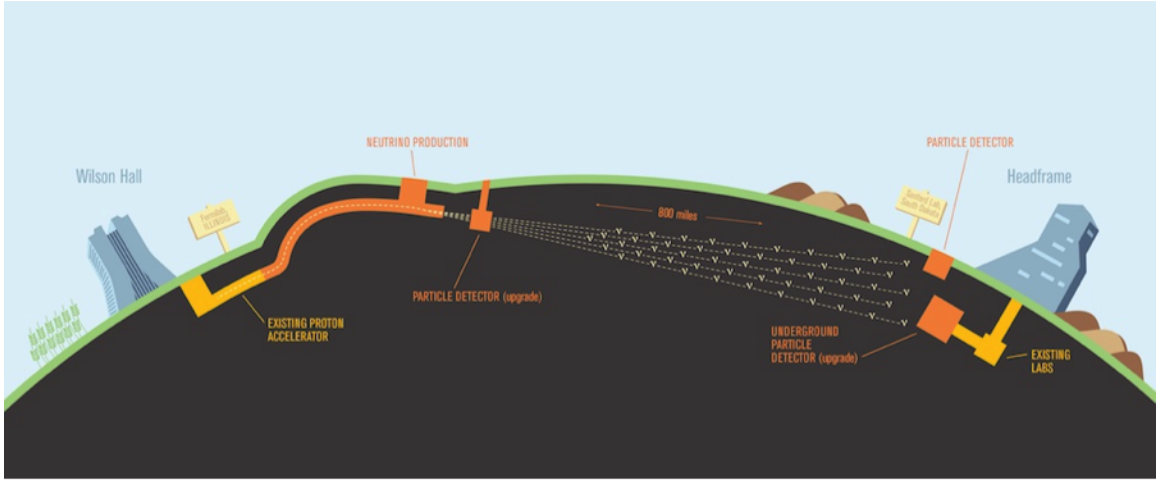
Solar | Atmospheric Reactor | Atmospheric | Majorana Phases

- Each mixing angle related to a mass splitting between the two mass states.



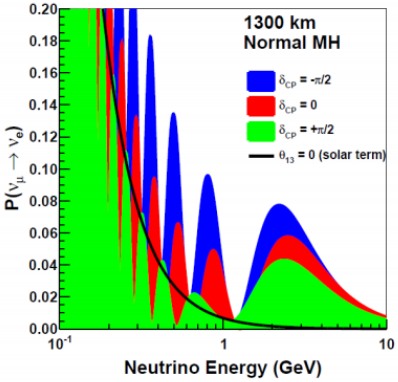


DUNE experiment

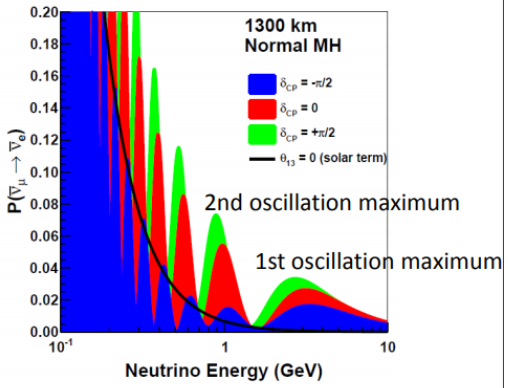


- ν_e appearance amplitude depends on Θ_{13}, Θ_{23}, CP phase and mass hierarchy.
- Large value of Θ_{13} allows significant ν_e appearance.
- DUNE has 1300km baseline, a wide-band beam and 40kt fiducial mass, allowing significant signal observation.

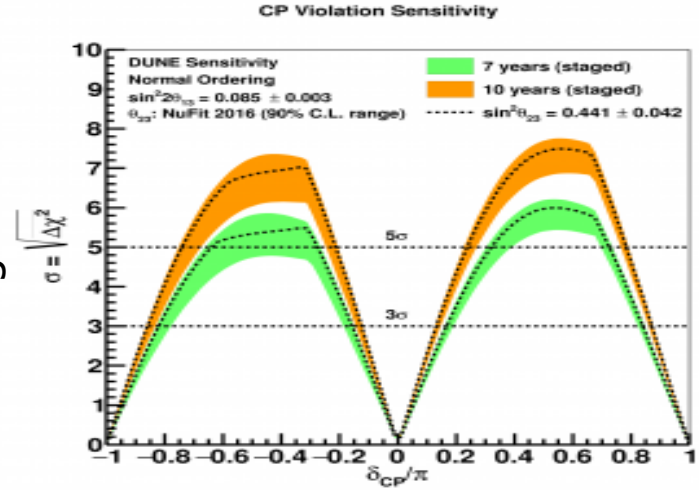
ν mode



Anti-ν mode

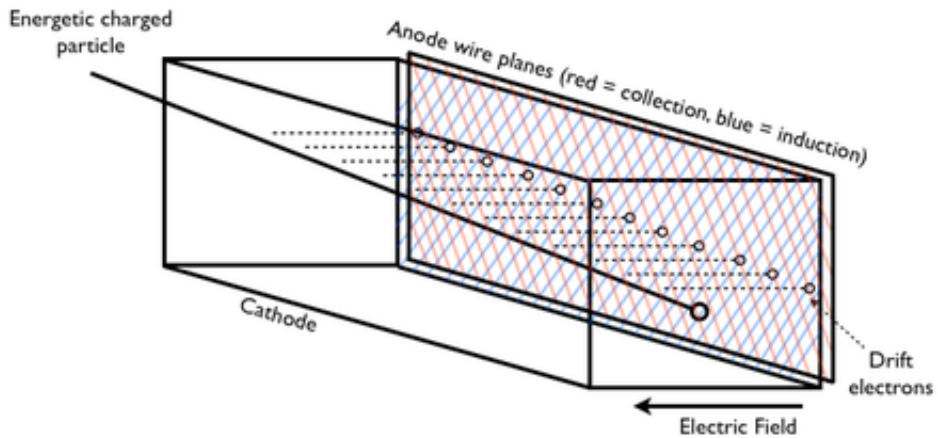


significance



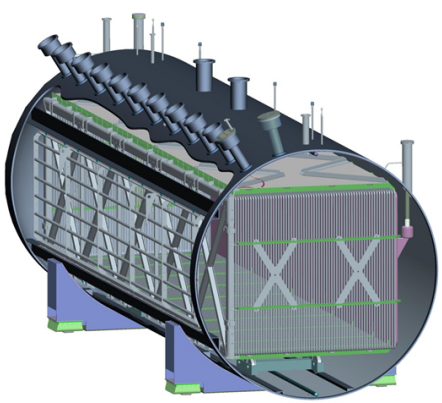
CP phase

Liquid Argon TPC



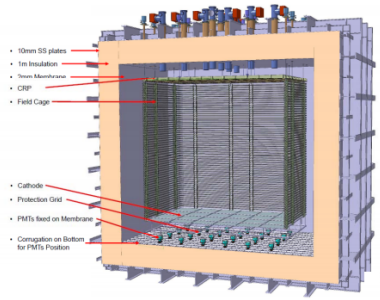
- In the single phase, signals cannot be amplified, so we care about the noise level in the read-out in the cold.
- The noise level directly determine the threshold of particle tracks.

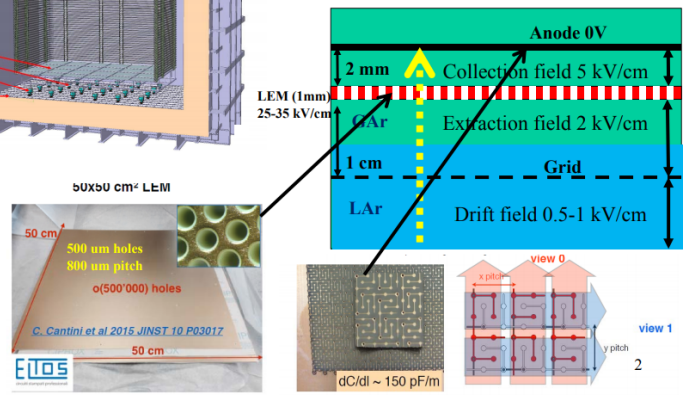
MicroBOONE



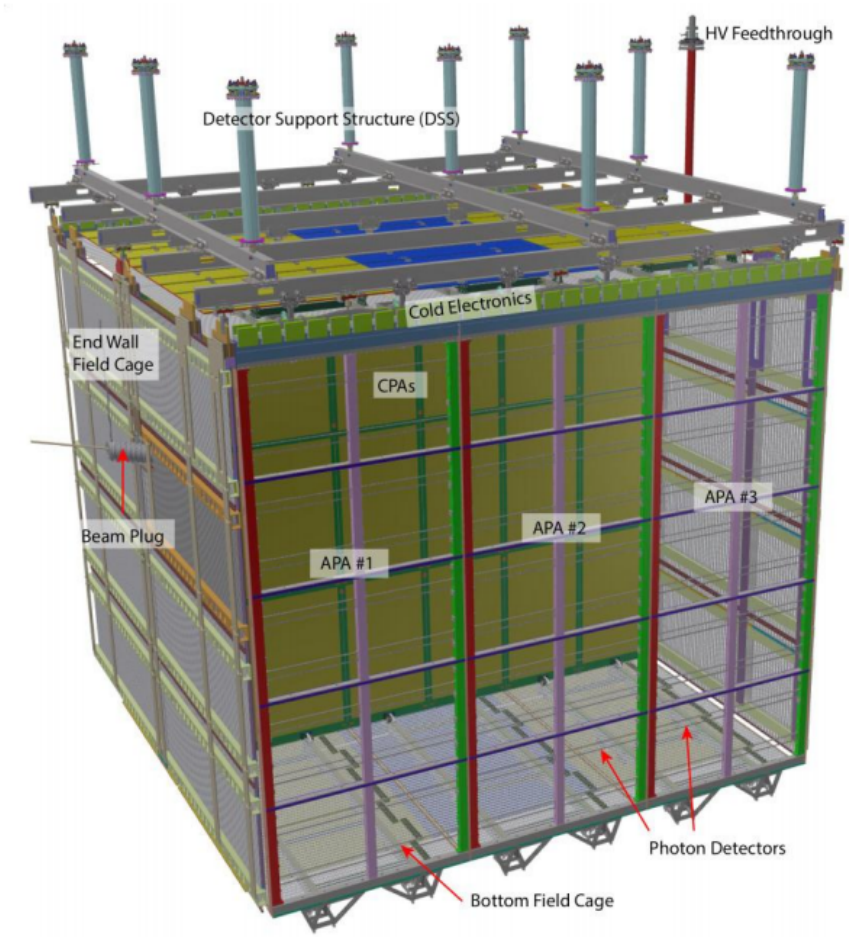
80 ton active mass

Proto-DUNE
Dual-phase LAr TPC





Proto-DUNE SP detector



10 kt FD module needs an intermediate detector to validate, so the goals of Proto-DUNE:

- Prototype the production and installation

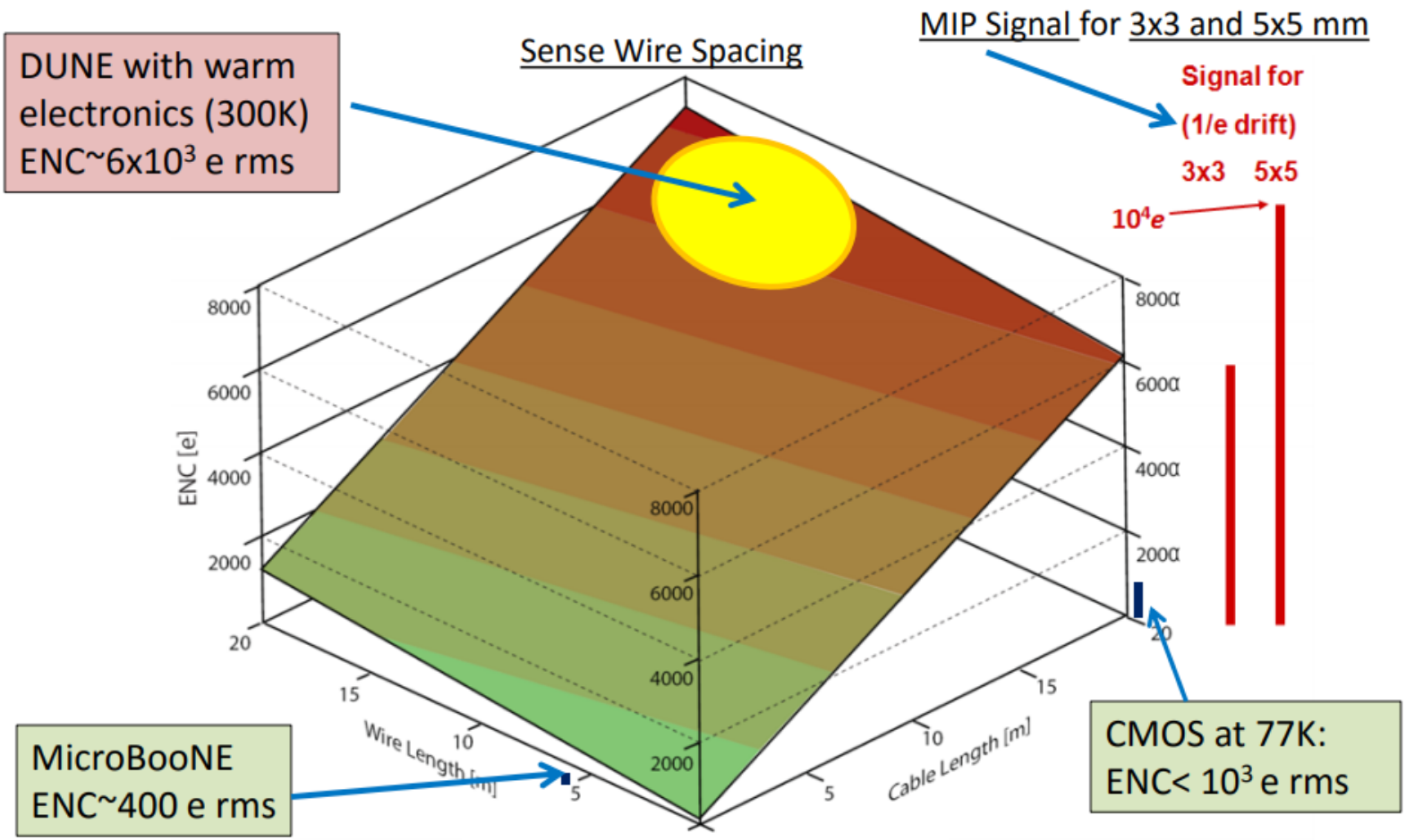
- Validate the design from the perspective of basic detector performance

- Accumulate test-beam data to calibrate the response of the detector

- Demonstrate operational stability

Active volume: 6m x 7m x 7.2m (height, width, drift) 0.77kt total Lar, ~3520 wires/APA

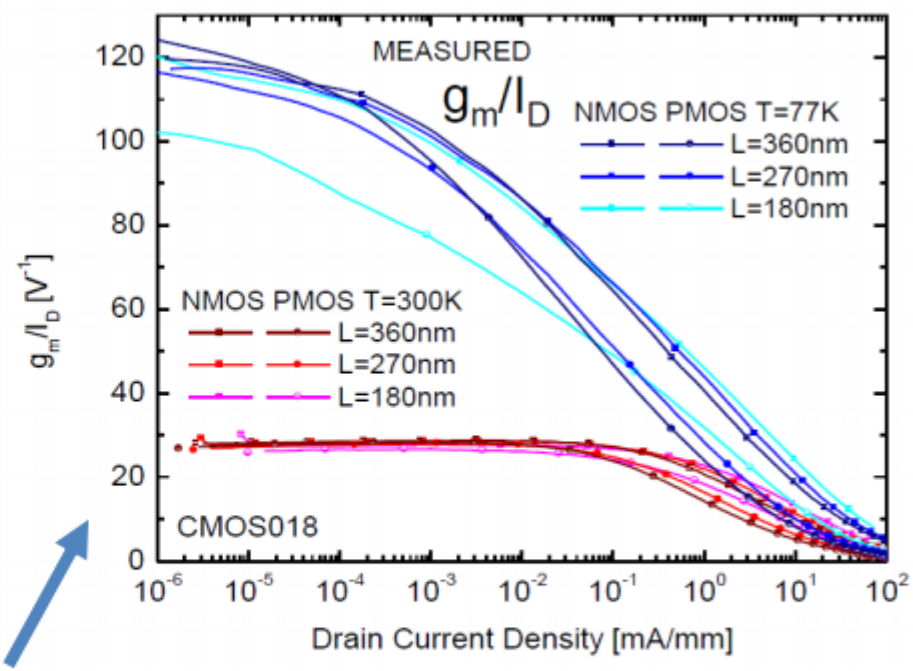
Why do we care about the electronics ?



CMOS in Cryostat

Physics Procedia 37 (2012) 1295-1302

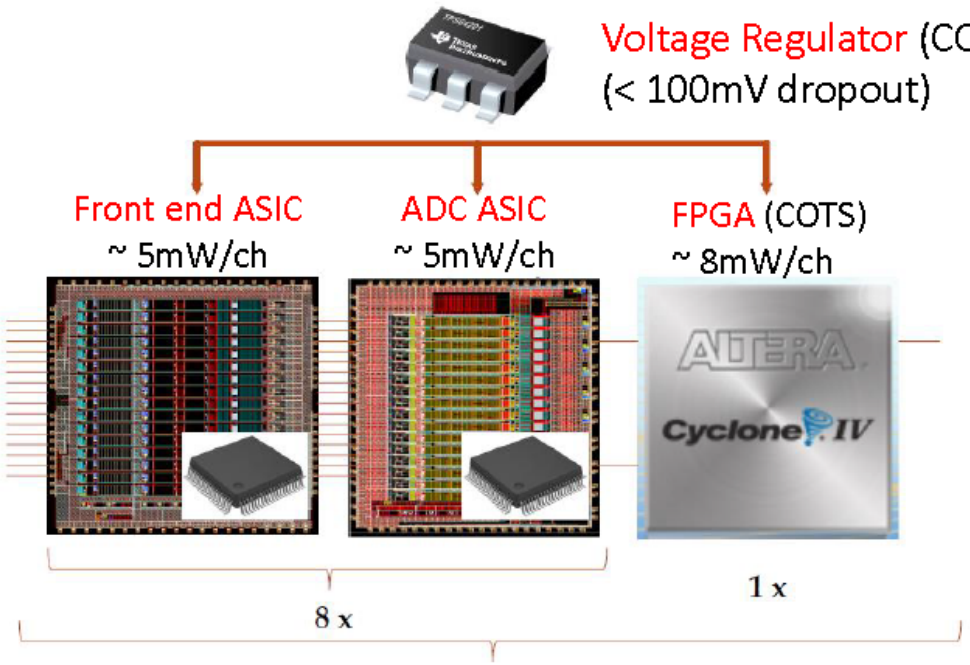
At 77-89 K, charge carrier mobility in silicon increases and thermal fluctuations decrease, resulting in a higher gain, higher g_m /I_D and lower noise.



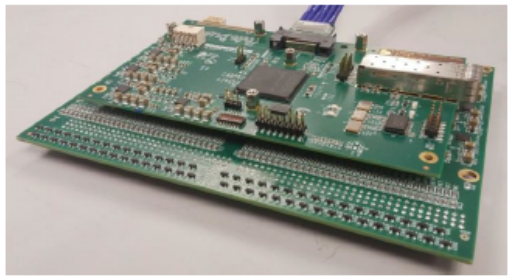
Transconductance / drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

Key ASICs for ProtoDUNE



FEMB used in the integration test



Dynamic range and Noise requirement

- Dynamic range

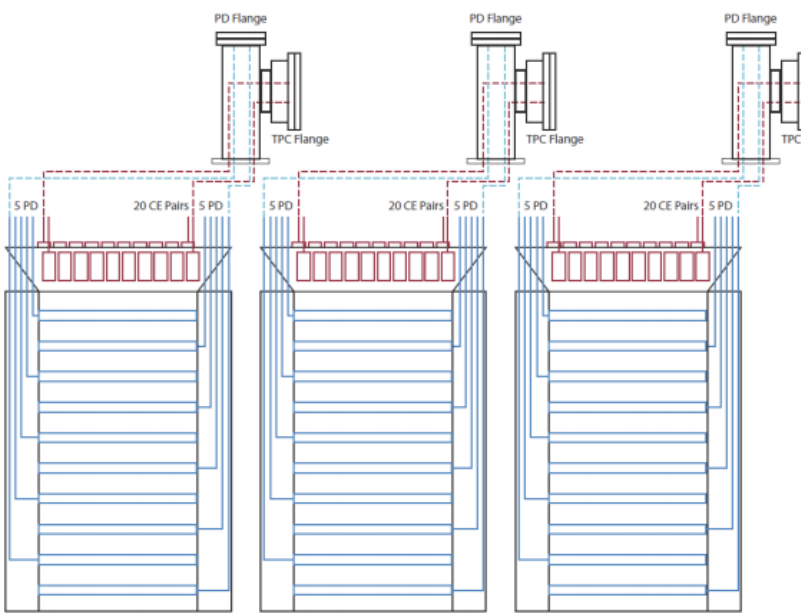
- Lower limit:
  - Assume MIP happens in the Cathode plane, it gives ~12K e- in APA wires. If 1% charge resolution is required, 116e- per ADC count is needed.

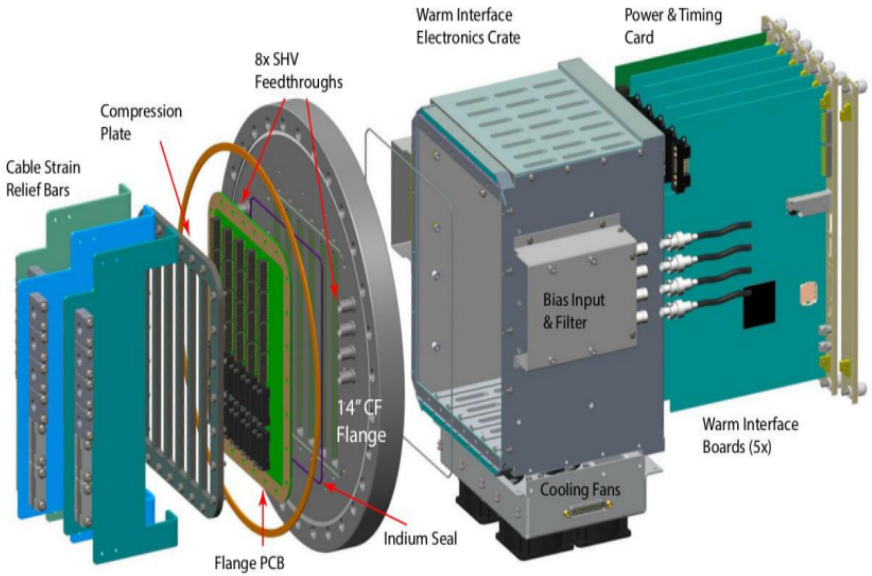
- higher limit:
  - Considering two protons deposit all energies in a single wire, largest energy per proton is 22.5k e- ,then 12 bit ADC is sufficient for 45k e- in single wire.

- Noise requirement

- For MIP track from Cathode plane, signal arriving single wire is ~12,000 ENC.
- If we require 1/10 noise/signal ratio, then
  - ~ 1200 ENC for collection wire.
  - ~ 600 ENC for induction wire.

Cold electronics integration

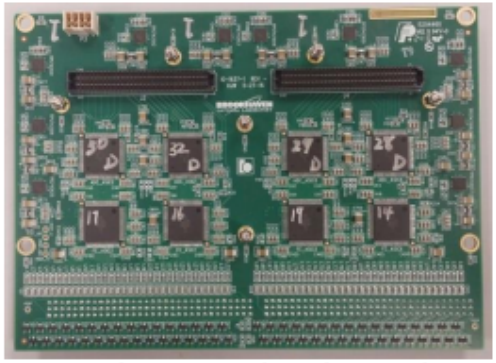




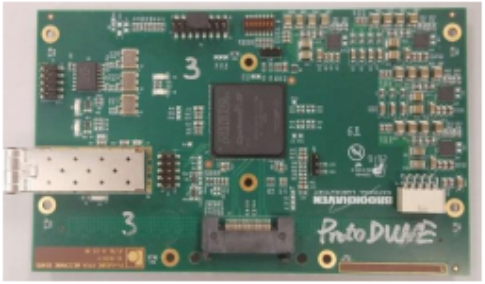
- For 6 APAs, each one contains 20 FEMBs.
- Each FEMB contains 8 FE and ADCs.
- Each FE/ADC contains 16 channels.
- Every 4 FEMBs can be controlled by one Warm Interface Board.

Front end board

- 128 channels of digitized TPC wire readout
  - Analog Mother Board
    - 8 FE ASICs/ 8 ADC ASICs
- FPGA Mezzanine
  - multiplexing and readout of digitized detector signals

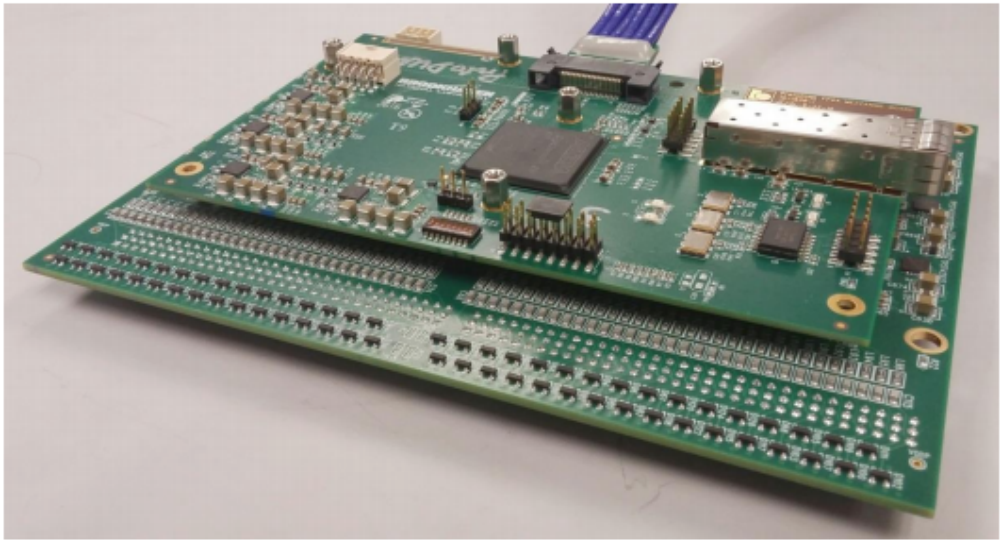


Analog Motherboard



FPGA Mezzanine

4 1Gb/s serial links to transmit 128 FE channels of data



Front End Mother Board Assembly

Front End ASIC

Bandgap Reference

$$V_{BGR} \approx \begin{cases} 1.185\ \text{V at } 300\ ^\circ\text{K} \\ 1.164\ \text{V at } 77\ ^\circ\text{K} \end{cases}$$

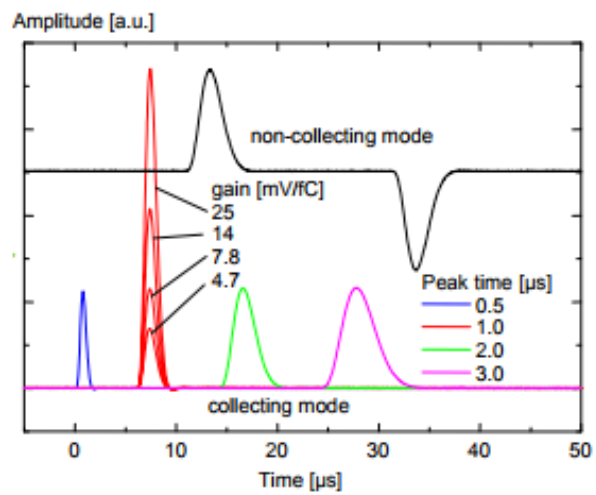
variation = 1.8 %

Temperature Sensor

$$V_{TMP} = \begin{cases} 867.0\ \text{mV at } 300\ ^\circ\text{K} \\ 259.3\ \text{mV at } 77\ ^\circ\text{K} \end{cases}$$

~ 2.86 mV / K

Shared among the 16 channels in the FE ASIC are the bias circuits, programming registers, a temperature monitor, an analog buffer for signal monitoring, and the digital interface.

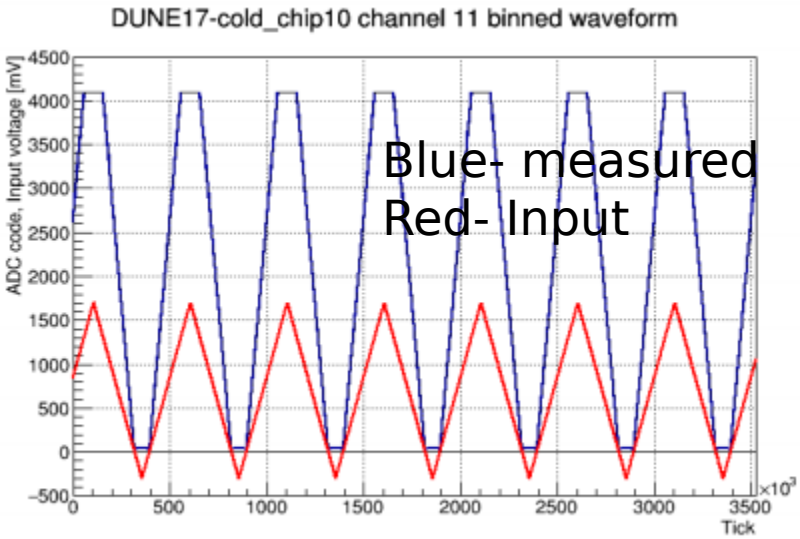


Possible configurations:

- Baselines 200 or 900 mV: 900 for induction and 200 for collection.

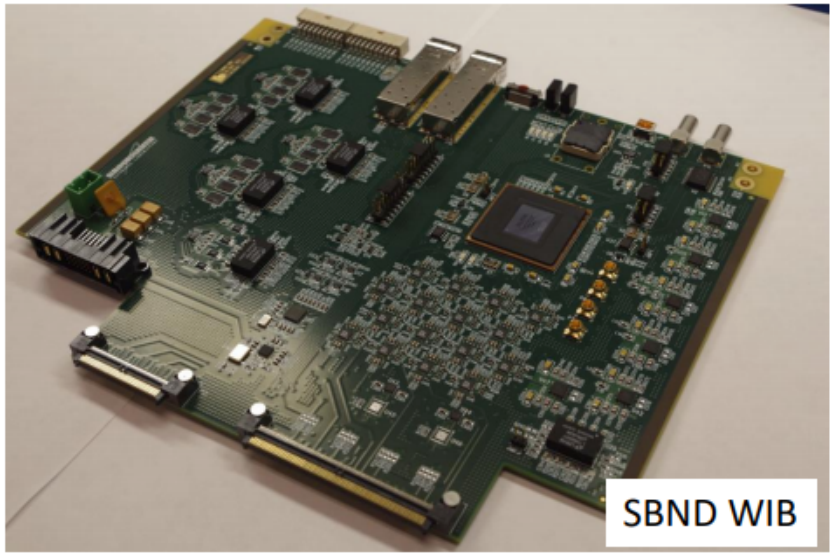
- Gain: 4.7, 7.8, 14, 25 mV/fC
- Shaping time: 0.5, 1, 2, 3 mus
  - time integrated over the integrated waveform, so no significant differences once the waveform peaks are covered.
  - good for the LAr wire resolution.

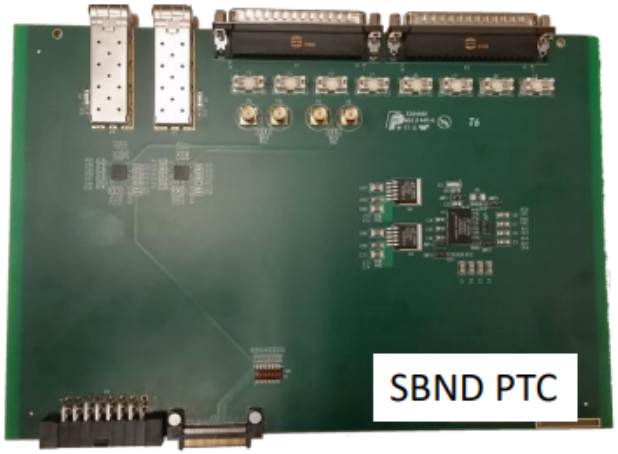
ADC cold test



- Lower the ADC chips into liquid nitrogen.
- Function generators input different kinds of waveforms.
- Test the non-linearity and channel-to-channel variation performance in the cold.
- In warm, it works well but in cold, some of the connection issues come out.

Warm interface electronics



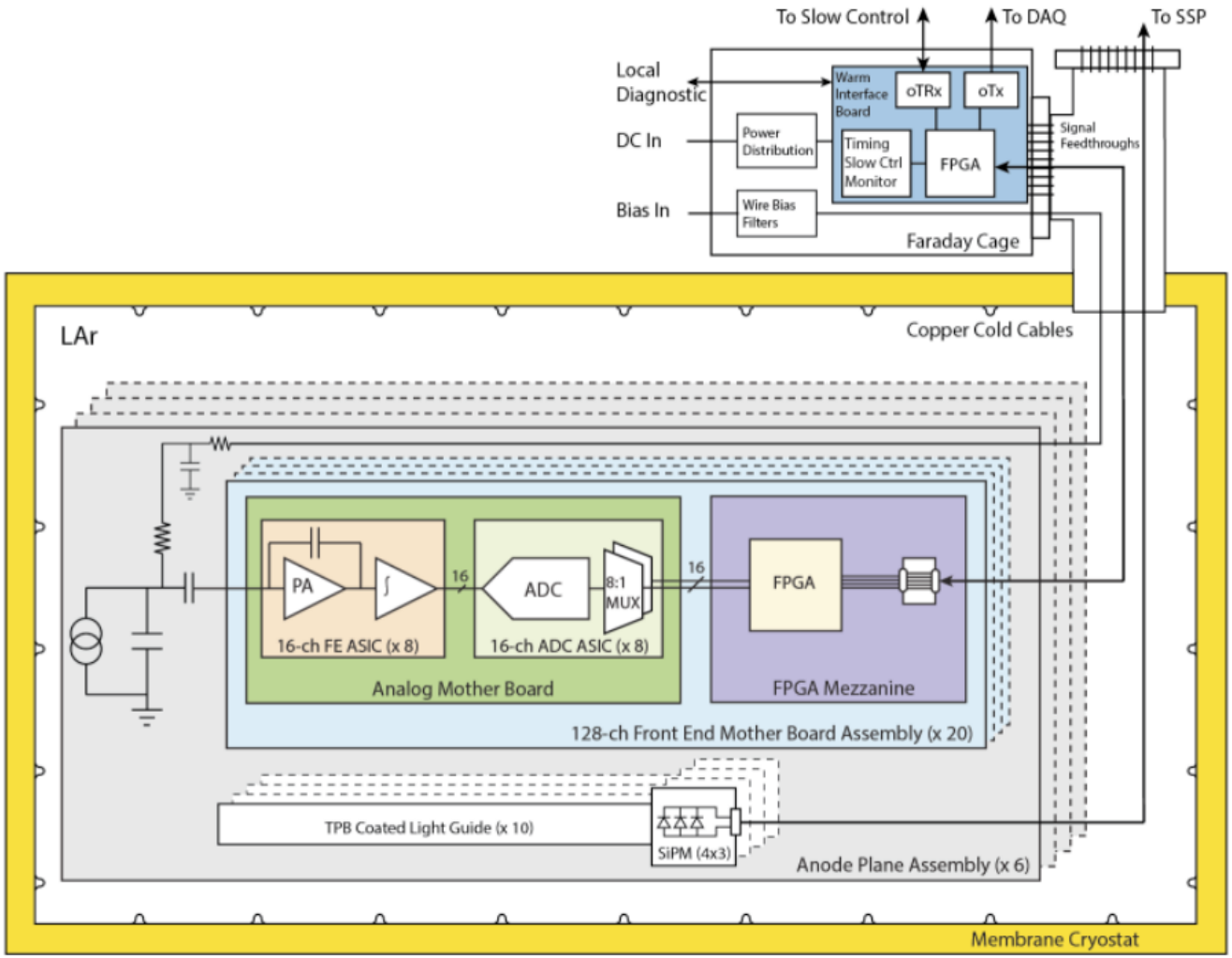


- WIB (Warm interface board)
  - proto-DUNE-SP WIB design is being finalized
  - SBND WIB is being used for ProtoDUNE-SP firmware development currently

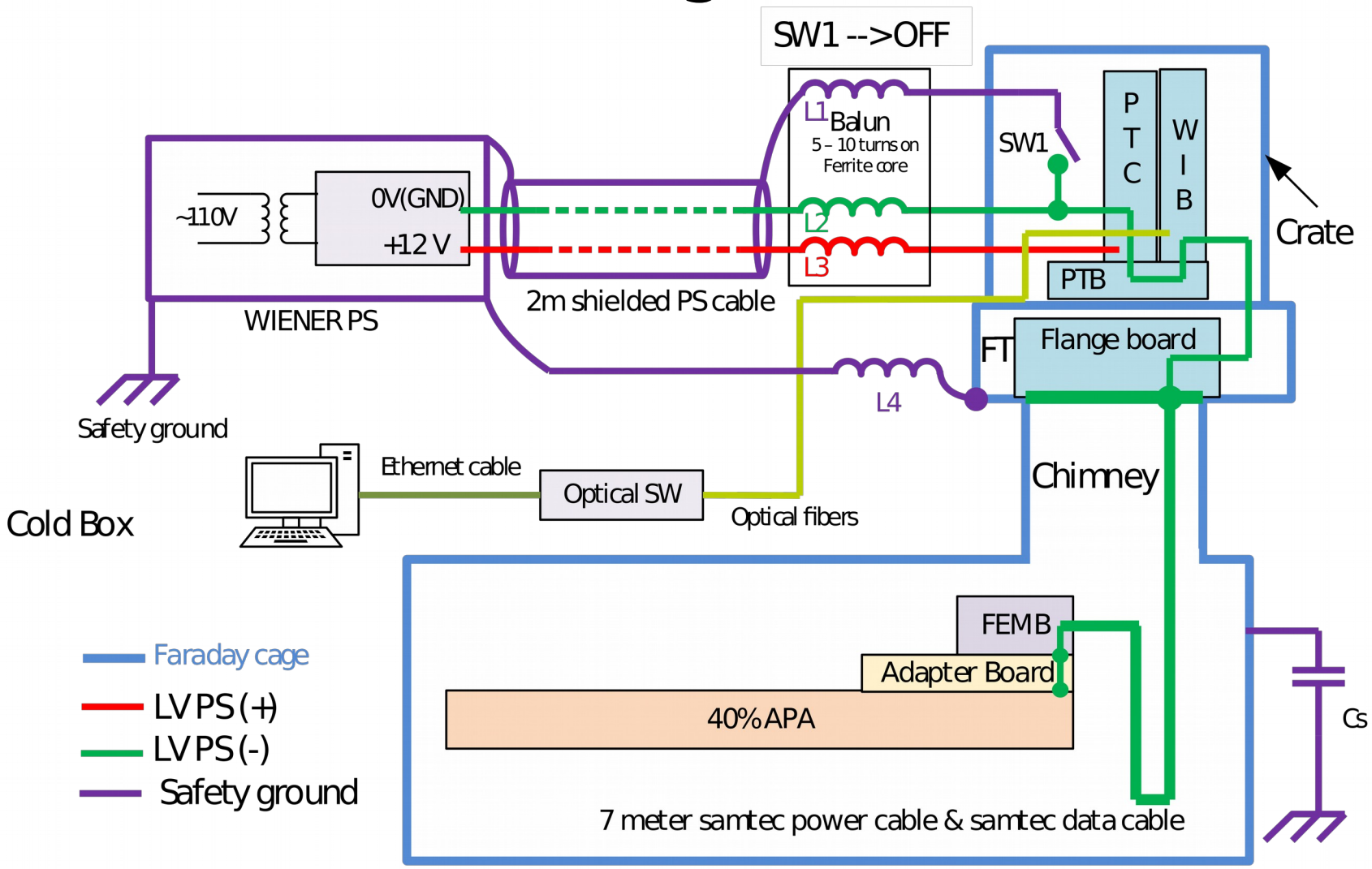
-PTB (Power and timing Backplane)
  - Distributes system clock and Sync/Cntrl signals to each WIB

-PTC (Power and timing Card)
  - ProtoDUNE-SP design is being finalized by UC Davis

Integration test in BNL



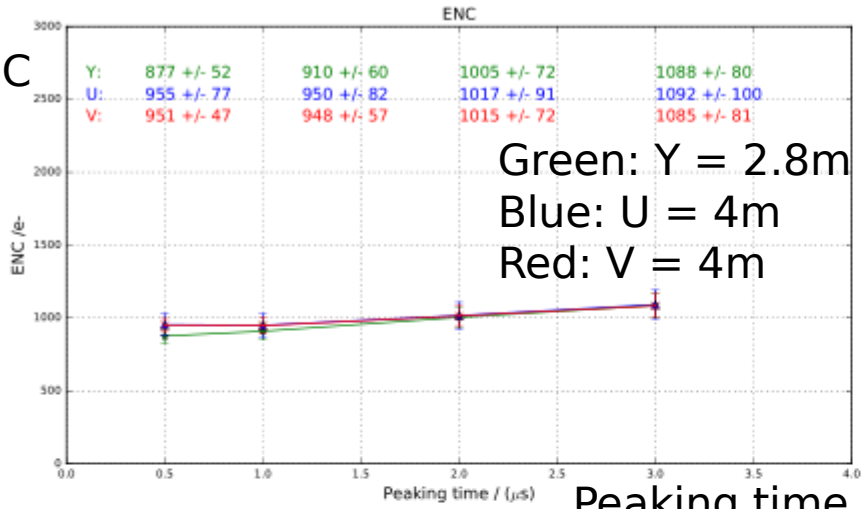
Grounding Scheme



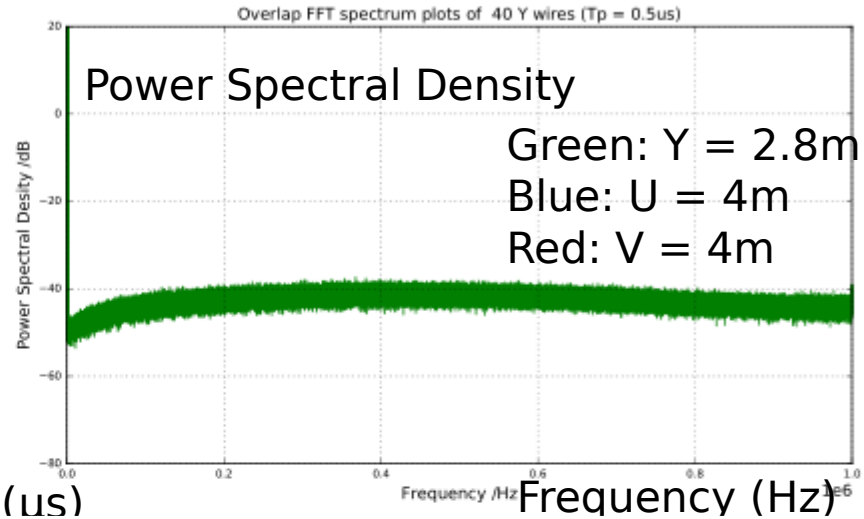
Setup in BNL

Results at room temperature

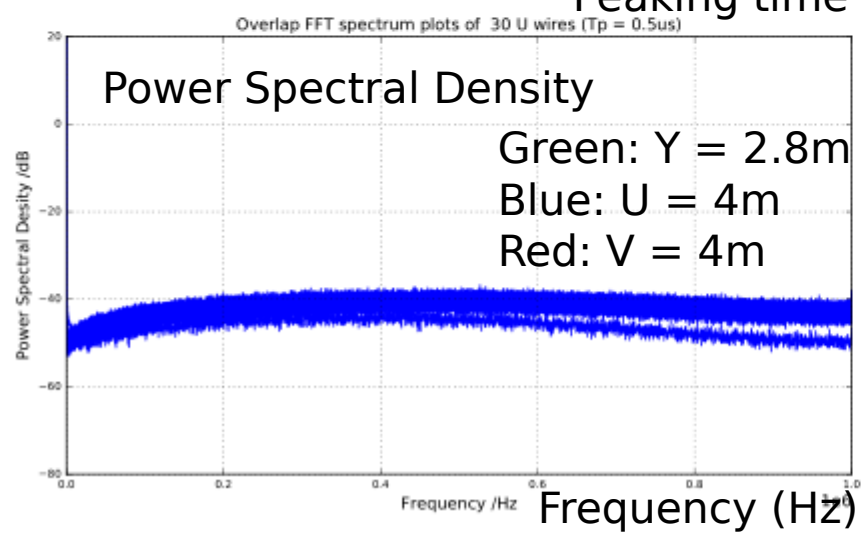
ENC



Peaking time (us)



Frequency (Hz)



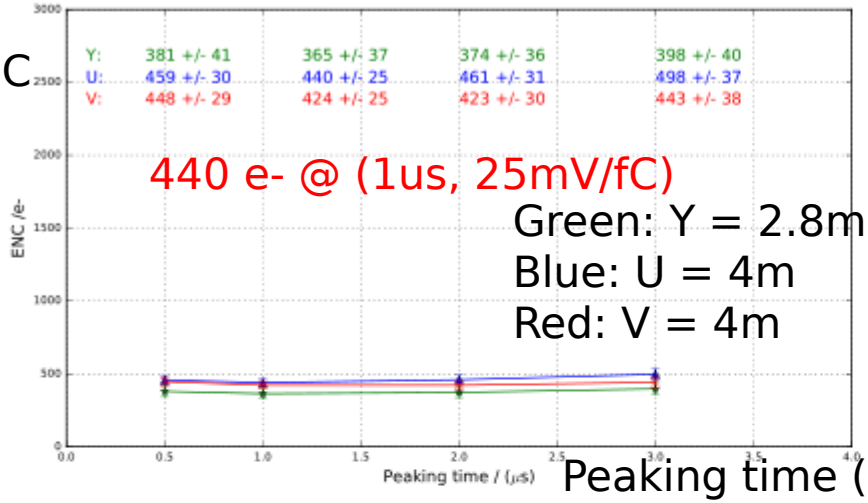
Frequency (Hz)

40% APA:
2.8 m x 1.0 m

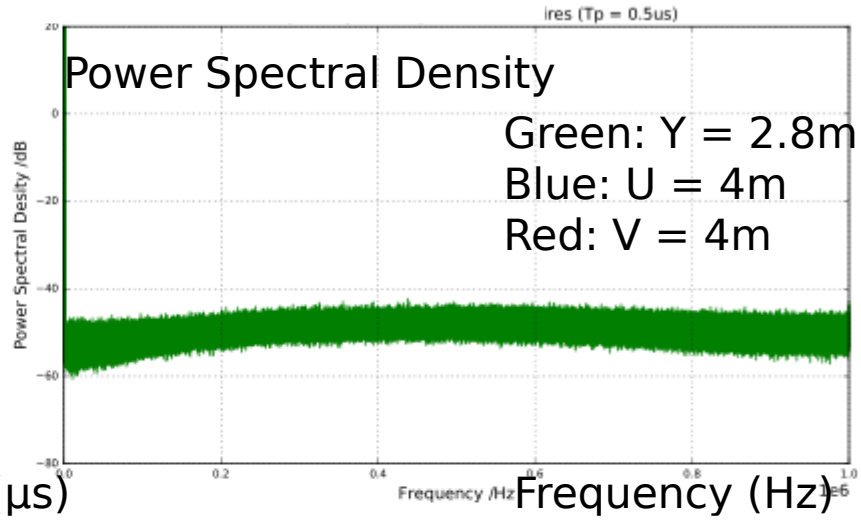
DUNE APA:
6 m x 2.3 m
(7.4 m induction wire)

Result from Cold Test

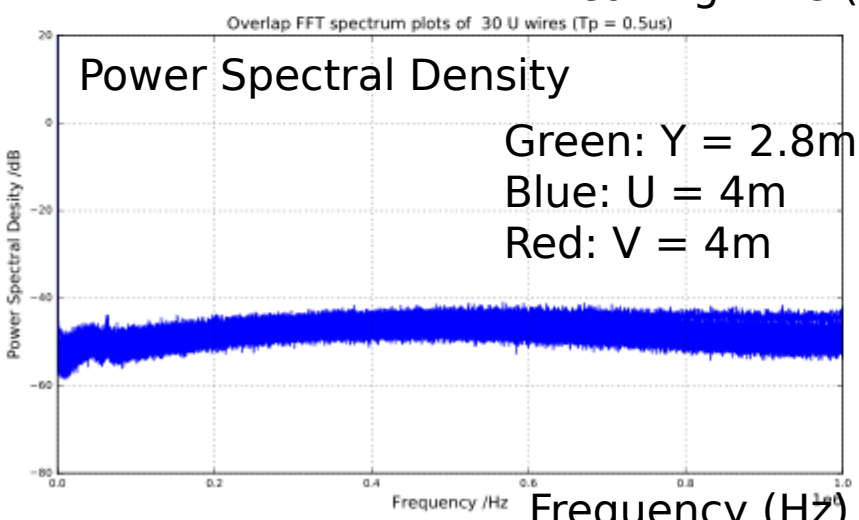
ENC



Peaking time (μs)



Frequency (Hz)



Frequency (Hz)

40% APA:
2.8 m x 1.0 m

DUNE APA:
6 m x 2.3 m
(7.4 m induction wire)

Summary

- As a prototype detector, protoDUNE cold electronics is crucial for the development of DUNE experiment.

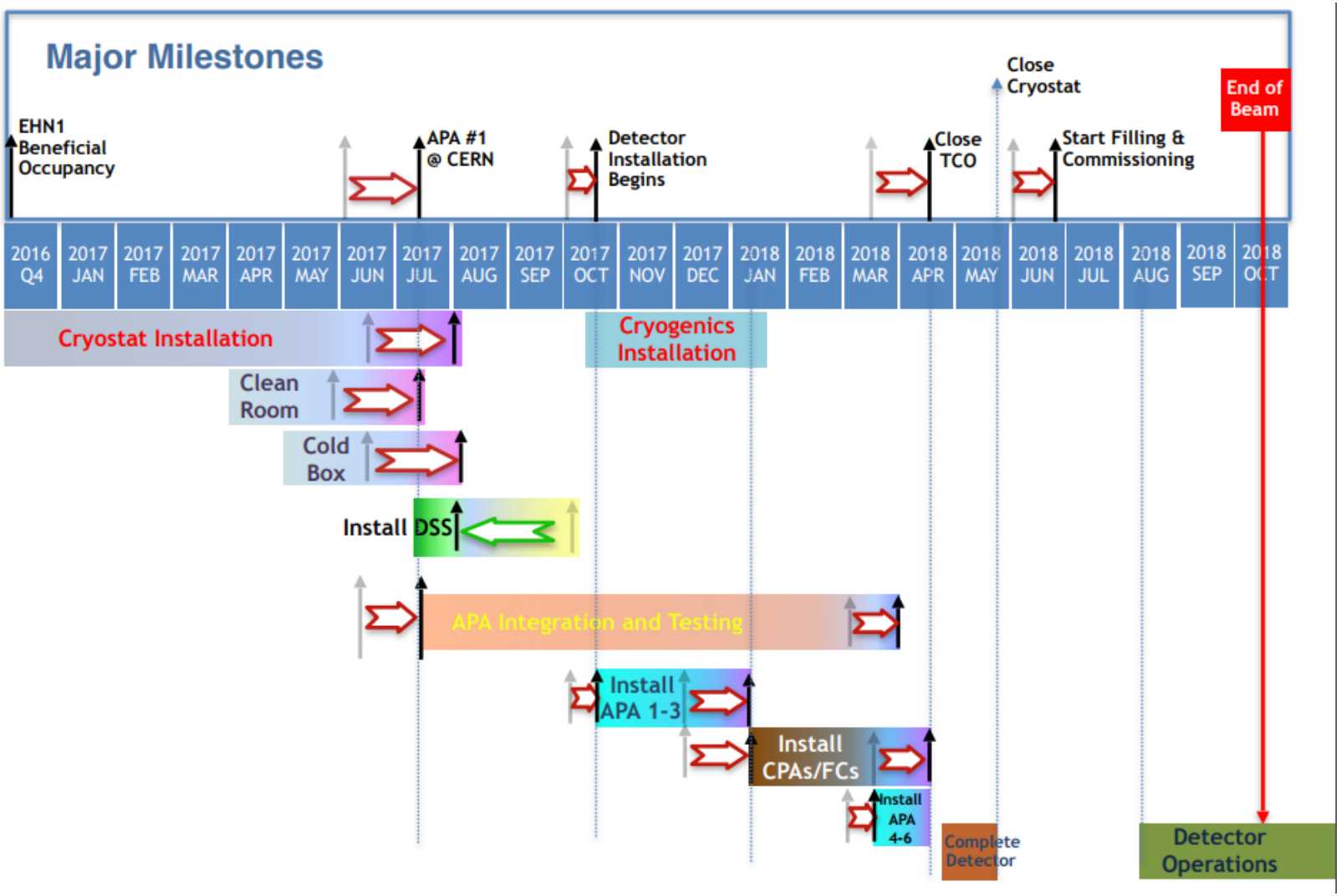
- The cold integration test has been done in BNL with collaboration with many other institutions.

- we are able to obtain clean & smooth FFT, and ENC performance shows improvement comparing to previous cold test as well.

- A preliminary result shows ENC ~ 440 e- @ (1us, 25mV/fC) for the 40% APA. Projecting to Proto-DUNE APA, ~700 e- is expected.
  Considering the 1/10 Noise/Signal requirement is 600 e- and 1200 e- for the induction and collection wires, this gives ~ 1/9 Noise/Signal ratio.

BACKUPS

Time line


Major Milestones
EHN1 Beneficial Occupancy
APA #1 @ CERN
Detector Installation Begins
Close TCO
Close Cryostat
Start Filling & Commissioning
End of Beam
2016 Q4
2017 JAN
2017 FEB
2017 MAR
2017 APR
2017 MAY
2017 JUN
2017 JUL
2017 AUG
2017 SEP
2017 OCT
2017 NOV
2017 DEC
2018 JAN
2018 FEB
2018 MAR
2018 APR
2018 MAY
2018 JUN
2018 JUL
2018 AUG
2018 SEP
2018 OCT
Cryostat Installation
Cryogenics Installation
Clean Room
Cold Box
Install DSS
APA Integration and Testing
Install APA 1-3
Install CPAs/FCs
Install APA 4-6
Complete Detector
Detector Operations

Different neutrino experiments

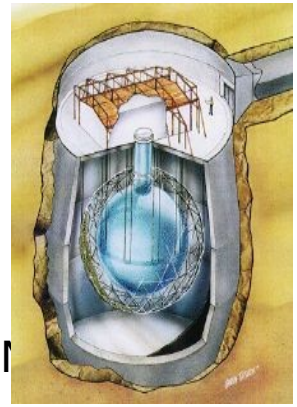
Solar: BOREXINO, SNO…

Atmospheric: Super-K…

Accelerator: MINOS, NOvA, T2K…

Reactor: Daya Bay, Double Chooz, REN
KamLAND…

Cosmic: IceCube…

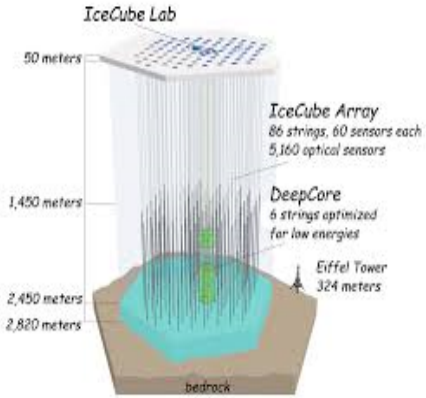


SNO ($\nu_e \rightarrow \nu_{\mu,\tau}$)

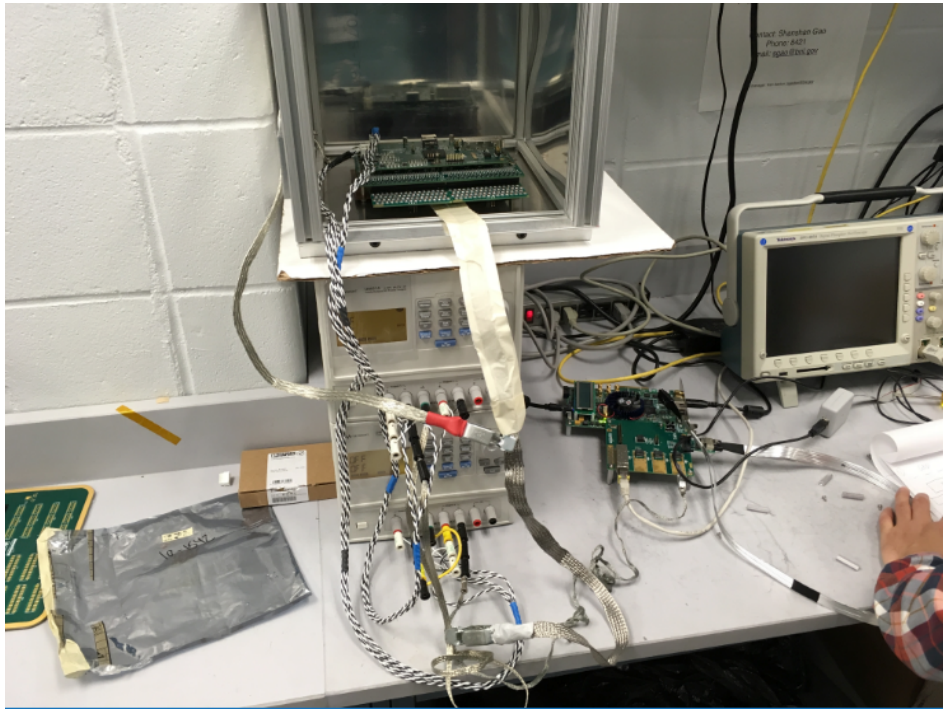
Super-K($\nu_\mu \rightarrow \nu_\tau$)

T2K

Daya Bay ($\nu_e \rightarrow \bar{\nu}_e$)



IceCube



Possible configurations:

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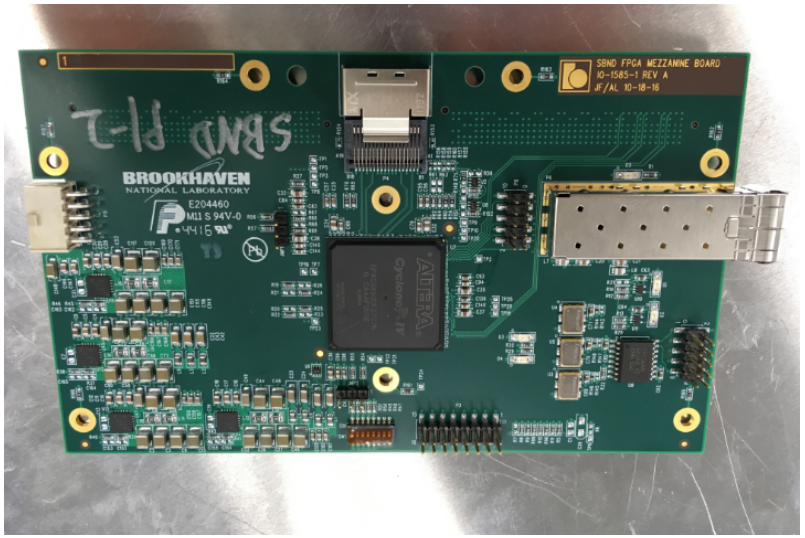
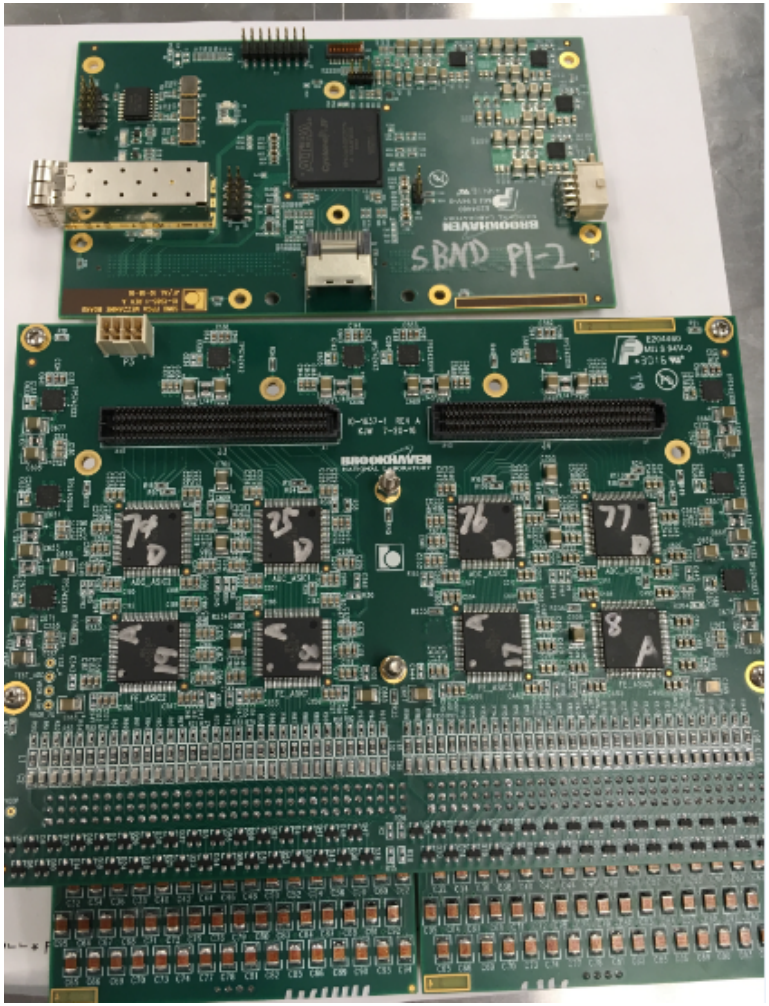
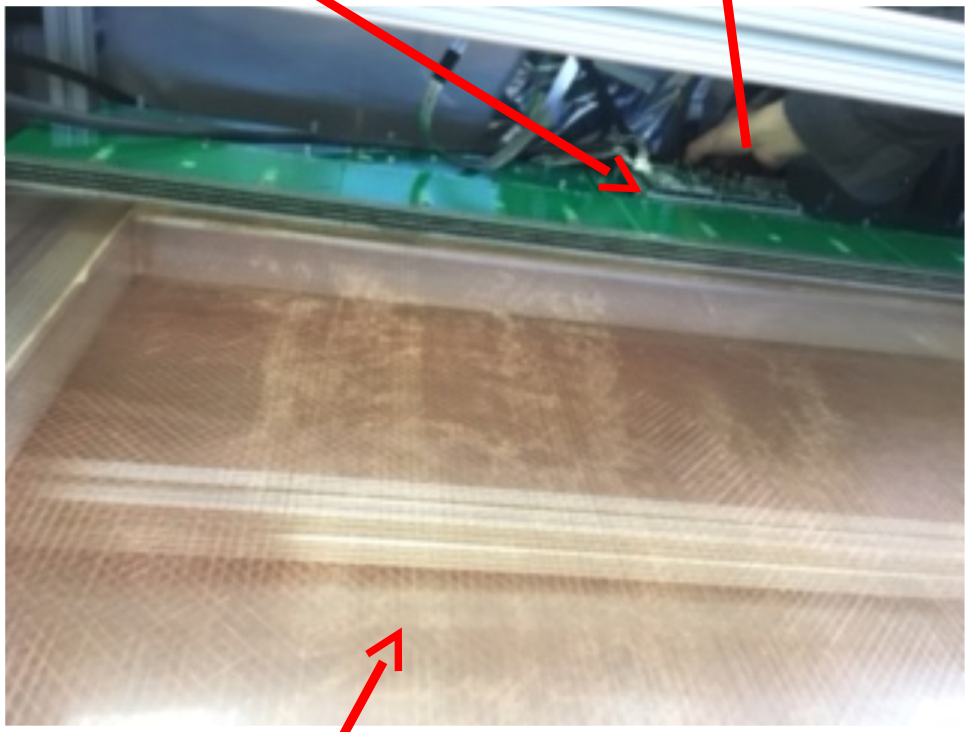




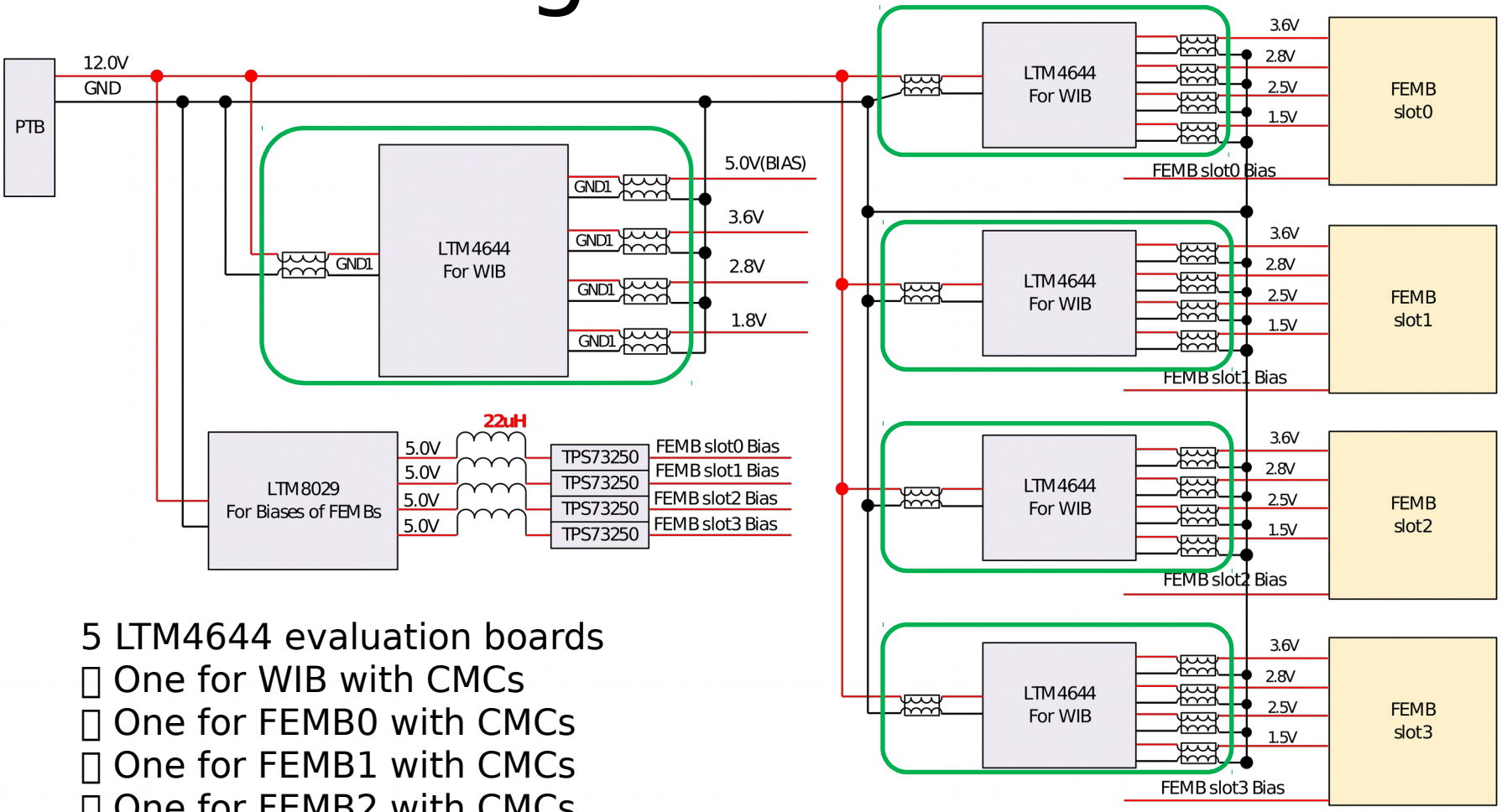
Basic measurements to determine a FEMB and WIB:
- Waveform check
- Fast Fourier Transformation check
- Noise RMS
- Gain calibration: internal or external pulser used

Steps for analysis:
- Hardware test stand setup
- Data taken with Python or LabVIEW
- De-code the data packed by WIB: binary raw data to understandable data format (root etc.)
- Do the measurement analysis above

Setup in BNL



WIB configuration

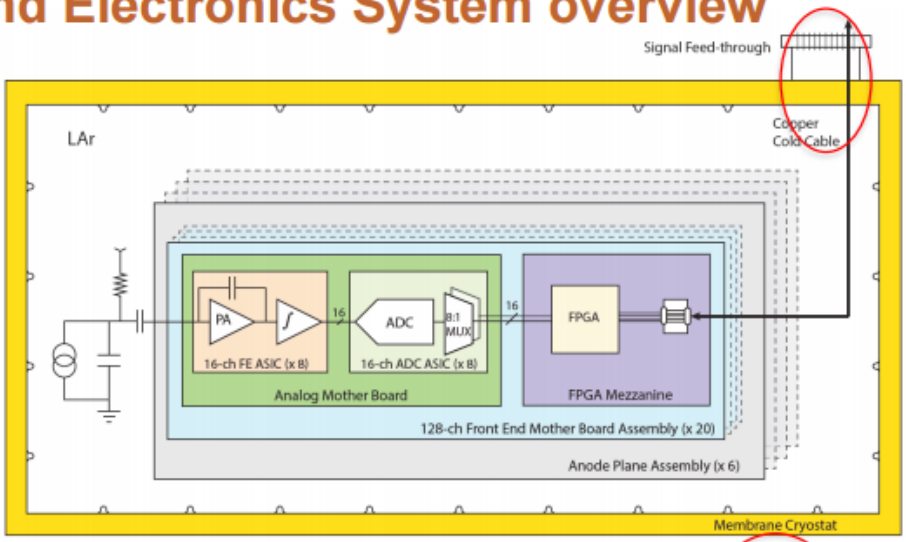


5 LTM4644 evaluation boards

- One for WIB with CMCs
- One for FEMB0 with CMCs
- One for FEMB1 with CMCs
- One for FEMB2 with CMCs
- One for FEMB3 with CMCs
- 5.0 Bias for FEMBs from on-board regulators (TPS73250) after DCDC LTM8029

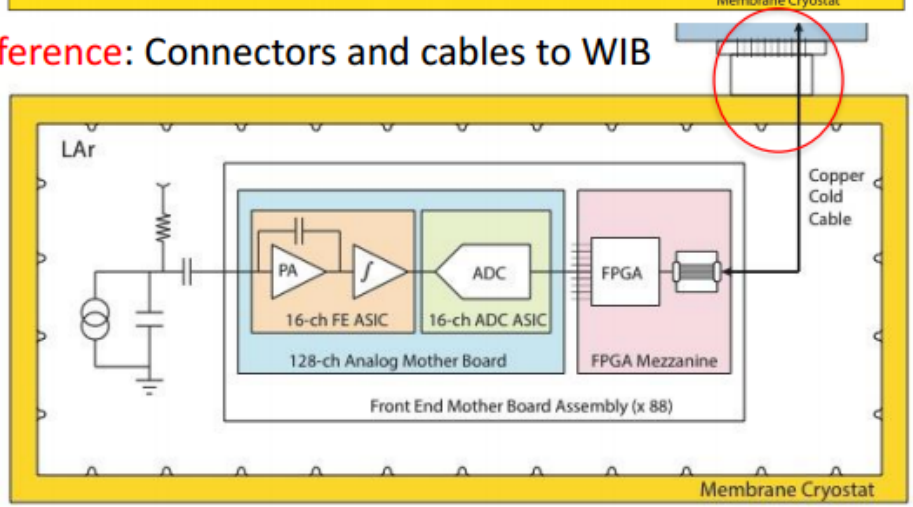
ProtoDUNE TPC Front End Electronics System overview

- ProtoDUNE TPC FE
  - 6 APAs
  - 120 FEMBs
  - 128-ch per FEMB
  - Connector: Samtec HSEC8
  - Samtec twinax cable (7m)



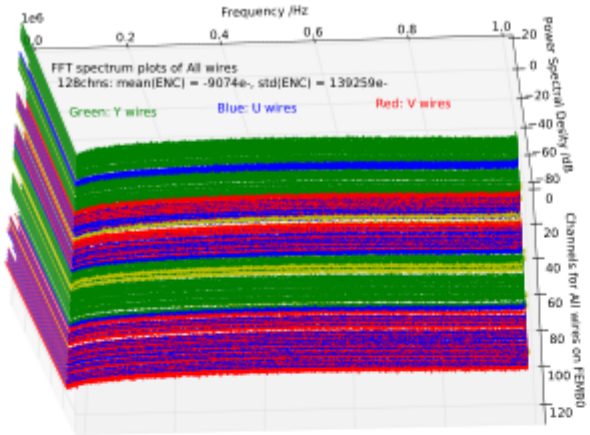
Difference: Connectors and cables to WIB

- SBND TPC FE
  - 4 APAs
  - 88 FEMBs
  - 128-ch per FEMB
  - Connector: Molex 75783-0132
  - 3M miniSAS cable (7m)

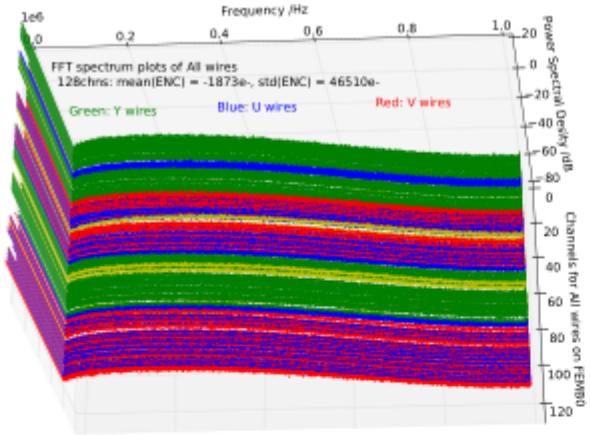


From Shanshan Gao (BNL)

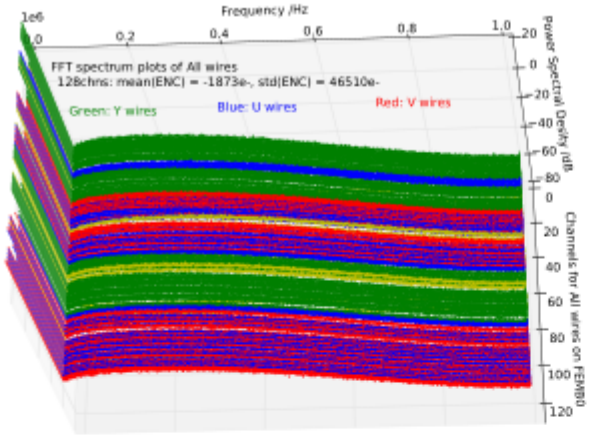
Results at room temperature (FEMB0)



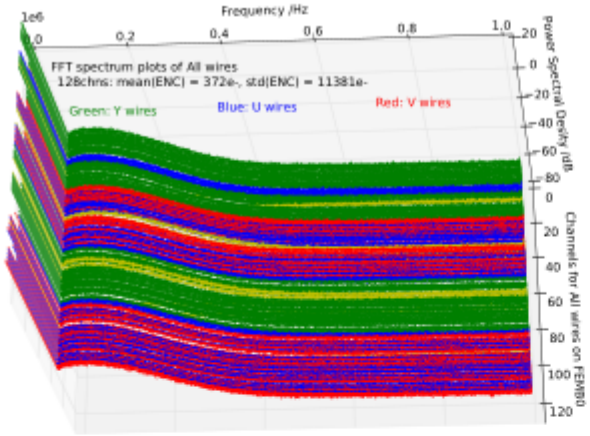
Tp = 0.5us



Tp = 1.0us

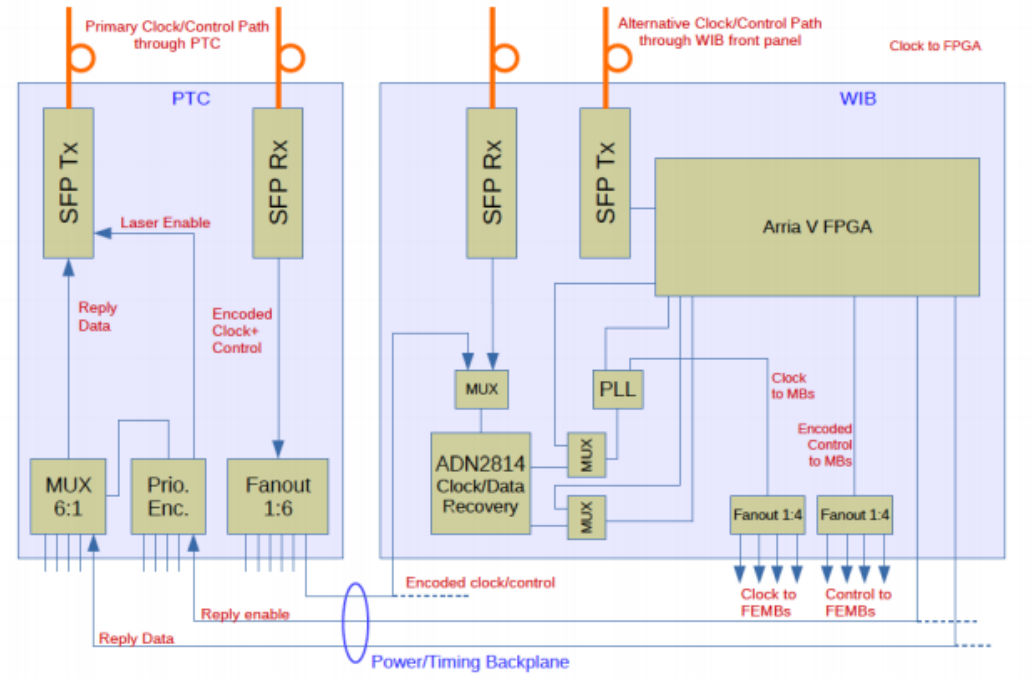


Tp = 2.0us



Tp = 3.0us

Warm Interface Electronics

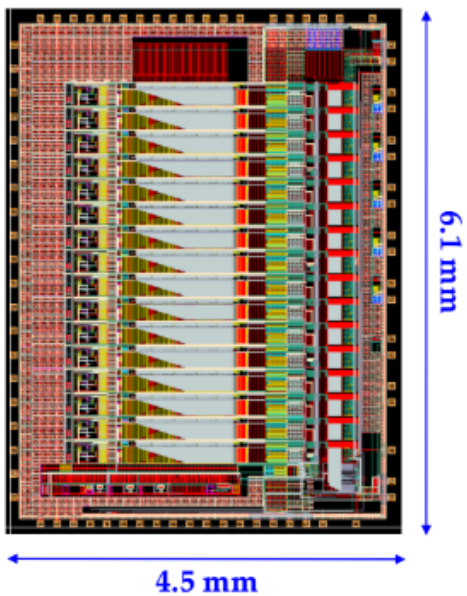


- Warm interface electronics is installed on top of the warm flange board
- Each Warm Interface Electronics Crate (WIEC) contains the following
  - 5 Warm Interface Boards (WIB), each WIB controls up to four 128-ch FEMBs
  - One Power and Timing Backplane (PTB) and one Power and Timing Card (PTC)
  - WIEC is a faraday cage with only power and optical signals going in and out

Table 2.3: APA design parameters

Parameter	Value
Active Height	5.984 m
Active Width	2.300 m
Wire Pitch (U,V)	4.67 mm
Wire Pitch (X,G)	4.79 mm
Wire Position Tolerance	0.5 mm
Wire Plane Spacing	4.75 mm
Wire Angle (w.r.t. vertical) (U,V)	35.7°
Wire Angle (w.r.t. vertical) (X,G)	0°
Number Wires / APA	960 (X), 960 (G), 800 (U), 800 (V)
Number Electronic Channels / APA	2560
Wire Tension	5.0 N
Wire Material	Beryllium Copper
Wire Diameter	150 μm
Wire Resistivity	7.68 $\mu\Omega$-cm @ 20° C
Wire Resistance/m	4.4 Ω/m @ 20° C
Frame Planarity	5 mm
Photon Detector Slots	10

ADC ASIC (P1 Version)

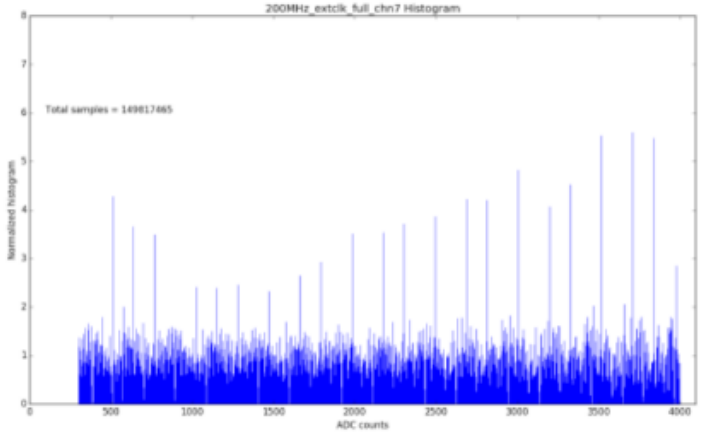


Datasheet: DUNE Doc 1485

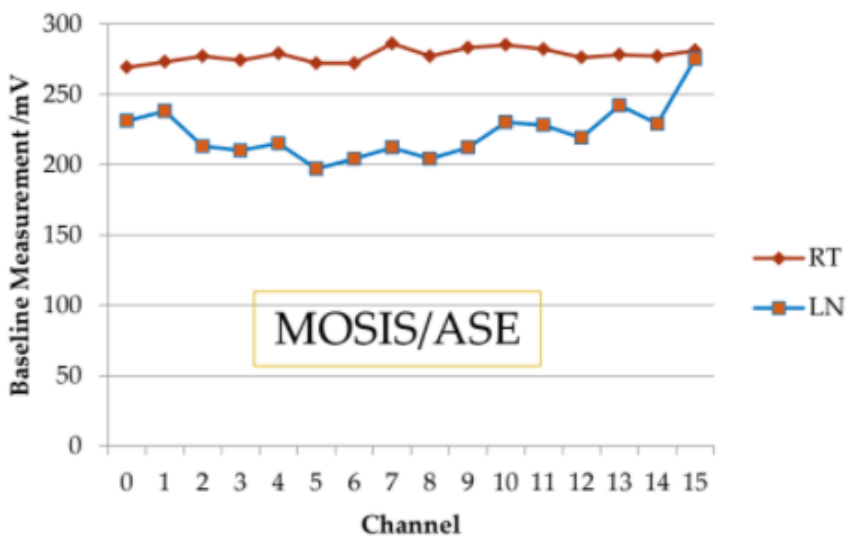
- Current-mode domino architecture
- 12-bit ADC at 2MS/s sampling rate
- 16 channels, programmable
- FIFO 192s bit wide x 32 bits deep
- Adjustable offsets
- Designed for 77-300K operation
- Designed for long lifetime

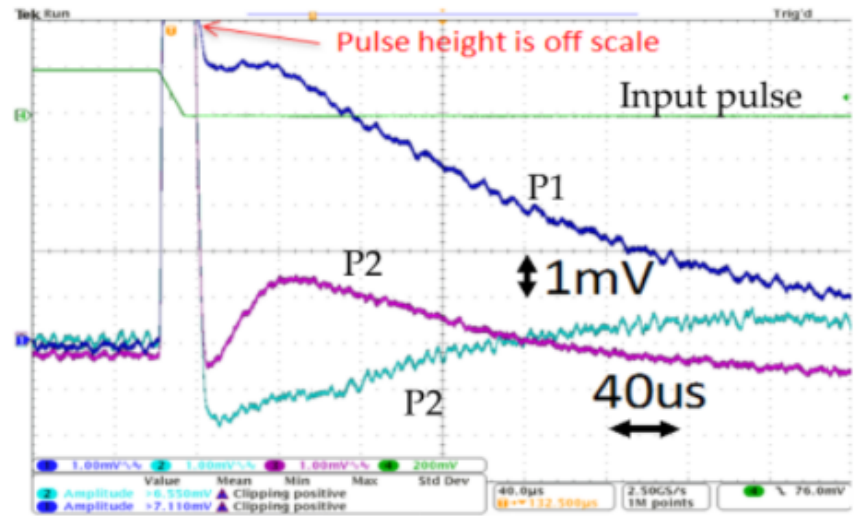
New features

- Address early saturation and roll-back
- Implement COLDATA compatible interface and FE ASIC compatible configuration
- Implement power-on default configuration and extend soft-control functions
- Revise BGR start-up circuit
  - No issue seen in ~2000 chip*cycles
- Increase ESD protection on I/O
- Improve ADC INL/DNL (not completely resolved)
  - Stuck codes still exists
  - However, both peak and area linearity test show reasonable INL (< 0.5%)



Improvements on P2 FE ASIC





(Green: Calib Pulse); (Dark Blue: P1 chn14); (Light Blue: P2 chn2), (Pink: P2 chn14)

Address baseline non-uniformity in LN2

→ Caused by combination of thermal pad and packaging stress

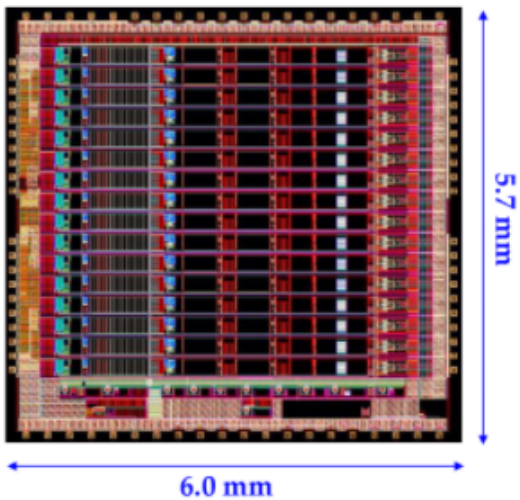
→ Tested three vendors: Quik-Pak, Novapak, and MOSIS/ASE

→ **MOSIS/ASE provides the best packaging solution**: low stress compound w/o thermal pad

Address pole-zero cancellation

→ P2 FE baseline recovery dispersion is ~1.5% of peak height

Front End ASIC (P2 Version)

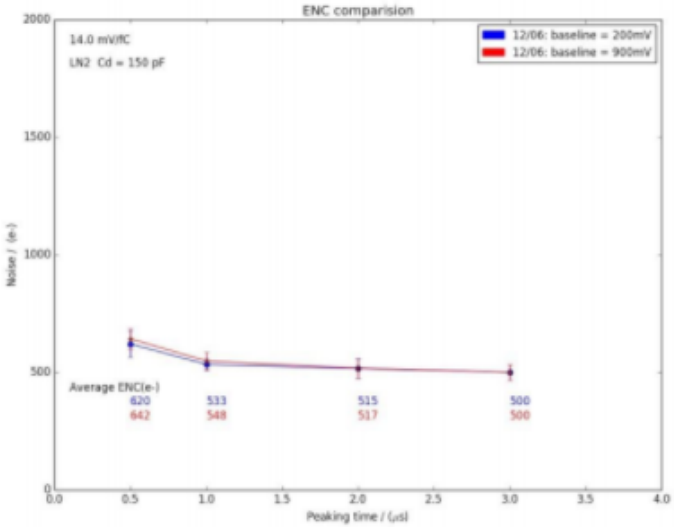


Datasheet: DUNE Doc 1484

- 16 channels, programmable
- Low power consumption: ~5.5mW/channel
- Charge amplifier, high-order filter
- Adjustable gain: 4.7, 7.8, 14, 25mV/fC
- Adjustable filter time constant: 0.5, 1.0, 2.0, 3.0 us
- Selectable collection/non-collection mode
- Designed for 77K-300K operation
- Designed for long lifetime

New features

- Built-in 6-bit DAC for calibration pulse generation
- Built-in analog monitoring output for debug
- Add higher bias current (1nA and 5nA) options and smart reset
- Revise BGR start-up circuit
  - No issue seen in ~2000 chip*cycles
- Increase ESD protection on I/O

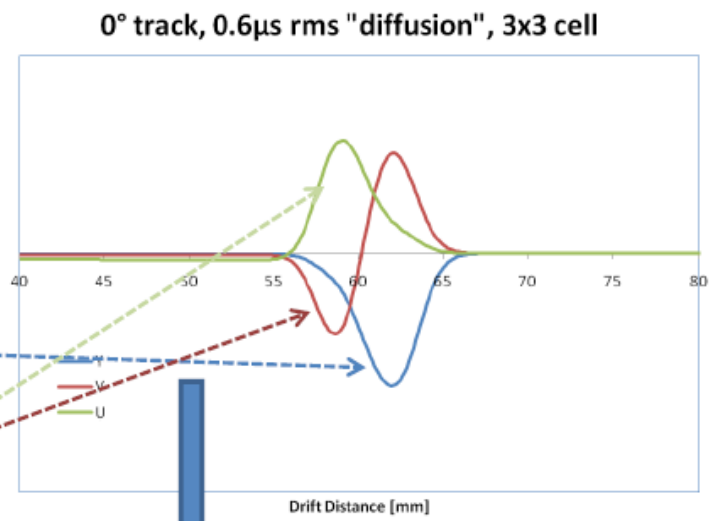


ENC < 550 e^- @ 1us when C_d = 150pF

Signals in LAr TPC

- Charge signal
  - A 3mm MIP track should create 210keV/mm x 3mm /23.6eV/e = 4.3fC
  - After a 1/3 initial recombination loss: ~2.8fC
  - Assume the drift path to equal the charge life time, reducing the signal to 1/e≈0.368
  - The expected signal for 3mm wire spacing is then ≈1fC=6250 e, … and for 5mm, ≈10^4 e, for **the "collection signal"**
  - The induction signals are smaller
  - The time scale of TPC signals is determined by the **wire plane spacing** and **electron drift velocity**, (~1.5 mm/μs at 500 V/cm)

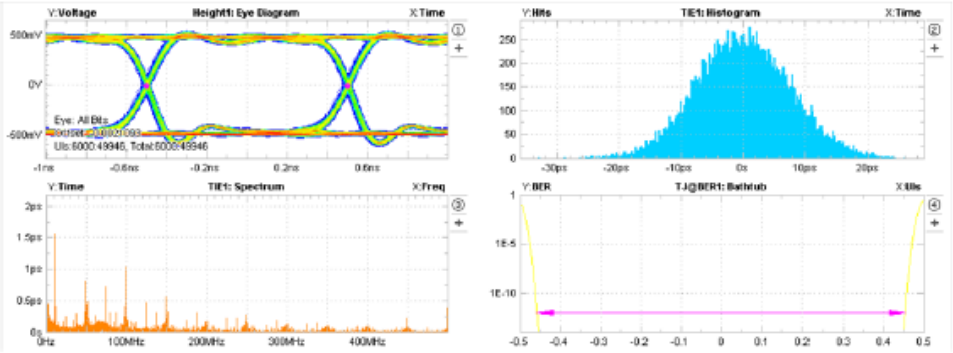
Induced Current Waveforms on 3 Sense Wire Planes

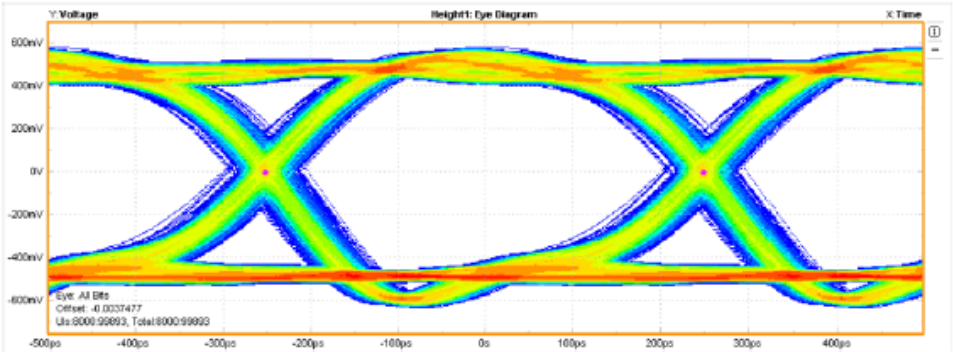


Sampling rate **≤ 2 Ms/s**

Cold FPGA (COTS)

- Many commercial FPGA were tested by BNL
  - Altera Cyclone IV FPGA GX is qualified FPGA for cold operation



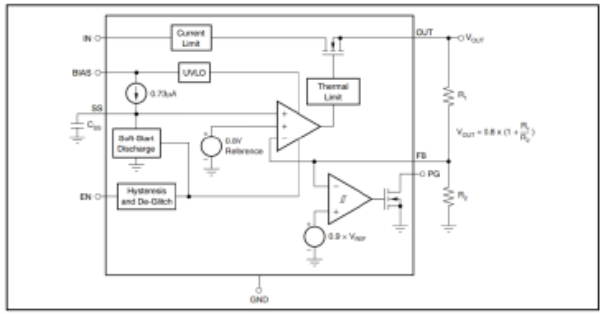


Test of Cyclone IV GX Transceiver Starter Board in LN2

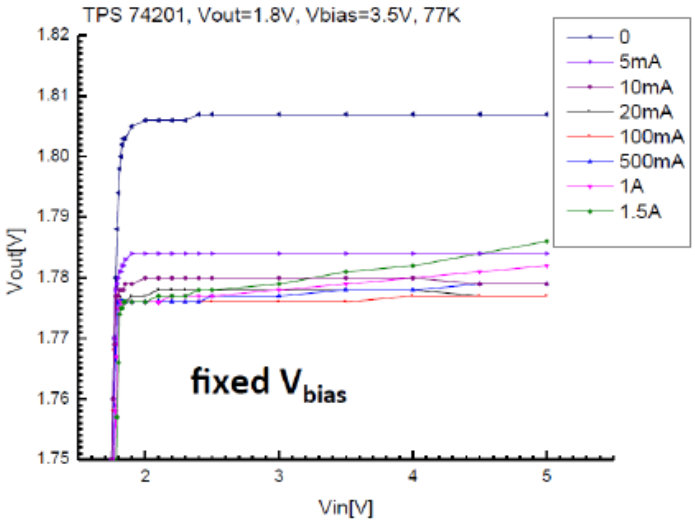
- Transceiver works well at both 1Gbit/s and 2Gbit/s
- Height
  - 839mV @ 1Gbit/s
  - 823mV @ 2Gbit/s
- Eye Width
  - 914ps @ 1Gbit/s
  - 357ps @ 2Gbit/s
- On board SRAM works with BIST
  - 18-Mb SRAM from ISSI IS61VPS102418A-250TQL
  - Cyclone IV GX is running with Nios II processor and utilization of ~80% fabric resources

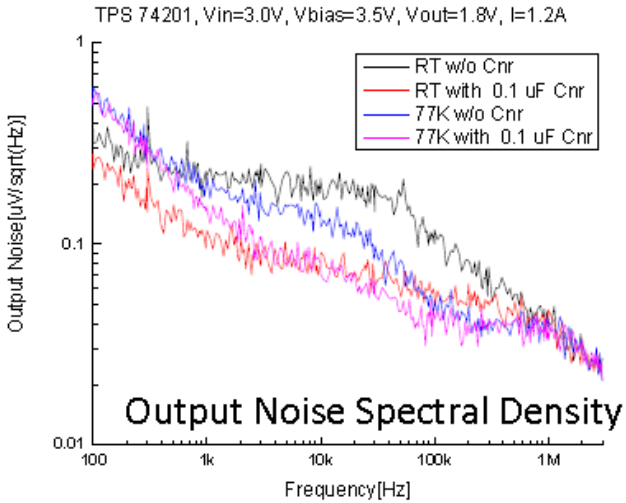
Cold Voltage Regulator (COTS)

- TI TPS742xx voltage regulator family has been identified working well at cryogenic temperature by BNL

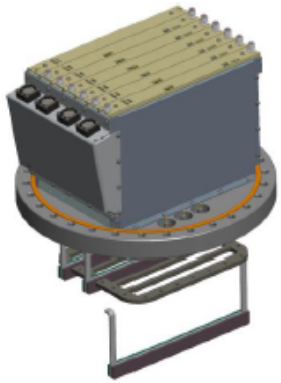


- 1.5A max I_{out}, 0.8V-3.6V adjustable V_{out}, and 55mV drop-out (typical @1.5A) makes it an ideal candidate for all of the cold electronics chain
- Low frequency noise will need to be filtered out properly to achieve optimum noise performance of cold electronics

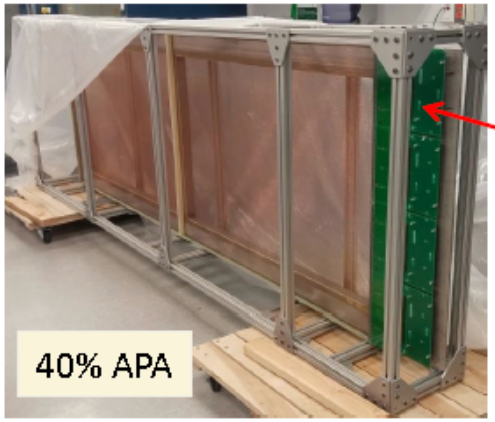


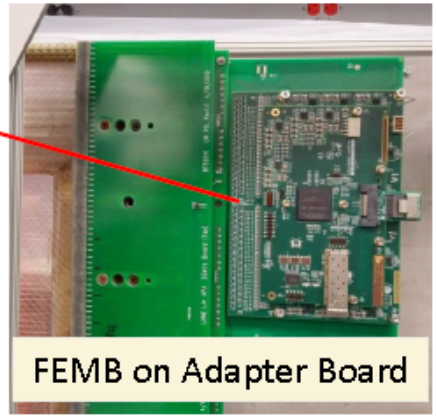


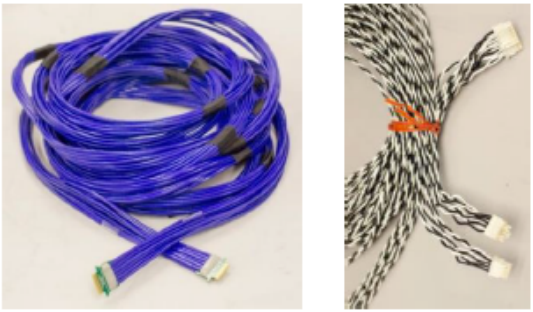
Integration Test stand



Cold box will house APA+CE, plus cold LV and data cable.
Cold box can be tilted to submerge FEMB+cable in LN2







7m Cold Data Cable and Power Cable

Dynamic Range

The requirement to measure a MIP-size charge from the cathode with a precision of 1% in the collection plane determines the lower end of the dynamic range. The need to collect charge deposited at the vertex of a neutrino event (mainly by protons) without suffering satura0on sets the upper end.

- Lower end calculation
  - To obtain 1% charge resolution requires 1% of 11.6k e^-: ~116 e^- per ADC count
- Upper end calculation
  - Proton energy distribution is isotropic in the range 10-100 MeV
  - Worst case assumption: all energy deposited in one 0.5cm voxel
  - Proton at wire plane: no drift losses, instantaneous deposition

$$\frac{E_{loss}\,(0.5\text{ cm})}{\text{LAr } E_{ee}} \times \frac{\text{Recombination}}{(500\text{ V/cm})} = \frac{21\text{ MeV}}{23.6\text{ eV}} \times 0.25 = 222.5\text{k } e^-$$

  - For CC ν_e - Ar interactions assume a mean of 2 protons/vertex
  - 445k e^- maximum charge ÷ 116 e^- /count = 3,836 counts

12-bit ADC is sufficient for digitization

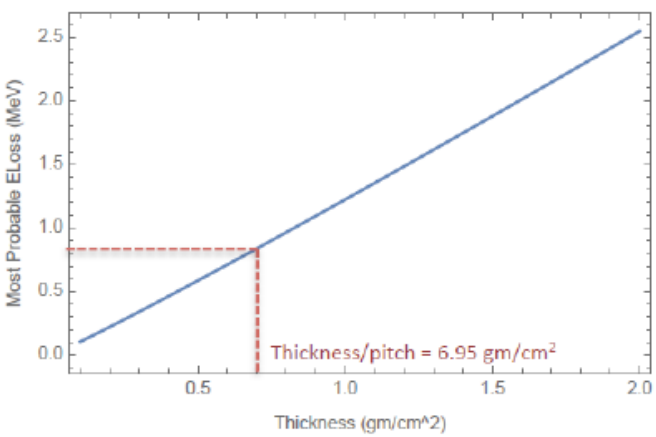
Signal to Noise

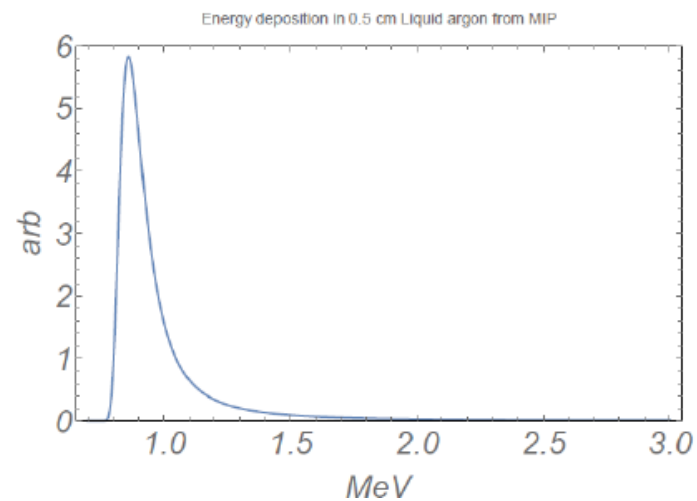
Total equivalent noise charge (ENC) shall be less than 1/9 of the expected worse case instantaneous charge arriving at the APA from a MIP.

- Driven by far detector S:N requirement to "distinguish a Minimum Ionizing Particle (MIP) track cleanly from electronic noise everywhere within the drift volume."
- Simple calculation of charge from a MIP track at the cathode parallel to the wire spacing:

$$\frac{E_{loss}\,(0.5\text{ cm})}{\text{LAr } E_{ee}} \times \frac{\text{Recombination}}{(500\text{ V/cm})} \times e^{-\frac{\text{DL/velocity}}{e^- \text{ lifetime}}} = \frac{0.83\text{ MeV}}{23.6\text{ eV}} \times 0.7 \times e^{-\frac{3.6\text{m}/1.6\text{ m/ms}}{3\text{ ms}}} = 11{,}629\ e^-$$

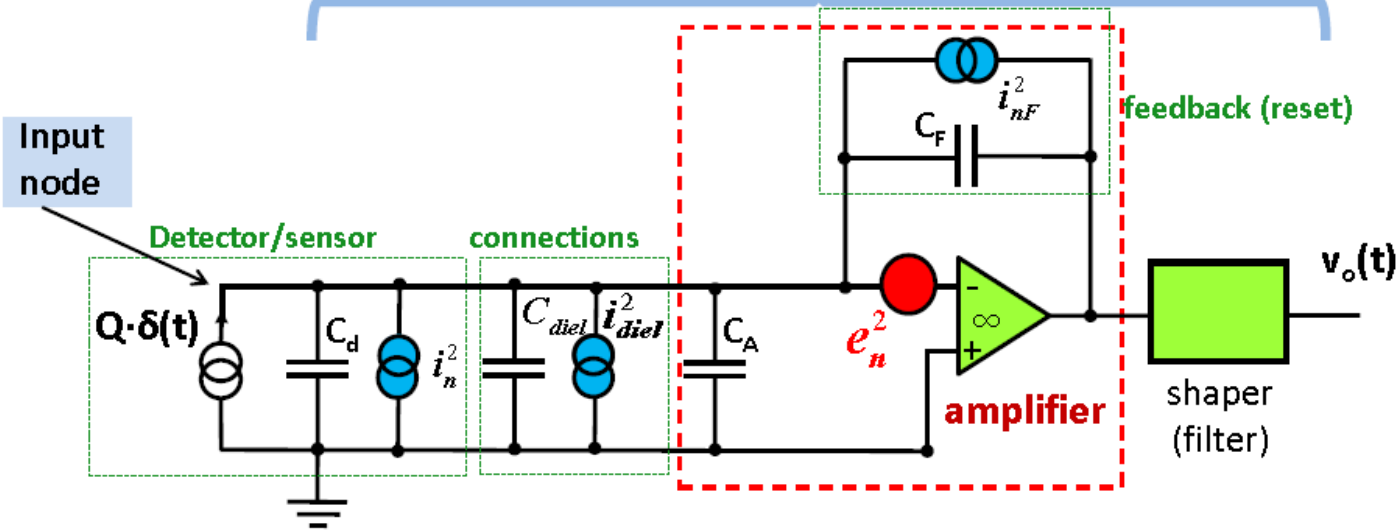
- Sets the collection wire noise parameter at ENC < 1300 e^-
- Equivalent charge on the induction wires is expected to be 0.5 x collection wire charge
- Induction wire noise parameter ENC < 650 e^-





Noise Sources in Detector-Amplifier

Overall system processing function: $h(t); w(t); H(j\omega)$



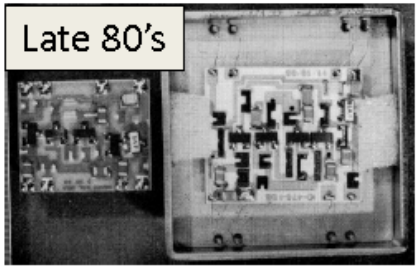
Dominant noise sources are from the components and circuits **directly connected to the input node**. Noise sources from the rest of the signal processing chain should be made negligible.

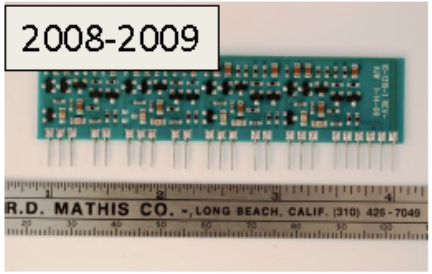
- i_n^2 arises in the sensor, e.g., from the leakage (dark) current; i_{nF}^2 may arise in feedback circuit
- i_{diel}^2 thermal fluctuations in dielectrics (dielectric loss noise)
- e_n^2 **noise associated with the input transistor:**
  MOSFET gain: "*series white noise*"
  trapping-detrapping: *1/f* eq. noise voltage generator in series

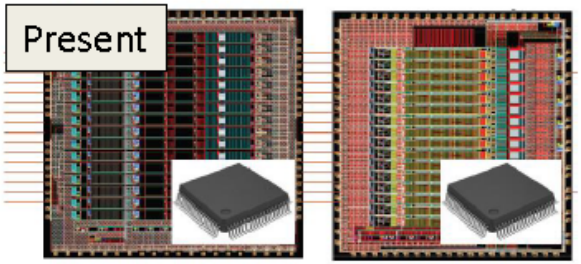
24

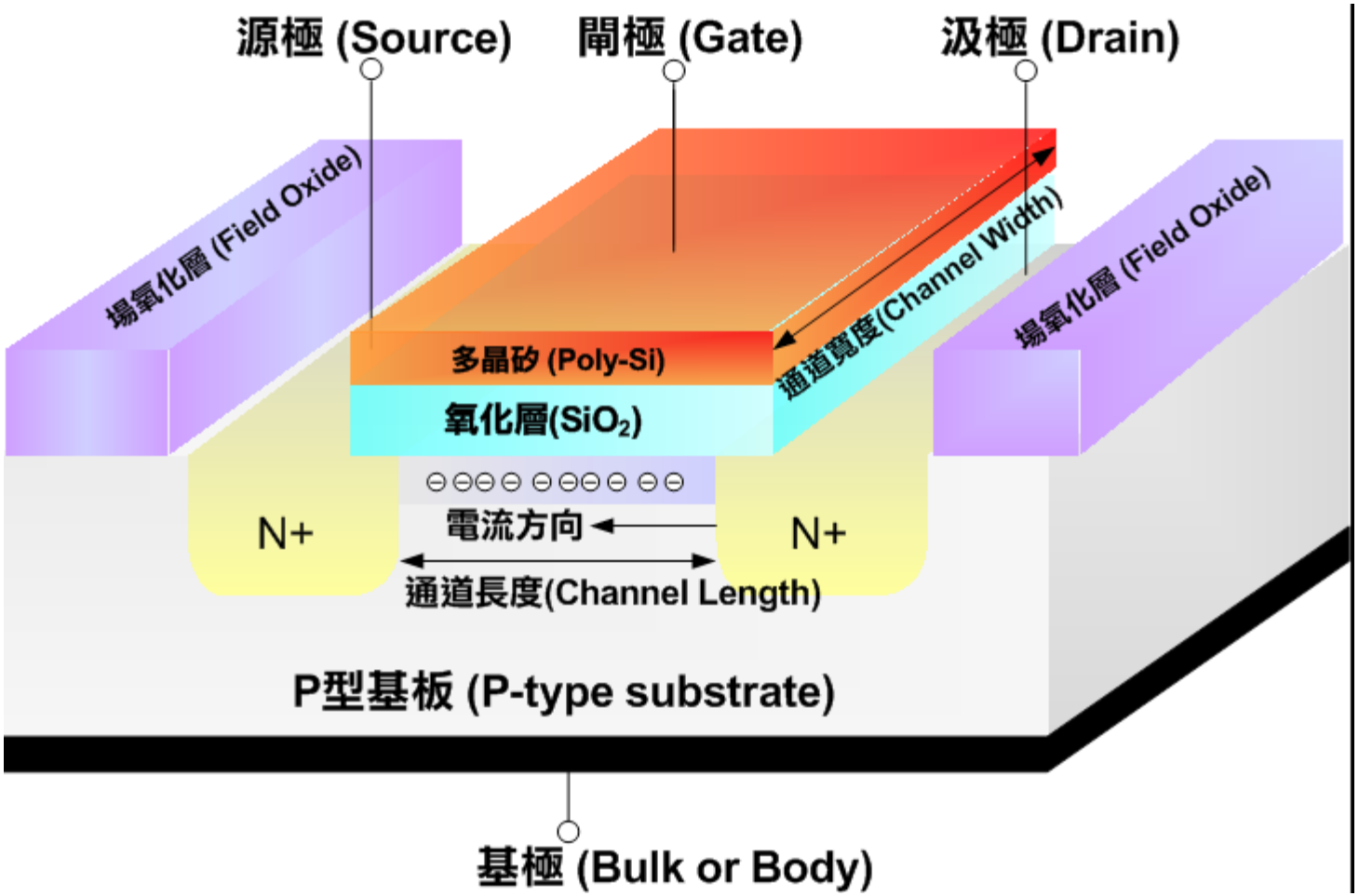
A Brief History of Cold Electronics

- Motivation of CE
  - Cold electronics decouples the electrode and cryostat design from the readout design. With electronics integral with detector electrodes, the noise is independent of the fiducial volume (signal cable lengths), and much lower than with warm electronics
- Late 80's, Cryogenics Front-End based on JFET
  - Liquid Argon calorimeter, 576 preamplifiers
- 2008-2009, MicroBooNE front-end design started from JFET
- Present, cryogenic CMOS ASIC for SBND and ProtoDUNE-SP
  - MicroBooNE has adopted the cryogenic CMOS analog front end ASIC developed for LBNF/DUNE LAr TPC program in 2010








源極 (Source)
閘極 (Gate)
汲極 (Drain)
場氧化層 (Field Oxide)
場氧化層 (Field Oxide)
多晶矽 (Poly-Si)
氧化層(SiO2)
通道寬度(Channel Width)
N+
N+
電流方向
通道長度(Channel Length)
P型基板 (P-type substrate)
基極 (Bulk or Body)