

Construction of the Phase 1 Upgrade of the CMS Pixel Detector

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on behalf of CMS Collaboration

**Fermi National
Accelerator Laboratory**

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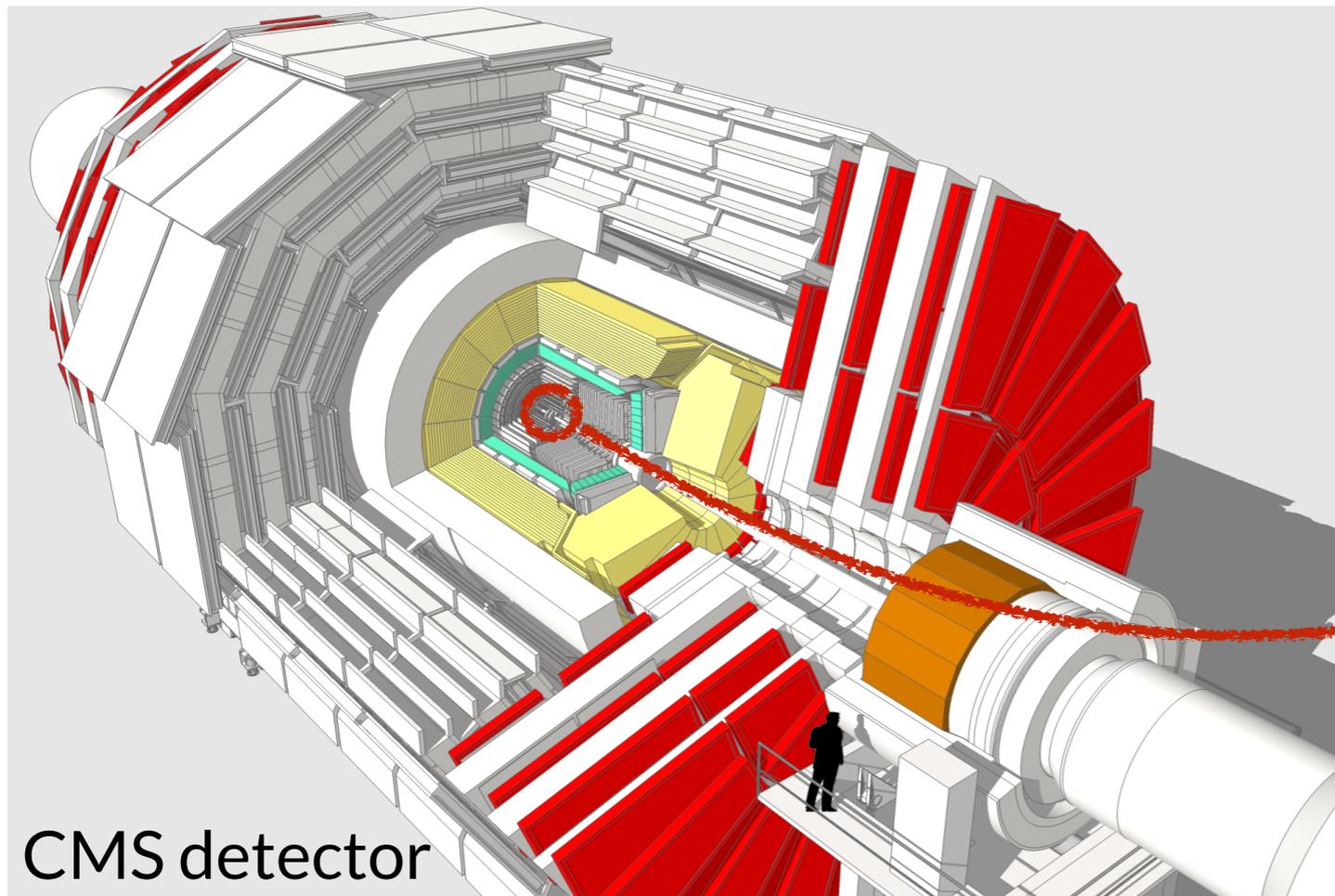
August 1st, 2017

Outline

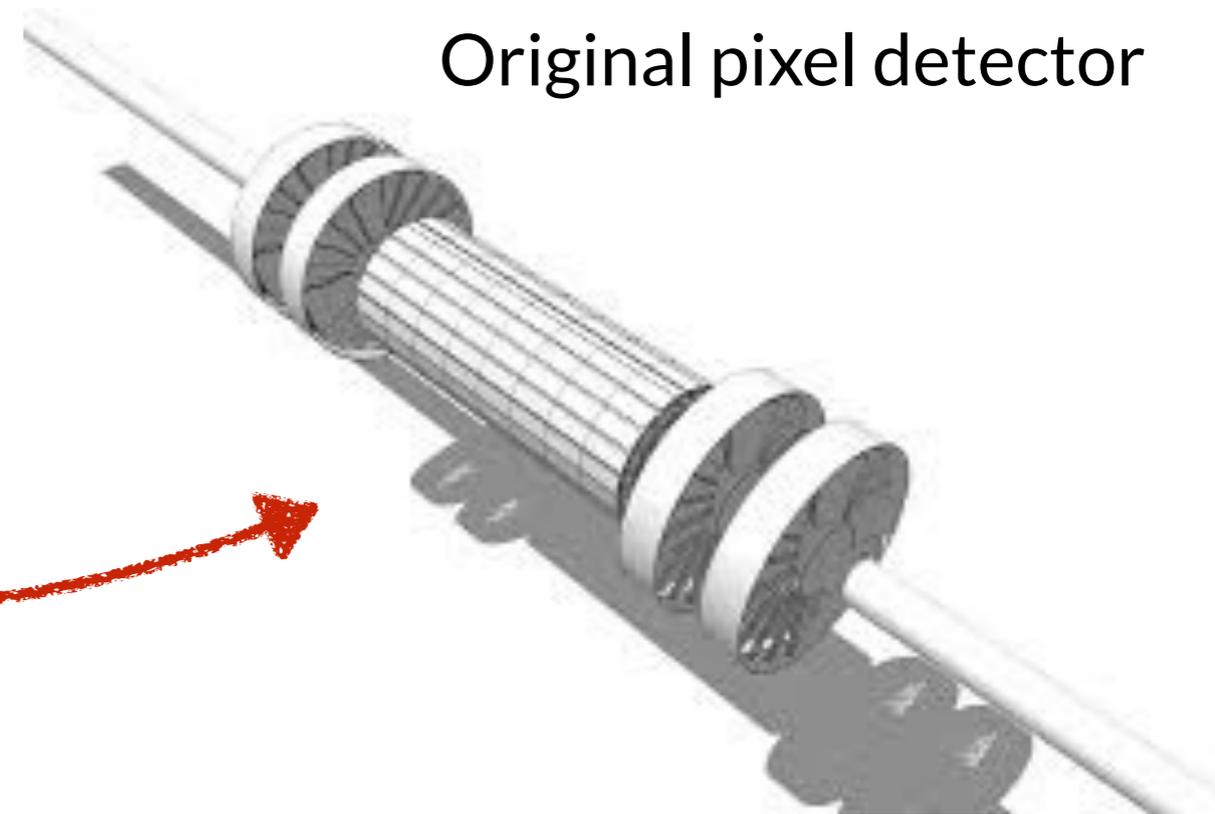
- The original pixel detector
- Upgrade motivation
- The upgraded pixel detector (including some of the construction challenges)
 - The upgraded pixel tracker layout
 - Sensor modules and readout chips
 - Mechanics
 - Cooling



The Original Pixel Tracker



CMS detector

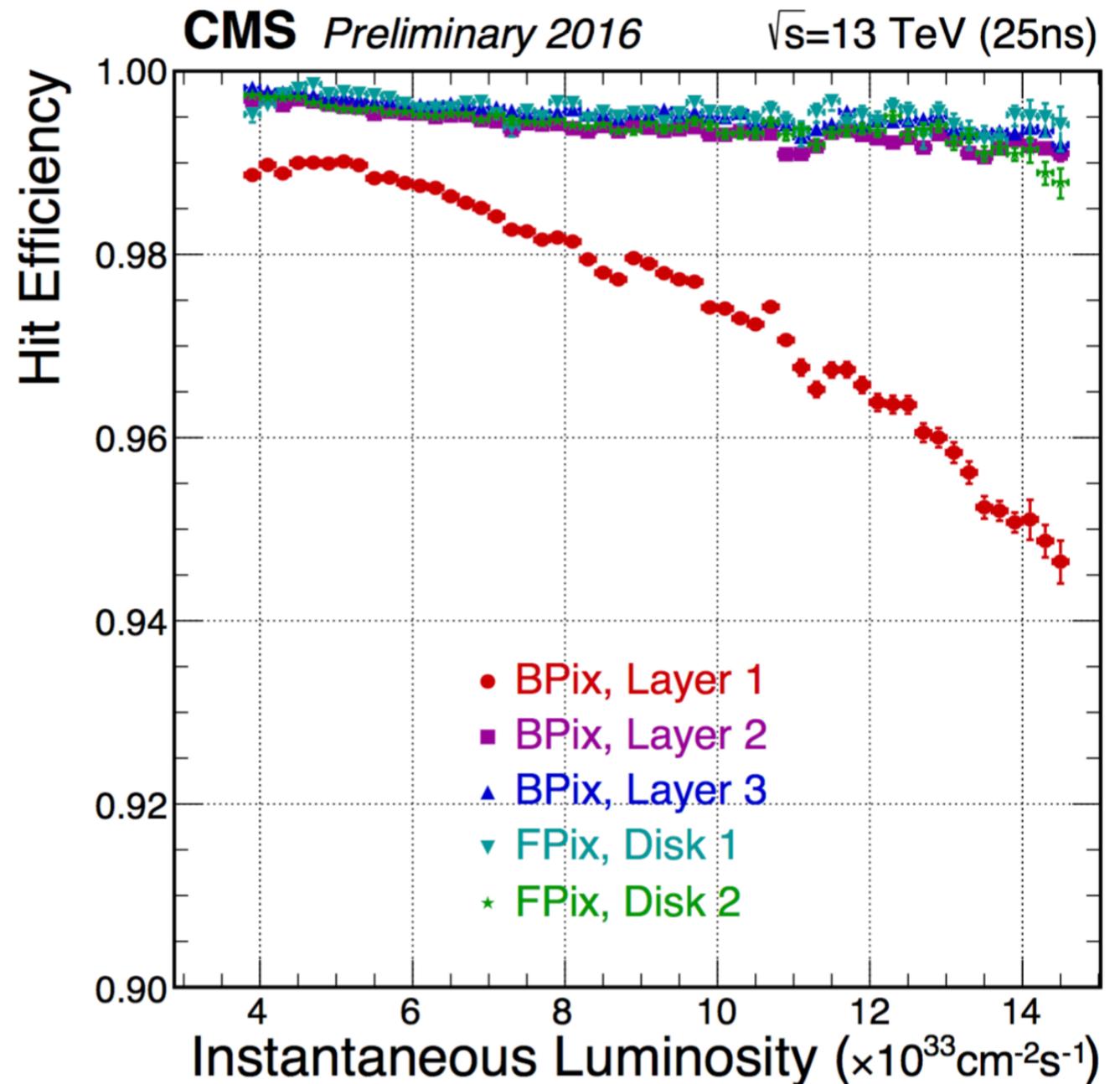


Original pixel detector

- The original pixel tracker of the Compact Muon Solenoid (CMS) experiment is:
 - The innermost CMS sub-detector (closest to the collision point)
 - Used for reconstruction of the tracks and vertices of charged particles

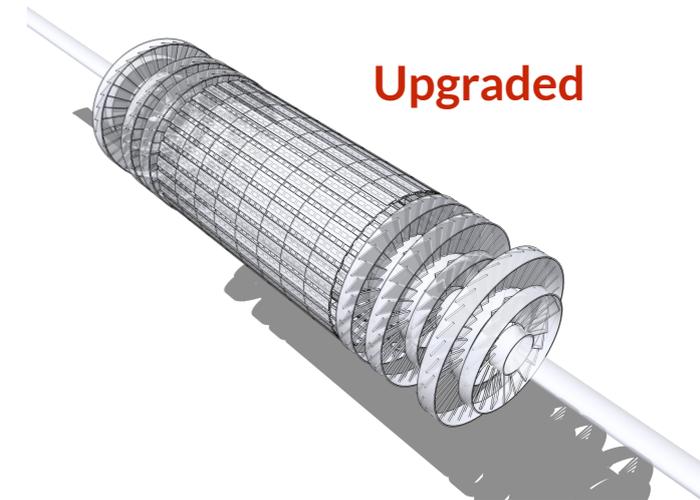
Upgrade Motivation

- The LHC has exceeded the designed instantaneous luminosity of $10^{34} \text{ cm}^{-2} \text{ s}^{-1}$
- Dynamic inefficiencies / dead time caused by limited size of readout bandwidth, affecting detector performance for instantaneous luminosity $> 1.6 \times 10^{34} \text{ cm}^2 \text{ s}^{-1}$

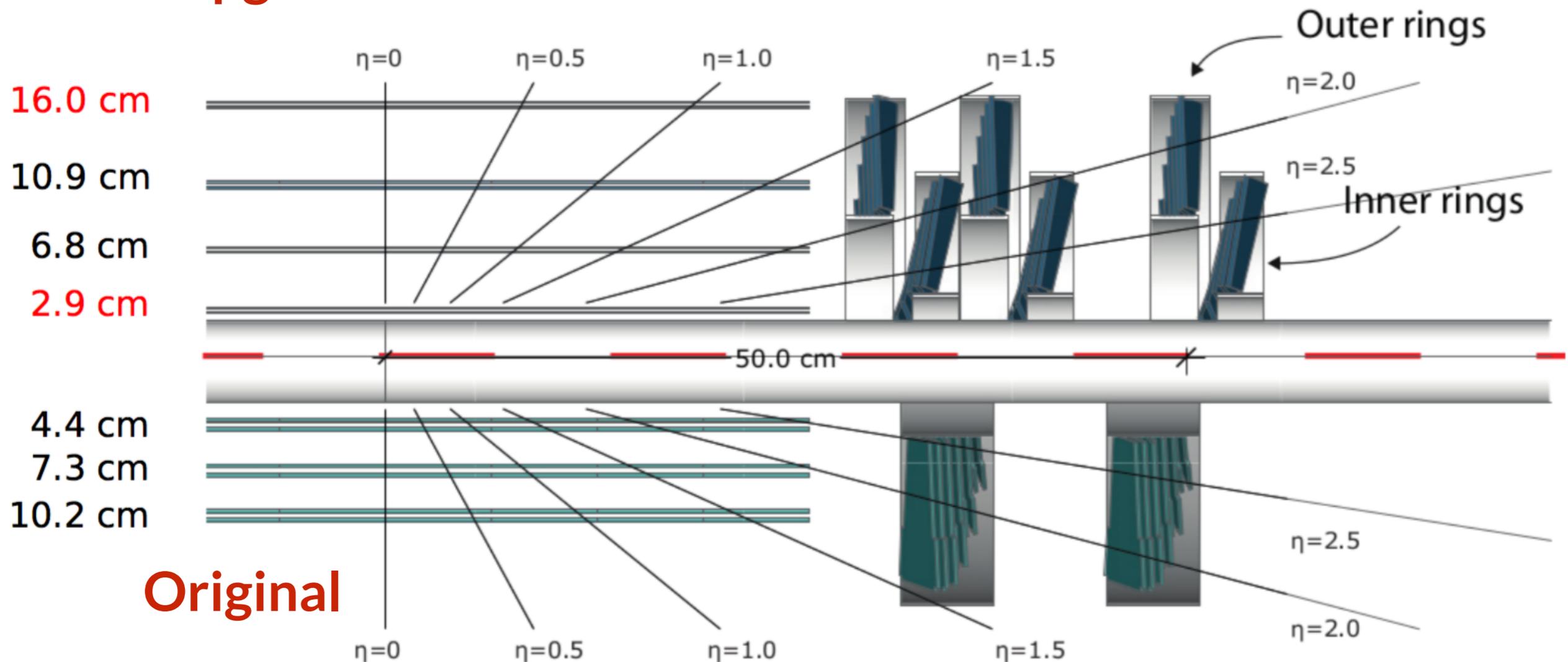


Upgraded Pixel Tracker Layout

- One additional barrel layer and forward disk
- Inner most layer moved closer to the interaction point
- Outer most layer moved further from the interaction point

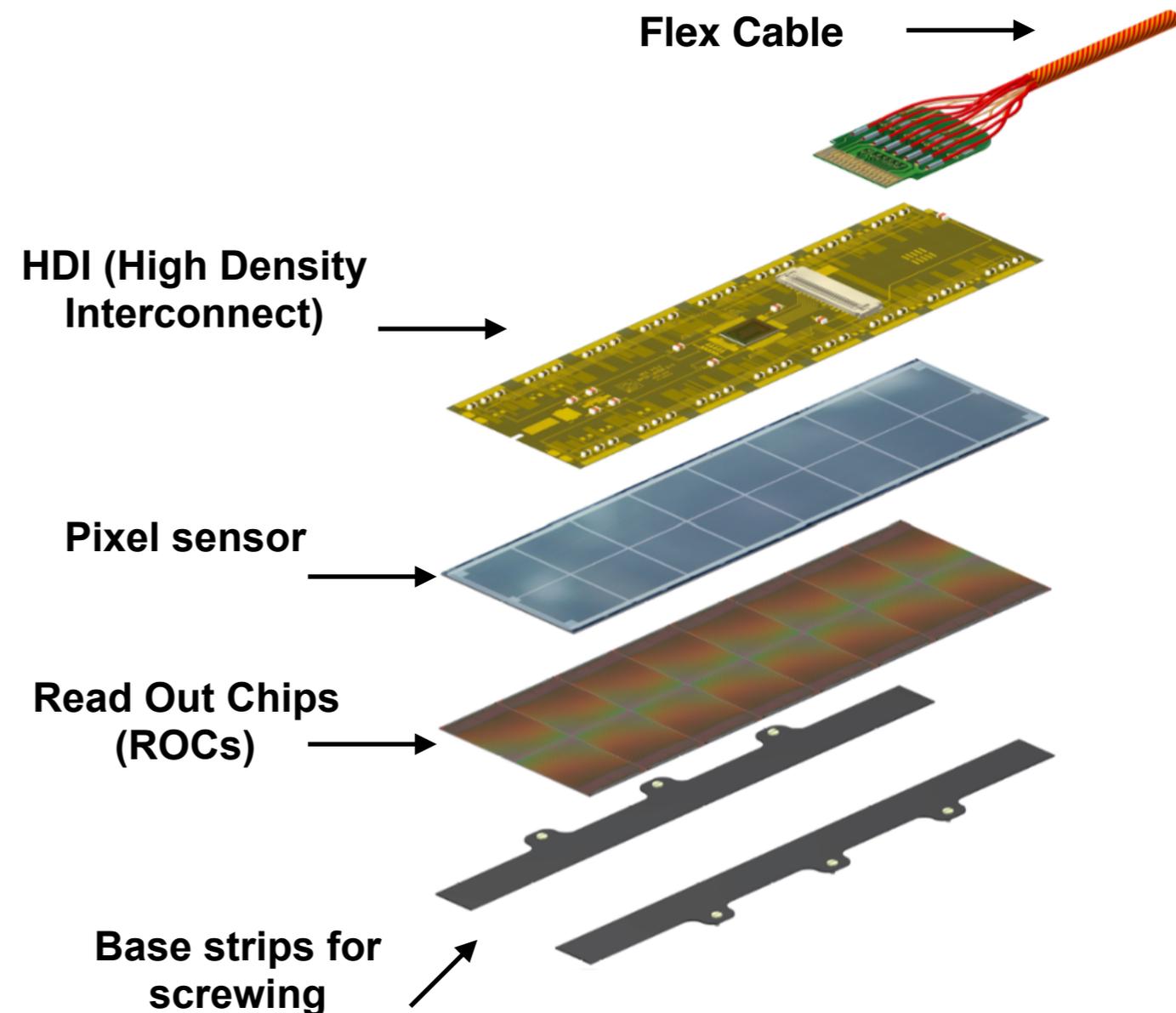


Upgraded



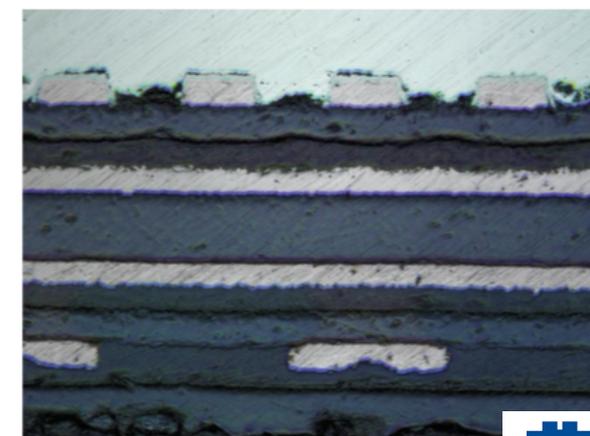
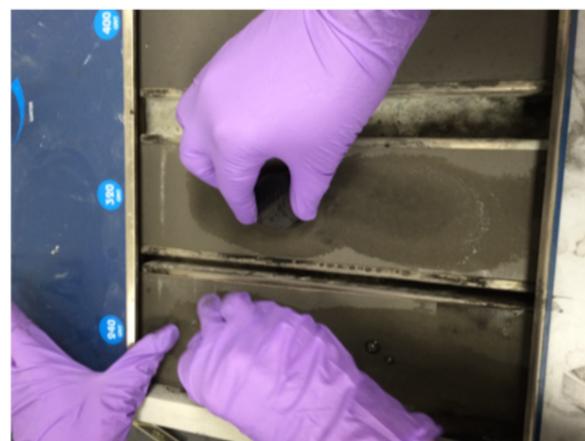
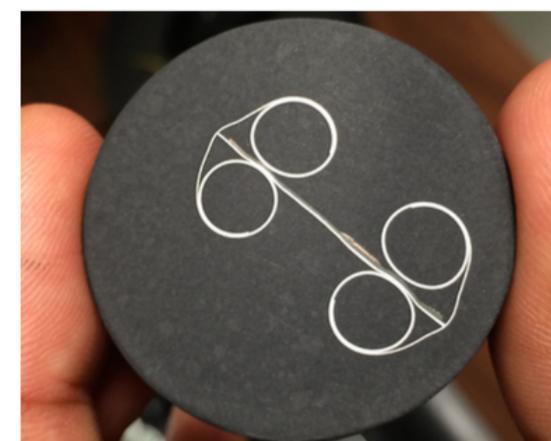
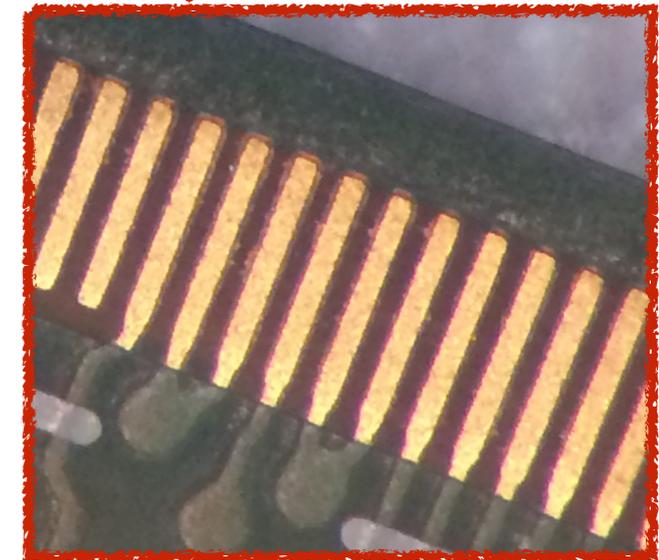
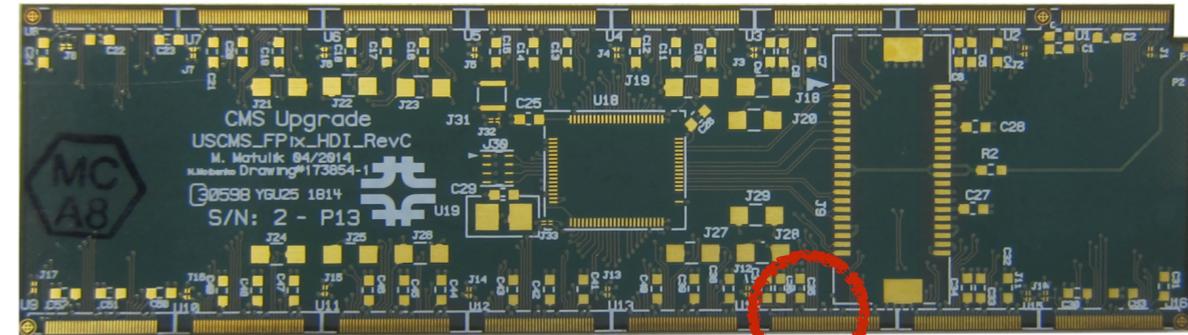
New Sensor Modules and Readout Chips

- Upgraded sensor and module design:
 - 285 μm thick n⁺-in-n silicon sensors (same as original)
 - 100x150 μm^2 pixel size (same as original)
 - Only one sensor geometry through entire pixel detector
 - 2 × 8 readout chips (ROCs) per module
- New faster digital ROCs are used
 - 40 MHz analog -> 160 Mbit/s digital
- Module readout bandwidth increased by a factor of 8
 - 40 Mbit/s -> 320 Mbit/s



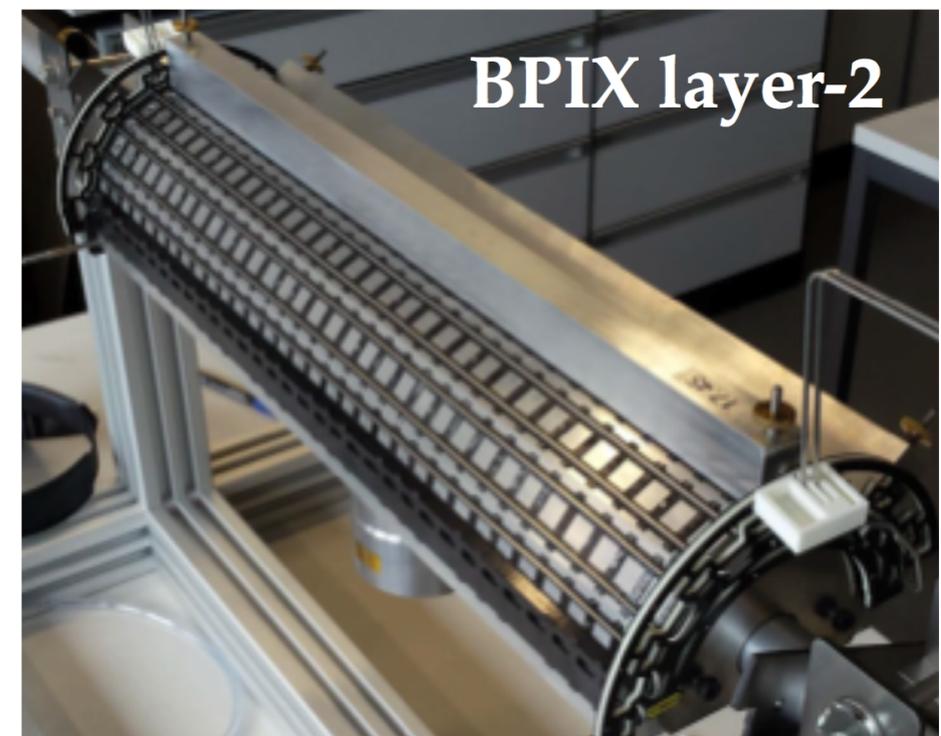
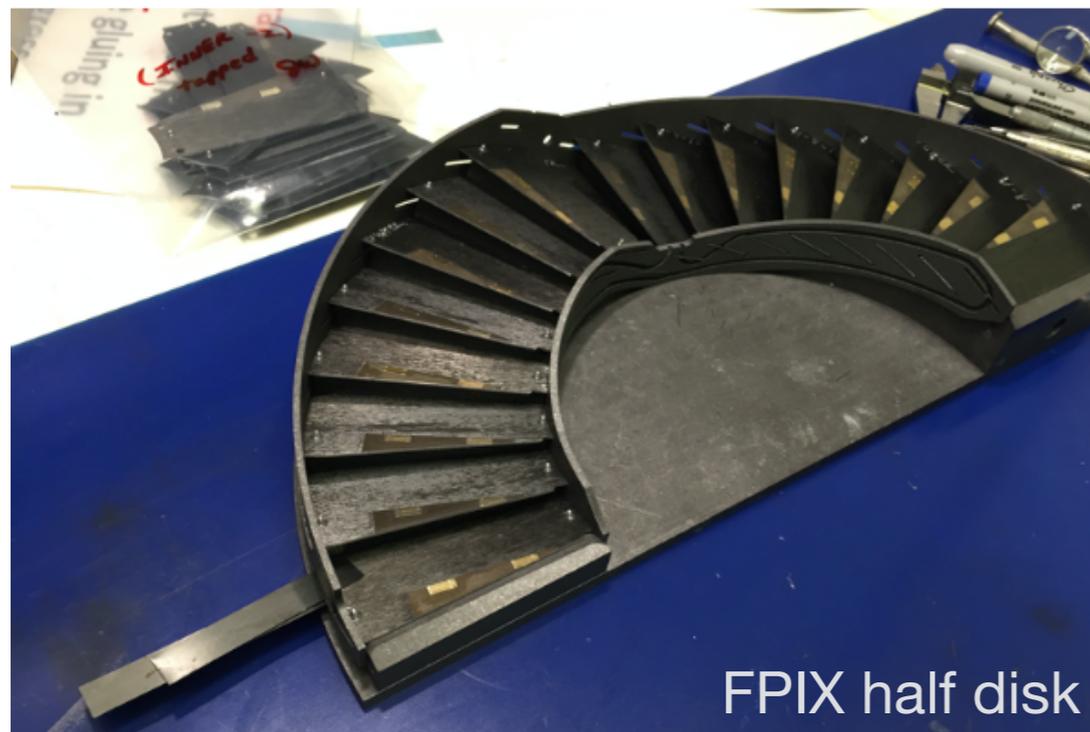
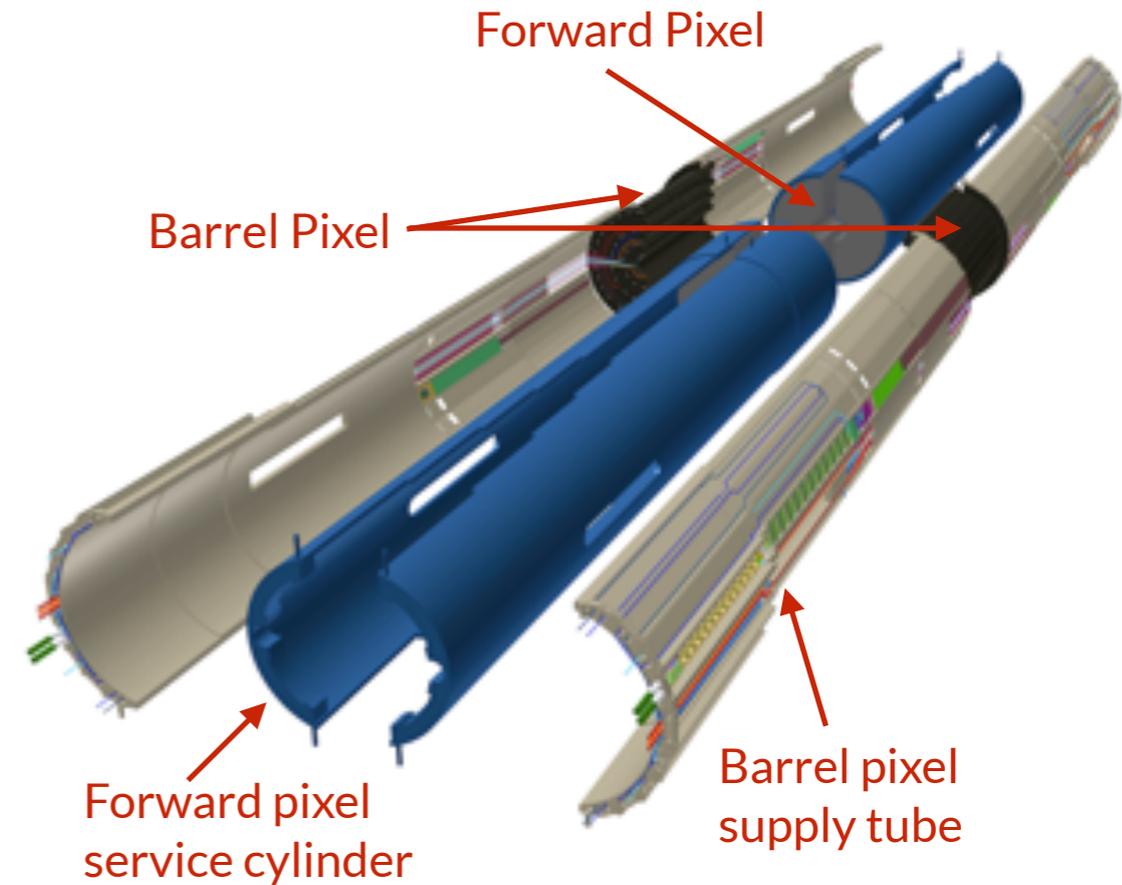
High Density Interconnects Challenges

- Problems encountered:
 - Wire bonding difficulties due to the insufficient thickness of Copper under the wire-bonding pads
 - High voltage breakdowns
 - Yield issues
- Solutions:
 - Improving visual inspections
 - Making thickness measurements on the thicknesses of layers on selective high density interconnects from each batch
 - Preventing high voltage breakdowns by improving the backing of the HDIs besides adding an additional layer of Kapton.
 - Making more batches, improving fabrication process (vendor)



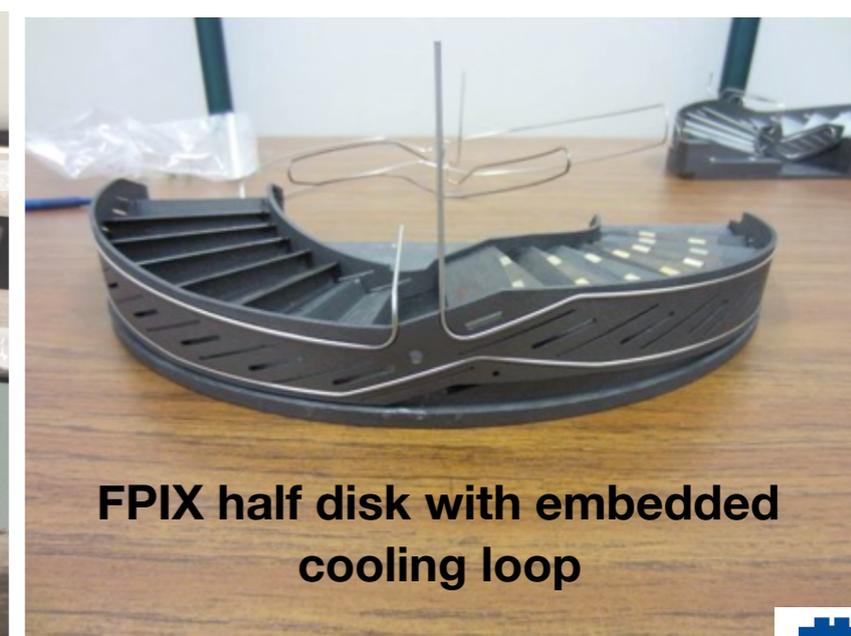
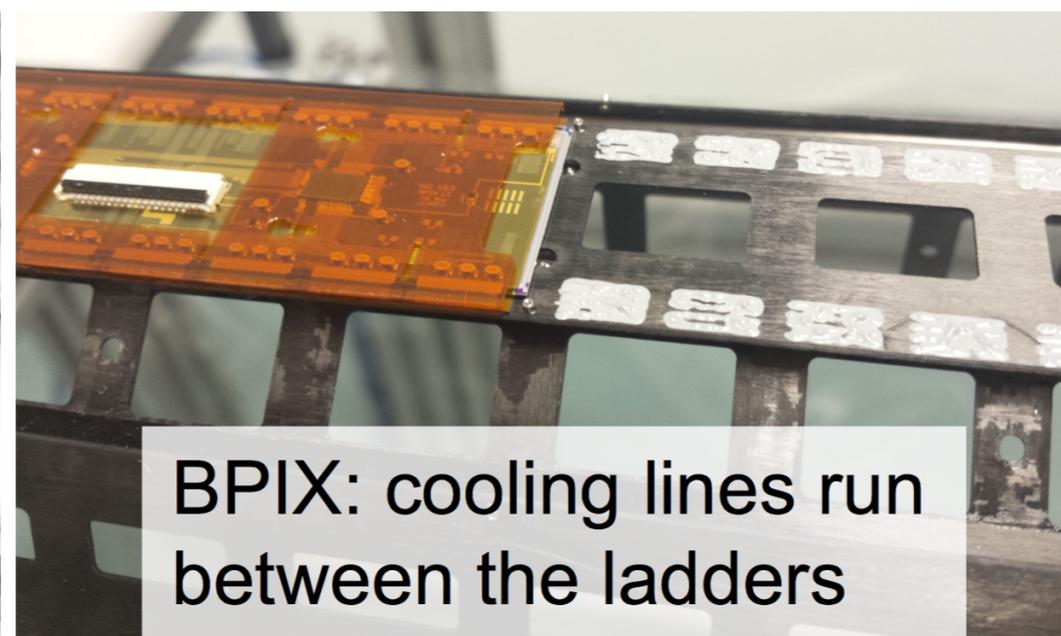
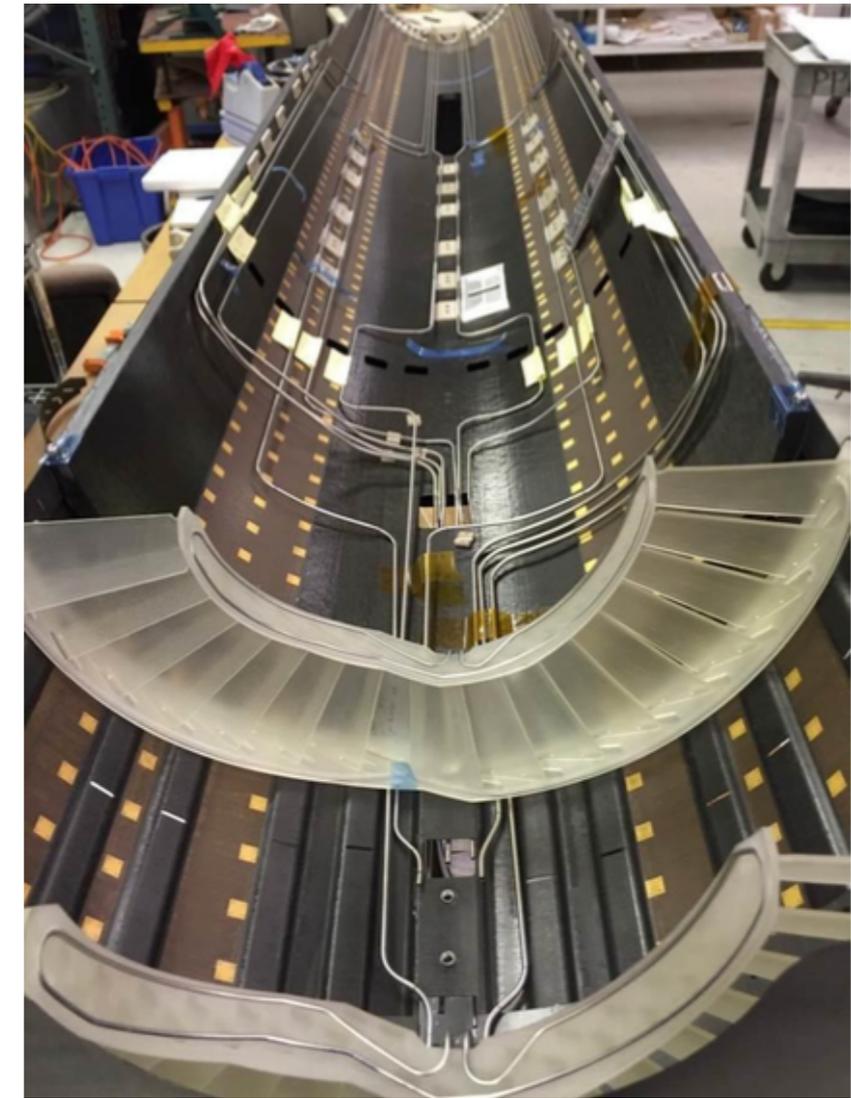
Mechanics

- Light weight Carbon Fiber structure supports services and cooling tubes
- Barrel pixel modules are installed on Carbon Fiber plates
- Forward pixel modules are installed on Thermal Pyrolytic Graphite (TPG) blades encapsulated with Carbon Fiber and glued to Graphite rings

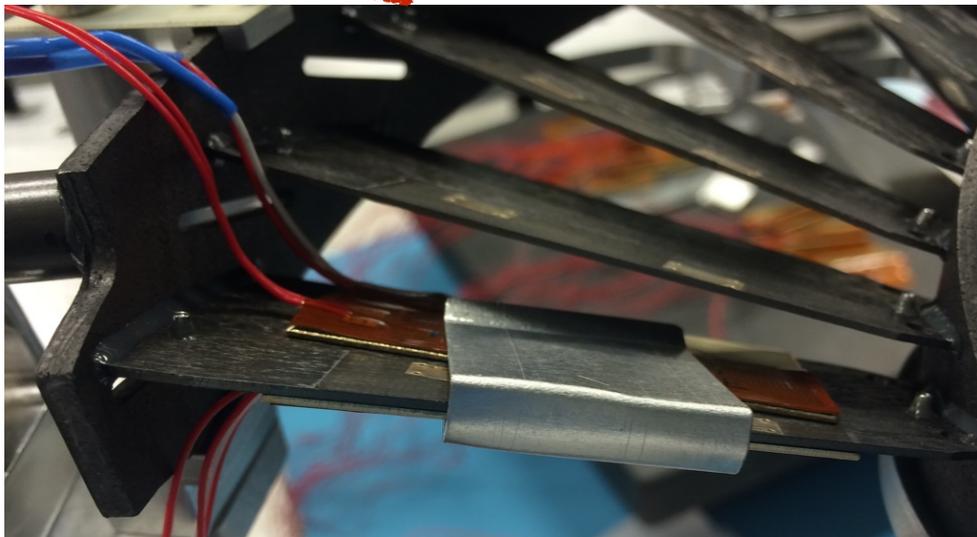


Cooling

- Mono-phase C_6F_{14} is replaced with Two-phase CO_2
 - More effective heat removal through latent heat
 - Thinner cooling tubes (≤ 0.5 of original tubes)
 - Tube wall thickness: 50-100 μm
 - Benefitting from high thermal conductivity of Carbon Fiber/Graphite/Thermal Pyrolytic Graphite
 - Operating point 20 bars at $-20^\circ C$

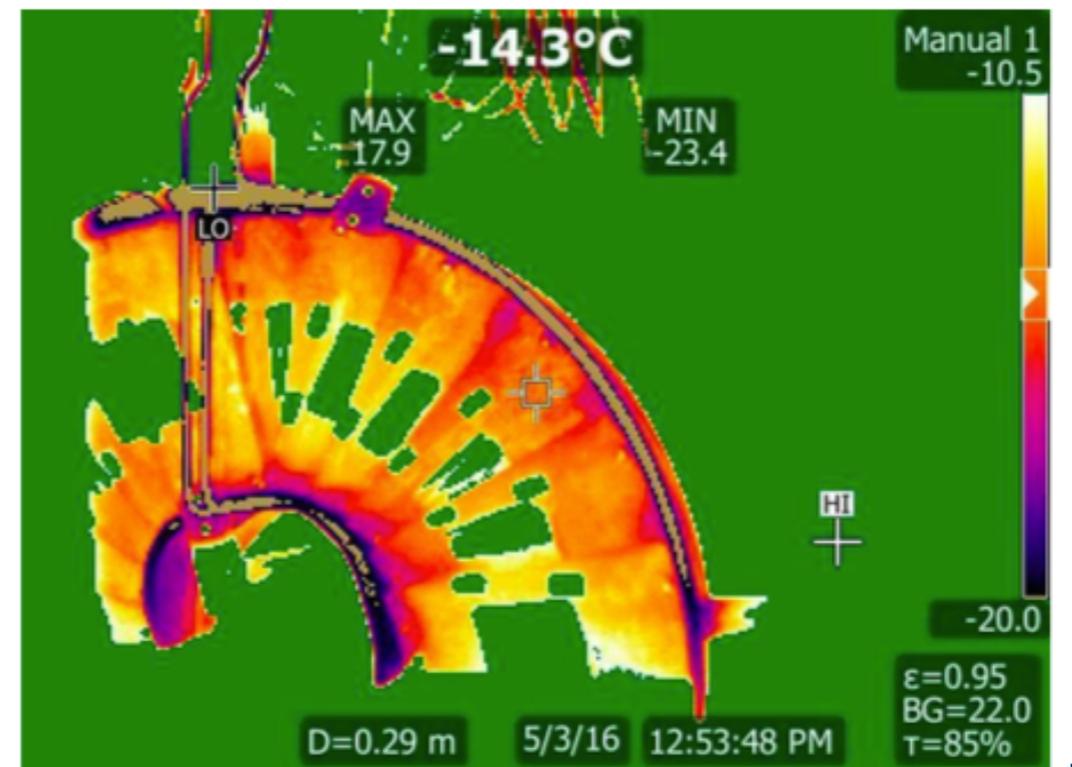
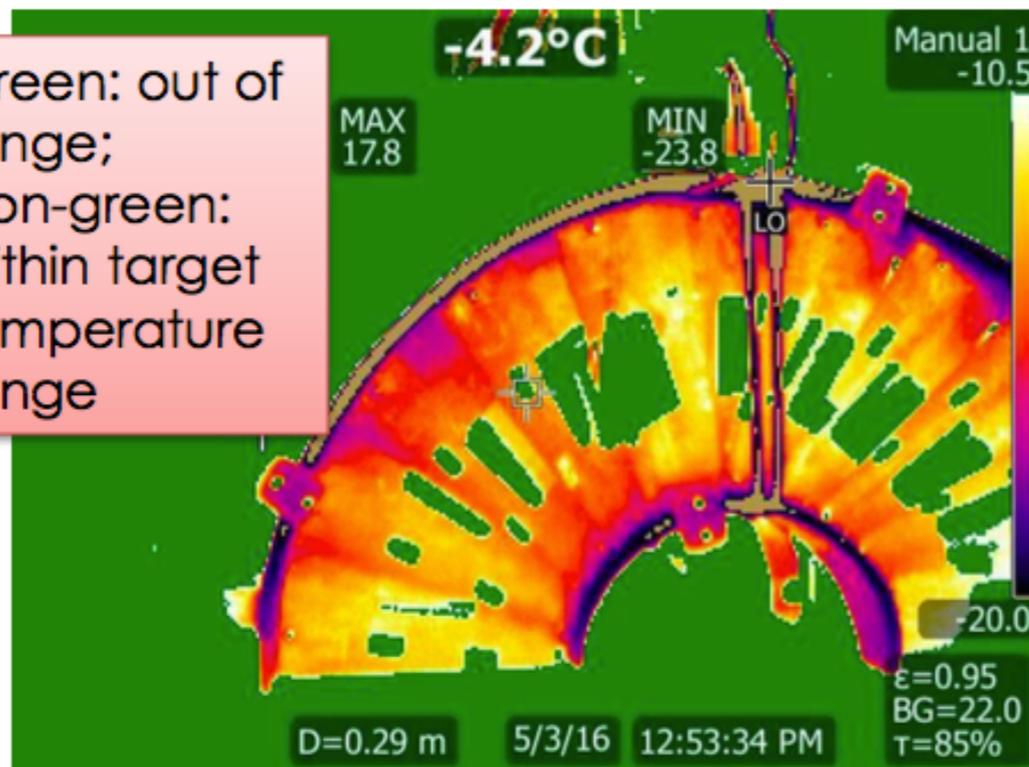


Cooling Performance



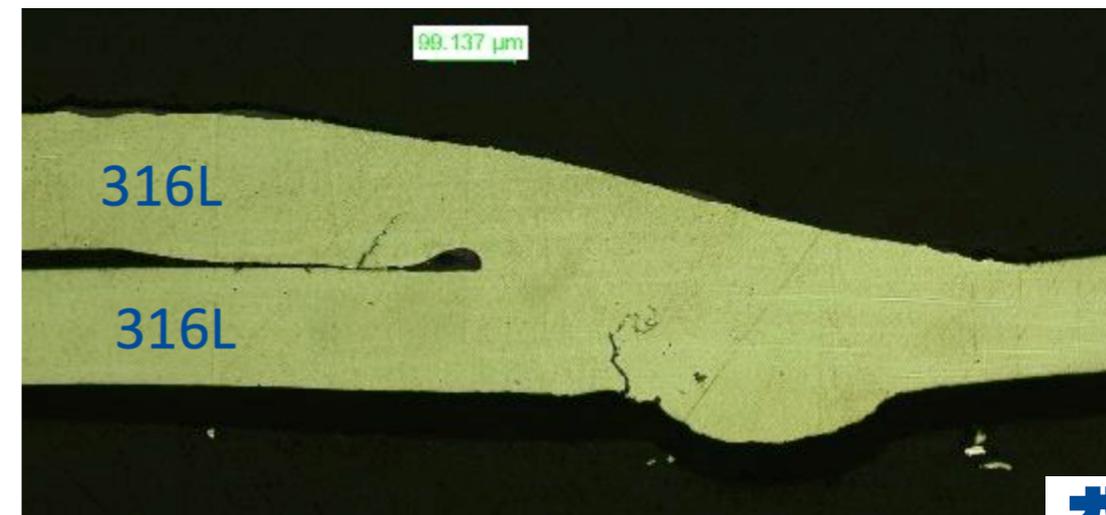
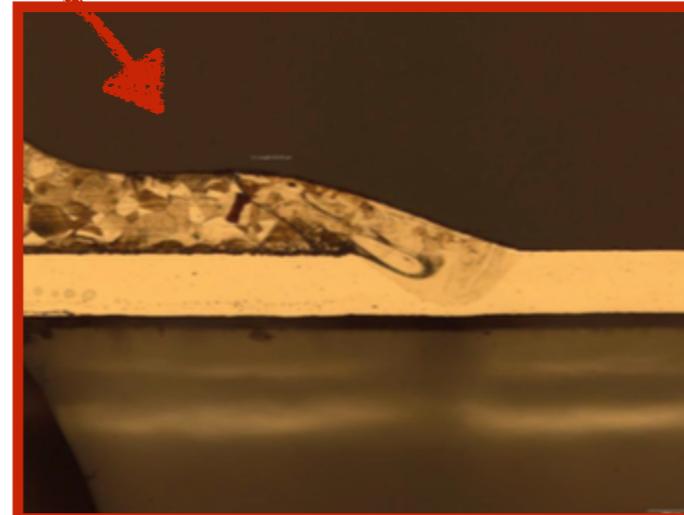
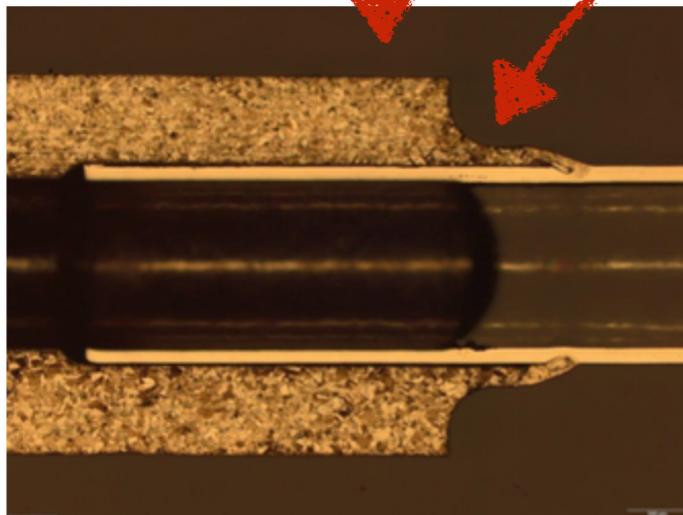
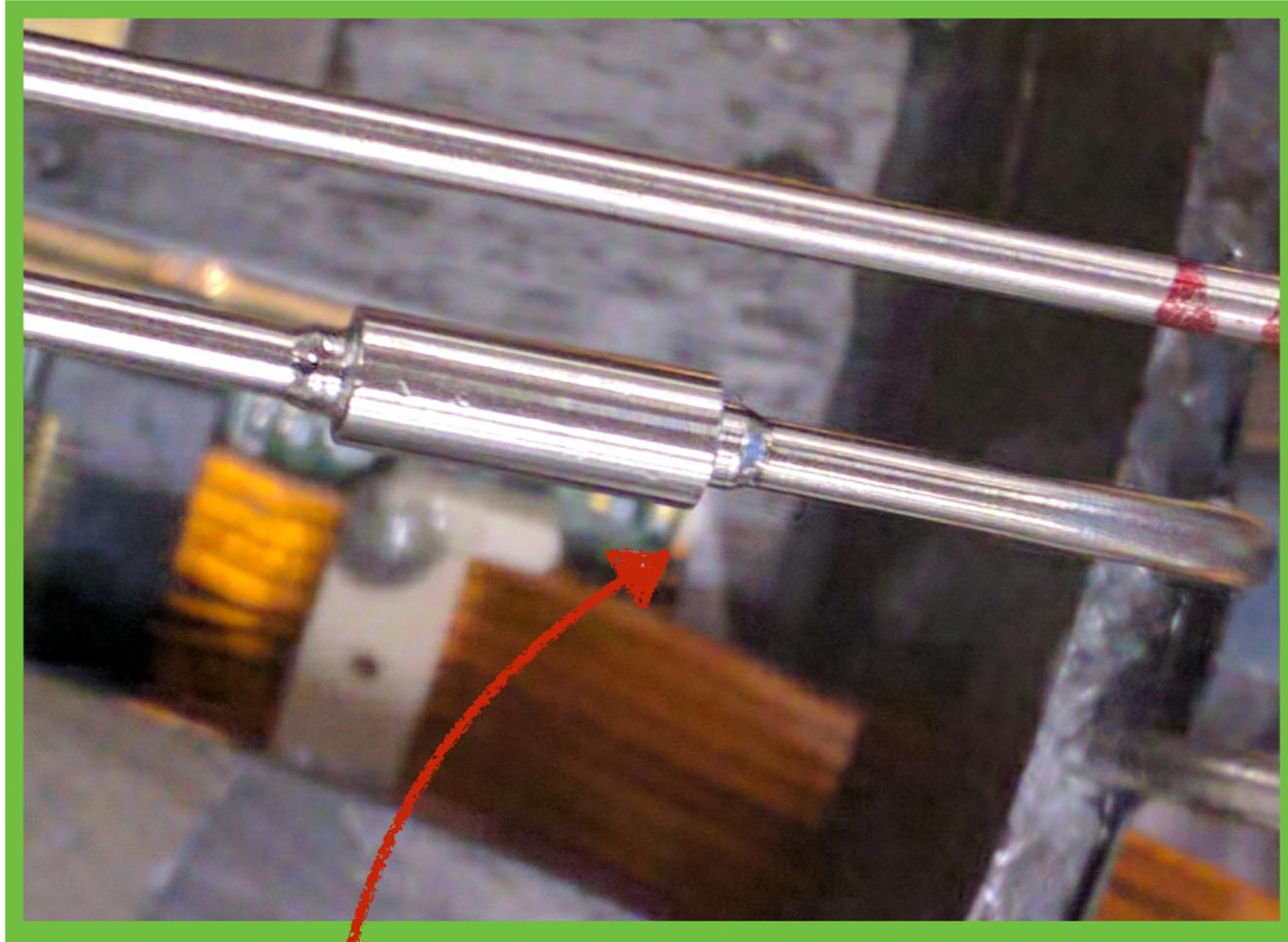
- Forward pixel blade-ring joint is critical
 - Tight control of tolerances and of assembly technique is necessary
- Half disk thermal tests are done:
 - Mimicked the full end of life heat load on each blade (3Watts/module)
 - Made thermal measurements using an infrared camera
 - Achieved $\Delta T_{\text{module-coolant}} < 10^{\circ}\text{C}$

Green: out of range;
Non-green:
within target
temperature
range



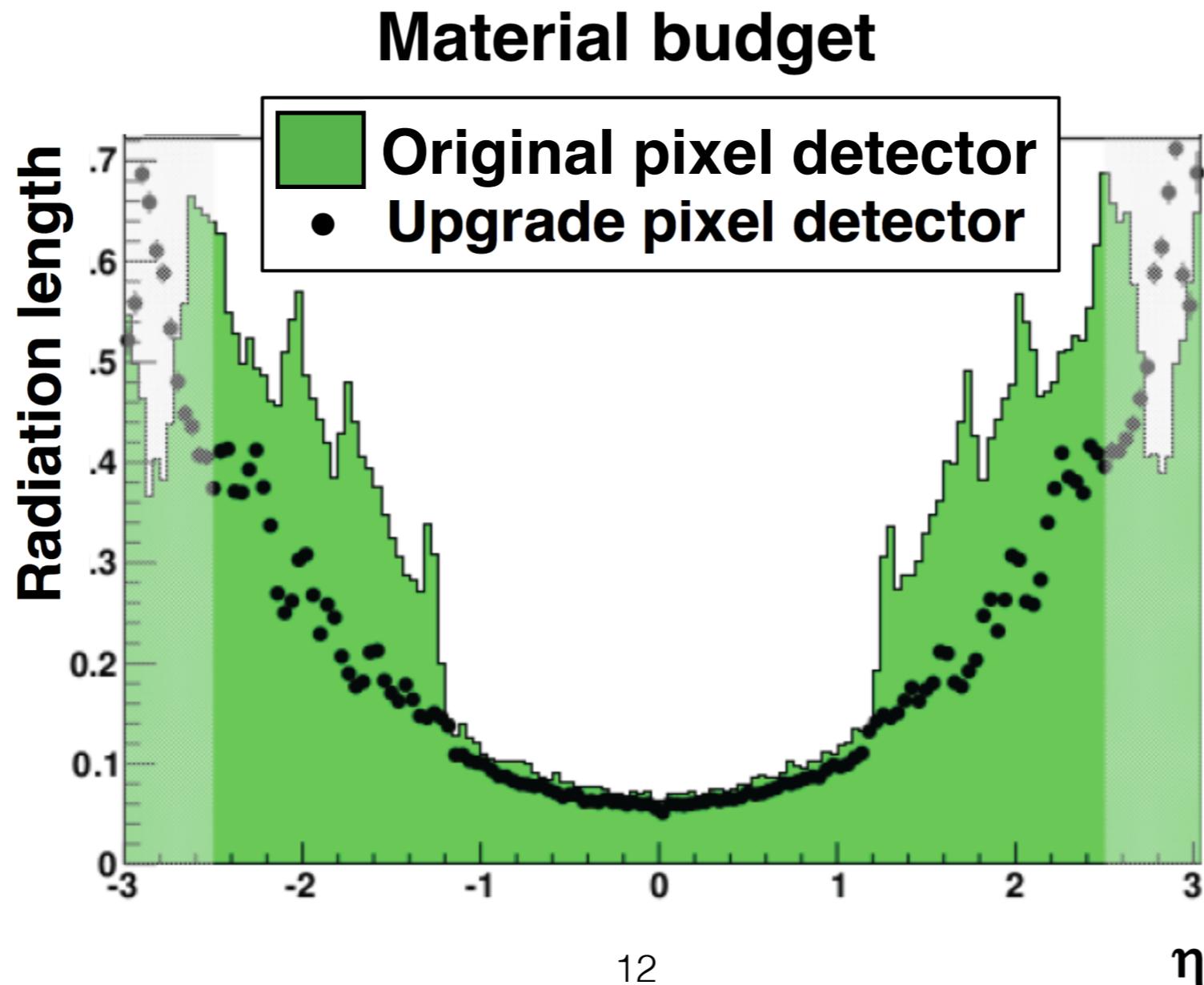
Welding Challenges

- Welds were needed on each forward pixel CO₂ cooling loop
- Problem encountered:
 - Concerns over hot cracking were raised and it was decided to micrograph welds and investigate
- Lesson learned:
 - Material composition plays a role in final microstructure and cracking susceptibility
 - The weld pool mixture of ultra high purity 304L Stainless Steel + 316L Stainless Steel lowers susceptibility to cracking (refer to Stephanie Timpone's talk at FTDM 2016 for more details)



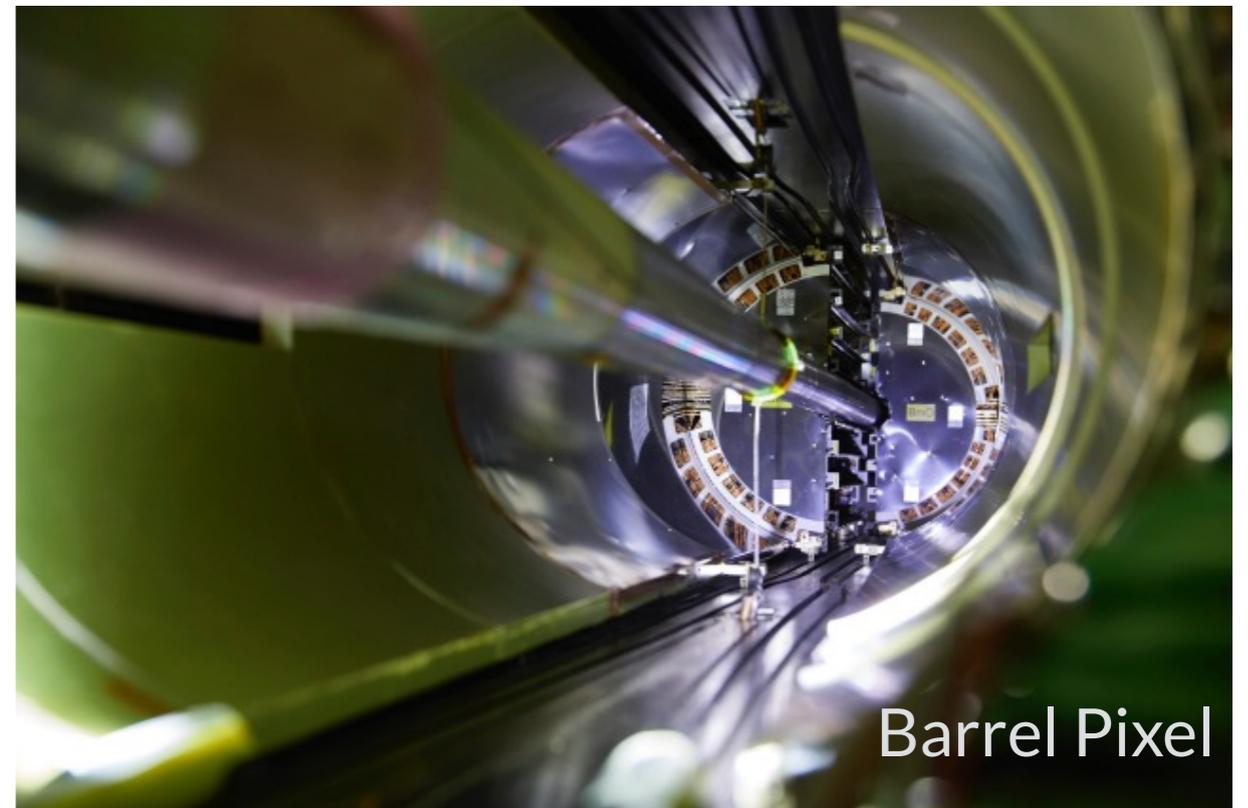
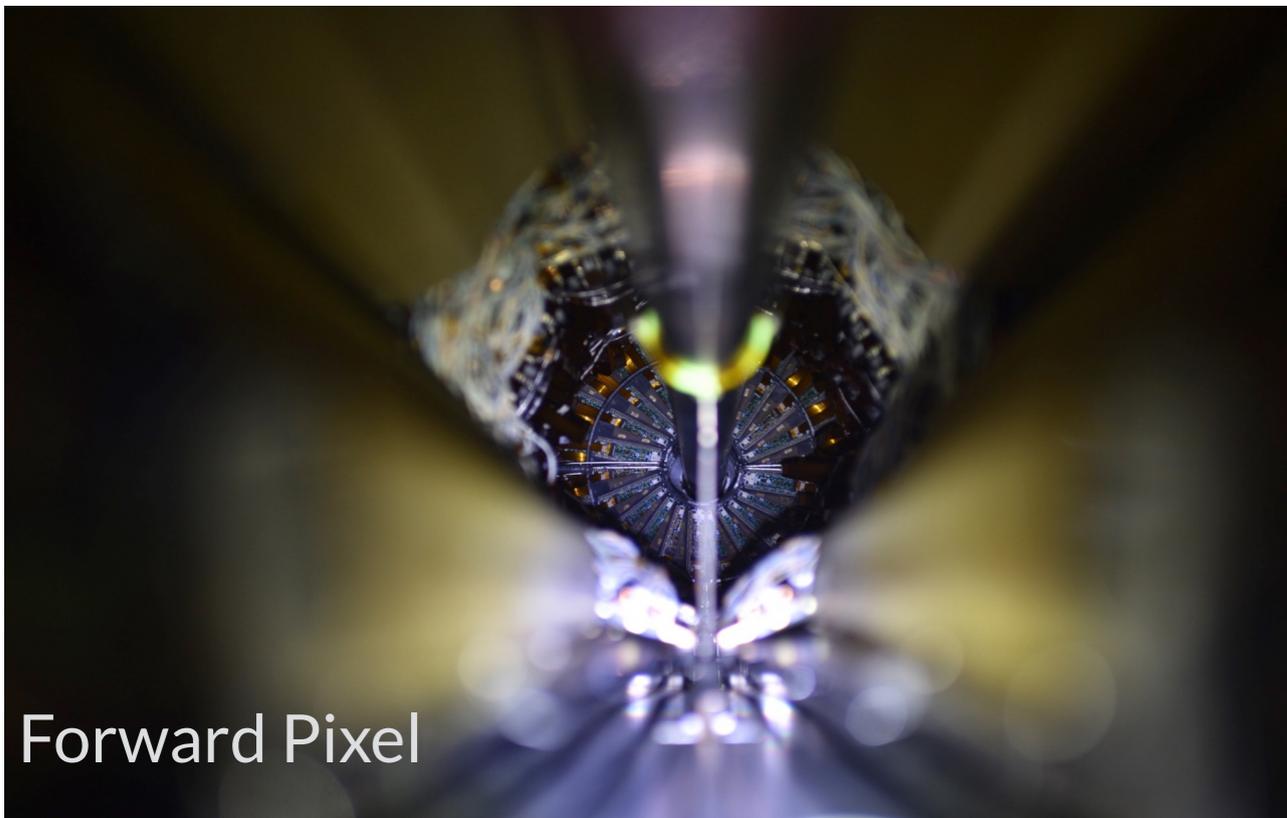
Pixel Tracker Material Budget

- Reduced material budget:
 - Choice of lighter material
 - More efficient cooling system
 - Moving service electronics further away from the interaction point
 - Adopting the powering scheme



Summary

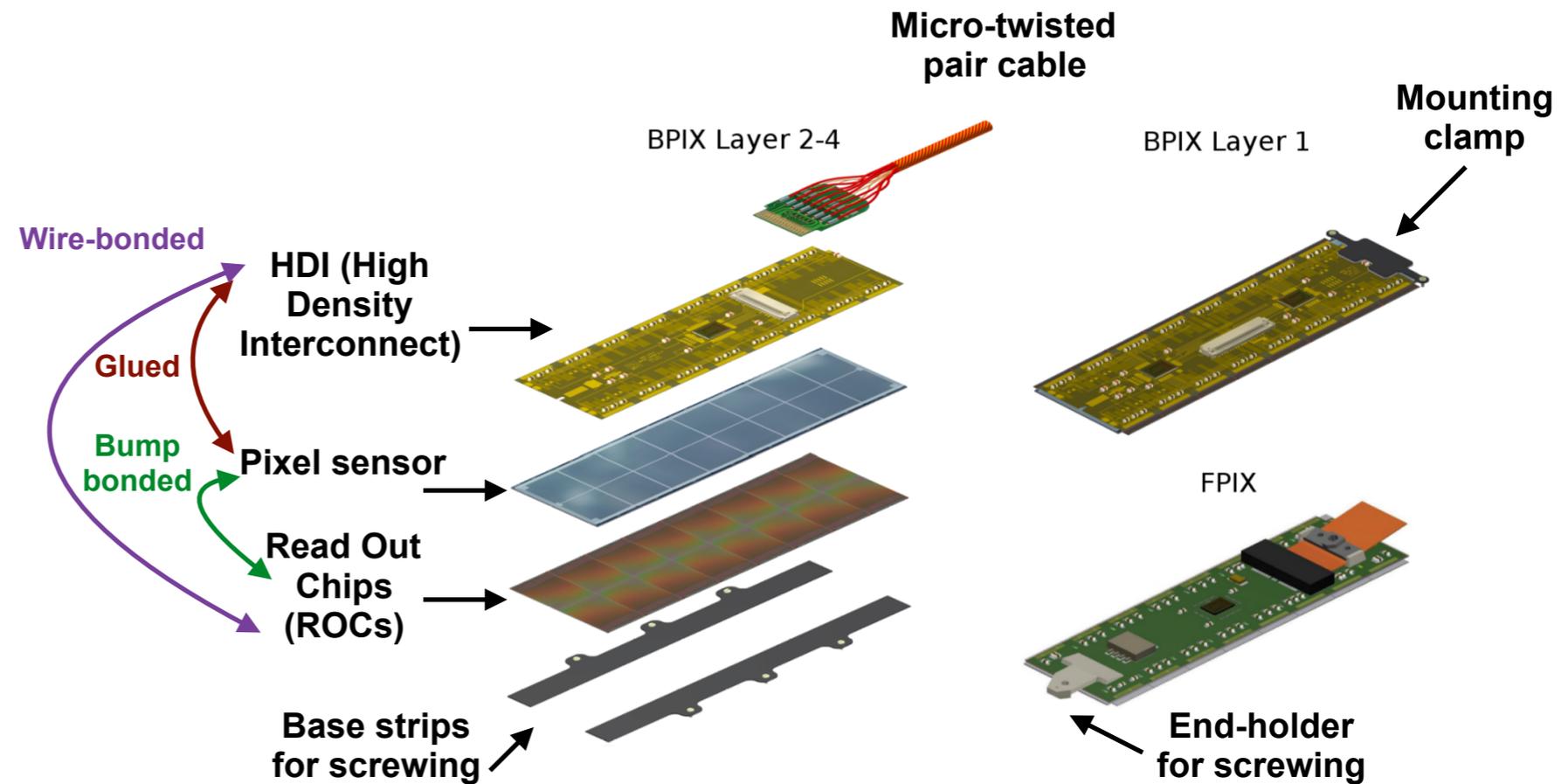
- The upgraded pixel detector is successfully installed in CMS
- The performance of the pixel detector is improved by the upgrade:
 - Higher rate capability
 - Reduced material budget
 - An additional tracking layer in forward and barrel regions
 - Increased number of channels
 - Forward pixel: 18 M \rightarrow 45 M
 - Barrel pixel: 48 M \rightarrow 79 M



Back-up



New Sensor Modules



- New readout chips are used:
 - Layer 1 requires dedicated chip to meet data transmission needs
- The readout data is merged in a single output stream by the Token Bit Manager chip (TBM)
 - Aggregates and formats the data
 - Sends it to the detector back-end with a rate of 320 Mbit/s (parallel readout)
 - 1 single data stream per module in FPIX and BPIX Layer-3/L4 (1 "TBM8" chip)
 - 2 data streams per module in BPIX L2 (1 "TBM9" chip)
 - 4 data streams per module in BPIX L1 (2 "TBM10" chips)

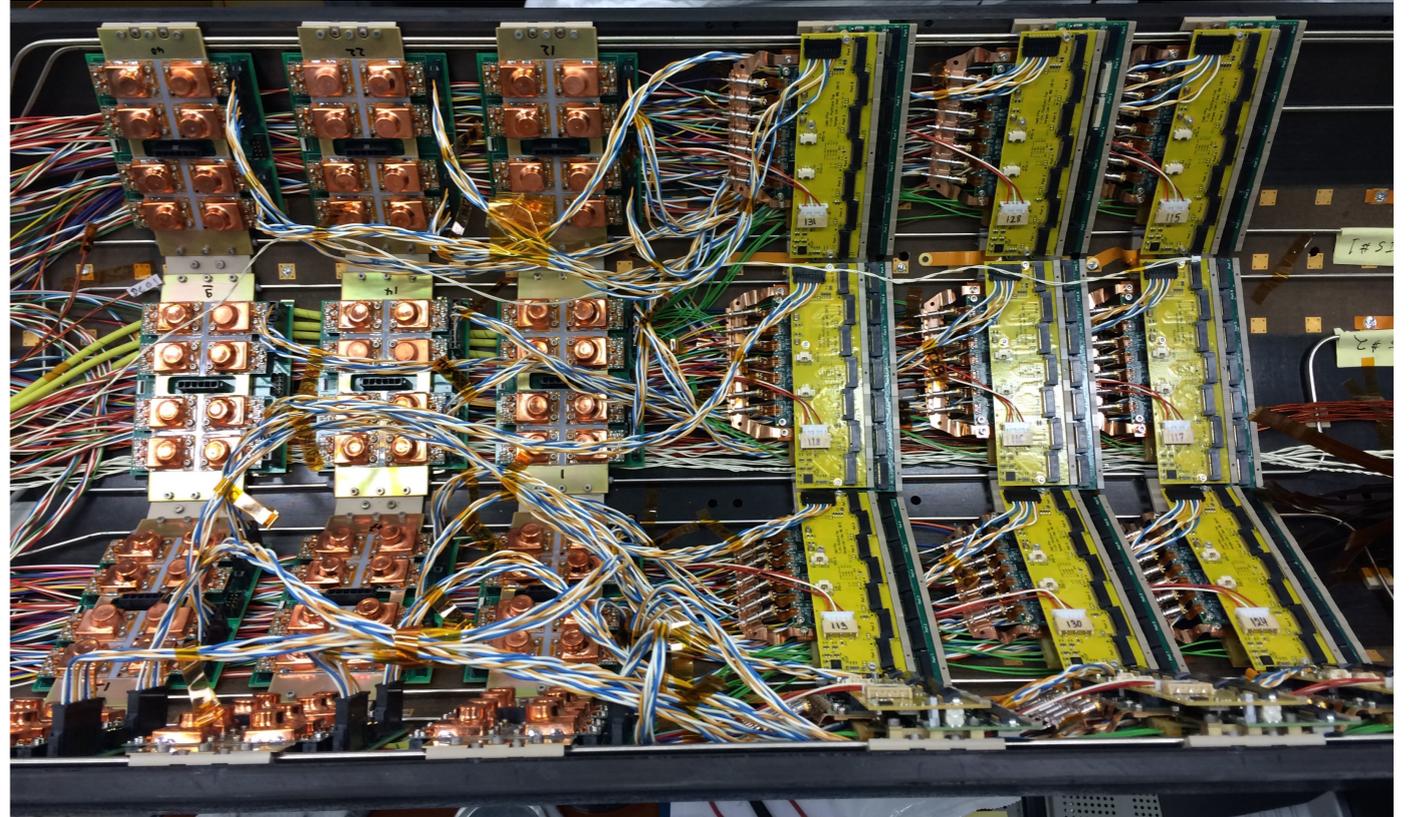


Readout Chip Design

- BPIX L2-L4 and FPIX use "psi46dig v2.1"
 - Evolution of ROC of previous detector
 - Double column drain architecture
 - 8bit ADC on chip, data transmission at 160 Mbps
 - Larger buffers to reduce inefficiency at high occupancy
 - Lower threshold: from 3500 e⁻ (current detector) to ~1800 e⁻
 - Redesigned power distribution to reduce cross talk noise
 - Faster comparators to reduce time-walk
 - Data streams from 2 ROC banks merged inside the TBM
- BPIX Layer 1 uses "PROC600"
 - Handles hit rate of 600 MHz/cm²
 - Improve data throughput by building 2x2 clusters in the double columns and transmitting cluster information
 - Further increase in buffer sizes in ROC periphery
 - Performance not degraded well beyond dose expected for Layer 1 (120 MRad)



DC-DC converters

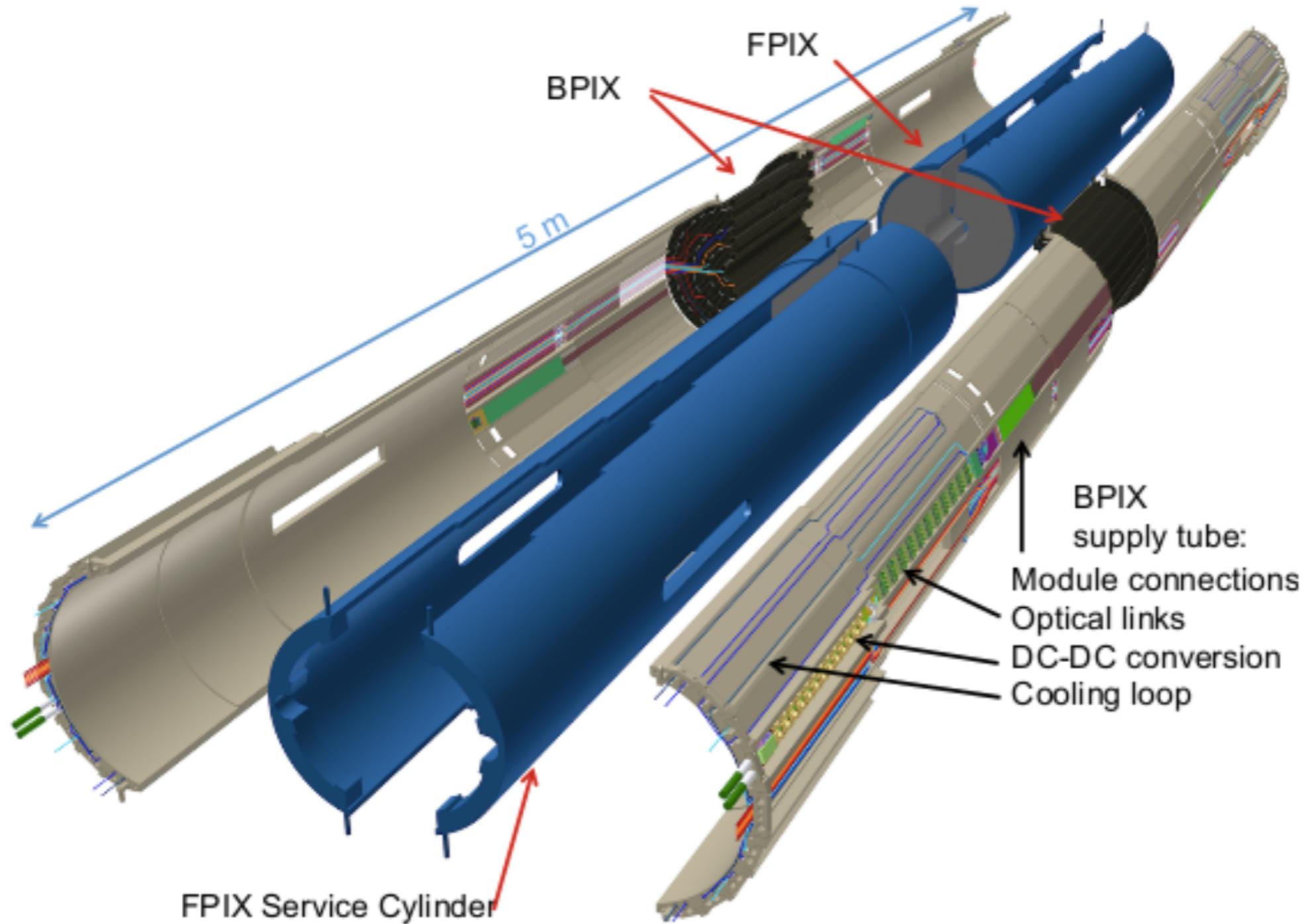


Forward pixel half cylinder DC-DC converters

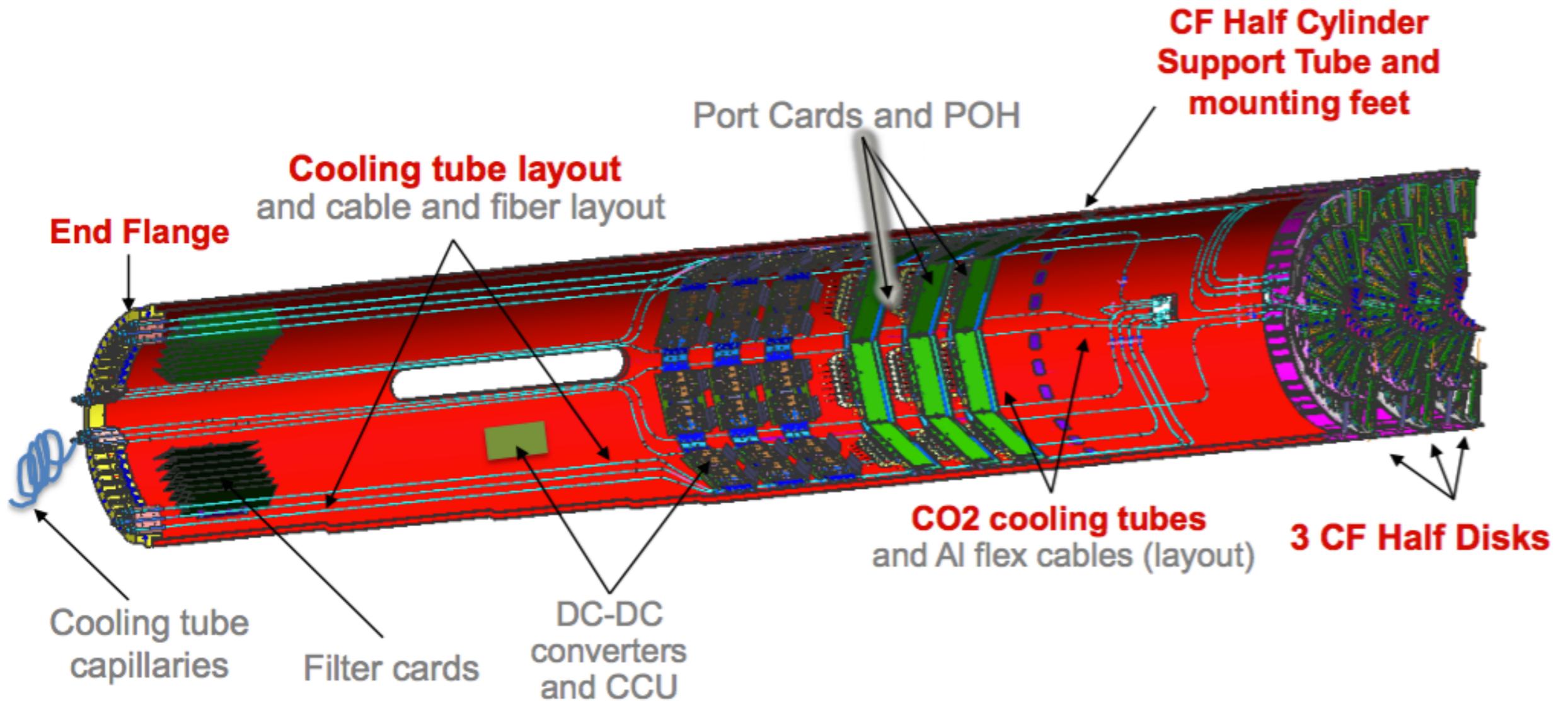
- A factor of 1.9 more channels in upgraded pixel detector
- Avoided replacing power supply cables:
 - Adopted powering scheme with DC-DC converters
 - Trading high current / low voltage in the power cables for high voltage and low current
 - Reduces the power losses in the cables.
 - Power supplies deliver 10 V to the detector
 - 10 V input is converted to to 2.4/3.3V (analog/digital)



Barrel Pixel Service Tube



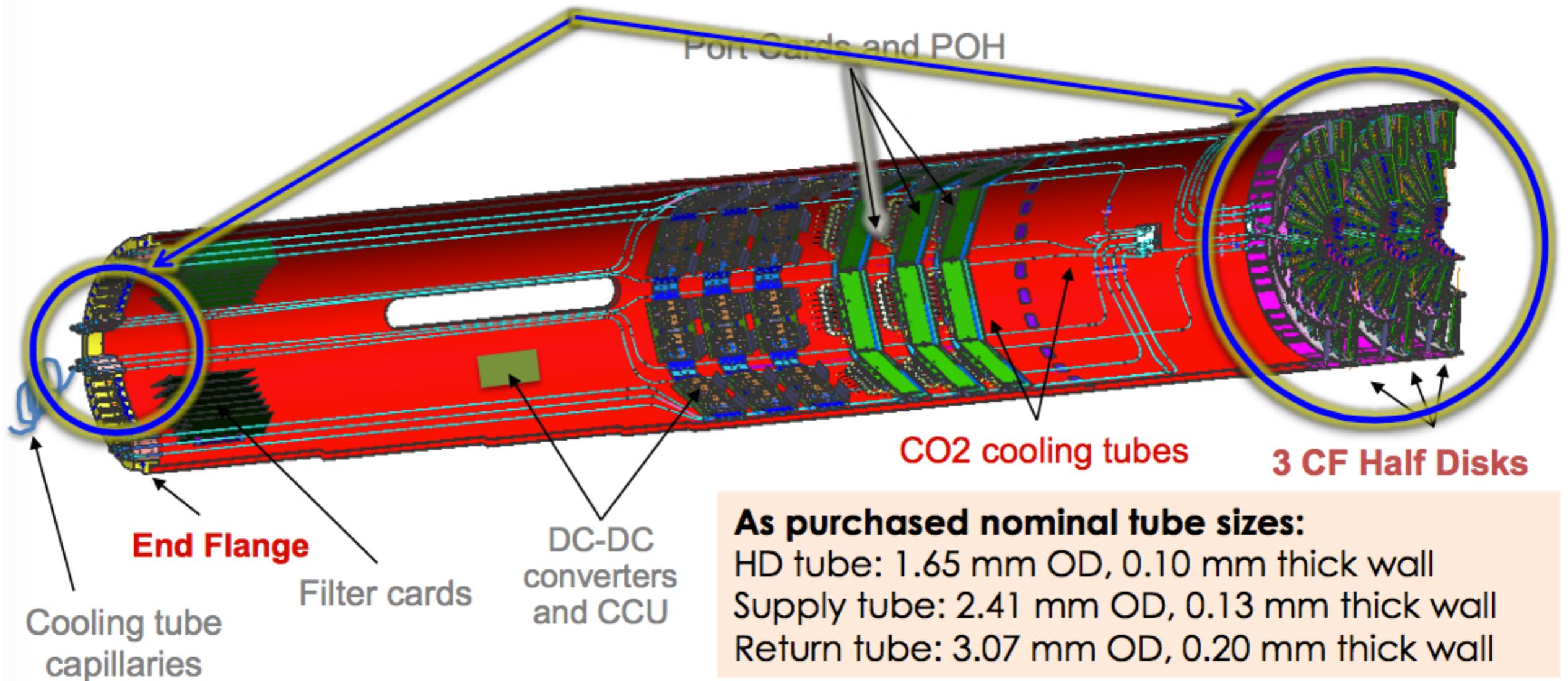
Forward Pixel Half Cylinder



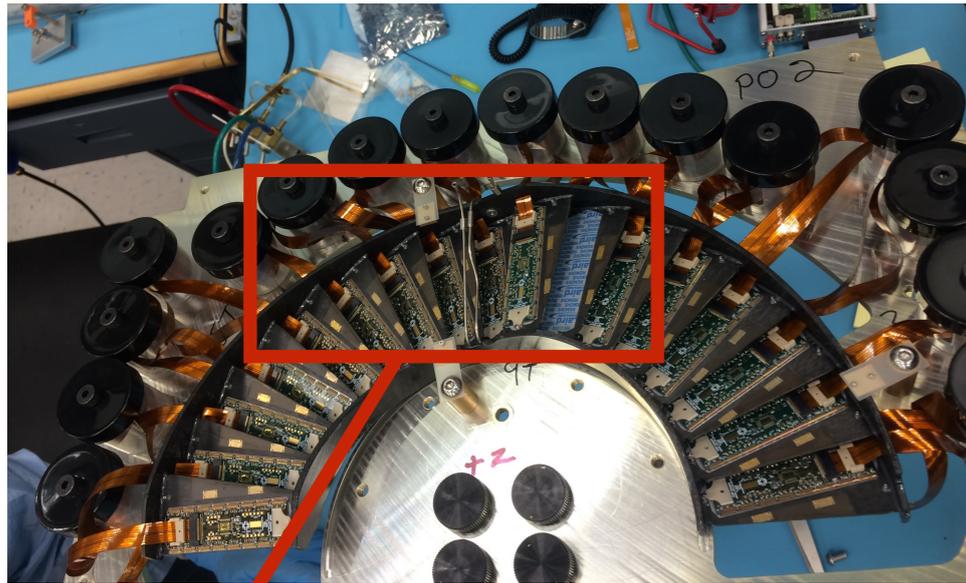
Forward Pixel Cooling Tubes

6 stainless steel CO₂ cooling loops/HC (supply-HD-return)

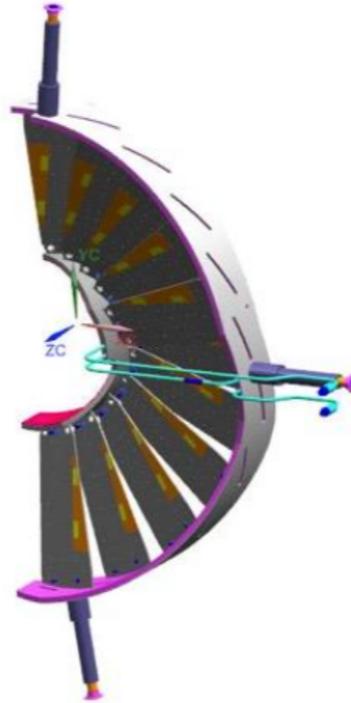
- 8 Welds per loop (2 on supply tube, 4 on HD tube, 2 on return tube)
- 48welds/HC,192 welds in FPIX



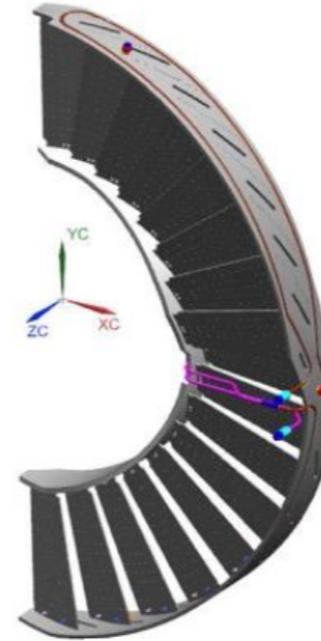
Location of Forward Pixel Welds



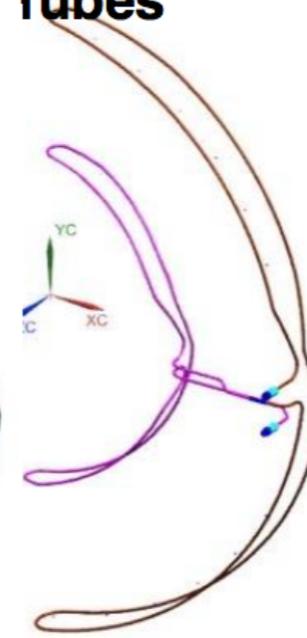
Inner Assembly



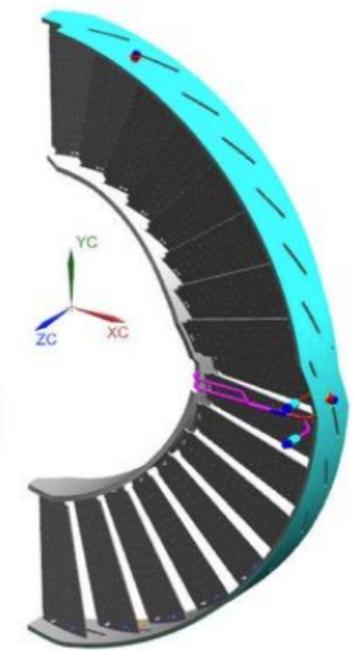
Outer Assembly



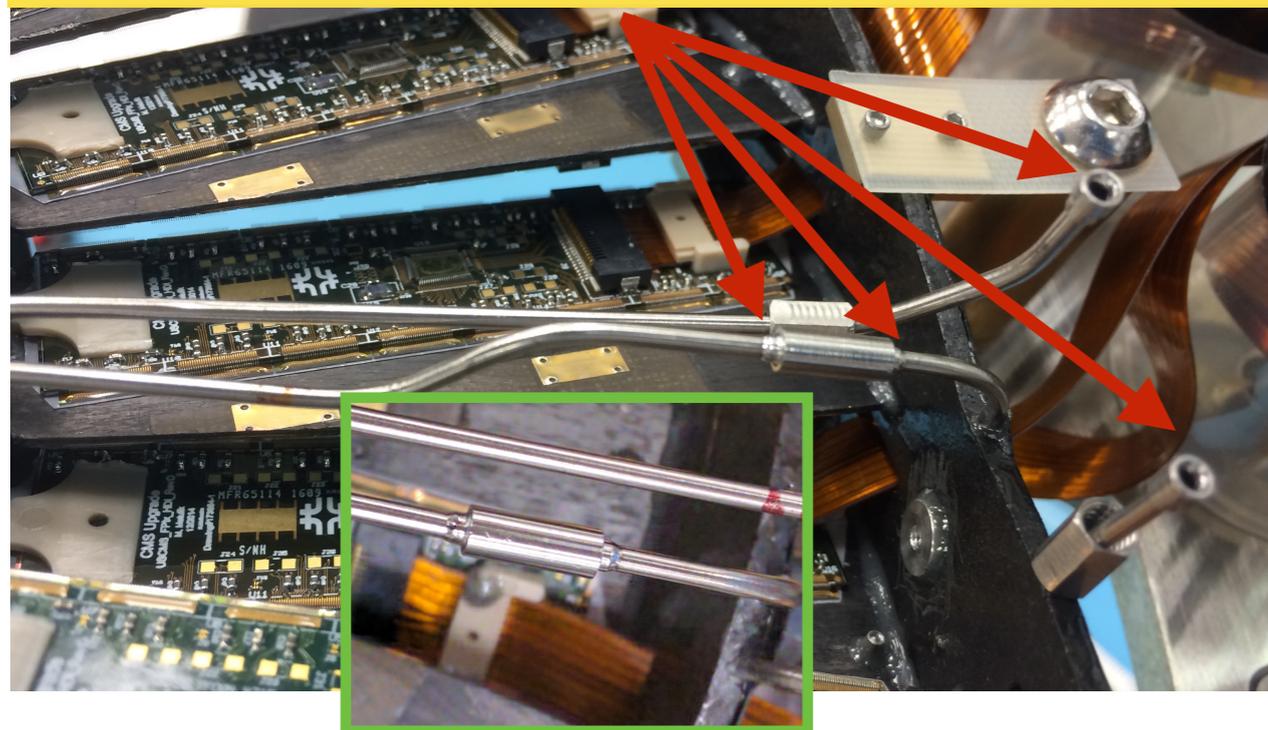
SS Cooling Tubes



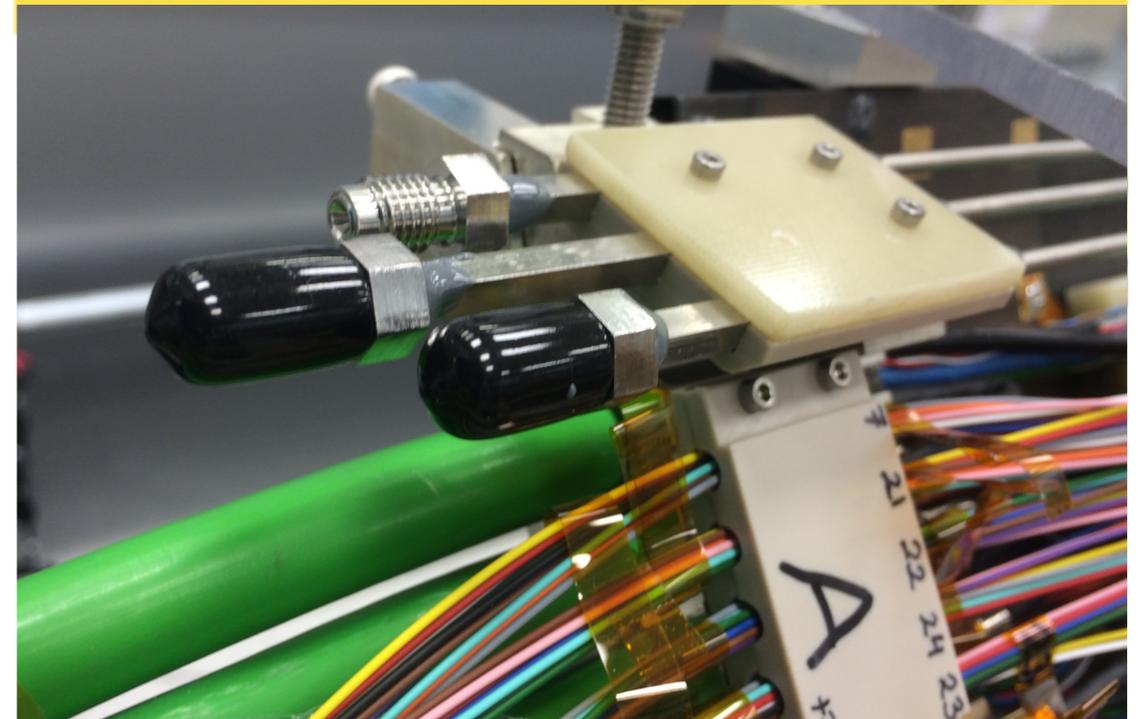
With tubing and CF facing



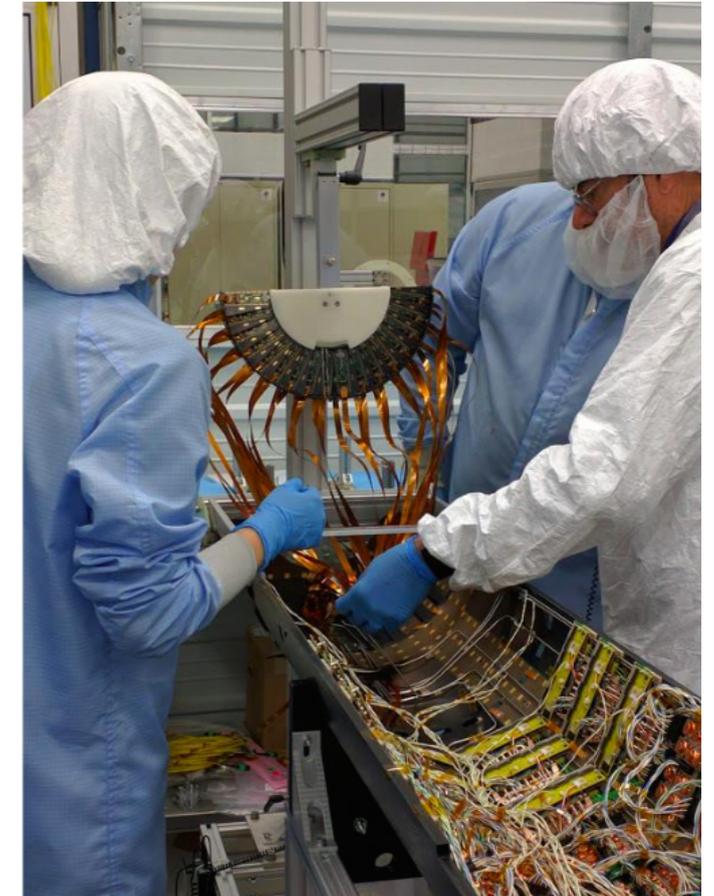
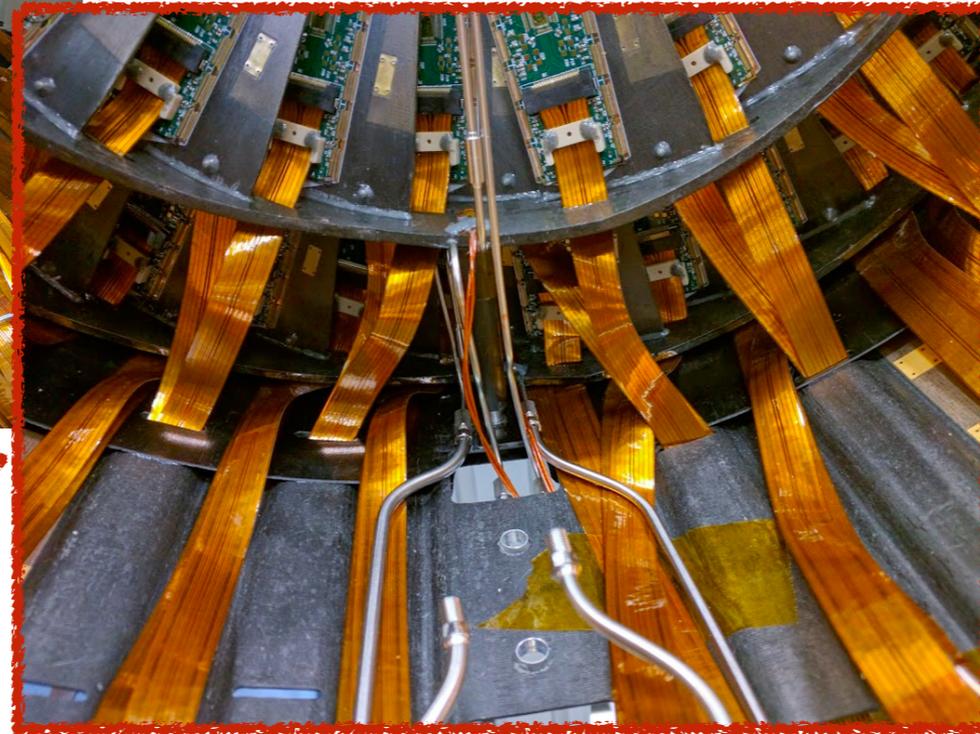
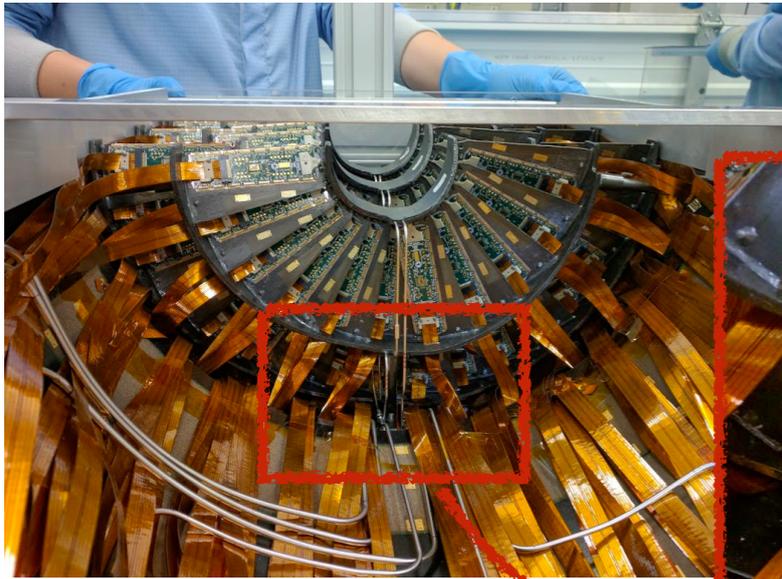
4 welds (for each inner and outer HD)



Weld on VCR fitting at end-flange



Aluminum Flex Cables



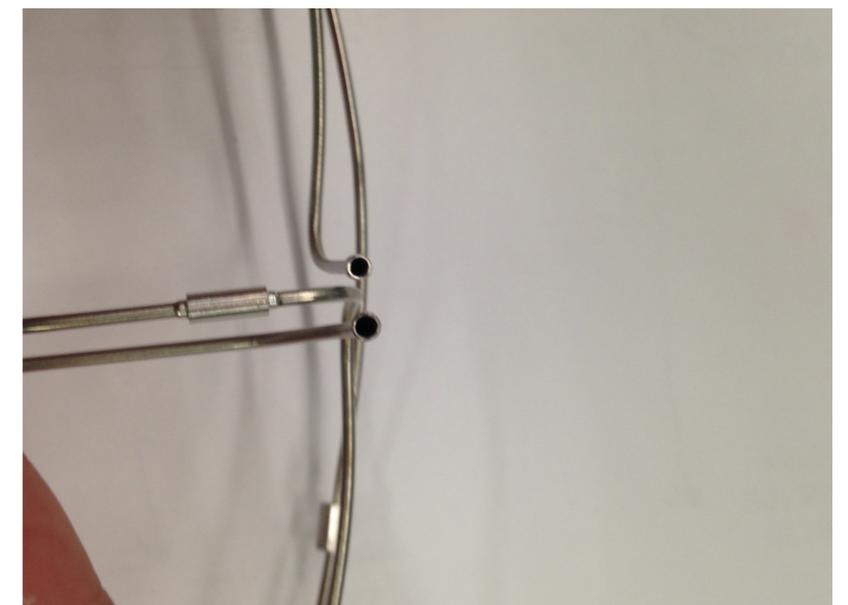
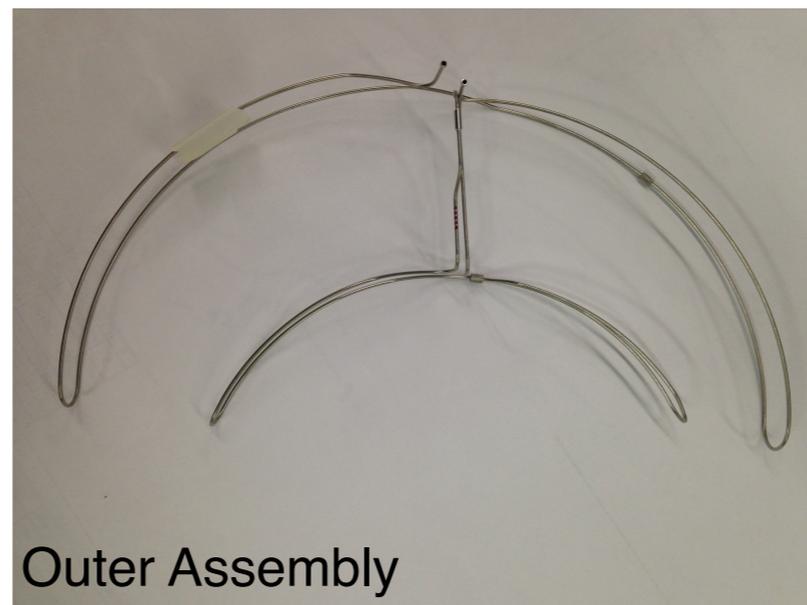
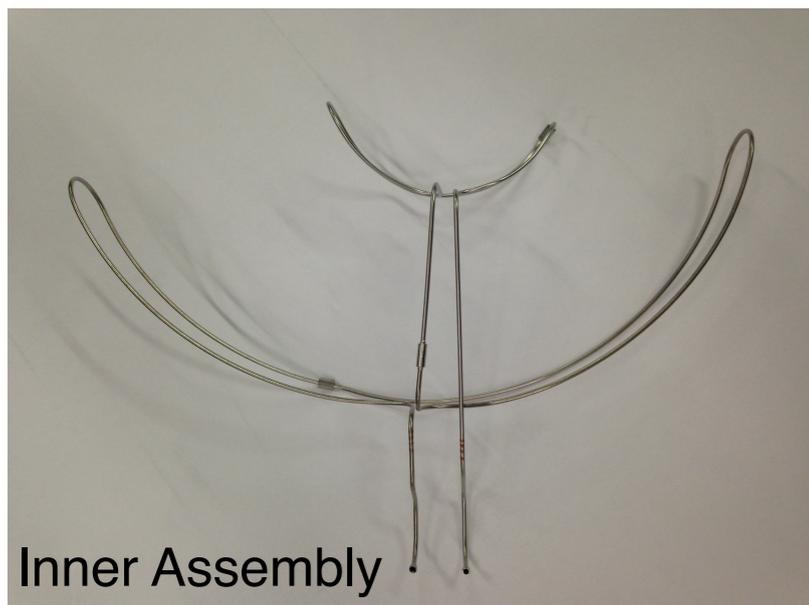
- FPIX Cylinders with disks were assembled and tested at Fermilab, then disassembled and shipped separately to CERN for reassembly and retest
 - Motivation for separate shipping of disks was to reduce risk – minimization of forces on disks (same procedure as for original FPIX)
- Problem encountered:
 - Trace breakage at port card end of module flex cables, induced by handling
- Lessons learned:
 - Aluminum flex cables are more delicate than expected
 - A specifically designed cable end cover would've been more protective compared to an ad-hoc tape-based protection
 - Minimizing the assembling, disassembling and re-assembling process during shipment



Forward Pixel Cooling Loop QA/QC

Each cooling loop as final qualification before committing the loop to the detector (both HC and HD):

- Upon completion, parts are cleaned and visual inspected.
- After an initial pressure test, each loop undergoes 10 cycles from liquid Nitrogen to room temperature.
- Upon completion, each loop is brought gradually up to 2280 PSI (157 bars) in 5 steps and leak checked in a water bath. Once reached 2280 PSI (157 bars), the loop is held at this pressure for one hour.
- This is followed by 24hr leak test at 1600 PSI (110 bars) with the loop still in the water bath. Leak tightness is checked both visually and by pressure decay measurement with a gauge.
- Helium leak checking is faster and more precise than leak-down test or looking for bubbles, but can not replace high pressure test



Welding Batch Validation

Forward Pixel Detector

One complete sample loop for each welding batch is extensively tested in order to validate the welding process for each weld fabrication batch (both HC and HD loops).

- A total of 200 cool-down/warm-up cycles from liquid Nitrogen temperature to room temperature.
- Pressure test at 2280 PSI (157 bars) for 1 hour and leak test at 1600 PSI (110 bars) for 24 hours.
- All welds of the sample loop will then be potted, ground and polished, and inspected for defects under a microscope both before and after etching.

