A Novel Readout System for High Efficiency Cosmic Ray Veto for the Mu2e Experiment

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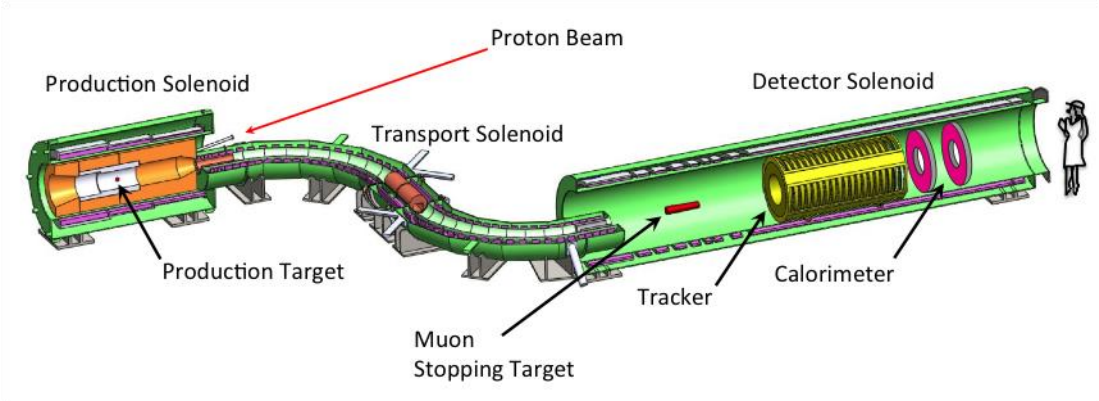
Overview of Mu2e



- Observe coherent, neutrinoless $\mu^- \rightarrow e^-$ conversion
- Single event sensitivity $R_{\mu e} = 3\times10^{-17}$
- Run time 3 years

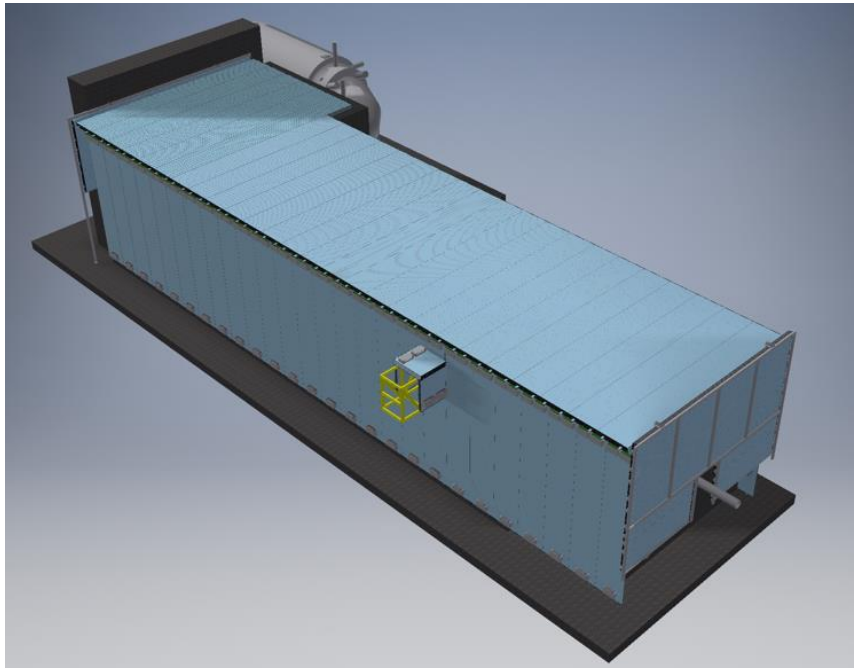
$$R_{\mu e} = \frac{\mu^- + A(Z,N) \rightarrow e^- + A(Z,N)}{\mu^- + A(Z,N) \rightarrow \nu_\mu + A(Z-1,N)}.$$

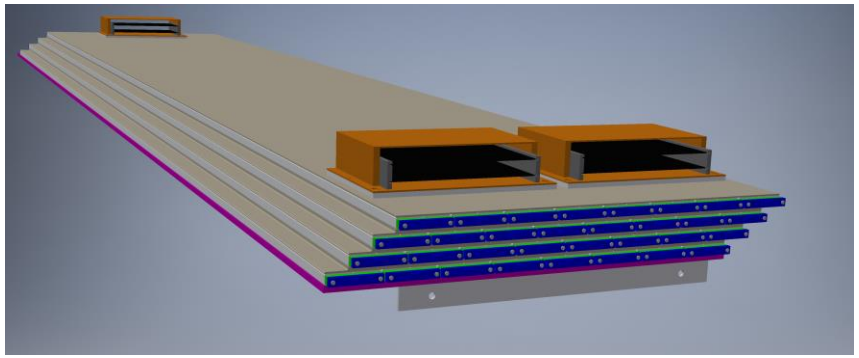
Cosmic Ray Veto

- Anticipate ~1 signal-like CR event per day.
- Goal: 0.1 signal-like events over 3 year run time.
- Need 99.99% efficient CR detection.

Design:

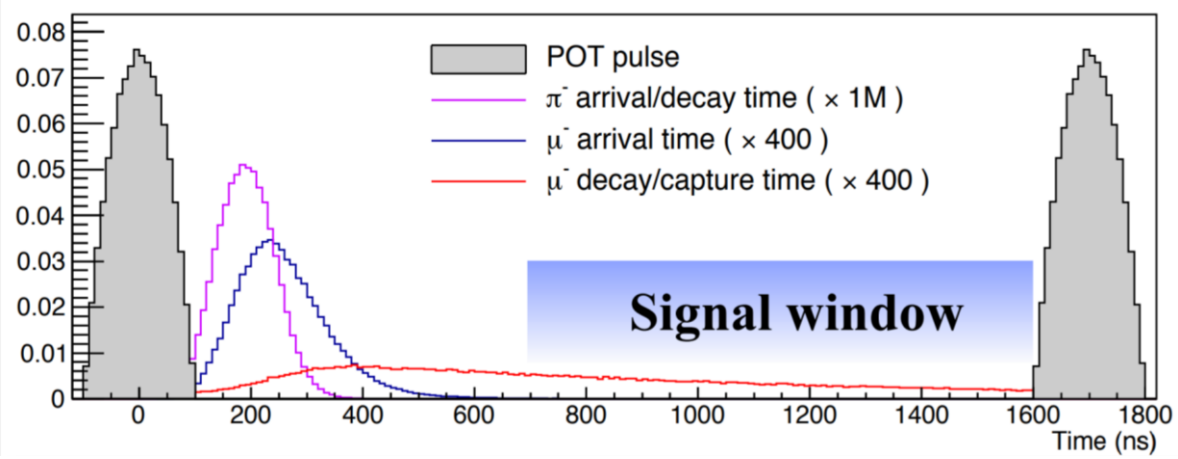
- Active shielding surrounding (nearly) entire experiment
- 4-layer scintillator, two wavelength shifting fibers running length of extrusion
- SiPMs at both ends of each scintillator extrusion
- Aluminum absorber between layers
- Area: 327m^2





Beam Structure

- 4×10^7 protons per microbunch
- 1695ns between microbunches
- 900ns live gate beginning 700ns after flash
- 3×10^4 microbunches per 53ms spill
- 8 spills in 0.4s with 1s interspill, 1.4s supercycle



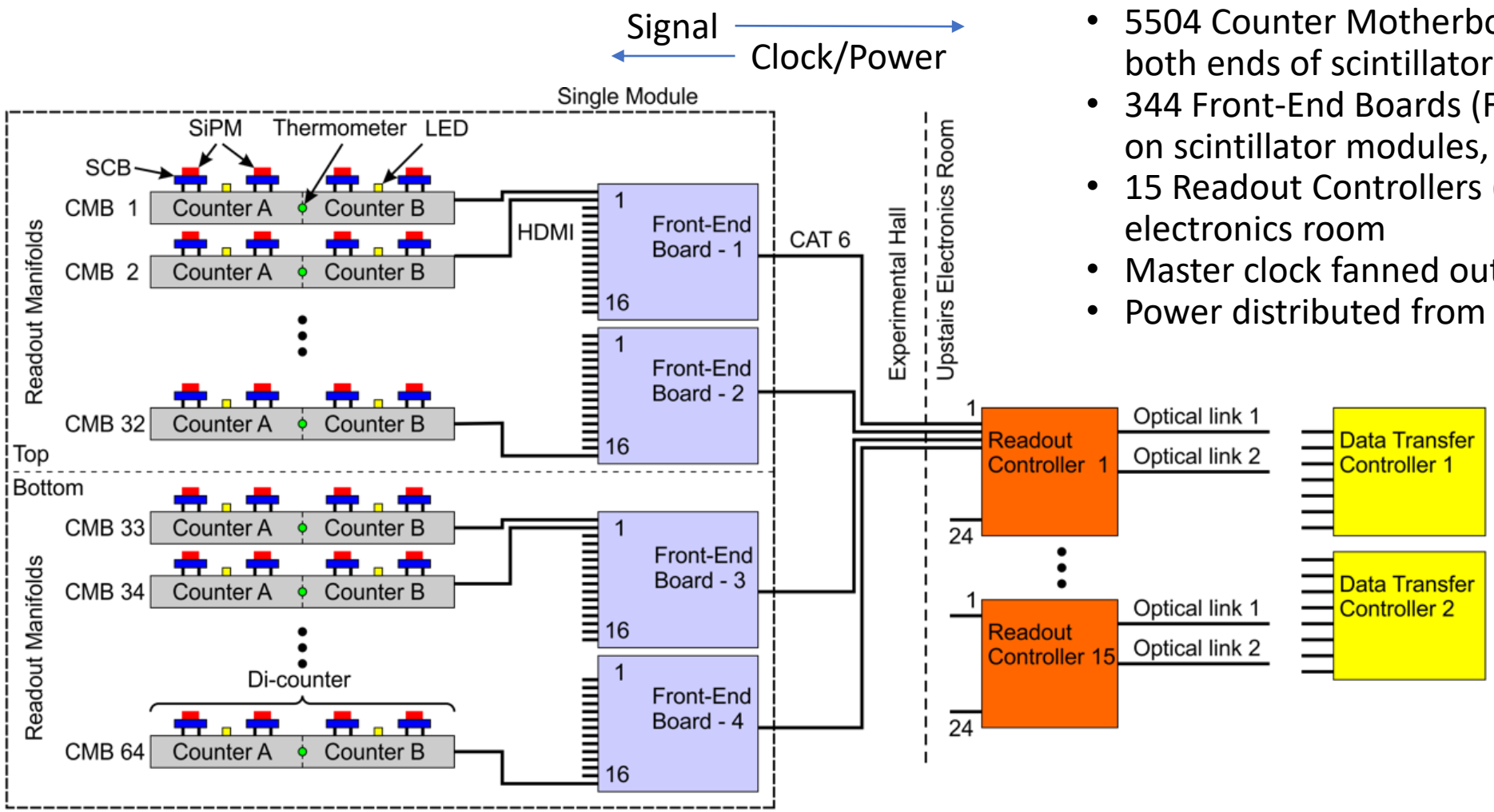
Electronics Requirements

- Operate in 400 Gauss ambient field
- Tolerate $5\times10^9/cm^2$ neutron dose over lifetime
- Data buffering 1.4s
- On-demand readout of 1% of buffered data, triggered by other detectors
- Reduce SiPM bias during beam flash
- Instrument/readout physically large array

Design Philosophy:

- Hierarchical design
- Standardized commercial components
- Minimal cables

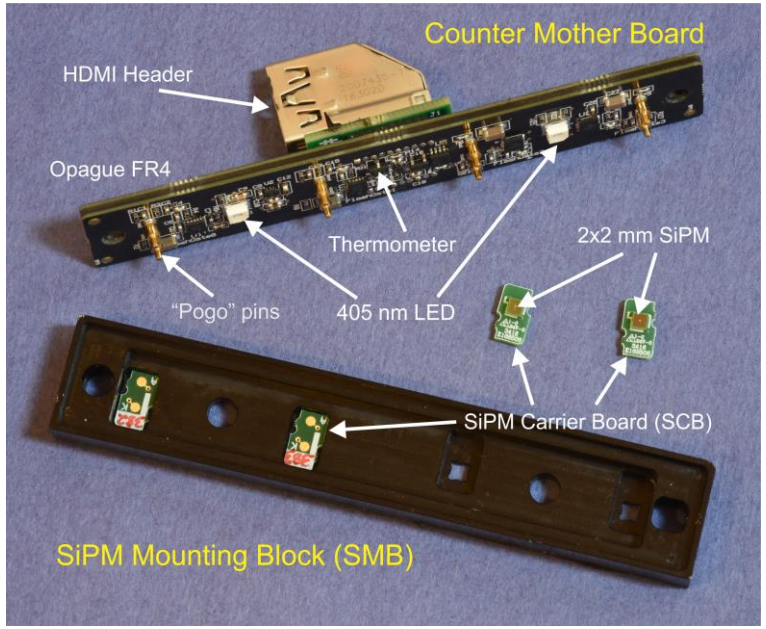
Electronics Overview

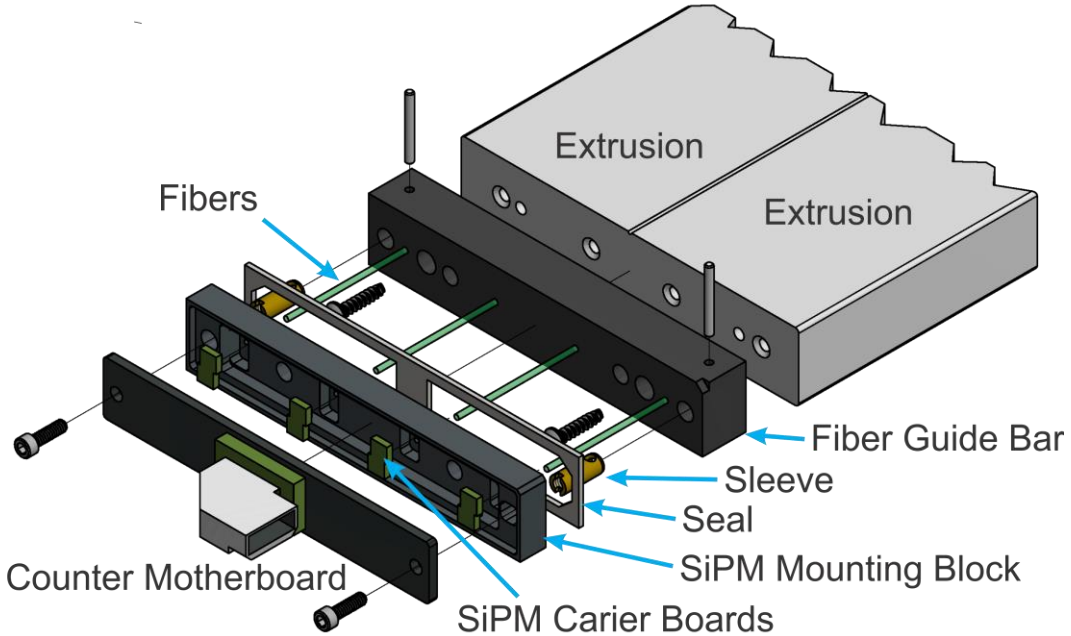


- 5504 Counter Motherboads (CMB), on both ends of scintillator extrusions
- 344 Front-End Boards (FEB), mounted on scintillator modules, 1m cable
- 15 Readout Controllers (ROC), in electronics room
- Master clock fanned out from TDAQ
- Power distributed from the ROC

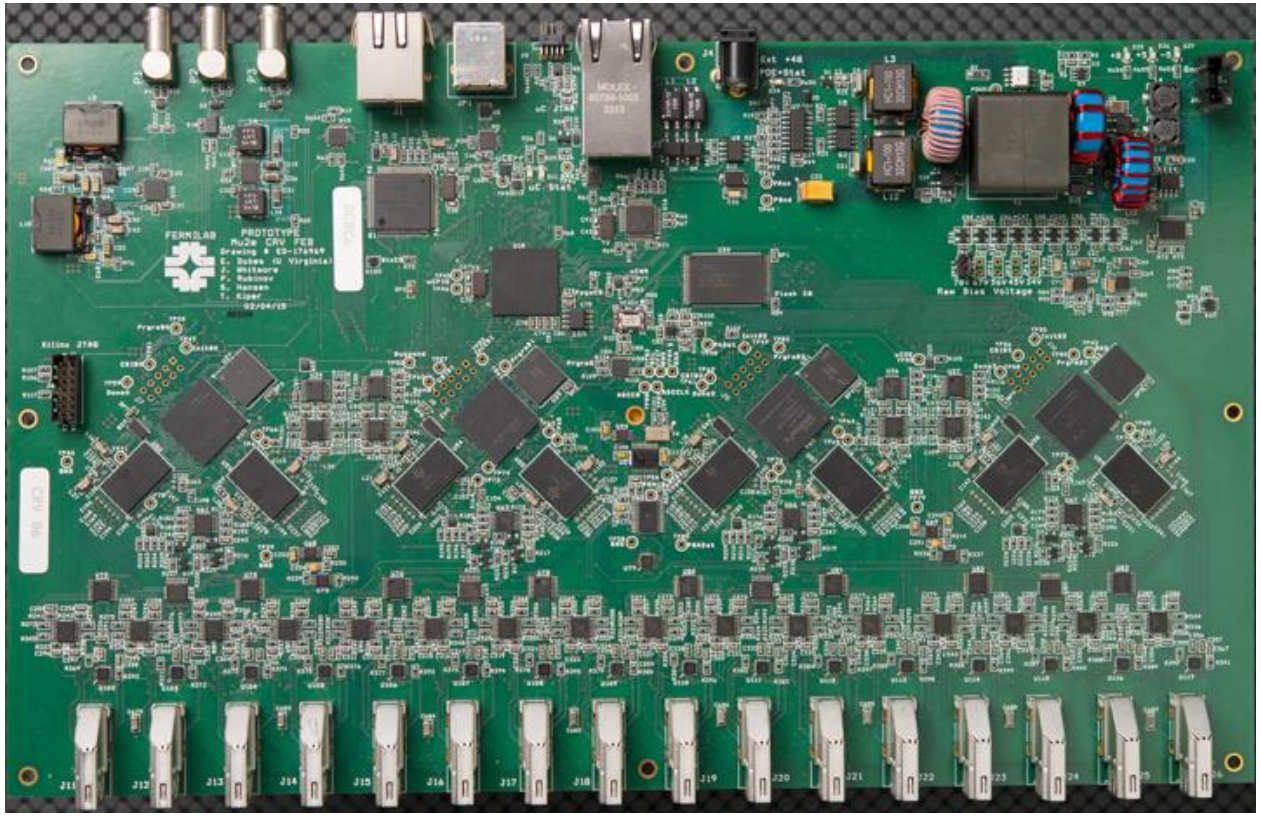
Counter Motherboards (CMB)

- Opaque FR4 PCB
- Four 2mm×2mm Hamamatsu SiPMs
- Pogo pins for SiPM mounting
- Two LED flashers
- Temperature sensor onboard
- Switch for each SiPM for reducing bias
- HDMI connection to FEB
- AC coupled signal and DC coupled bias on same line





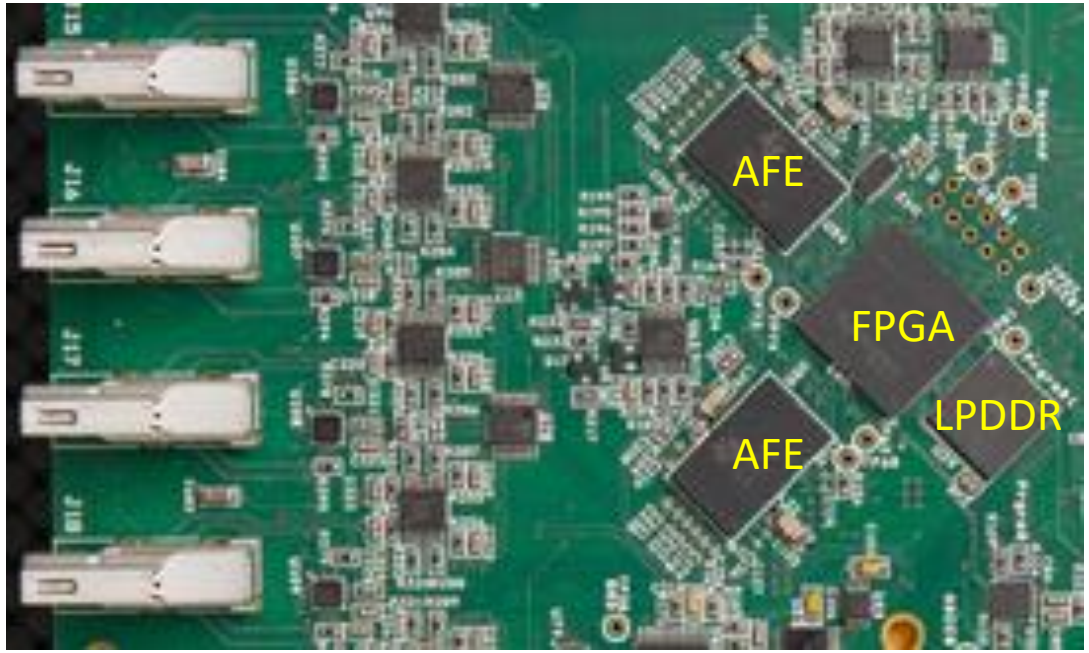
Front-End Boards (FEB)

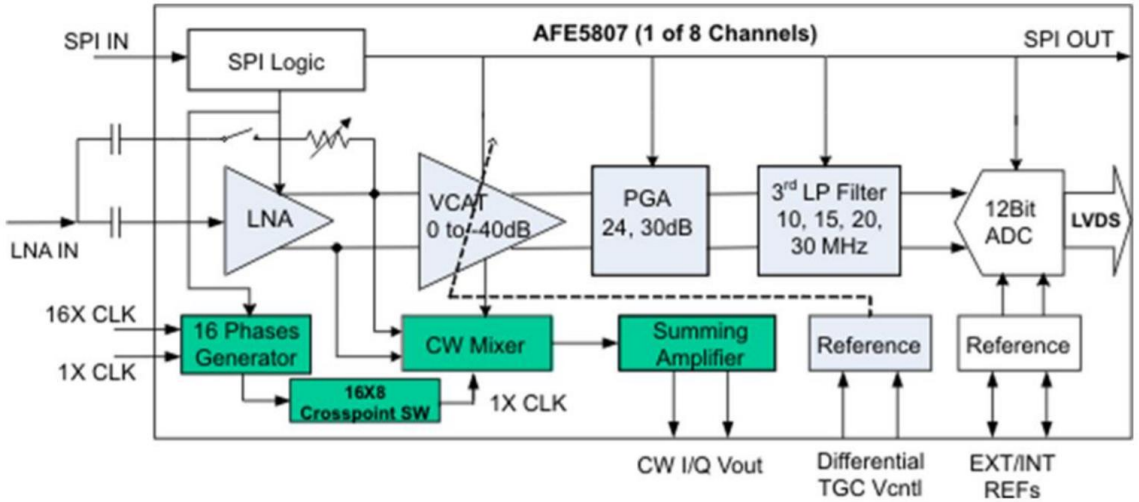


- 64 channels, 16 CMB
- Four FPGAs
- Power and signal over single ethernet cable
- Transformer isolated power, POE
- Onboard Cockcroft-Walton for up to 78V SiPM bias.

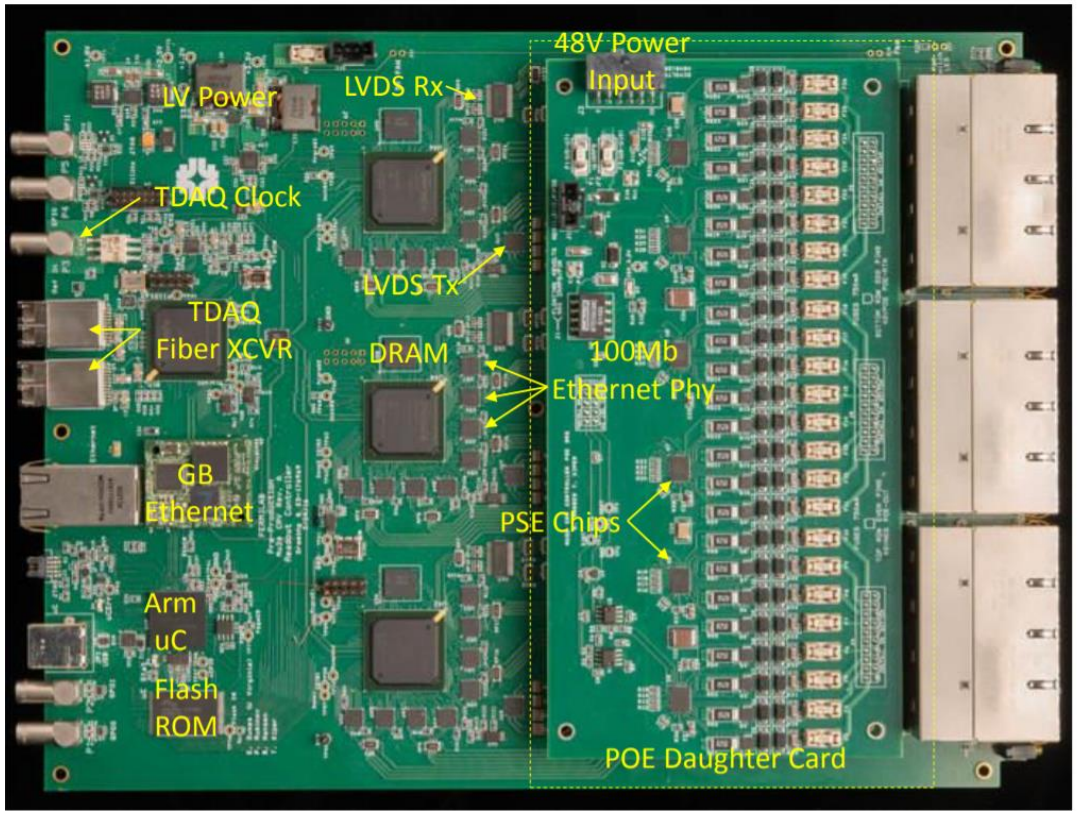
Front-End Boards (FEB)

- Four instances of 16 channel units per FEB
- Xilinx FPGA with 16 960Mbaud serial inputs
- 2mV bias resolution, 0-78V range.
- TI AFE5807 commercial ultrasound chip
  - 8 channel, one per two CMB
  - Low noise preamp and variable gain amp
  - 80 MHz, 12 bit ADC
  - $54 each
- 2Gb LPDDR RAM for buffer

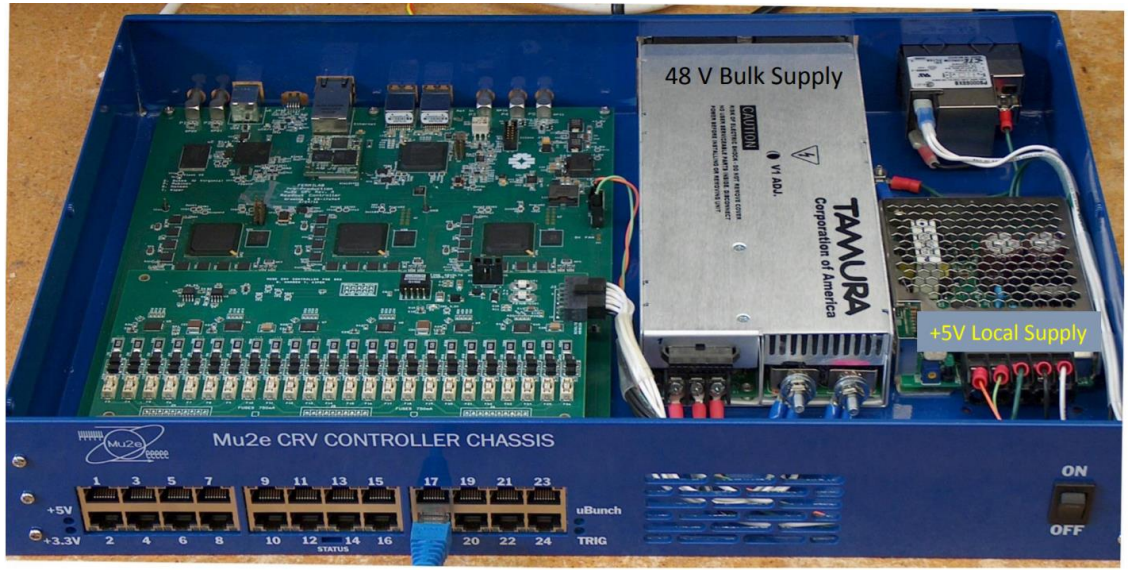




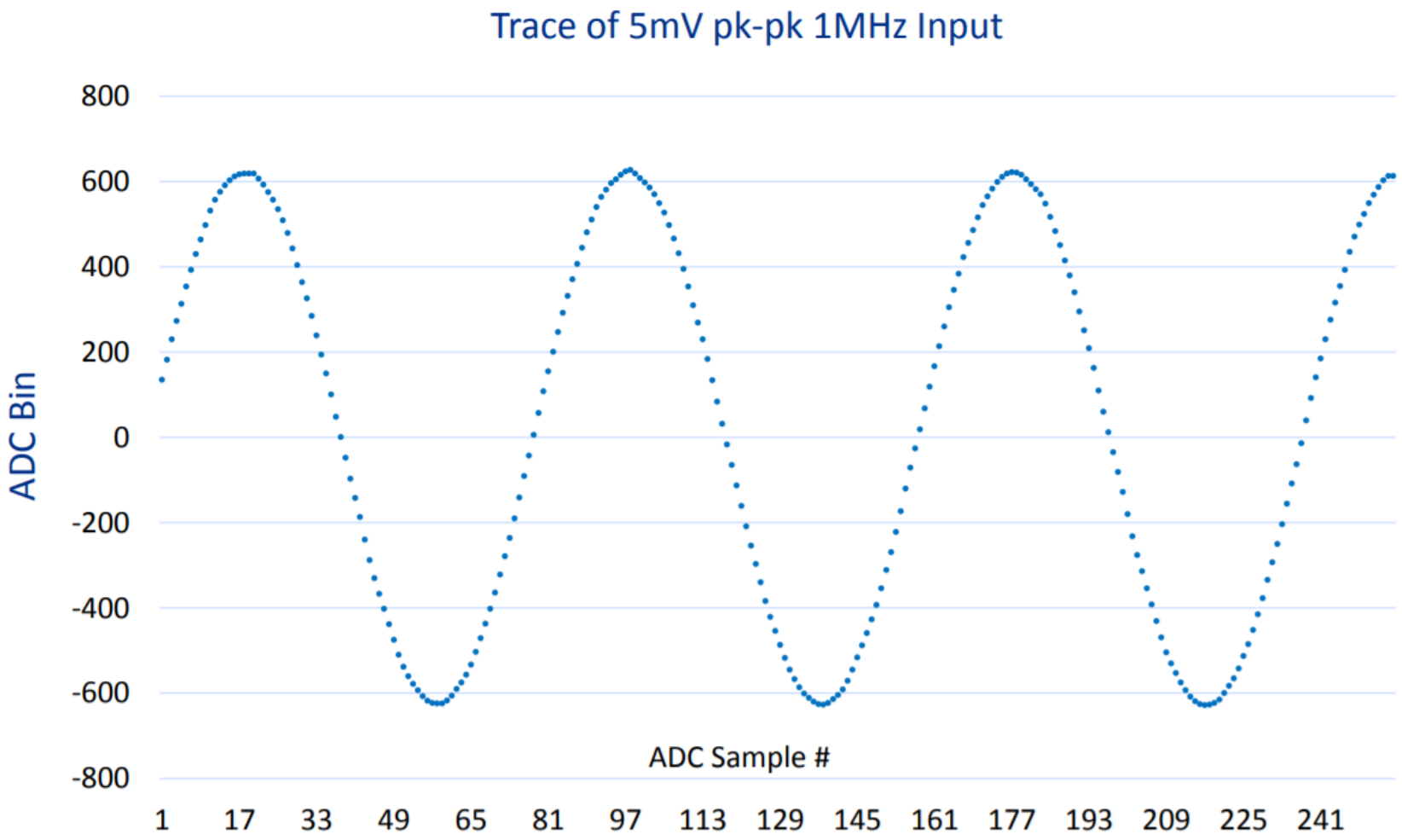
Readout Controllers (ROC)



- 24 low-bandwidth Ethernet from FEB
- To one high-bandwidth optical cable to TDAQ
- POE FEB power supply

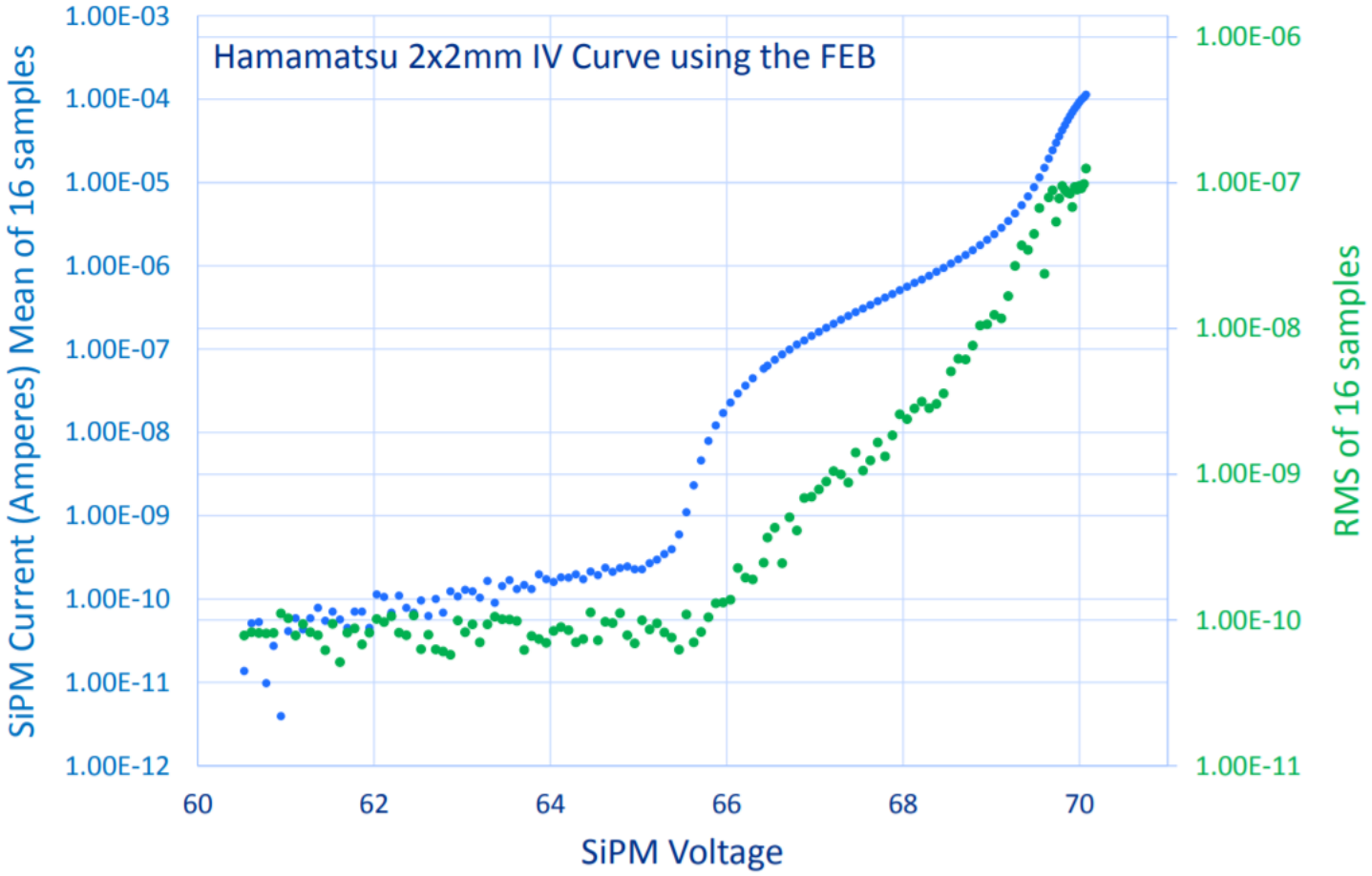


Performance: Ultrasound Chip ADC



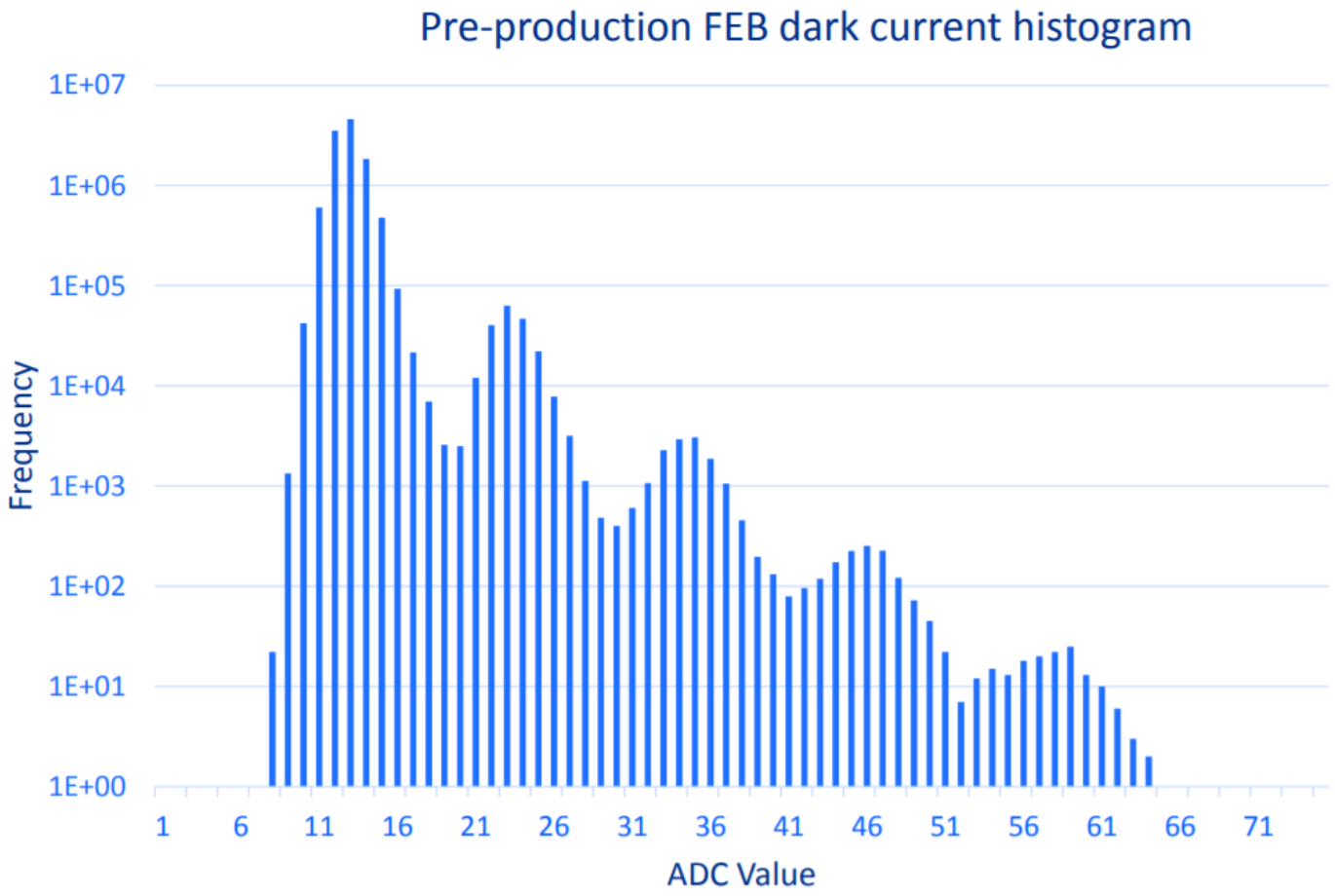
1 PE = 0.5 mV

Performance: I-V curve read out by FEB



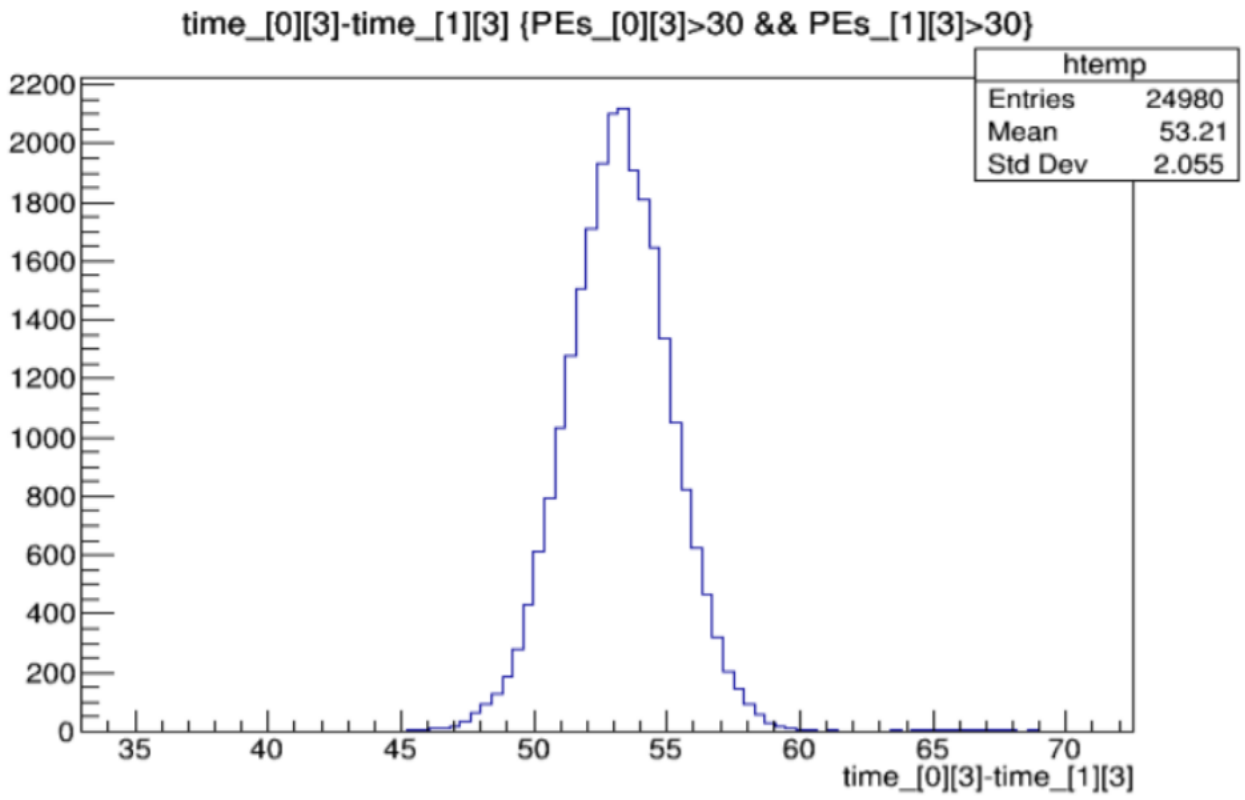
Performance: Dark Current Histogram in FEB

Log scale



Performance: Time Resolution

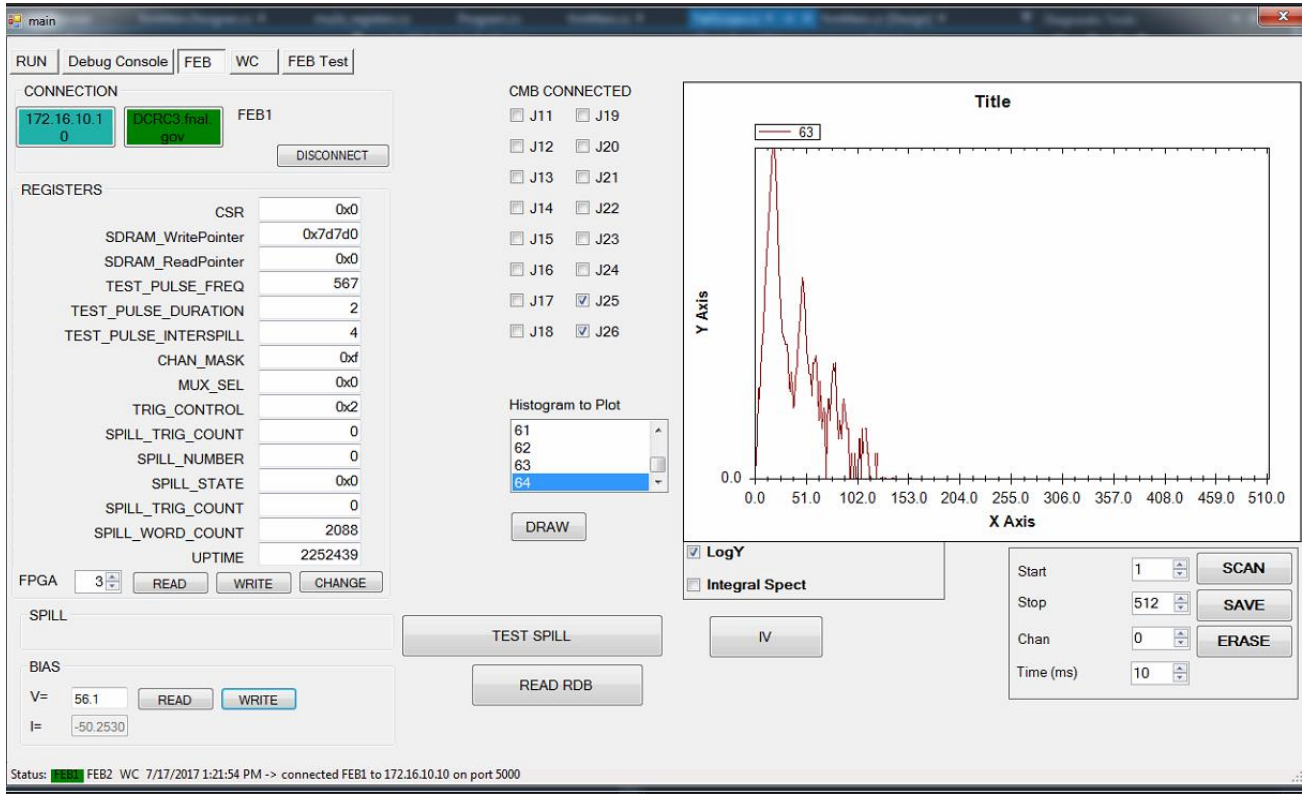
- 3m module
- Separate FEBs at either end



Plot of arrival time difference (ns) between opposites counter ends
Test Beam data 06/17. 120 GeV protons 2cm beam diameter

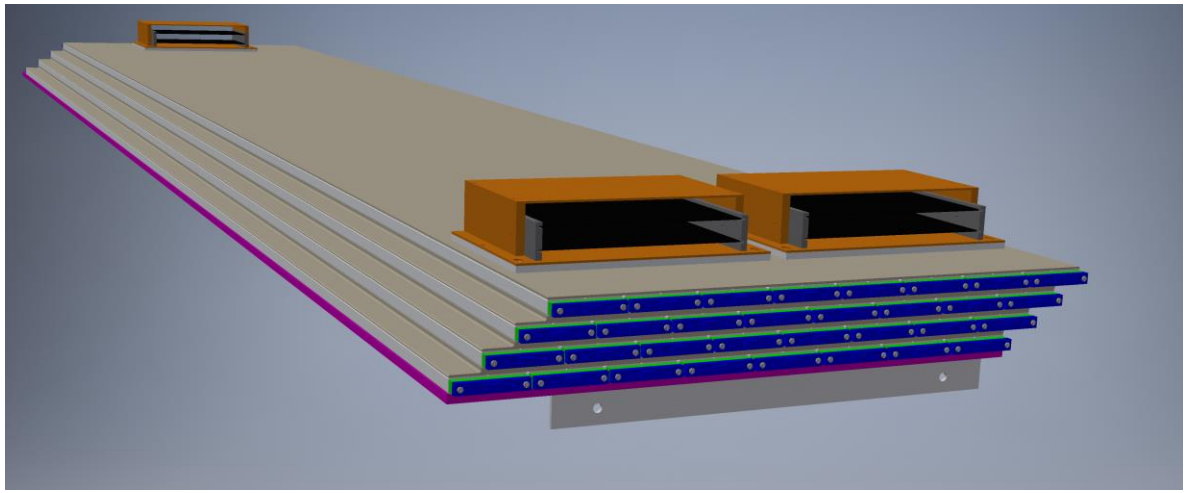
Status

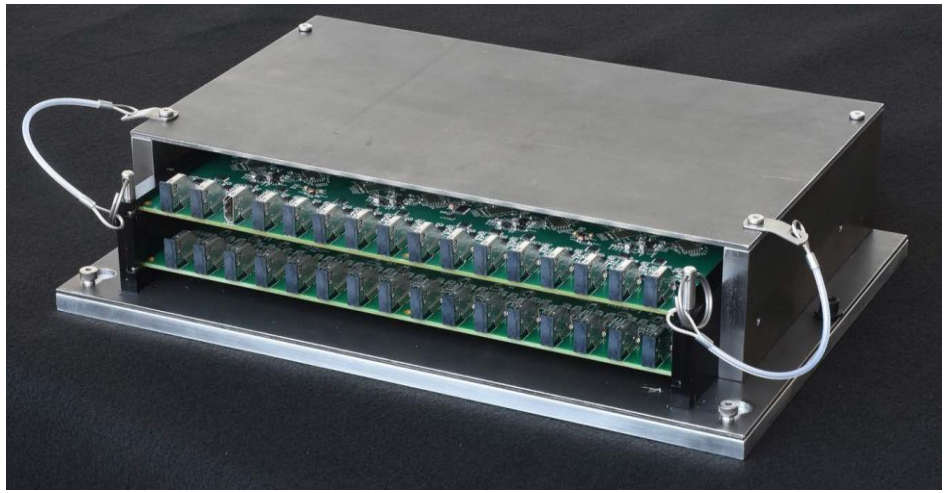
- Radiation exposure of 5x10^10 200MeV protons using medical accelerator showed no measurable change in behavior.
- Pre-production versions of all components on hand.
- QA/QC/performance testing underway.
- 1000 SiPMs on carrier boards at NIU.
- 200 CMB built by FNAL
- 28 FEB at KSU.
- 5 ROC built and tested at FNAL.



Backup

FEB Mounting Configuration





- FEB close to CMB, ~1m cable
- Mild steel housing
- Mounting oriented parallel to B-field
- Only one Cat-6 cable per FEB