Front End Digitization of tRPCs in the ATLAS Muon Spectrometer Phase-I Upgrade

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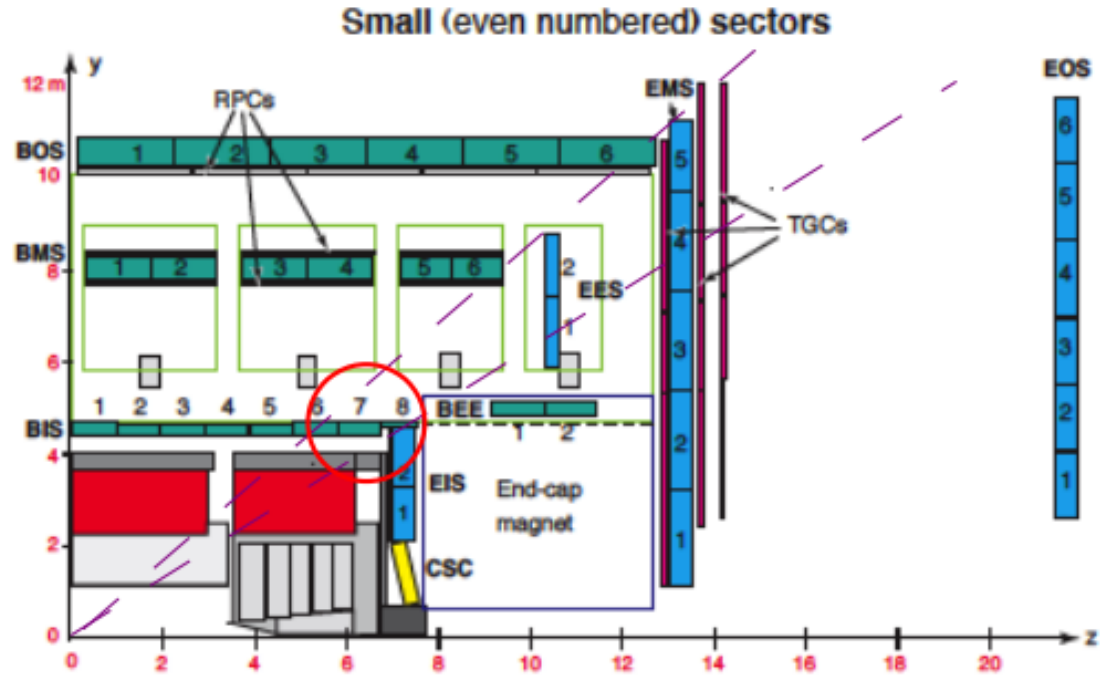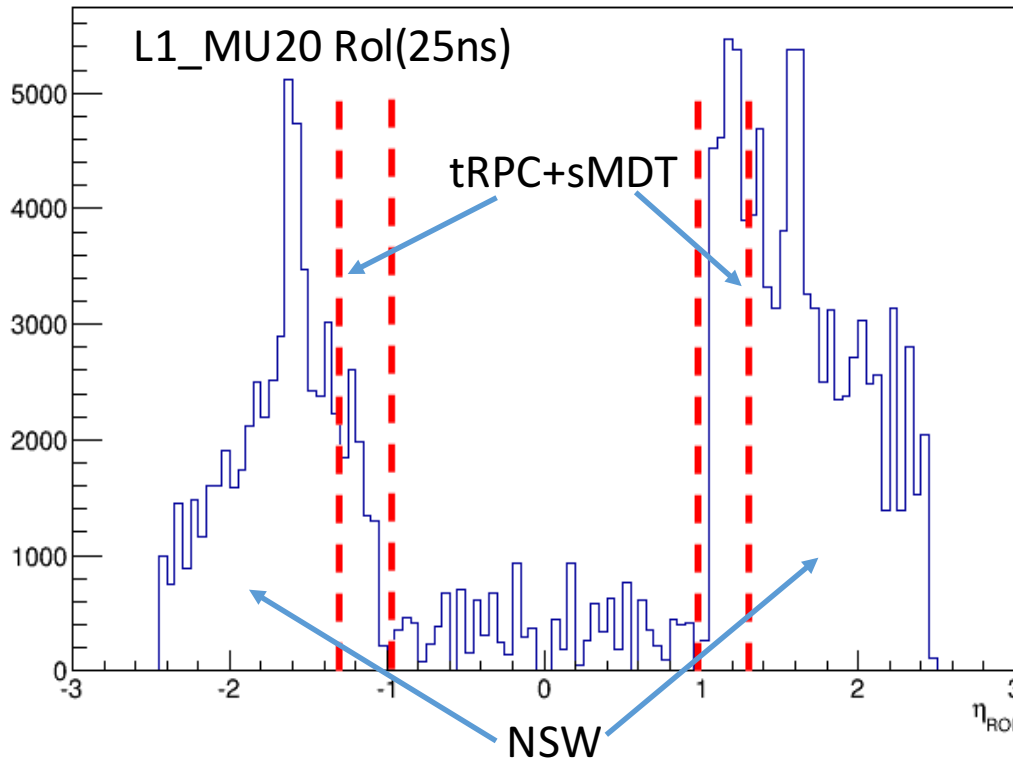
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Outlines

- Introduction of the Front End Signal Digitization- High Performance Time to Digital Converter (HPTDC) chip

- Latency simulation and hardware test

- Prototype design and test

- Front End digitization card design

- Conclusion

ATLAS thin RPC trigger upgrade project

- ❏ Current ATLAS muon trigger has a problem of large fake LVL1 trigger rate.
  - ❖ 70% of the rate from $|\eta| > 1.3$.
  - ❖ 22% of the rate from $1.0 < |\eta| < 1.3$
- ❏ To reduce fake rate:
  - ❖ The New Small Wheels(NSW) in ATLAS muon Phase-I upgrade cover transition region $1.3 < |\eta| < 2.5$.
  - ❖ thin Resistive Plate Chambers($\textbf{\textit{tRPC}}$) and small_tube Monitored Drift Tube(sMDT) chambers cover $1.0 < |\eta| < 1.3$.

thin RPC readout
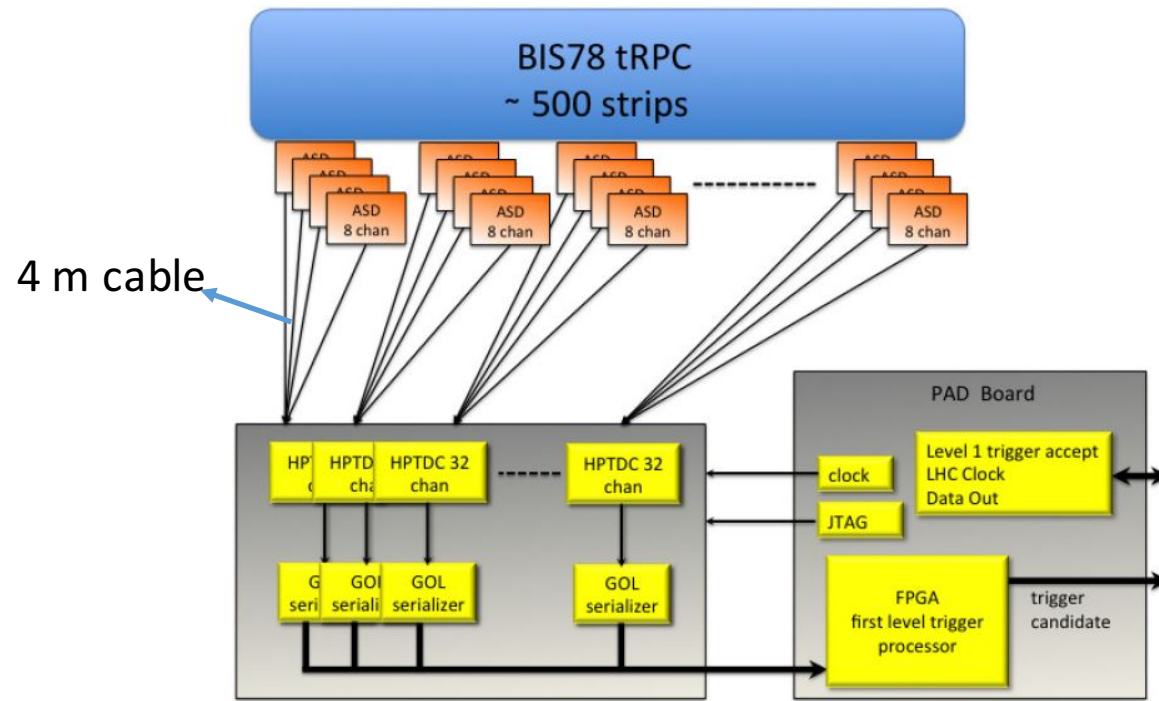
black diagram of readout of tRPC

tRPC readout electronic total latency requirement:
43* BC=1075ns

components	time(ns)
TOF	27 ± 1
Strip propagation	10
ASD+TOT	10
Digitization	<350
GOL(Gigabit Optical Link)	50
Pad board	<160
Fiber to USA15	416 ± 24

High Performance Time to Digital Converter (HPTDC) is a multi-channel Time-to-Digital (TDC) ASIC.

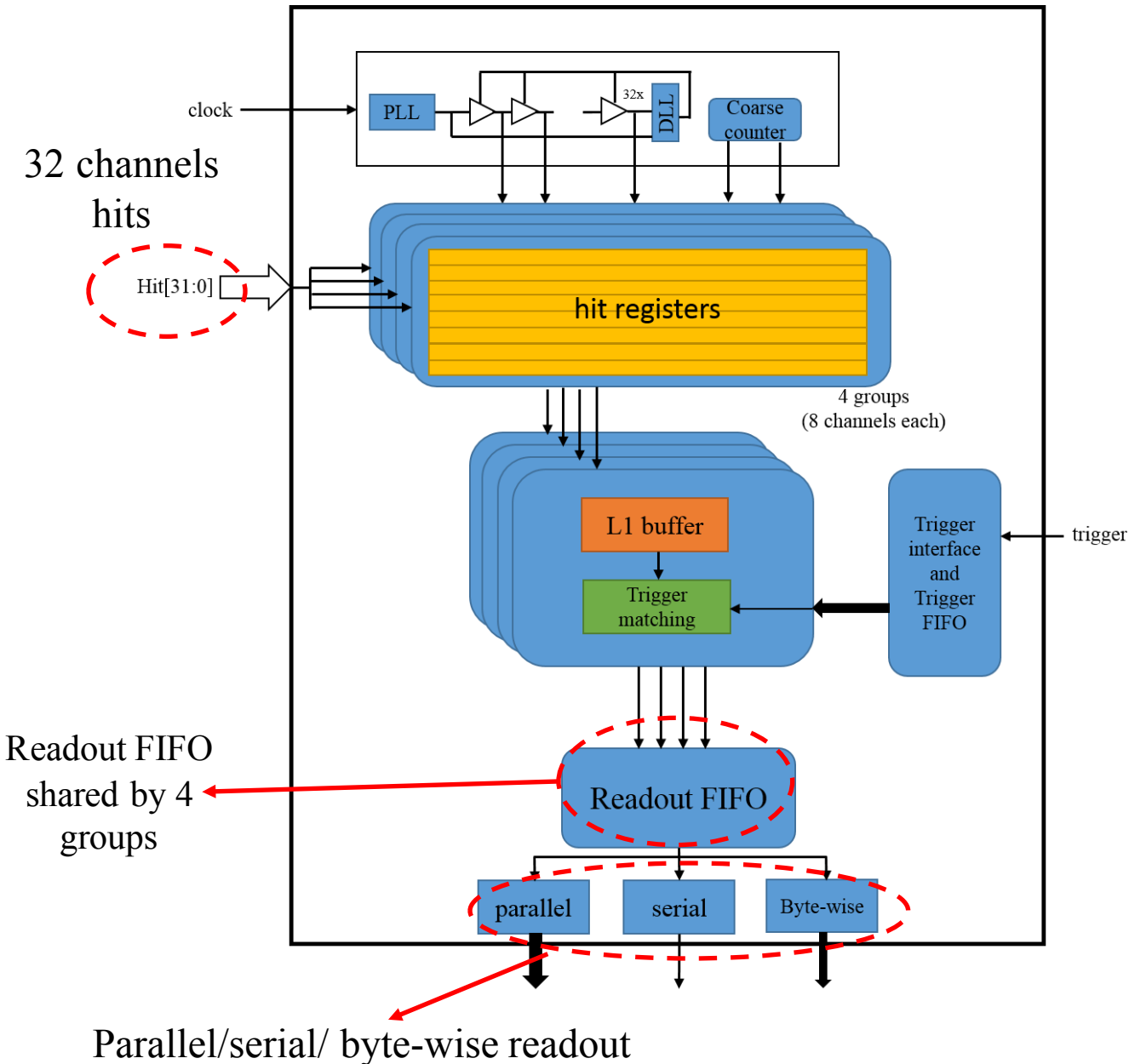Option considered to digitize the detector signal from tRPC detector.

4

thin RPC front end board
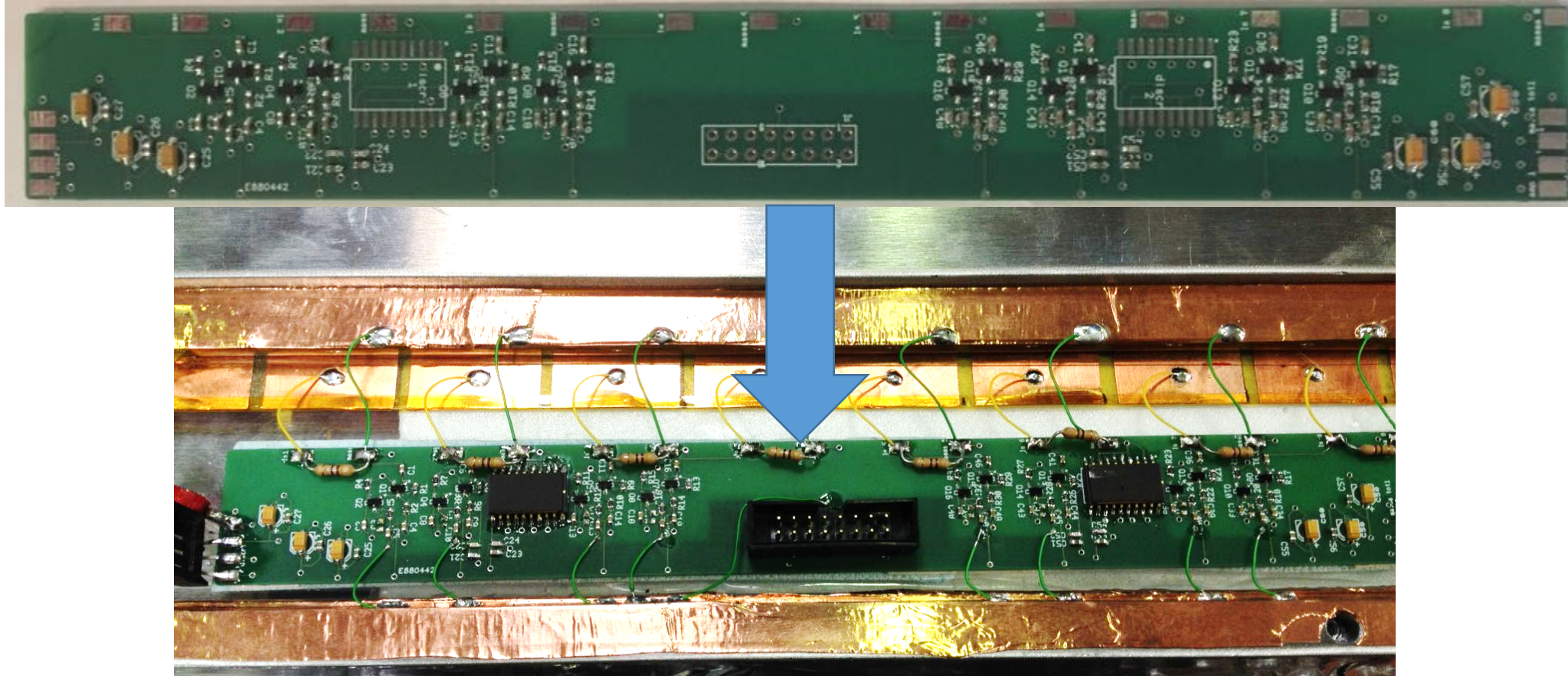
from Giulio Aielli's talk

Each front end board will handle 8 strips signals, and send 8 Low-voltage differential signaling(LVDS) signal to digitization card.
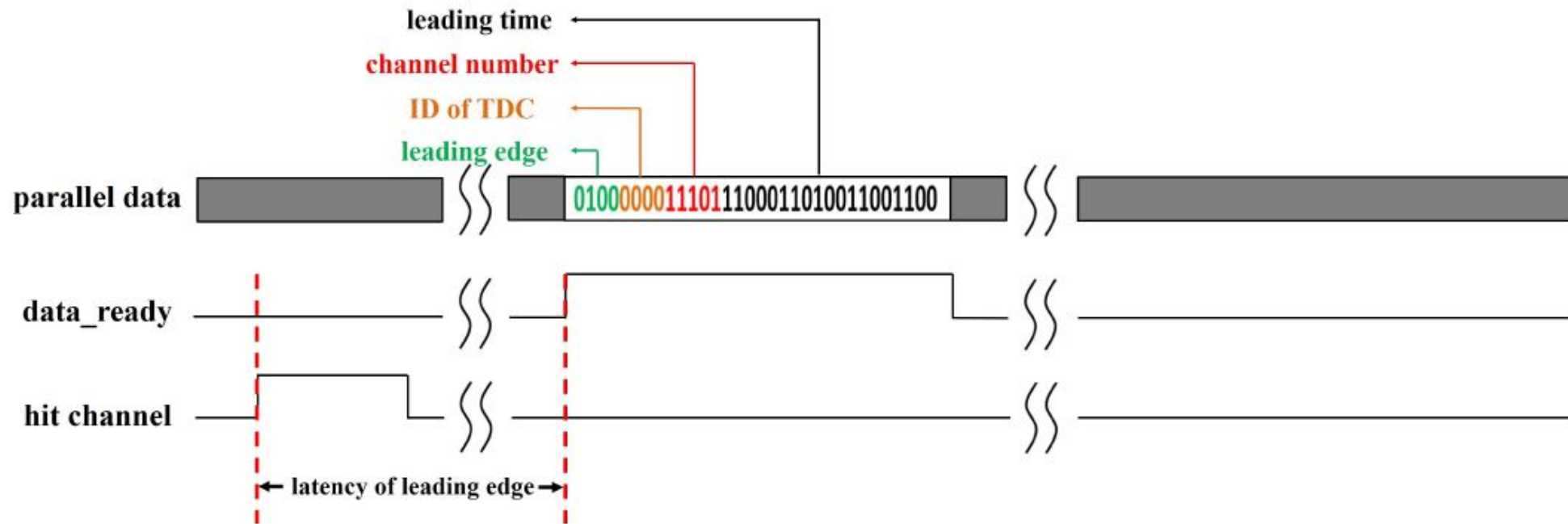
HPTDC key features

32 channels hits

Hit[31:0]

clock

PLL · · 32x DLL · Coarse counter

hit registers

4 groups
(8 channels each)

L1 buffer

Trigger matching

Trigger interface and Trigger FIFO

trigger

Readout FIFO shared by 4 groups

Readout FIFO

parallel · serial · Byte-wise

Parallel/serial/ byte-wise readout

- 32 TDC channels
- Trigger mode / triggerless mode
- Three types of readout: parallel, serial and byte-wise readout
- Programmable time resolution
- Internal logic core speed: 40 MHz, 80 MHz, 160 MHz
- Four types of measurement modes:

leading edge mode   trailing edge mode

leading and trailing edge mode   pair mode

width
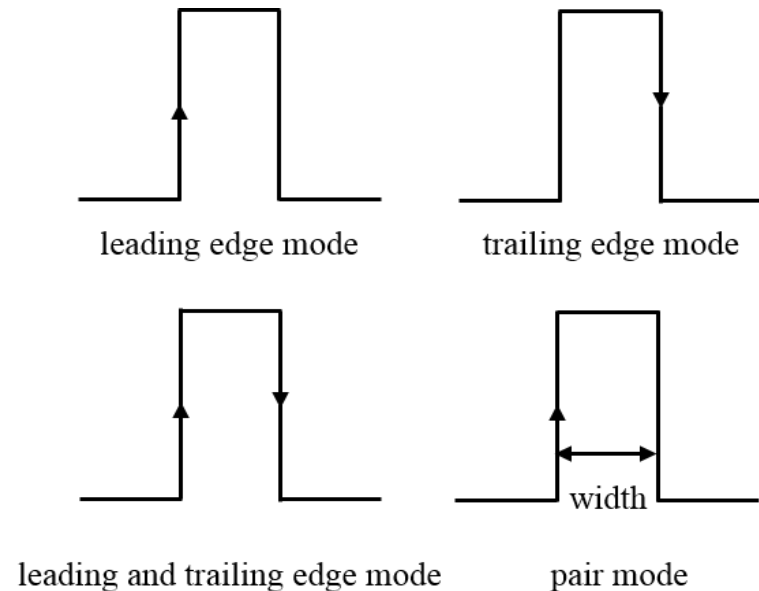
Latency definition in the HPTDC

Data_ready is a flag to show 32 bit parallel data of hit is sent out from HPTDC, so latency is time difference between the leading edge of hit and the leading edge of its correspond data_ready flag

Latency simulation summary

To study the latency of HPTDC in the triggerless mode for the ATLAS tRPC upgrade:

1. Core clock speed should be set at 40, 80, 160 MHz (80 MHz was selected)

2. The number of correlated hits in one RPC layer from a single track (1-3)

3. Correlated hits should be distributed either to

   a. **sequential channels** in the same memory buffer

   b. **alternating channels** in each of four memory buffers

4. Measurement mode can be set to either leading edge mode or pair mode.

Based on the simulation results, we design a prototype of digitization card to measure latency and evaluate the combined function of HPTDC and GOL.
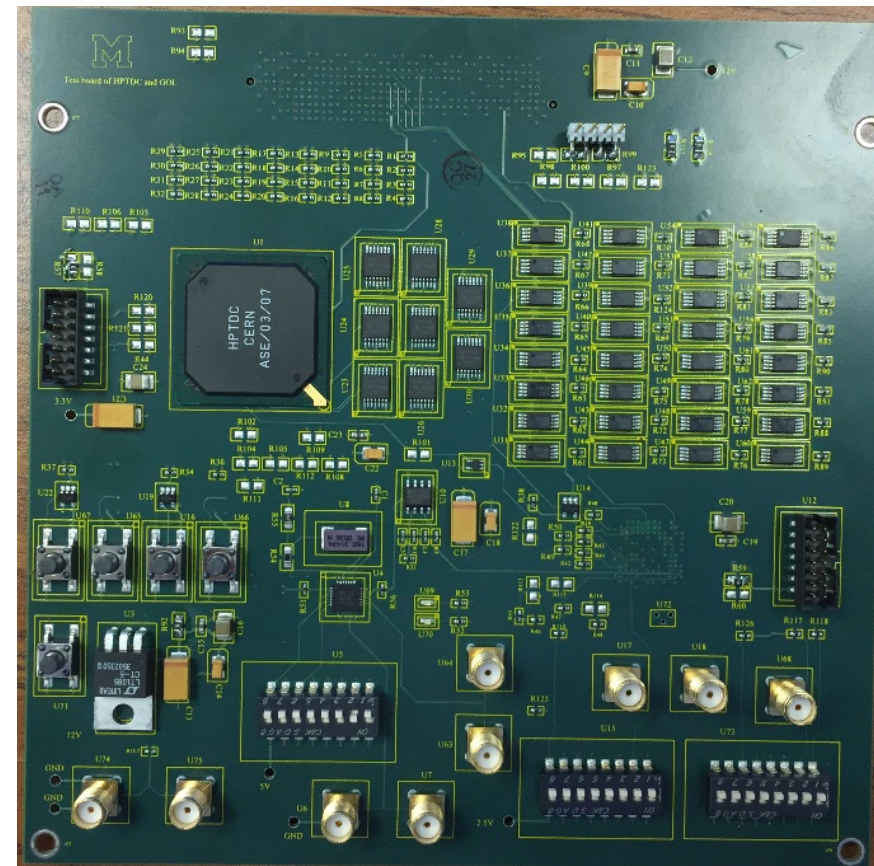
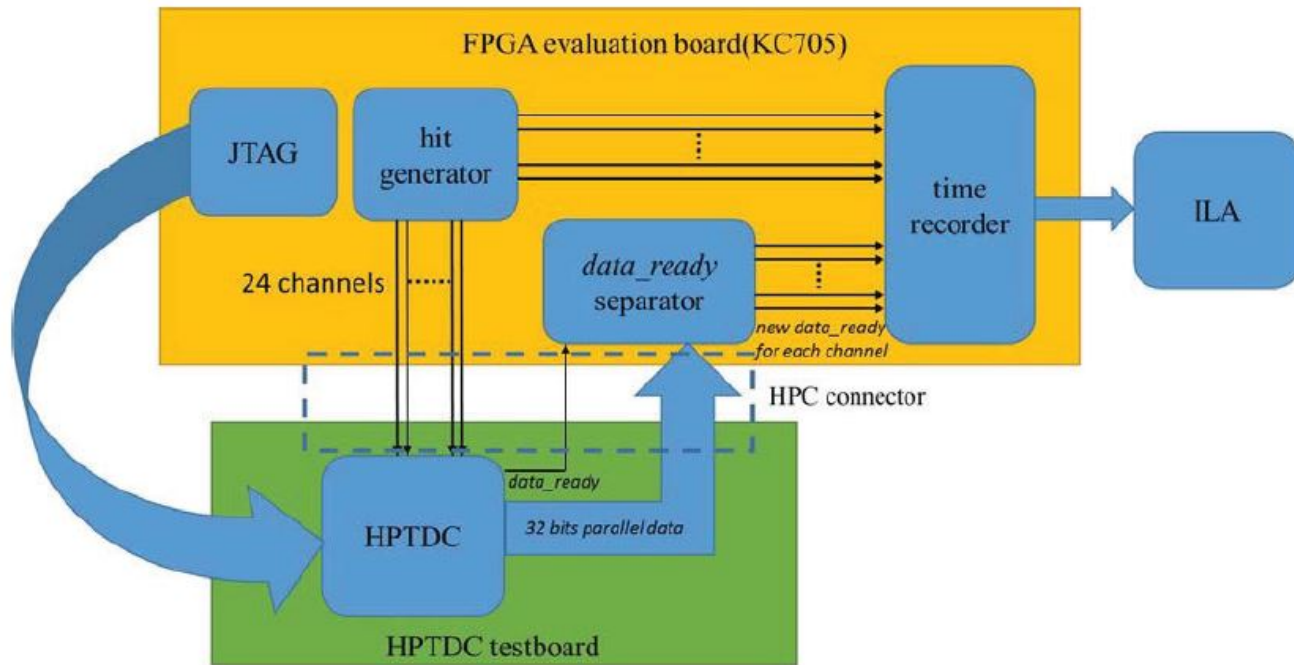Results are shown in the following slides

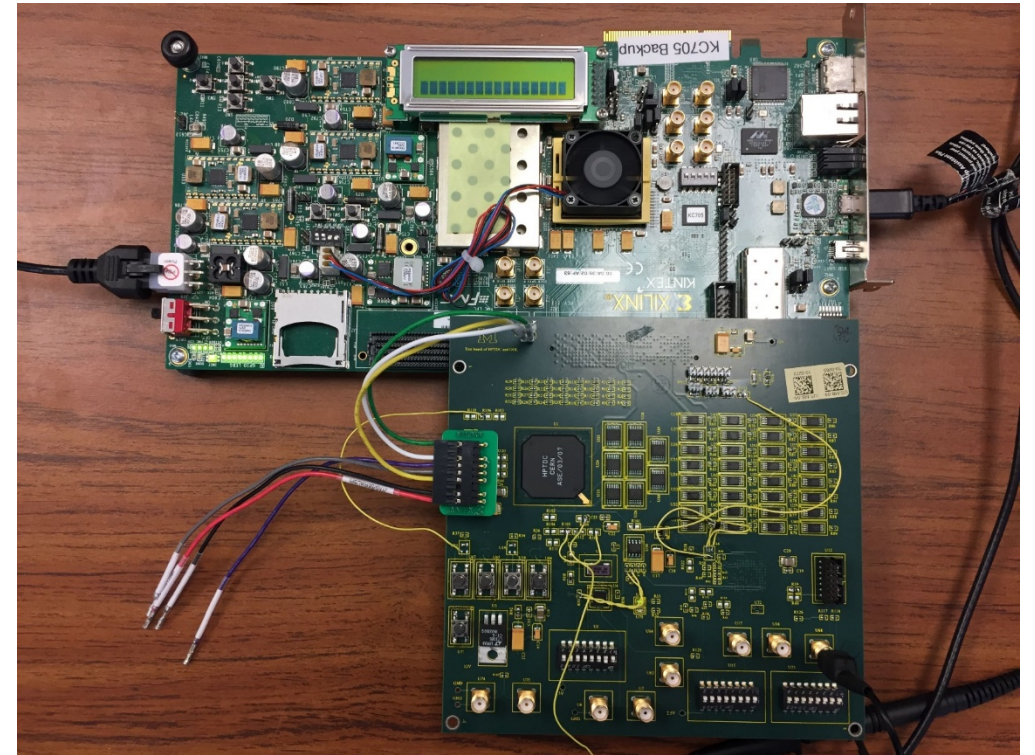# Prototype of digitization card
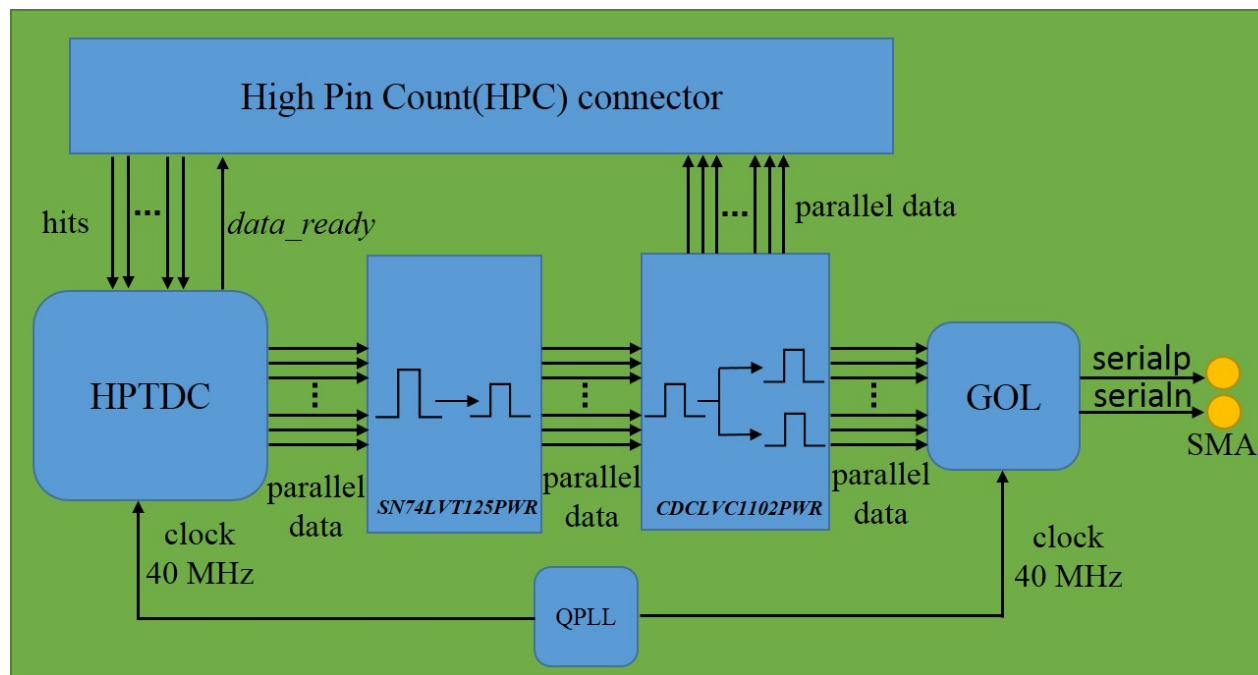
Schematic of prototype

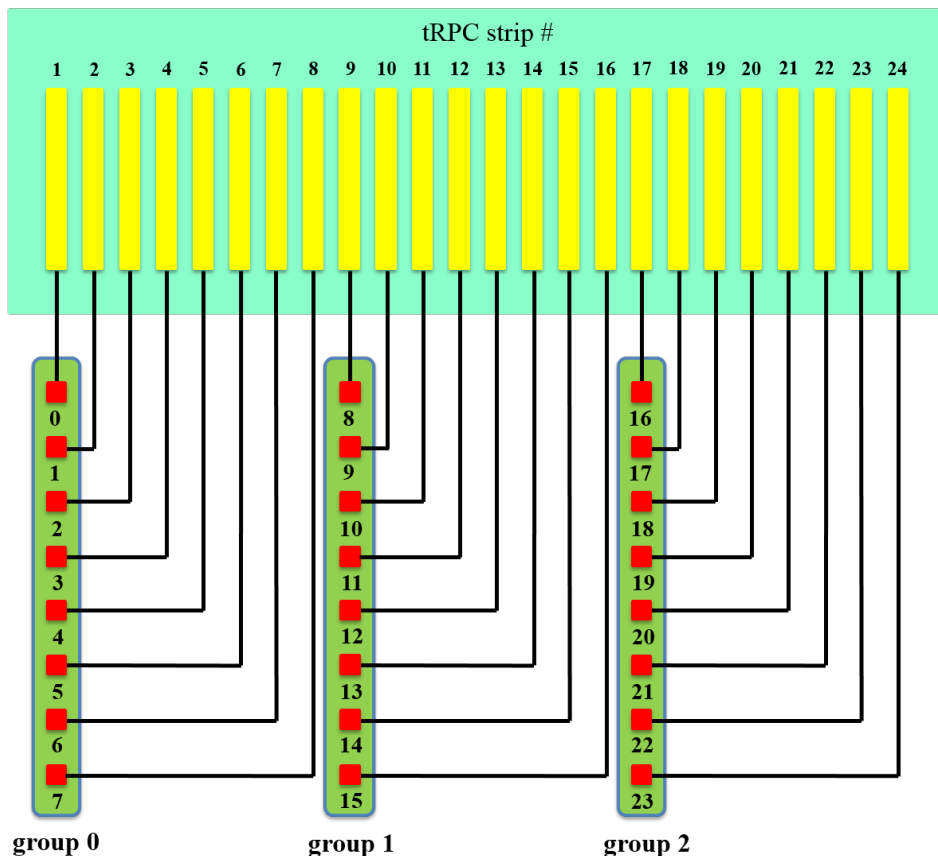prototype

Setup of latency test
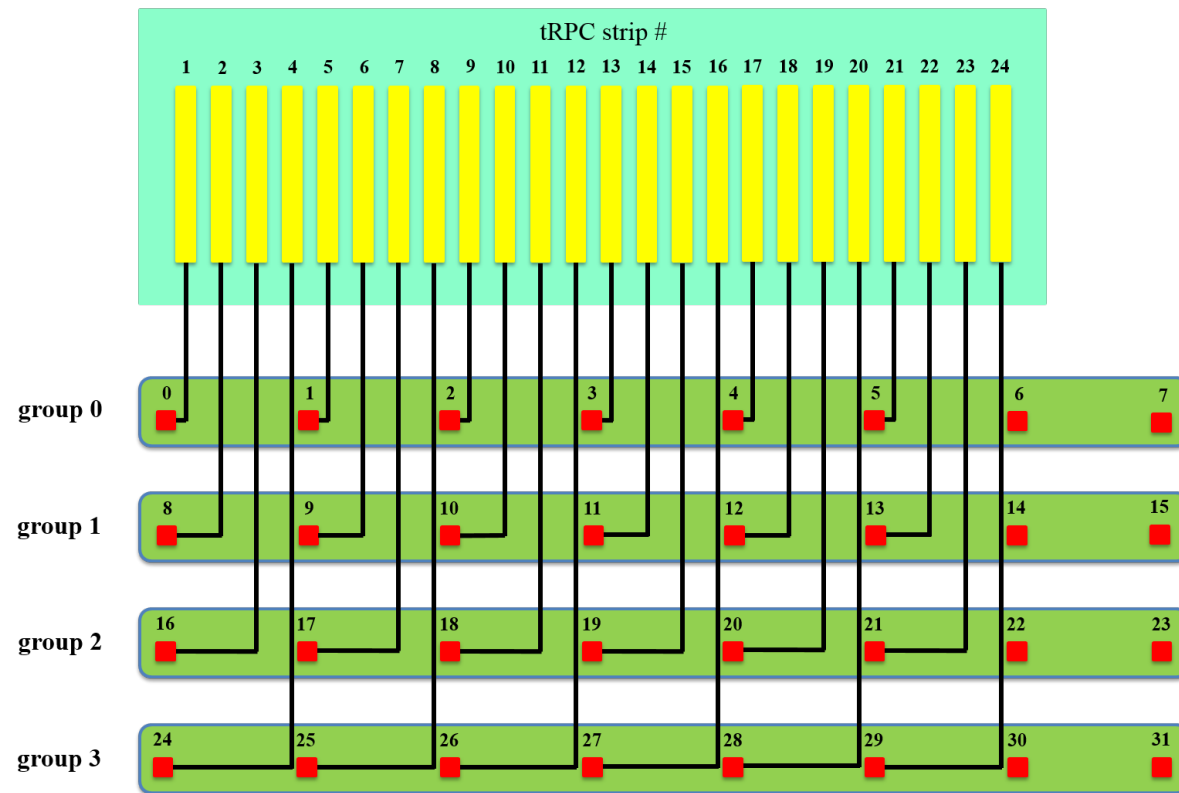

Schematic of setup

Real setup

alternating mapping vs Sequential mapping

There are two mapping for the connection between strips of tRPCs and input of HPTDC: alternating mapping and sequential mapping.
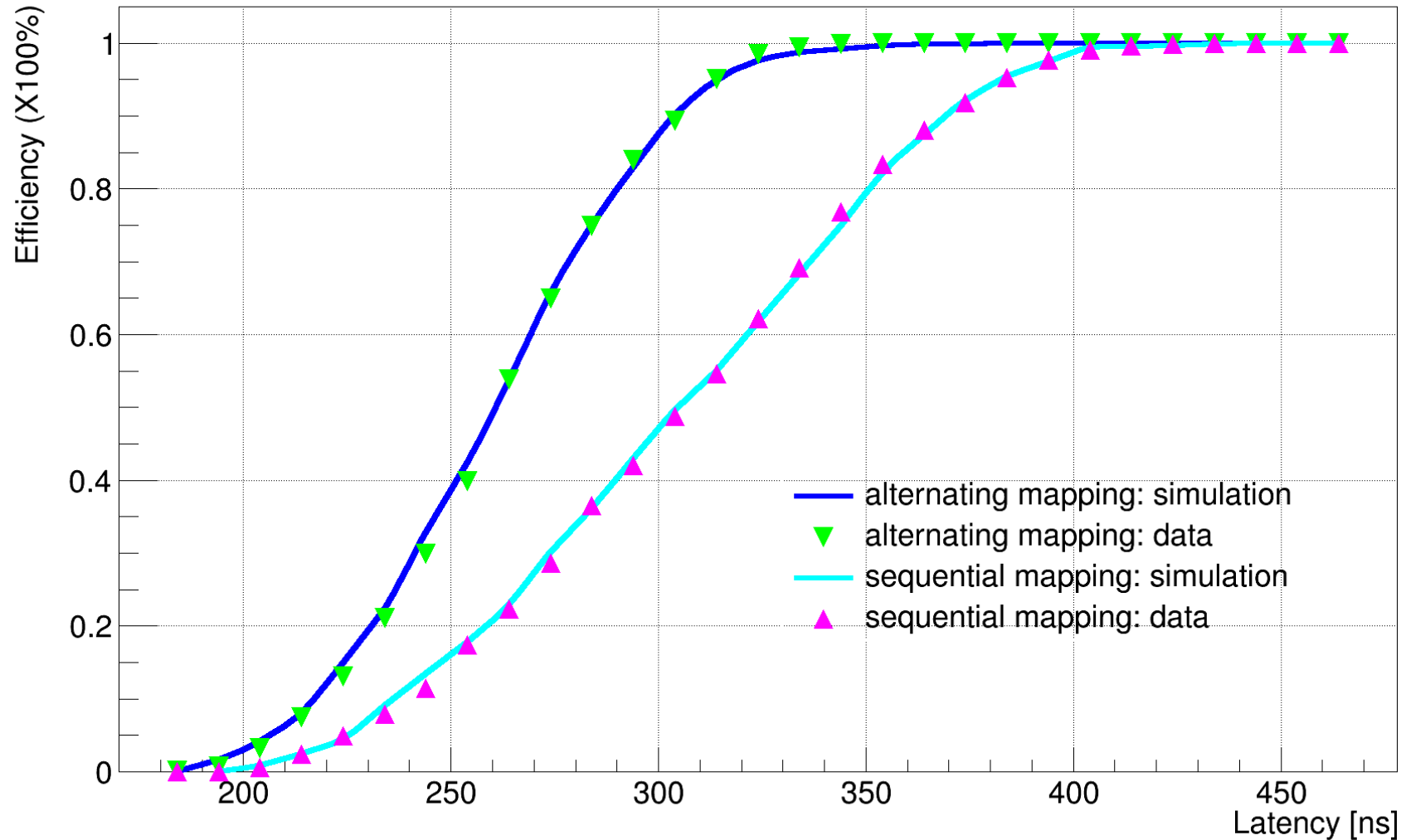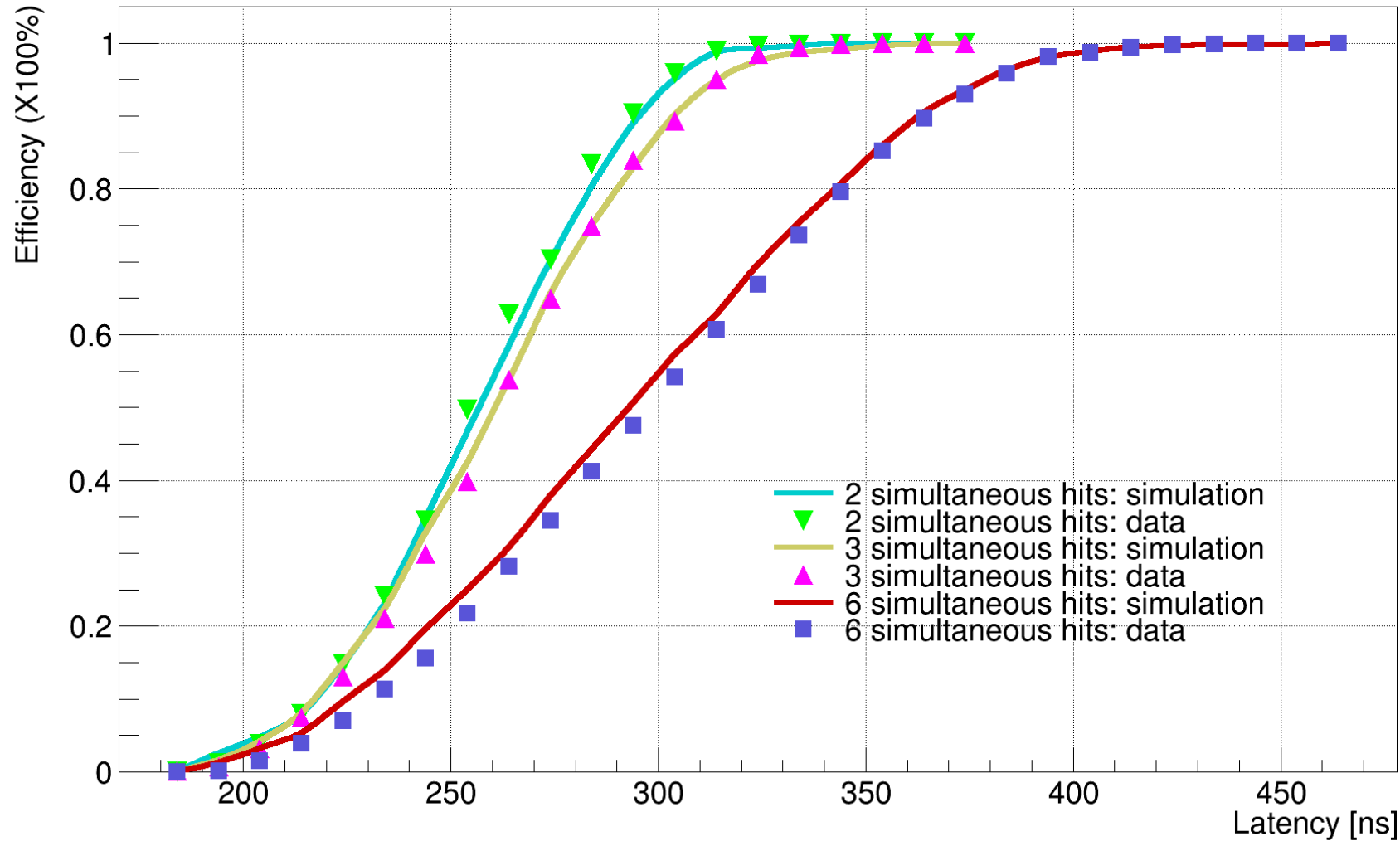

Sequential mapping

alternating mapping

alternating mapping vs Sequential mapping

300 kHz random hit @ 24 channel
as background
For sequential mapping
3 kHz simultaneous hit @ channel
0,1,2.
For alternating mapping:
3 kHz simultaneous hit @ channel
0,8,16.

Number of simultaneous hits

Using alternating mapping;

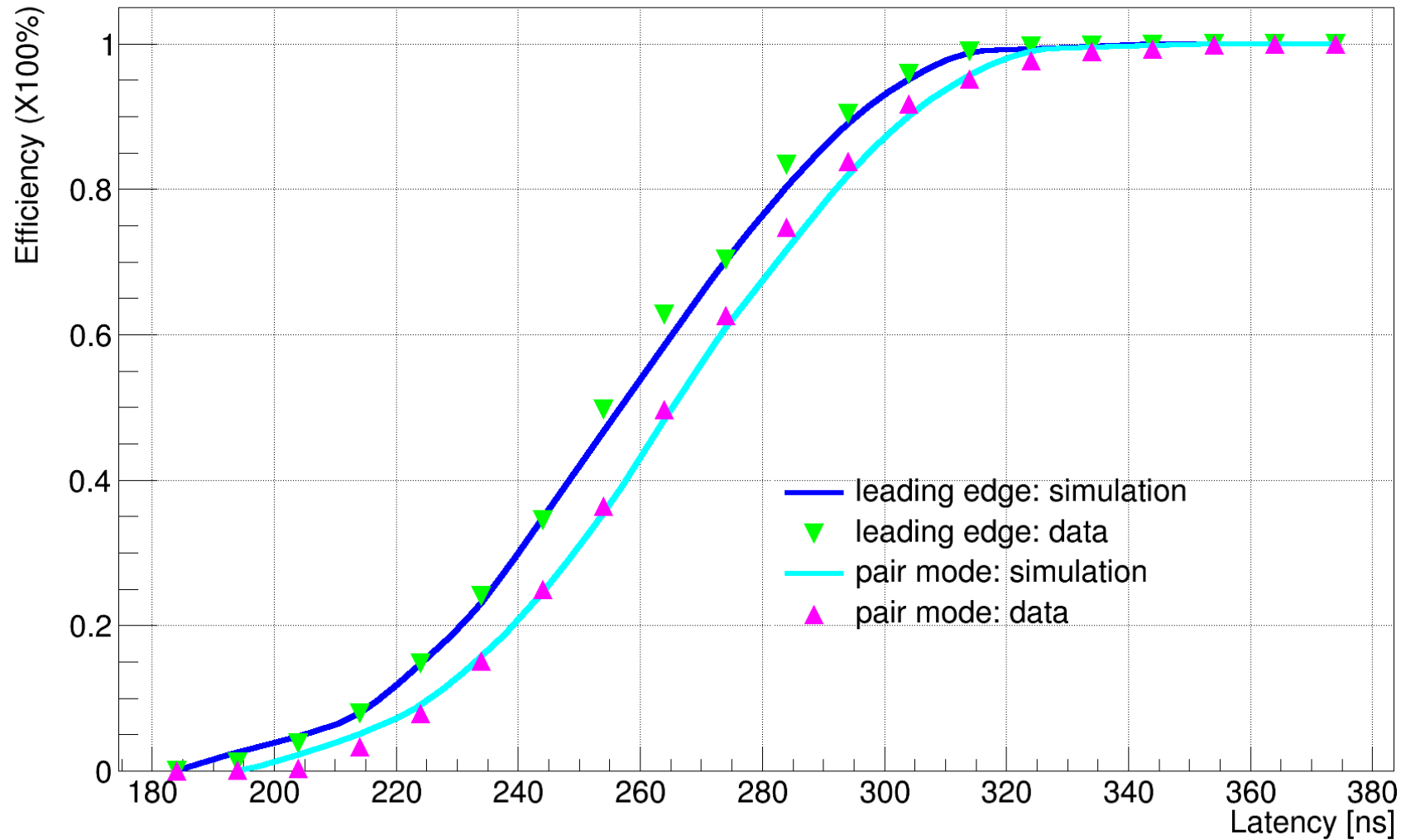300 kHz random hit @ 24 channel as background
For 2 simultaneous hit
3 kHz simultaneous hit @ channel 0,8.
For 3 simultaneous hit
3 kHz simultaneous hit @ channel 0,8,16.
For 6 simultaneous hit
3 kHz simultaneous hit @ channel 0,8,16,24,1,9.

Measurement mode

Using alternating mapping;

300 kHz random hit @ 24 channel as background
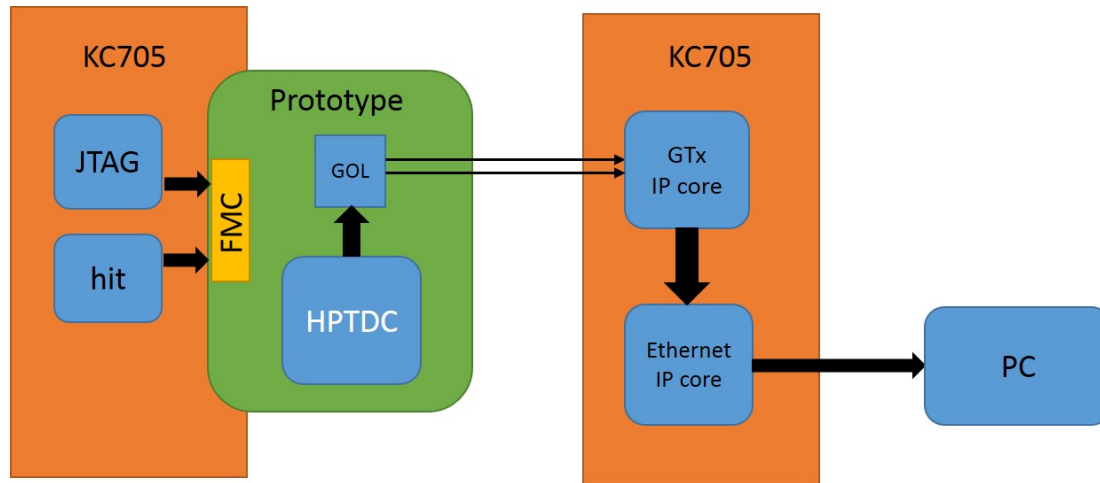For leading edge:
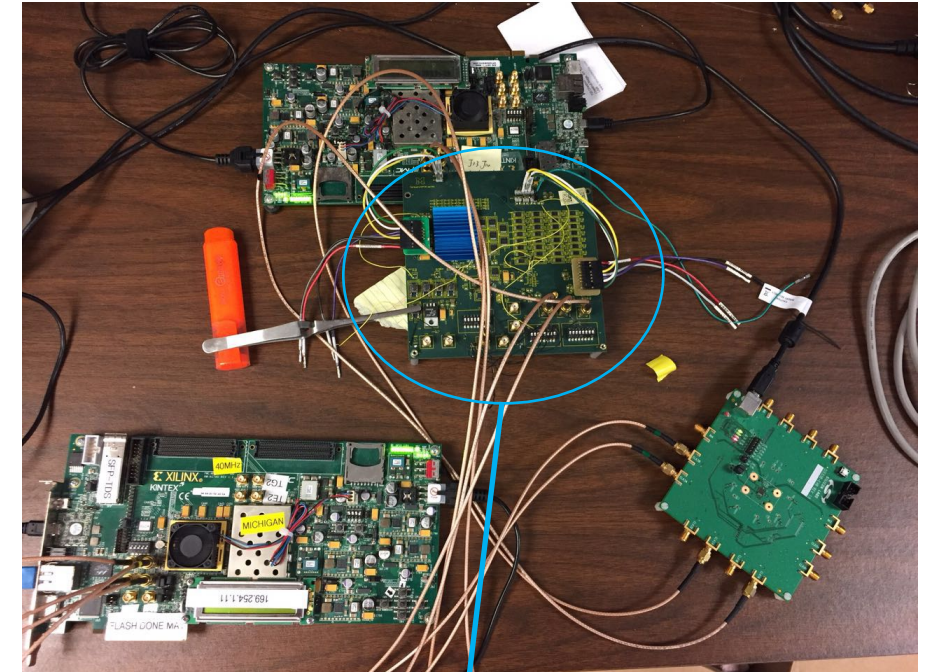3 kHz simultaneous hit @ channel 0,8.
For pair mode:
3 kHz simultaneous hit @ channel 0,8.
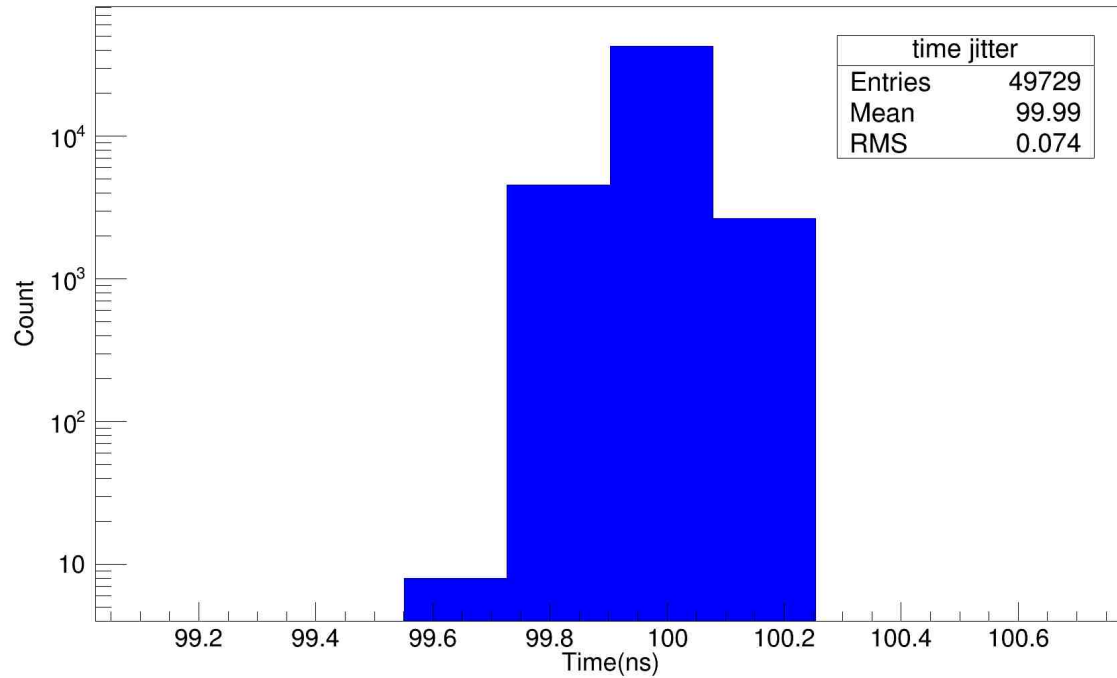
Final Prototype Test of HPTDC+GOL

Two KC705 FPGA evaluation board were used. One is used to do configuration for HPTDC and send hit, the another one is used to receive output of GOL and send data to PC.
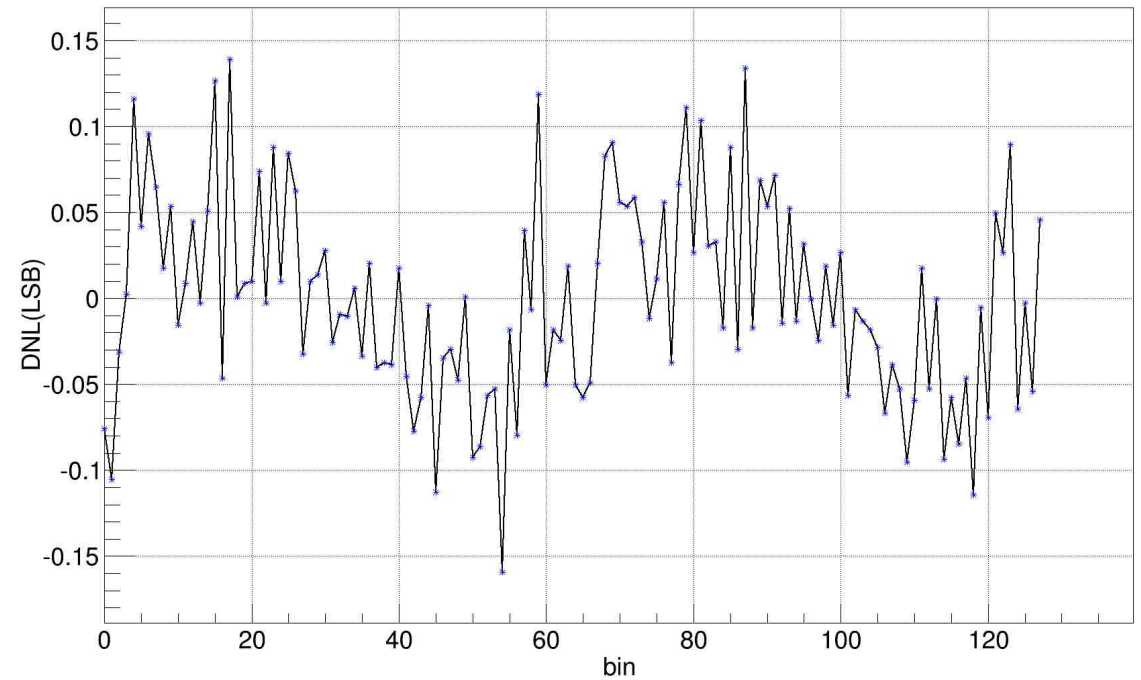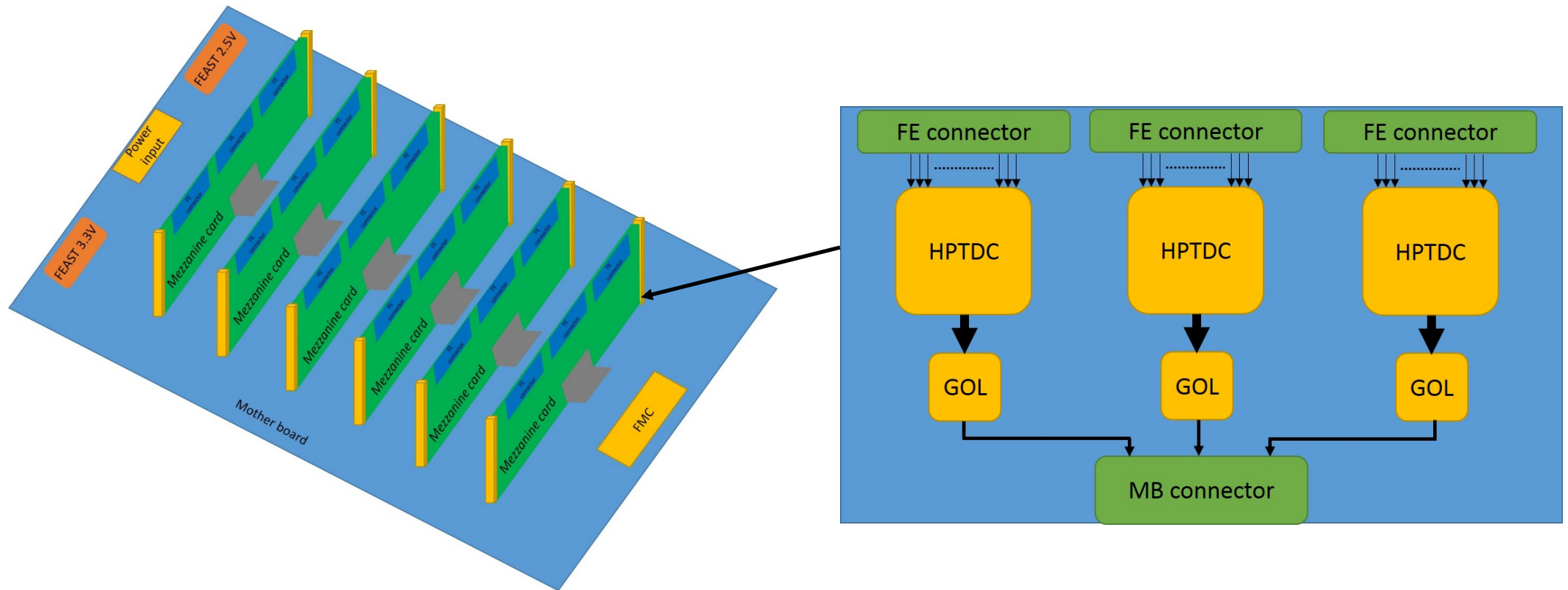

prototype

Measurement of prototype

DNL for HPTDC in medium resolution mode, 1LSB=195 ps

Time jitter result using 100 ns between rising edge
of successive pulses

Front end digitization card design

The total size of digitization card will be 35 cm(length)*25cm(width)*12cm(height)

The design of digitization will be submit soon.

Conclusions

A prototype was design to do the test of latency of HPTDC and the basic function of HPTDC plus GOL.

➢ The latency test and simulation results show that the HPTDC can get the required latency by choosing the appropriate parameter.

➢ The basic function of HPTDC and GOL have been verified on the prototype, and they can work well.

➢ The front end digitization card was designed based on the prototype and will be submit soon.