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Front End Digitization of tRPCs in the ATLAS Muon Spectrometer Phase-1 Upgrade

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The ATLAS Muon Spectrometer Phase-1 high luminosity upgrade program includes the staging of thin Resistive Plate Chambers (tRPC) to increase trigger acceptance and reduce fake muon trigger rates in the barrel-endcap transition region, corresponding to pseudo-rapidity range 1<|η|<1.3. The tRPC signals will be processed with front-end digitization electronics that make use of the CERN based HPTDC and Gigabyte Optical Link microchips. Low level trigger candidates must be flagged within a maximum latency of 1075 ns, thus imposing stringent signal processing time performance requirements on the readout system in general, and on the digitization electronics in particular. In this talk we report on the design of the tRPC front end digitization electronics. The performance based on both Verilog simulations and measurements using a prototype board under realistic hit rate conditions indicates that the HPTDC in triggerless mode operation satisfies the timing, resolution and power requirements.

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