APS | DIVISION OF PARTICLES & FIELDS

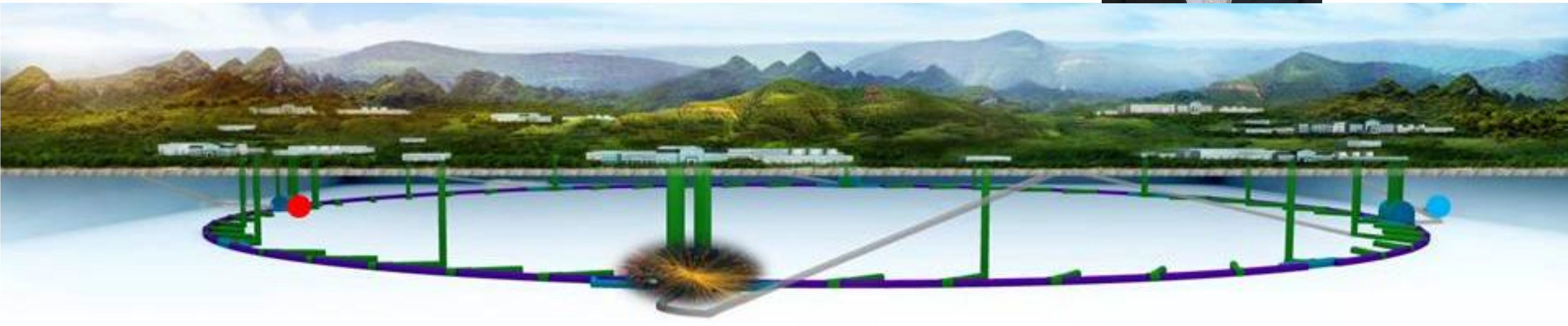
DPF 2017

MEETING OF THE AMERICAN PHYSICAL SOCIETY DIVISION OF PARTICLES AND FIELDS

Overview of the CEPC Vertex Detector

Hongbo Zhu (IHEP, Beijing)

On behalf of the CEPC Study Group



Outline

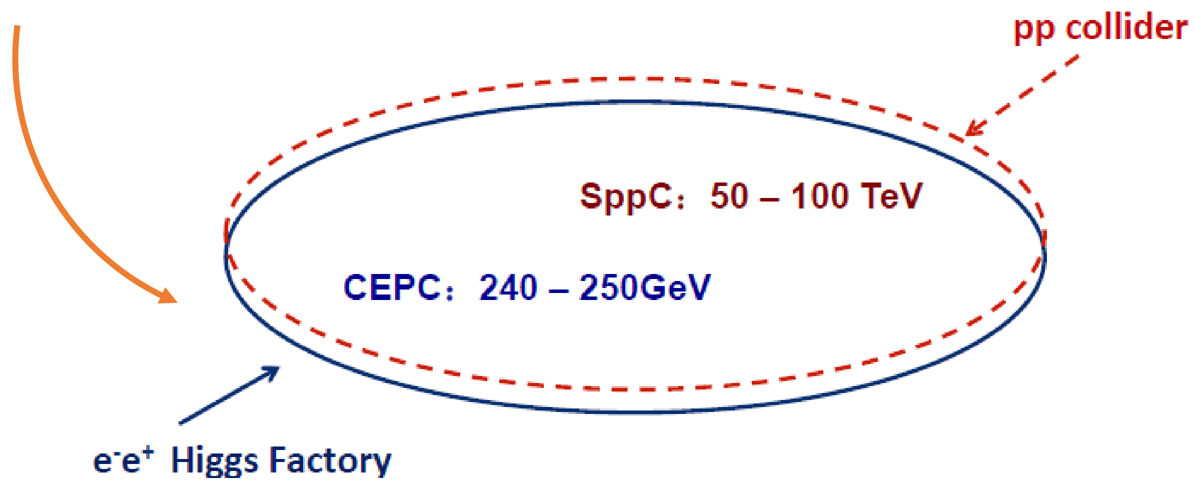
- Introduction to the CEPC
- The CEPC Vertex Detector
- Summary and Outlook

Introduction

- The **Higgs Discovery** in 2012 witnessed the breakthrough in the history of particle physics and triggered wave of thoughts on **Higgs Factories** around the world …

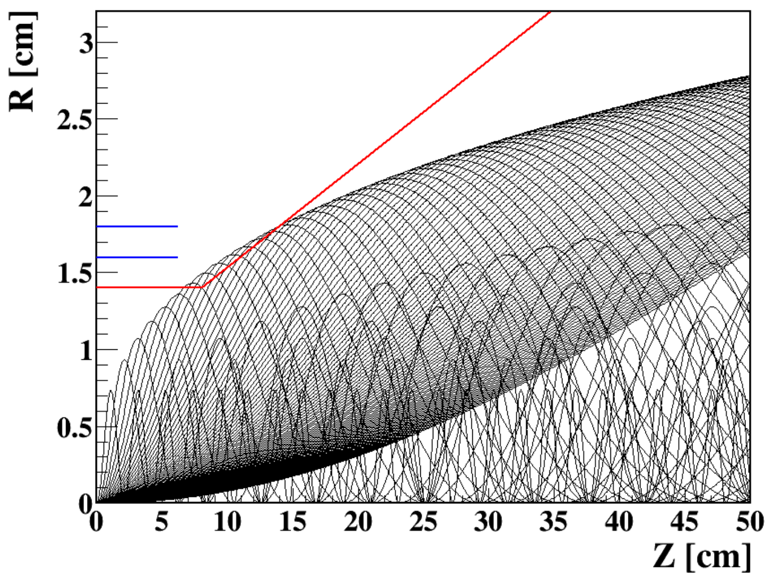
A. Bondel and F. Zimmerman, ***A High Luminosity e^+e^- Collider in the LHC tunnel to study the Higgs Boson***, arXiv:1112.2518, **even before the Higgs discovery!**

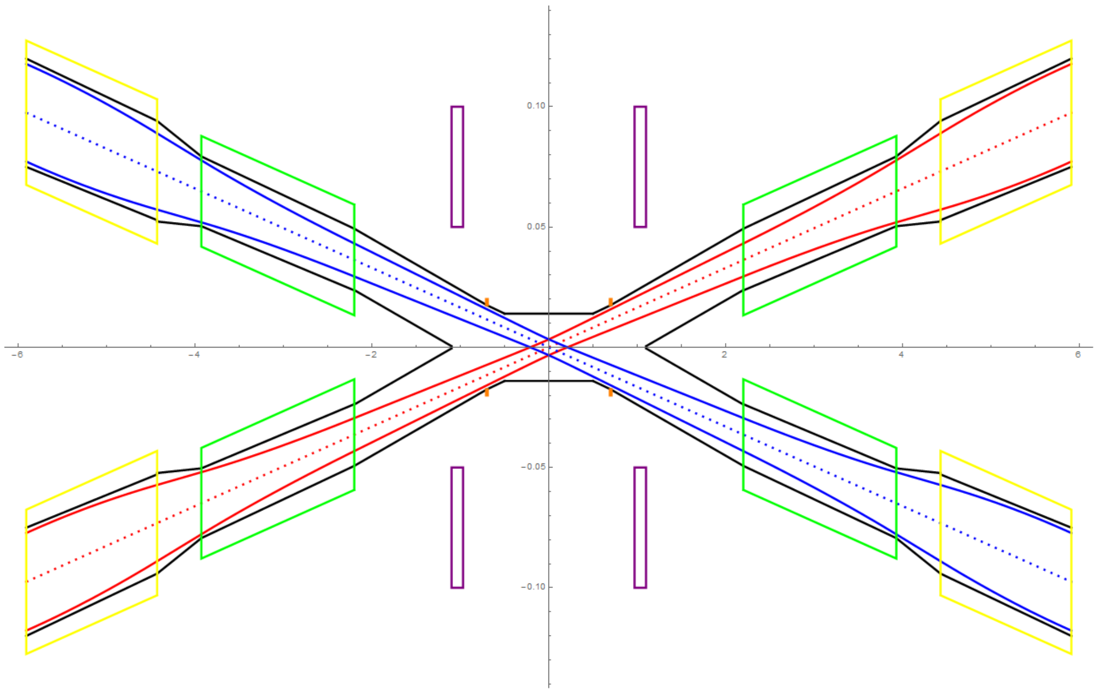
- **Where the story began** … presented by Prof. Qing Qin at the Accelerators for a Higgs Factory: Linear vs. Circular (HF2012)



Machine-Detector Interface (MDI)

- Extremely complicated and challenging → **Optimization (trade-off) between accelerator and detector performance**

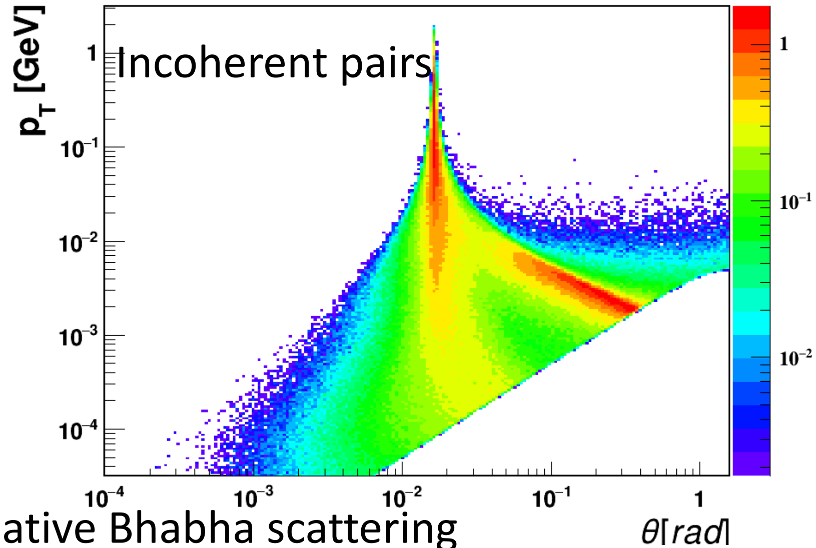


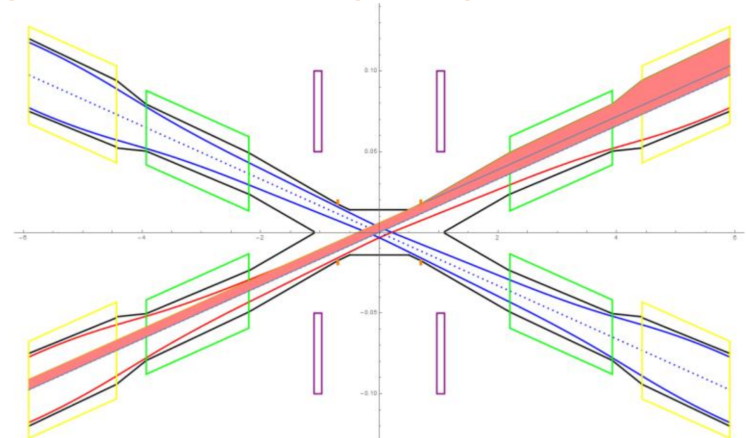


- Proper placement of accelerator and detector components in the **interaction region**
- Estimation of **radiation backgrounds**

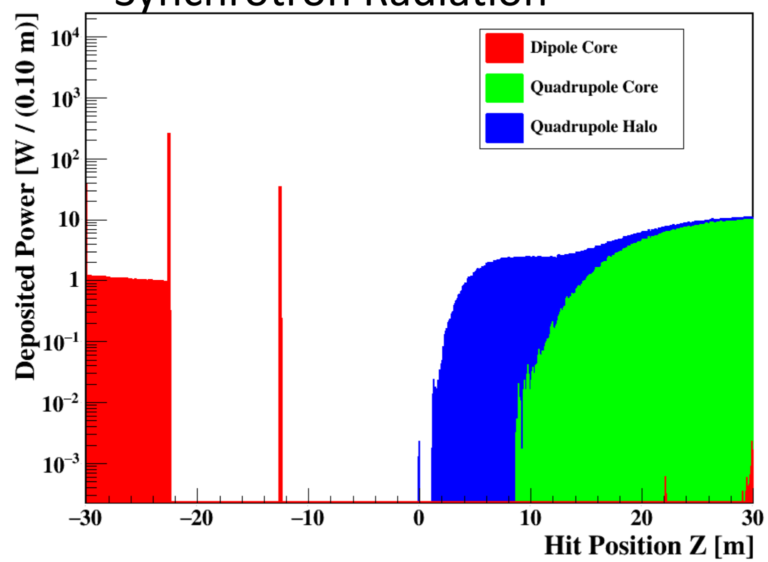
Radiation Backgrounds

- Updating the double ring results: **hit density, detector occupancy, radiation levels**

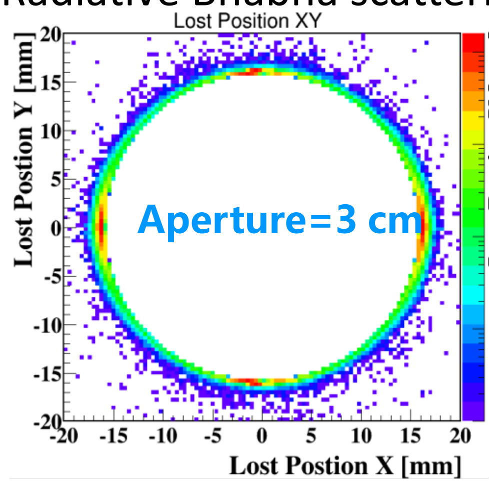


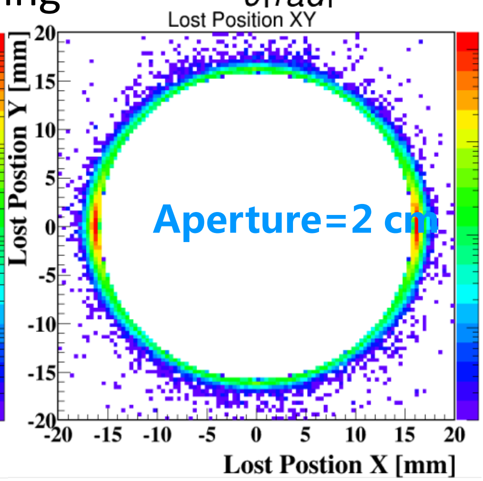


Synchrotron Radiation



Radiative Bhabha scattering





Vertex Detector Requirements

- To achieve high impact parameter resolution as required for heavy flavor (b/c) tagging → $\boldsymbol{H \to b\bar{b}/c\bar{c}/gg}$ branching ratios

$$\sigma_{r\phi} = 5 \oplus 10/p \cdot \sin^{3/2}\theta \ \mu\text{m}$$

- Imposing stringent requirements on the vertex detector
  - Spatial resolution near the interaction point σ_{SP} ~3 μm → high granularity
  - Material budget ≤0.15%X0/layer → monolithic pixel sensor (sensor + embedded electronics, thinned down to e.g. 50 μm) + air cooling (power dissipation ≤50 mW/cm^2, but power-pulsing not optional)
  - Low detector occupancy below 0.5% (empirical)→ high granularity and/or short readout time
  - Radiation tolerance (being updated): ~1 MRad/year (total ionization dose) and 10^{12} n_{eq}/cm^2/year (non-ionization energy loss)

Candidate Technologies

- Monolithic pixel sensor technologies considered:
  - **CMOS**: Ultimate installed for STAR PXL, ALPIDE for ALICE ITS upgrade, technologies pursued by ATLAS for Pixel Phase-II upgrade …
  - **SOI**: actively pursued for X-ray detection, potential issue with radiation tolerance but continuously improved
  - **DEPFET**: Belle-II pixel detector (attractive feature of self-supporting structure with low material budget in the active volume)
  - **3D-IC**: trials within the 3D IC consortium, promising (ultimate detector), technology not mature enough

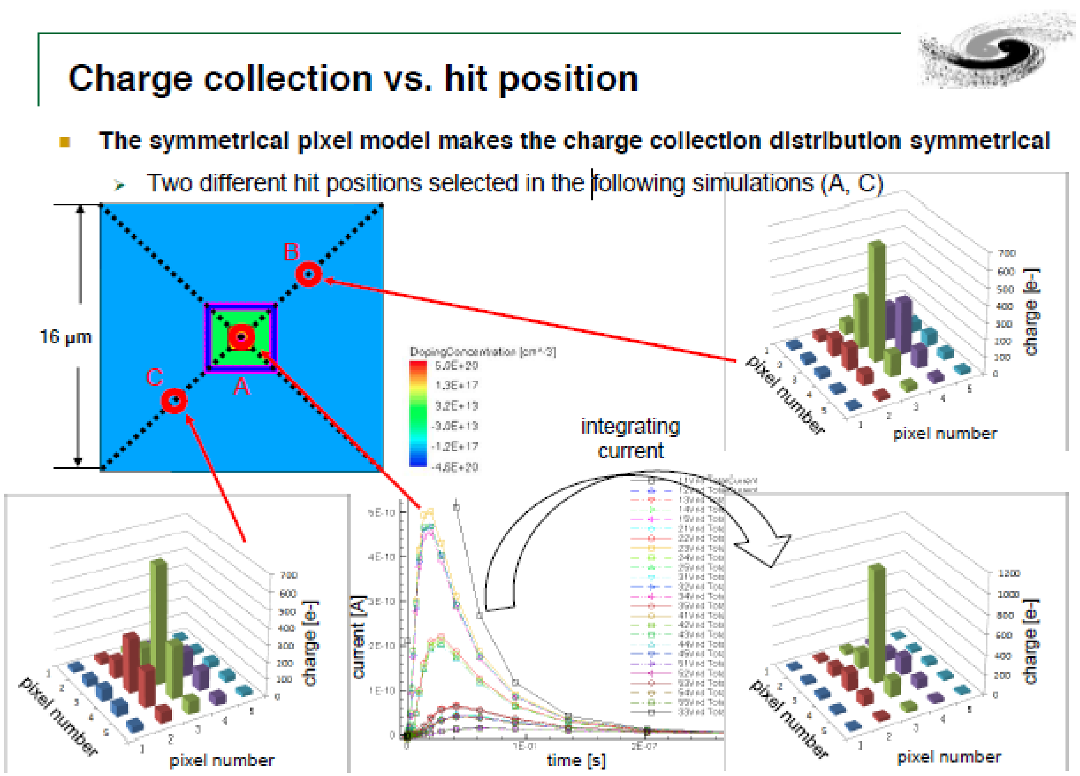
- **CMOS** and **SOI** technologies chosen for initial sensor R&D.

Sensor Design Considerations

- Sensing diode and front-end
  - Spatial resolution
  - Analog power consumption
- Readout architecture
  - Fast readout/time-stamping
  - Digital power consumption
  - Data compression and high-speed transmission
- Radiation tolerance
  - TID
  - NIEL
- Sensor thinning
  - Backside processing

CMOS Pixel Sensor

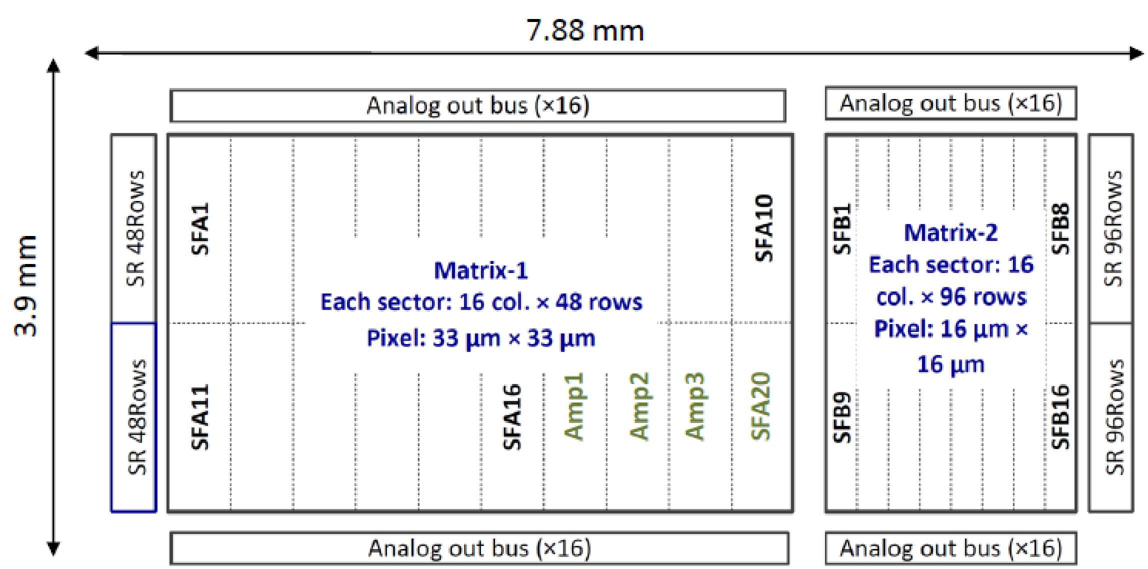
- Important to understand the charge collection efficiency with different diode geometries, epitaxial layer resistivity and thickness, radiation damage … , TCAD simulation followed by measurements → **sensor optimization**



Sector	Diode area	Footprint	Structure
SFB1	3 µm²	20 µm²	2T_nmos
SFB2	4 µm²	20 µm²	2T_nmos
SFB3	8 µm²	20 µm²	2T_nmos
SFB4	3 µm²	15 µm²	2T_nmos
SFB5	4 µm²	15 µm²	2T_nmos
SFB6	8 µm²	15 µm²	2T_nmos
SFB7	3 µm²	11 µm²	2T_nmos
SFB8	4 µm²	11 µm²	2T_nmos
SFB9	8 µm²	11 µm²	2T_nmos
SFB10	3 µm²	8 µm²	2T_nmos
SFB11	4 µm²	8 µm²	2T_nmos
SFB12	8 µm²	8 µm²	2T_nmos
SFB13	8 µm²	20 µm²	2T_pmos
SFB14	4 µm²	8 µm²	2T_pmos
SFB15	8 µm²	20 µm²	3T_nmos
SFB16	4 µm²	8 µm²	3T_nmos

Exploratory Prototype

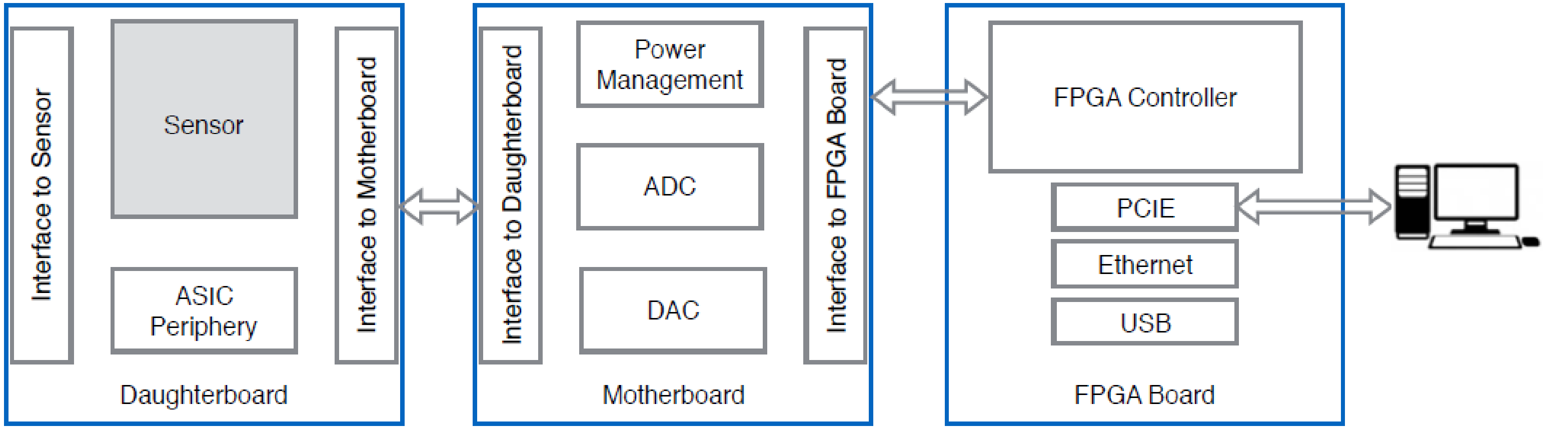
- Goals: sensor optimization and radiation hardness study
- Floorplan overview:
  - Two matrices: Matrix-1 with 33 × 33 μm² pixels (except one sector SFA20 with 16 × 16 μm² pixels), Matrix-2 with 16 × 16 μm² pixels.
  - Matrix-1: 20 sectors, each sector with 48 rows and 16 columns
  - Matrix-2: 16 sectors, each sector with 96 rows and 16 columns



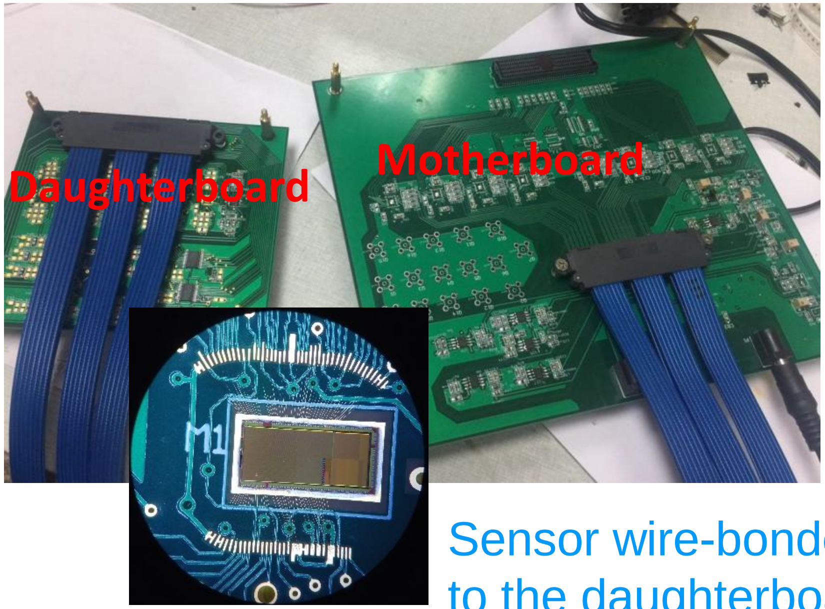
TowerJazz CIS
0.18 μm
November 2015
submission

With lots of help from IPHC

Sensor Characterization



- Low noise data amplifier
- Data acquisition circuit design
- PCIE and data processing
- Additional NI chassis interface



Final tunings of the test system

Sensor wire-bonded to the daughterboard

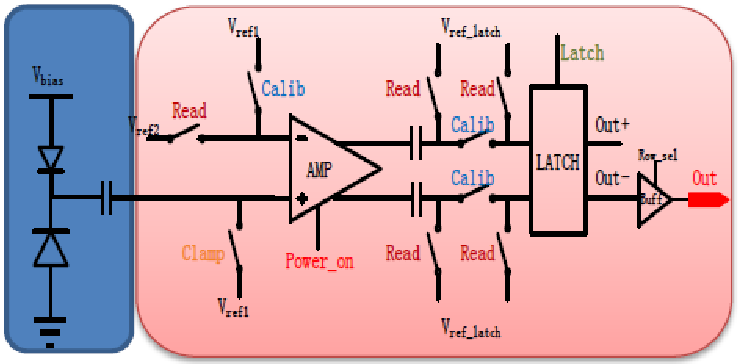
2^{nd} Submission: Digital Readout

Name	Structure	Pixel pitch	Integ.time	Power density	Spatial resolution
MISTRAL (IPHC)	Column-level comparator, Rolling-shutter	22 × 33 (66) μm²	30 μs	200 (100) mW/cm²	≈ 5μm
ASTRAL (IPHC)	In-pixel comparator, Rolling-shutter	24 × 31(IB) μm² 36 x 31 (OB) μm²	20 μs	85 mW/cm² 60 mW/cm²	
ALPIDE (CERN,INFN,CCNU, YONSEI)	In-pixel comparator, In-matrix zero compression readout	27 x 29 μm²	< 4 μs	< 39 mW/cm²	
Attempt	Rolling shutter & AERD	More compact	< 10 μs	< 80 mW/cm²	Higher resolution

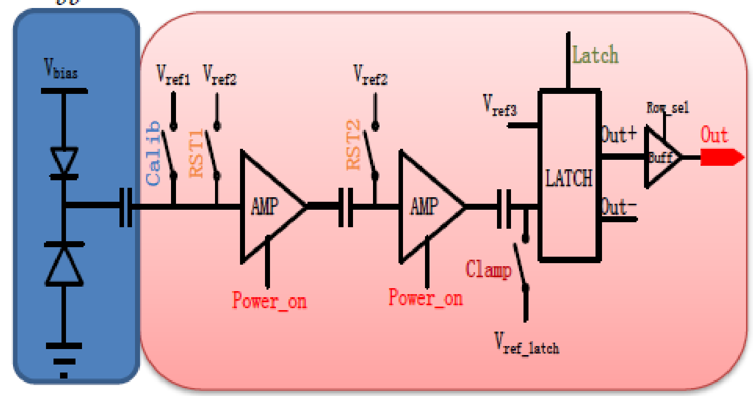
Design I: Rolling Shutter Readout

Yang ZHOU

Digital pixels in rolling-shutter readout mode: *2 different versions*

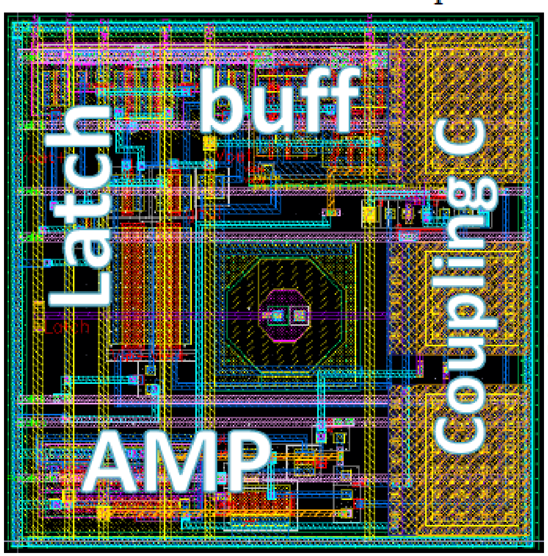


Version 1: differential amplifier + latch



Version 2: two stage CS amplifiers + latch

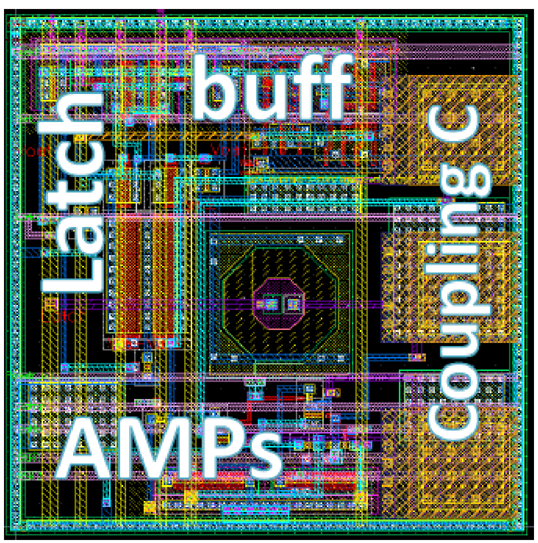
Pitch size: 22 μm



- Same amount of transistors;
- Offset cancellation technique;
- Version 2 has higher signal gain, but suffers "more" from "Latch" input voltage distortion.

Some key parameters in the design:

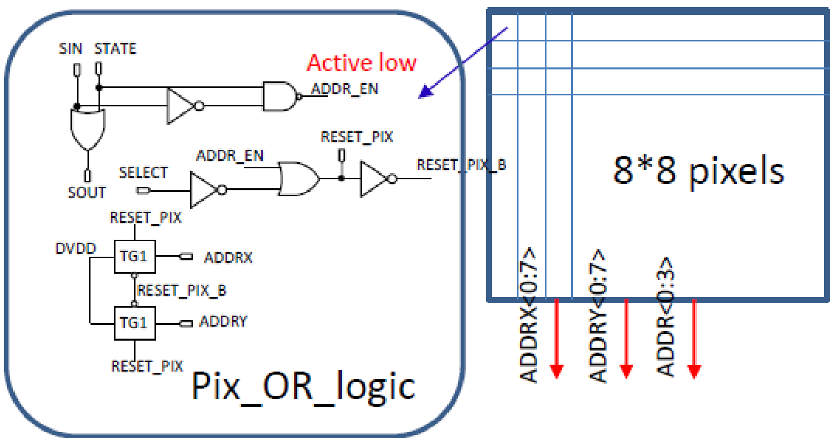
- **Sensing point**
- **AMPs:** noise/gain
- **Latch:** offset
- **Timing:** read out speed



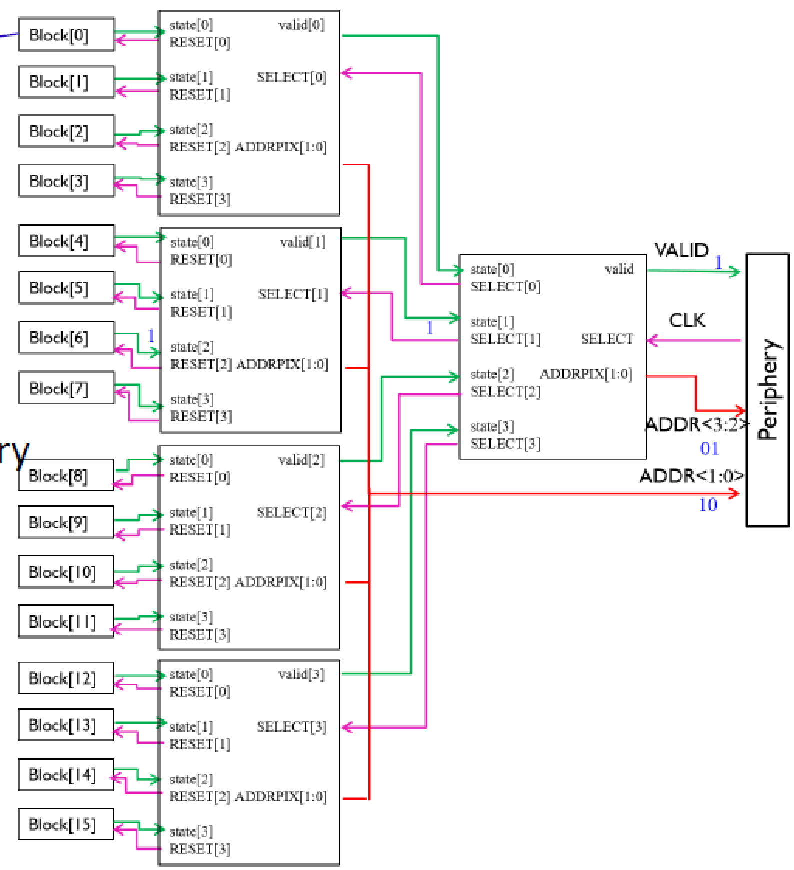
Pitch size: 22 μm

Design II: AERD Readout (MIC4)

Ping Yang



20 address lines to the Periphery



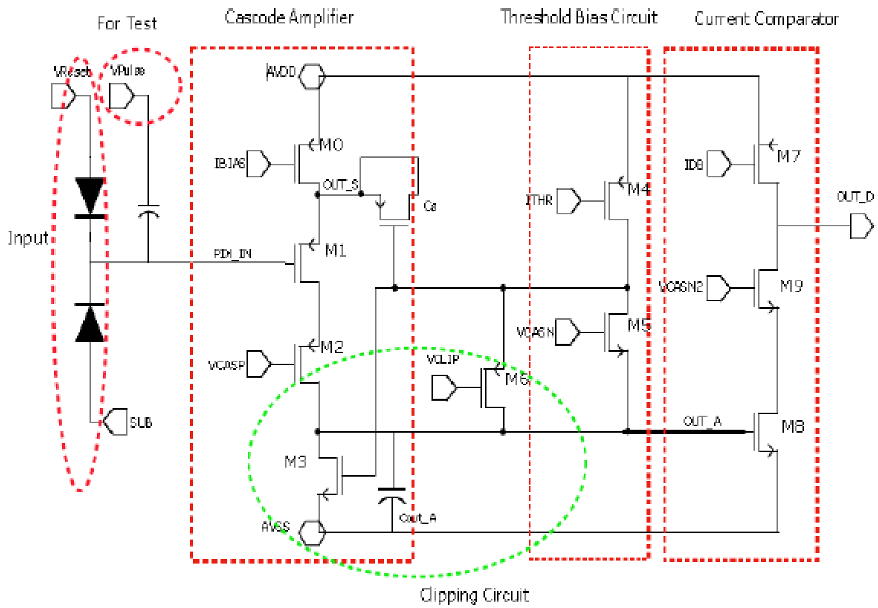
- ALPIDE matrix readout circuit AERD has many connection lines occupy larger area than the logic circuit itself;
- OR gate chain: speed is limited with the number of the chain pixels;
- Combine these two solutions: 64 pixels as a group using OR gate chain, groups using AERD structure to readout

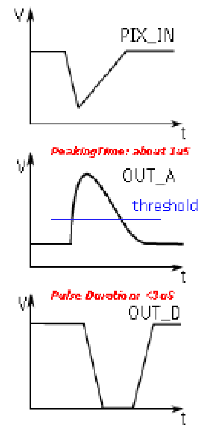
Macro pixel arrays + address lines

MIC4 FE: Current Comparator

Modifications to the FE of the ALPIDE for ALICE ITS Upgrade

Ping Yang





•Signal charge creates negative voltage step ΔV_{PIX_IN} at input node(PIX_IN).

•From OUT_A baseline voltage to point where discriminated output OUT_D flips when $I_{M8} > I_{DB}$.

$$\Delta V_{OUT\_A} \approx \frac{C_s \bullet \Delta V_{PIX\_IN}}{C_{OUT\_A}} = \frac{C_s}{C_{OUT\_A}} \bullet \frac{Q_{in}}{C_{PIX\_IN}}$$

Simulation results

- ENC: 8 e⁻
- Power cons.: 61 nA/pixel
- Threshold: 140 e⁻
- Peaking time < 1 us
- Pulse duration < 3 μs

Charge Sensitive Amplifier

Simple structure with high gain → compact layout

Ying ZHANG

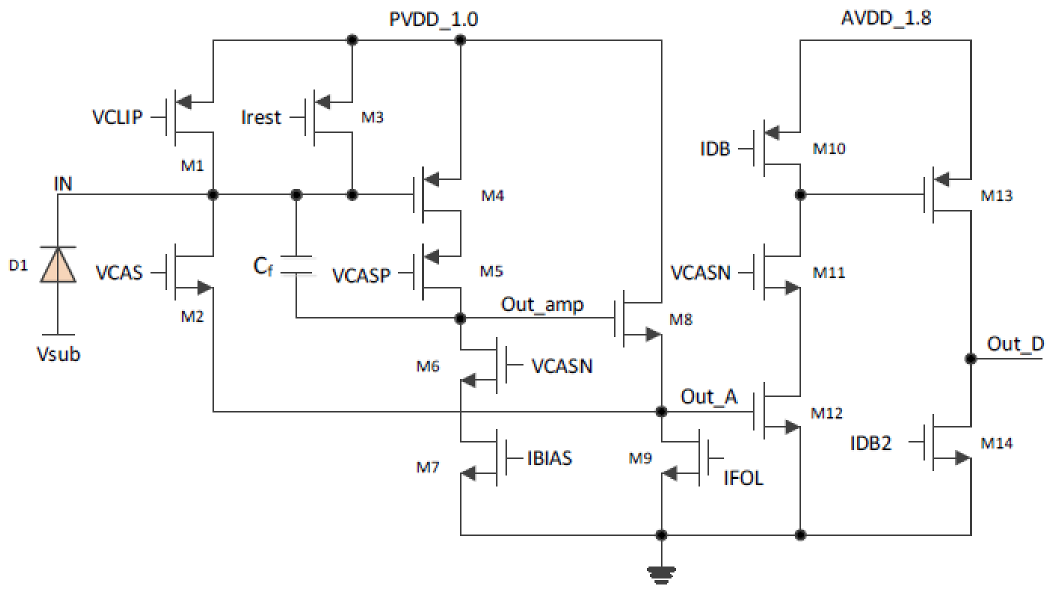
CSA based front-end circuit:

A direct cascode amplifier for the CSA

Simple structure with high gain → for a compact layout

A very low feedback capacitance C_f (0.2 fF) with low mismatch → for a high charge-to-voltage conversion gain, low noise and low mismatch between pixels

A single-end current comparator → for a compact layout

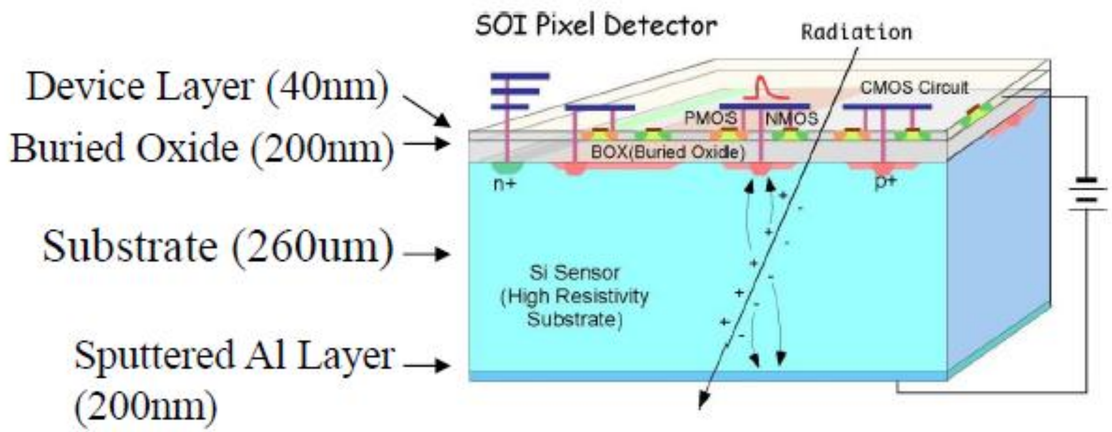


CSA based analog front-end circuit

Simulation results

- ENC: 24 e⁻
- Power cons.: 35 nW/pixel
- Threshold: 145 e⁻
- Peaking time < 550 ns @ Qin < 1.5 ke⁻
- Pulse duration < 8.3 µs @ Qin < 1.5 ke⁻

SOI Pixel Sensor



- LAPIS 0.2µm process
  - Fully depleted CMOS
  - HR substrate
- Early investigation with INTPIX2P5 (2015)
- Compact Pixel for Vertex (CPV)
  - CPV1/2 （2015/2016）
  - Focus on Sensing diode + Front-end

CPV Specifications

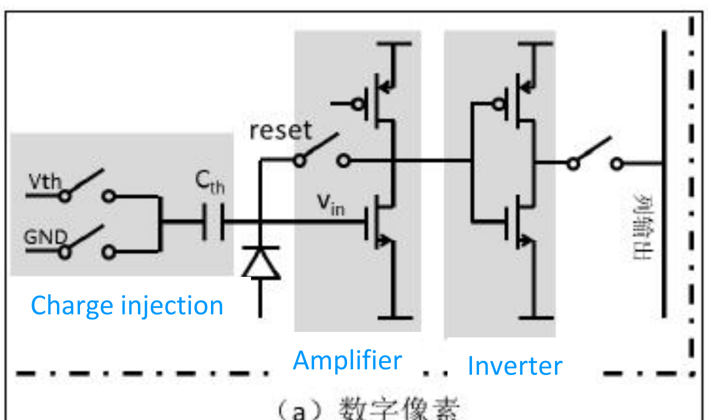
	ASTRAL	ALPIDE	CPV
Process technology	$0.18\ \mu m$ CMOS		0.2 μm SOI
Readout strategy	Rolling shutter	asynchronous	Rolling shutter
Readout time	20 µs	<2 µs	
Power	85 mW/cm^2	39 mW/cm^2	Analog power < 10 mW/cm^2
Pixel size	$22 \times 33\ \mu m^2$	$28 \times 28\ \mu m^2$	$16 \times 16\ \mu m^2$
Spatial resolution	$\approx 5 \mu m$		Expected < 3μm
Total signal for MIP	$\approx 1200\ e^-$ ($20 \mu m$ epi-layer partly depleted)		$\approx 4000\ e^-$ (back thinning to 50μm, fully depleted)

- Unique opportunity to explore very compact pixel circuit
  - 3 times larger MIP signal
  - Possibly smaller cluster size

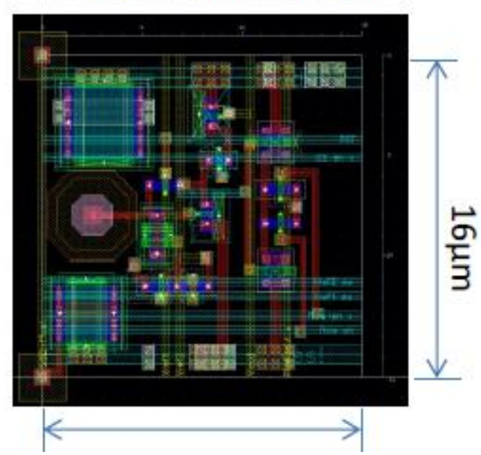
CPV1 Design

- First digital pixel of 16um pitch
- CS voltage amplifier, gain ~ 10
- Inverter as discriminator
- Threshold charge injected to sensing node
- Pixel array: 64*32 (digital) + 64*32 (analog)
- Double-SOI process for shielding and radiation enhancement
- Submitted June, 2015

Yunpeng LU

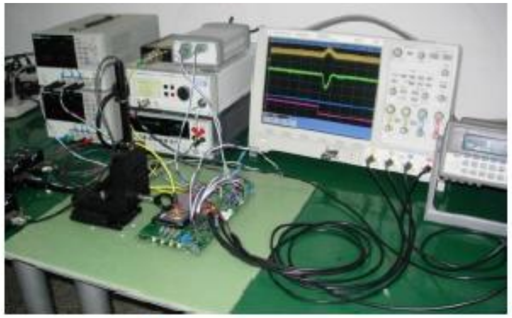


CPV1 digital pixel

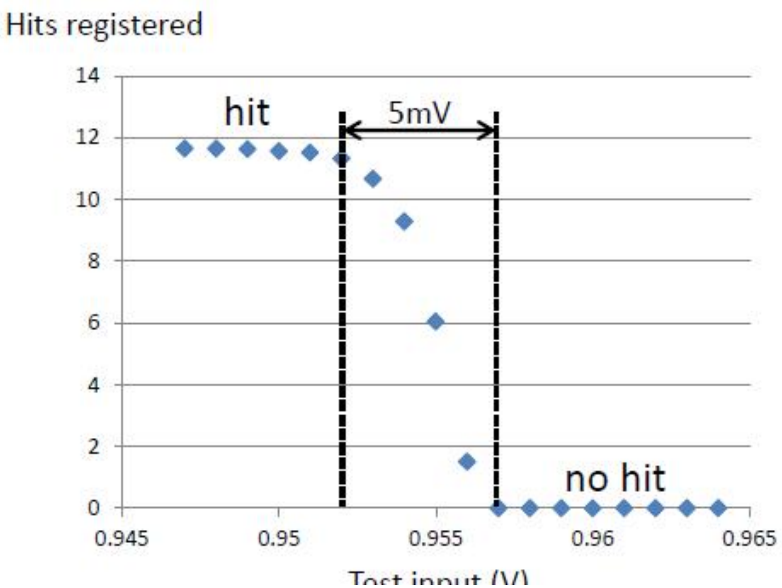


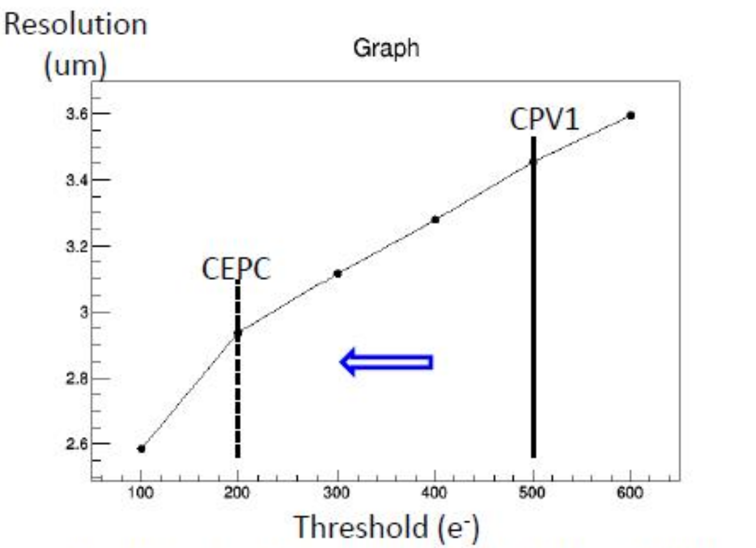
Single Pixel Response

- Chip circuit function verified on single pixel
  - Voltage gain of amplifier ~ 10
  - Threshold scan
  - Temporal noise ~ 50e$^-$ (< 20 e$^-$ expected)
- Bias voltage not applicable due to a design fault
  - Diode capacitance 3 times larger



Yunpeng LU
Zhigang WU





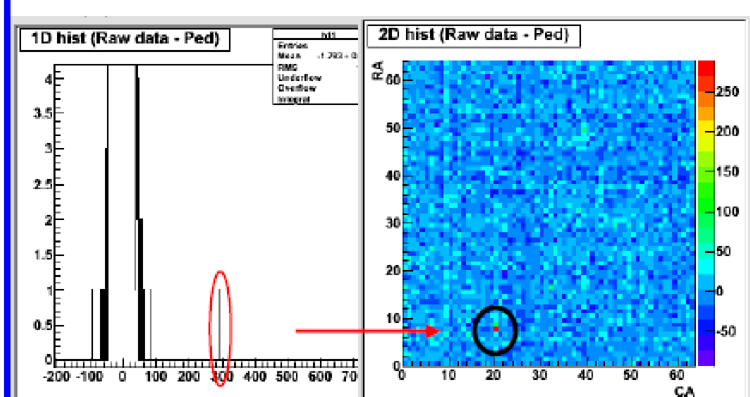
Resolution vs Threshold, Simulation by Z. WU

^{55}Fe Radiative Source Test

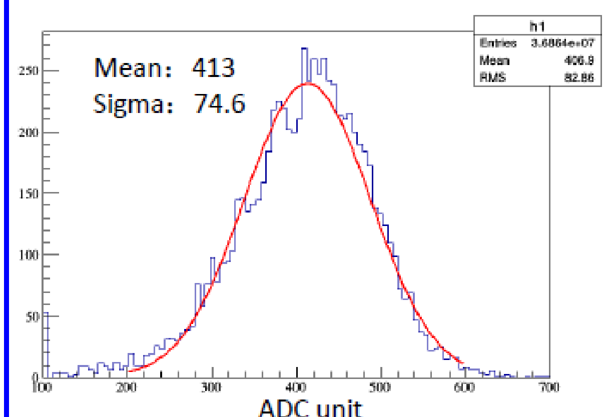
Yunpeng LU
Zhigang WU

- Analog pixel array
  - 5.9keV X-ray photon (1640e⁻);
  - Single photon event clearly visible;
  - Diode capacitance calibrated by using the 5.9 keV peak (3×3 cluster);
  - Average ENC = 47e⁻;
- First proof of principle obtained.
  - Evaluation of digital pixel array is underway.

Analog readout of 5.9keV single X-ray photon



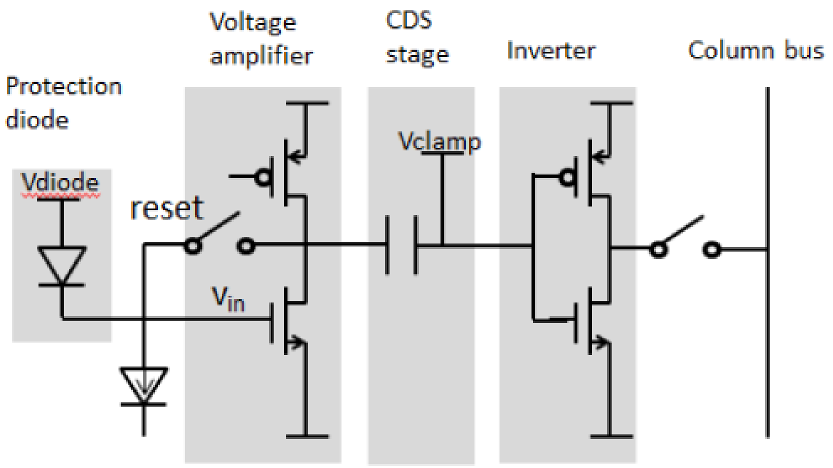
^{55}Fe energy spectrum



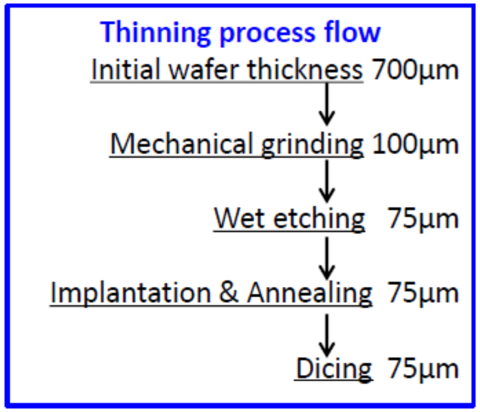
CPV2 Design

Yunpeng LU
Yang ZHOU

- Protection diode added
  - Enable full depletion on sensor
- In-pixel CDS stage inserted
  - improve RTC and FPN noise
  - replace the charge injection threshold
- Submitted June, 2016



Wafer thinning & dicing



Chips expected to be back in May 2017

Summary and Outlook

- Circular Electron Positron Collider (CEPC) proposed to measure precisely Higgs properties and Electroweak parameters
  - Evolving machine design and parameters → **Double Ring as the CDR baseline design**
  - On-going detector design and optimization; **R&Ds on critical detector technologies**
- Stringent requirements on the Vertex Detector; R&D with **CMOS** and **SOI**
  - **Continuous efforts on pixel sensor design and characterization**
  - Optimization of the detector layout, taking into account readout electronics, supporting structure, cooling, powering, etc.
- **International collaboration under discussion …**

BACKUP

CEPC-SppC

- **Phase I: Circular Electron-Positron Collider (CEPC)**
  - **Higgs Factory:** center-of-mass energy ~240 GeV (*ZH* threshold), peak luminosity ~2×10^{34} $cm^{-2}s^{-1}$, 2 interaction points, ~1M clean Higgs events over 10 years → **Higgs precision measurements**
  - Operation at **Z-pole/WW threshold** → **EW precision measurements**

- **Phase II: Super Proton-Proton Collider (SppC)**
  - **Discovery machine,** center-of-mass energy 50 - 100 TeV, peak luminosity~1×10^{35} $cm^{-2}s^{-1}$, 2 interaction points → **Energy frontier for New Physics**
  - Other possible collision modes: ***ep, eA, pA* and *AA***

LEP-LHC Style

CEPC Detector Performance

Table taken from the CEPC Pre-CDR

Table 6.1 Required performance of the CEPC sub-detectors for critical benchmark Higgs processes.

Physics Process	Measured Quantity	Critical Detector	Required Performance
$ZH \to \ell^+\ell^- X$	Higgs mass, cross section	Tracker	$\Delta(1/p_T) \sim 2 \times 10^{-5}$ $\oplus 1 \times 10^{-3}/(p_T \sin\theta)$
$H \to \mu^+\mu^-$	$\mathrm{BR}(H \to \mu^+\mu^-)$		
$H \to b\bar{b},\ c\bar{c},\ gg$	$\mathrm{BR}(H \to b\bar{b},\ c\bar{c},\ gg)$	Vertex	$\sigma_{r\phi} \sim 5 \oplus 10/(p \sin^{3/2}\theta)\ \mu\mathrm{m}$
$H \to q\bar{q},\ VV$	$\mathrm{BR}(H \to q\bar{q},\ VV)$	ECAL, HCAL	$\sigma_E^{\mathrm{jet}}/E \sim 3-4\%$
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\sigma_E \sim 16\%/\sqrt{E} \oplus 1\%\ (\mathrm{GeV})$

- To achieve significant precision improvements compared to previous (LEP) detectors or even current detectors (LHC/HL-LHC) in some aspects ← **driven by Higgs/EW precision measurements**
- **Physics feasibility studies based on the ILD-like detector**, optimization and/or re-design toward lower center-of-mass energies

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$H \to \mu^+\mu^-$	$\mathrm{BR}(H \to \mu^+\mu^-)$		$\oplus 1 \times 10^{-3}/(p_T \sin\theta)$
$H \to b\bar{b},\ c\bar{c},\ gg$	$\mathrm{BR}(H \to b\bar{b},\ c\bar{c},\ gg)$	Vertex	$\sigma_{r\phi} \sim 5 \oplus 10/(p \sin^{3/2}\theta)\ \mu\mathrm{m}$
$H \to q\bar{q},\ VV$	$\mathrm{BR}(H \to q\bar{q},\ VV)$	ECAL, HCAL	$\sigma_E^{\mathrm{jet}}/E \sim 3-4\%$
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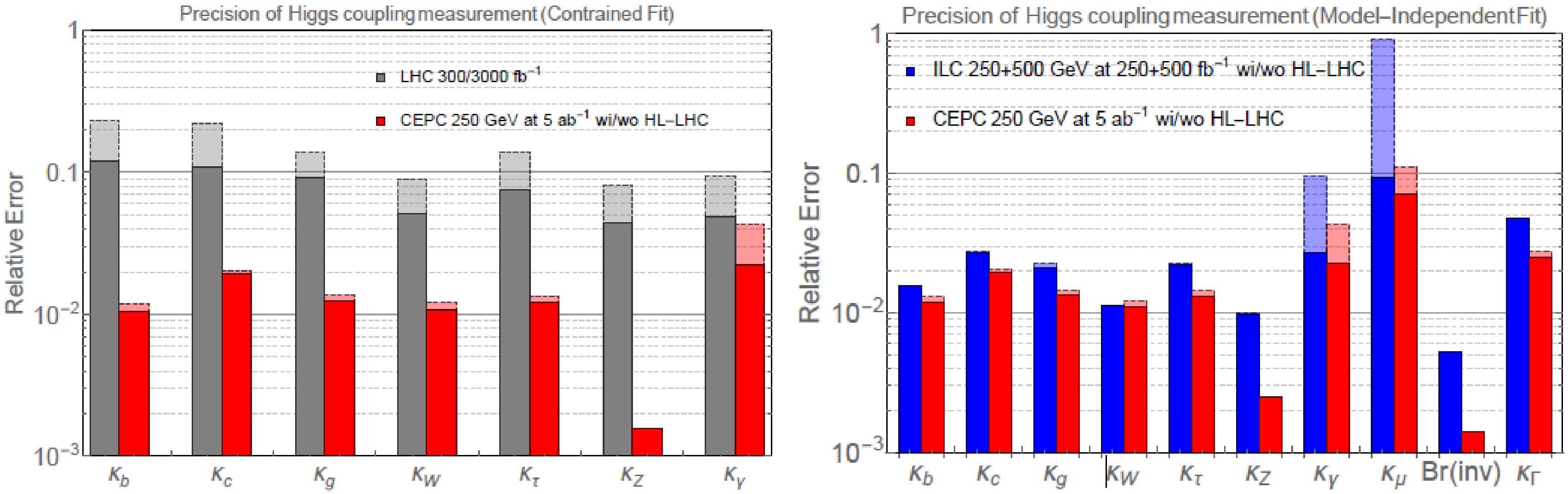
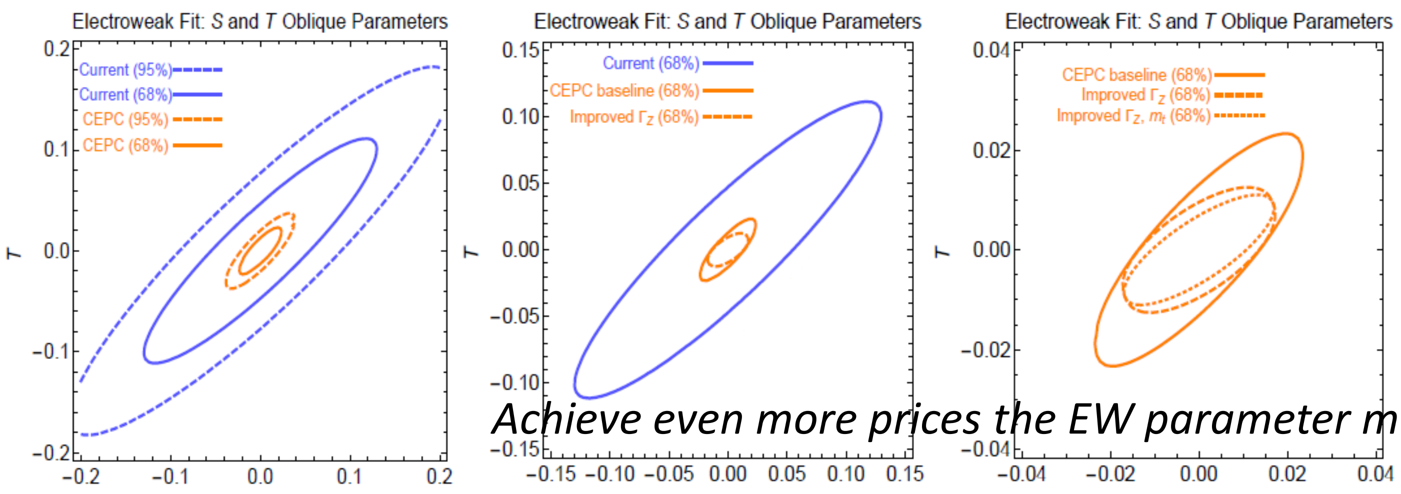
Machine Parameters

	Pre-CDR	H-high lumi.	H-low power	W	Z	
Energy (GeV)	120	120	120	80	45.5	45.5
Circumference (km)	54	100	100	100	100	100
SR loss/turn (GeV)	3.1	1.67	1.67	0.33	0.034	0.034
N_e/bunch (10^{11})	3.79	1.12	1.12	1.05	0.46	0.46
Bunch number	50	555	333	1000	16666	65716
SR power /beam (MW)	51.7	**50**	**30**	16.7	12.7	50
β_{IP} x/y (m)	0.8/0.0012	0.3/0.001	0.3/0.001	0.1 /0.001	0.12/0.001	0.12/0.001
Emittance x/y (nm)	6.12/0.018	1.01/0.0031	1.01/0.0031	2.68/0.008	0.93/0.0049	0.93/0.0049
ξ_x/ξ_y/IP	0.118/0.083	0.029	0.029	0.0082/0.055	0.0075/0.054	0.0075/0.054
RF Phase (degree)	153.0	0.083	0.083	149	160.8	160.8
V_{RF} (GV)	6.87	**2.0**	**2.0**	**0.63**	**0.11**	**0.11**
f_{RF} (MHz) (harmonic)	650	650	650	650 (217800)	650 (217800)	
Nature σ_z (mm)	2.14	**2.72**	**2.72**	**3.8**	**3.93**	**3.93**
Total σ_z (mm)	2.65	2.9	2.9	3.9	4.0	4.0
HOM power/cavity (kw)	3.6 (5cell)	0.75(2cell)	0.45(2cell)	1.0 (2cell)	1.6(1cell)	6.25(1cell)
Energy acceptance (%)	2	1.5	1.5			
Energy acceptance by RF (%)	6	1.8	1.8	1.5	1.1	1.1
Life time due to beamstrahlung_cal (minute)	47	52	52			
L_{max}/IP (10^{34}cm^{-2}s^{-1})	2.04	5.42	3.25	4.08	18.0	70.97

Physics Program

Deepen the understanding of the Higgs properties





Achieve even more prices the EW parameter measurements

Project Timeline

CEPC

1st Milestone: pre-CDR (by the end of 2014) → R&D funding request to Chinese government in 2015

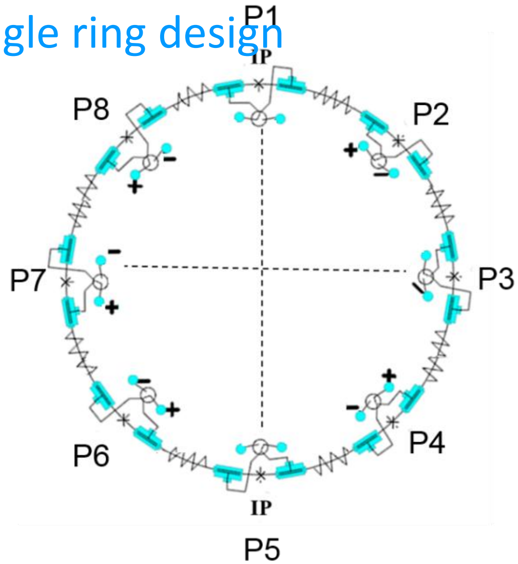
2nd Milestone: R&D funding from MOST (in Mid 2016); 3rd Milestone: CEPC Status Report (by the end of 2016); 4th Milestone: CEPC CDR Report (by the end of 2017); 5th Milestone: CEPC TDR Report and Proto (by the end of 2022); 6th Milestone: CEPC construction (by the end of 2030)

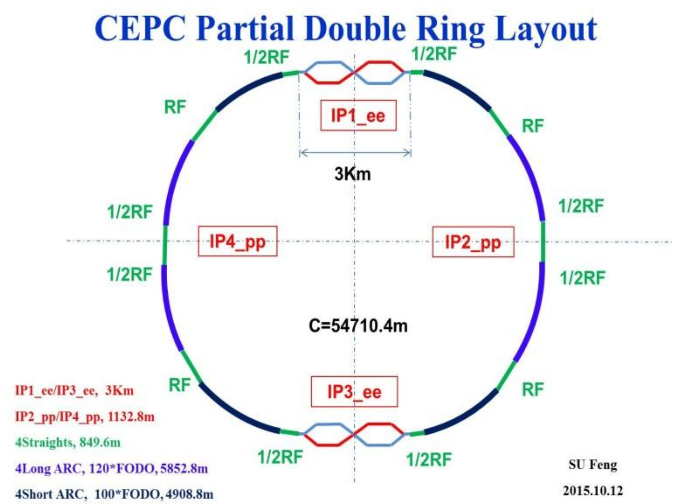
SppC

R&D program on High Temperature Superconducting magnets (HTS)

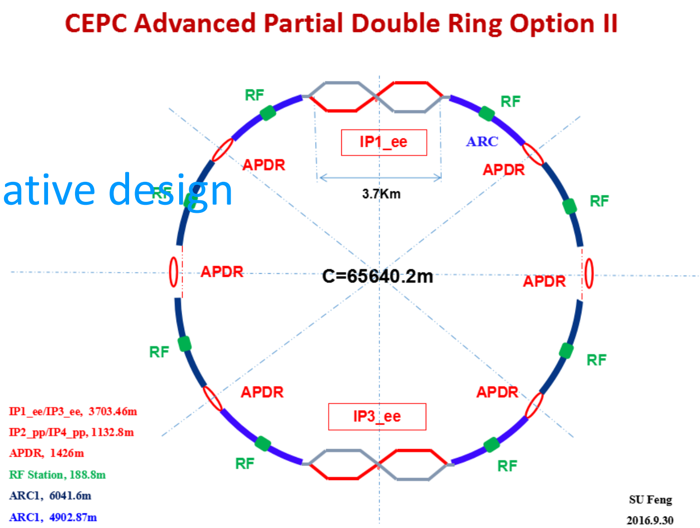
Machine Design Evolution

Pre-CDR single ring design

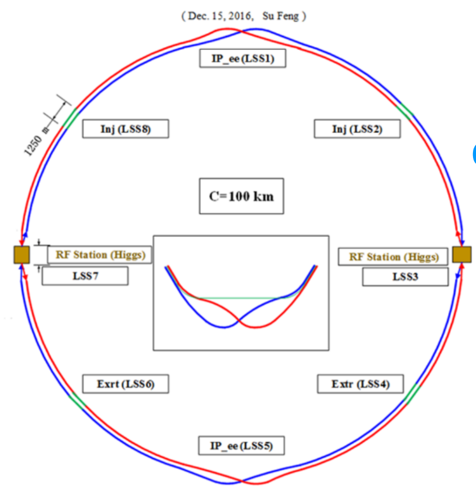




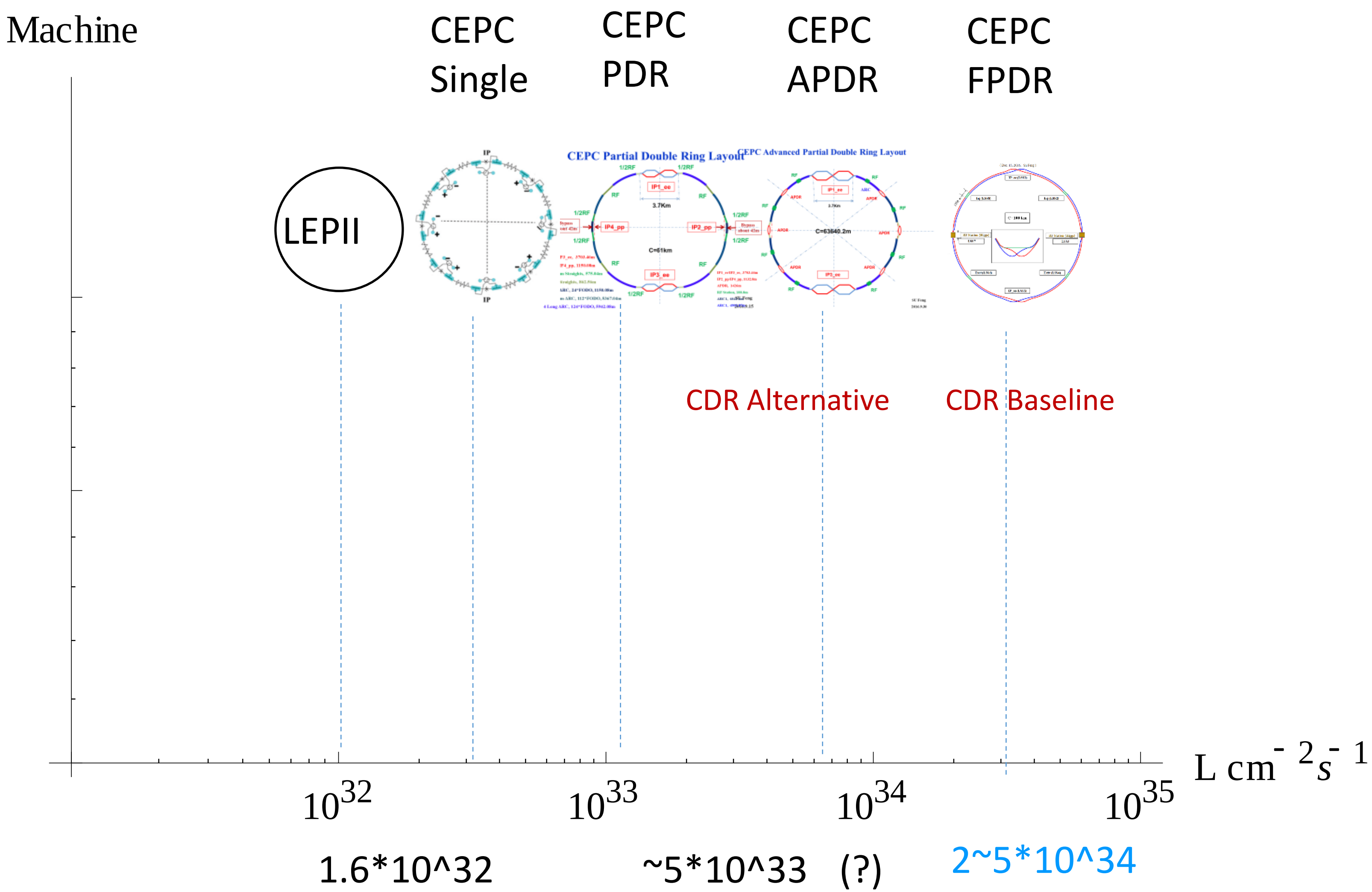
Alternative design



CDR baseline double ring design



Luminosity Potentials

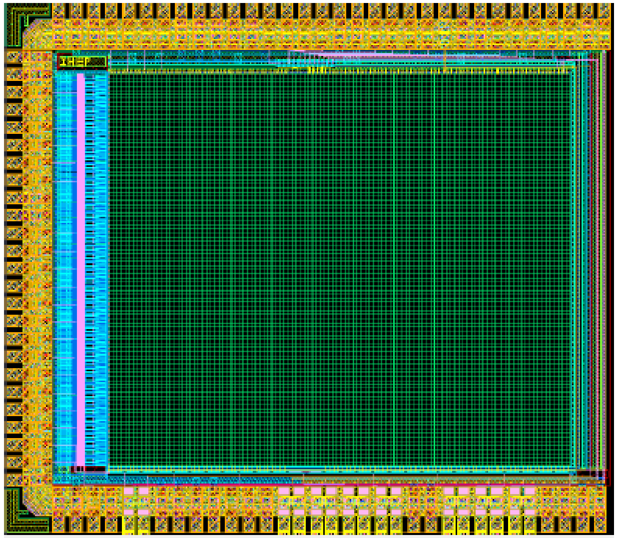


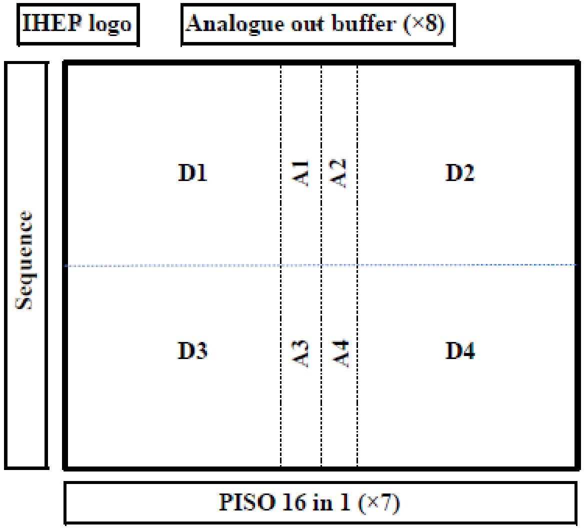
Machine Parameters

	Pre-CDR	H-high lumi.	H-low power	W	Z	
Energy (GeV)	120	120	120	80	45.5	45.5
Circumference (km)	54	100	100	100	100	100
SR loss/turn (GeV)	3.1	1.67	1.67	0.33	0.034	0.034
N_e/bunch (10^{11})	3.79	1.12	1.12	1.05	0.46	0.46
Bunch number	50	555	333	1000	16666	65716
SR power /beam (MW)	51.7	**50**	**30**	16.7	12.7	50
β_{IP} x/y (m)	0.8/0.0012	0.3/0.001	0.3/0.001	0.1 /0.001	0.12/0.001	0.12/0.001
Emittance x/y (nm)	6.12/0.018	1.01/0.0031	1.01/0.0031	2.68/0.008	0.93/0.0049	0.93/0.0049
ξ_x/ξ_y/IP	0.118/0.083	0.029	0.029	0.0082/0.055	0.0075/0.054	0.0075/0.054
RF Phase (degree)	153.0	0.083	0.083	149	160.8	160.8
V_{RF} (GV)	6.87	**2.0**	**2.0**	**0.63**	**0.11**	**0.11**
f_{RF} (MHz) (harmonic)	650	650	650	650 (217800)	650 (217800)	
Nature σ_z (mm)	2.14	**2.72**	**2.72**	**3.8**	**3.93**	**3.93**
Total σ_z (mm)	2.65	2.9	2.9	3.9	4.0	4.0
HOM power/cavity (kw)	3.6 (5cell)	0.75(2cell)	0.45(2cell)	1.0 (2cell)	1.6(1cell)	6.25(1cell)
Energy acceptance (%)	2	1.5	1.5			
Energy acceptance by RF (%)	6	1.8	1.8	1.5	1.1	1.1
Life time due to beamstrahlung_cal (minute)	47	52	52			
L_{max}/IP ($10^{34}cm^{-2}s^{-1}$)	2.04	5.42	3.25	4.08	18.0	70.97

Rolling Shutter Readout

Yang ZHOU

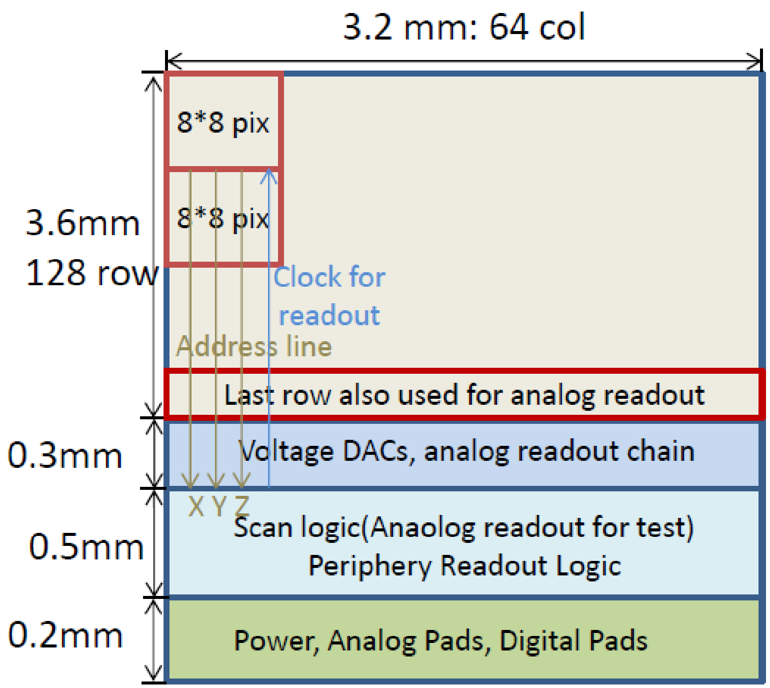




- *3 × 3.3 mm^2;*
- *96 × 112 pixels with 8 sub-matrix*
- Processing speed: 11.2 μs/frame for 100 ns/row;
- Output data speed: 160 MHz;
- Power:3.7 μA/pixel;

MIC4 Layout

Ping Yang



MIC4 Chip:

- *3.2 × 3.7 mm²;*
- *128 × 64 pixels*
- Integration time < 5 μs
- Speed: 40 MHz/pixel
- Power: <80 mV/cm²;

Chip periphery:

- *Band Gap*
- *Voltage DAC*
- *Current DAC*
- *LVDS*
- *Custom designed PADs*

MPW submission in May 2017