US Effort in the Phase II Upgrade of the ATLAS Muon Spectrometer

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Upgrades to the muon spectrometer are required to handle increased rates and fakes associated with HL-LHC luminosities ($\sim 7 \times 10^{34}$ cm$^{-2}$s$^{-1}$).

**Phase-1 Upgrade (LS2 ~ 2018): New Small Wheel**

**Phase-2 Upgrade (LS3 ~ 2023): Replace Tracking and Trigger Readout Electronics**
Muon Spectrometer (r-z)

- Thin-Gap Chambers (TGC) \textit{triggering}
- Resistive Plate Chambers (RPC) \textit{triggering}
- Monitored Drift Tubes (MDT) \textit{precision readout}

- End Cap Toroid
Muon Spectrometer (r-z)

- Resistive Plate Chambers (RPC) triggering
- Thin-Gap Chambers (TGC) triggering
- End Cap Toroid
- Monitored Drift Tubes (MDT) precision readout
Muon Spectrometer (r-z)

- Thin-Gap Chambers (TGC) triggering
- Resistive Plate Chambers (RPC) triggering
- Monitored Drift Tubes (MDT) precision readout

Graph: Efficiency vs. $p_T^{\text{offline}}$ [GeV]
- L1_MU20
- Angle method
- 3-point method
Example: Higgs $\to 4\mu$

$H \to ZZ^* \to 4\mu$

$m_H = 125$ GeV/c$^2$

- lowest $p_T$ muon
- highest $p_T$ muon

Number of events

$p_T^\mu$ [GeV/c]
US Scope: MDT Electronics and sMDT Detectors
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BI Upgrade ➔ sMDT + RPC’s

Thin-Gap Chambers (TGC) triggering
Resistive Plate Chambers (RPC) triggering
Monitor Drift Tubes (MDT) precision readout

End Cap Toroid

Efficiency

65% ➔ 94% Efficiency
sMDT Detectors

Thin-Gap Chambers (TGC) triggering
Resistive Plate Chambers (RPC) triggering
Monitored Drift Tubes (M precision readout)
End Cap Toroid
sMDT Detectors
Preparing for Construction

• **Using FARO Laser Tracker** - time of flight measurement using laser retroflection from a precision machined ball.

• **sMDT assembly requires 2.5m x 2.5m granite table**

For 5000 points taken
Flatness ~ 20 um
sMDT Assembly Dry Run

- Set up precision jigging on granite table
- Assemble prototype chamber with ‘mock up’ tubes
- Measure tube position precision
Diagram of the proposed system architecture for the MDT trigger and readout is shown below (See TDR for more details).

1. TDC receives discriminated signals from three ASD’s, creates a time stamp for leading and trailing edges, and forwards this information to the CSM.

2. CSM broadcasts hit timing information from up to 18 TDC’s to the L0MDT board, and provides TTC information to the mezzanine cards.

3. Within the L0MDT, segment-finding and track-fitting algorithms are performed on reduced resolution hits for trigger processing. The full resolution hits are sent to FELIX if a L0 Accept signal is received.
MDT Electronics in Phase II

Sector Logic

L0MDT

CSM

TDC

ASD

MDT Tubes

Track 4-Vector

RPC/TGC ROI

L0 Accept

Full Resolution Hits Sent On L0 Accept

Hits

TTC

Hits

TTC

FELIX
• CSM broadcasts hit timing information from up to 18 TDC’s to the L0MDT board, and provides TTC information to the mezzanine cards.

• Some Design Requirements:
  • Input bandwidth - 18 Mezzanine Cards @ 320 Mbps per card using existing cables/motherboards
  • Output bandwidth - 3 fibers @ 4.8 Gbps per fiber
  • Optimize for minimal latency, low power consumption, and cost/risk
  • Work with old mezzanine cards
CSM Design Choices

FPGA-Based CSM

• Key component - FPGA with enough I/O to handle all 18 mezzanine cards at 320 Mbps
• Tx which can send out data @ 4.8 Gbps on 3 fibers
• Generate calibration pulses, encoded reset, fan-out JTAG to mezzo

• Design Advantages
  • Flexibility in FPGA firmware

• Design Complications
  • Uncertainty about FPGA SEU performance in Phase II
  • Need to maintain firmware

GBTx-Based CSM

• Utilizes three GBTx chips - one master and two slave.
• GBT-SCA will perform configuration and monitoring.
• Small service chip (asic) needed to interface with current mezzanine and fan out JTAG signals from GBT-SCA.

• Design Advantages
  • Low cost, low power, rad hard ASIC’s from CERN
  • No firmware design/maintenance needed.

• Design Complications
  • Functionality fixed by GBTx chipset
  • Small additional chip needed for JTAG distribution
• Implementing FPGA-CSM in a Xilinx AC701 evaluation board.

• Used ‘simulated’ TDC signals to show very low error rate (BER < 7.8E-14) and measure latency (simulated = measured, 234 ns).

• Can interface the FPGA-CSM with a new hybrid mezzanine card (old ASD’s w/ new TDC) which was built & tested by Boston University.

• Successfully interfaced three mezzanine with the new TDC to the FPGA-based CSM (we only have 3).
GBTx-based CSM Prototype v1

- Demonstrated running GBTx on VLDB evaluation board (top right picture).
  - Able to loop back data between GBTx and an FPGA with the GBT code.
  - Receive required 80/160/320 MHz clocks from GBTx clock manager.

- First prototype in development
  - Design utilizes three GBTx, one master and two slave (bottom right picture).
  - Service chip for JTAG distribution is an FPGA
GBTx-based CSM Prototype v1

FEAST POWER

Input Connector 140Pin

GBTX

GBT-SCA

“Service” FPGA

VTTX

VTRX

Input Connector 140Pin

Elink Test Conn.
Service Chip for GBTx-CSM

- Service ASIC is required for GBTx-based CSM to provide JTAG signals to the mezzanine and check if mezzanines are online and operational.

- Critical component for GBTx-based CSM.

- Project led by Michigan Postdoc Allison McCarn Deiana

- Firmware developed using an Artix-7 evaluation board

- Successfully identifying mezzanine cards

- Will be integrated into CSM prototype v1.
We are here... AT CERN

First mock chamber soon -

First prototypes soon -
Backup
Getting to 3000 fb\(^{-1}\)

To cope with high rates at HL-LHC

- The readout electronics of the MDT system must be replaced, as well as the barrel (RPC) and end-cap (TGC) triggering system.

To reduce fakes & improve trigger efficiency

- Integrate MDT info at Level-0 to improve \(p_T\) selectivity of tracks.
- To reduce fakes at high \(\eta\) (2 < |\(\eta\)| < 2.4), new sTGC’s will be installed in the inner ring of the big wheel.
- RPC and sMDT chambers will replace current MDT chambers in the inner barrel to allow for a 3-station MDT trigger.
Readout electronics must be able to handle 300 kHz/tube hit rate and a 1 MHz trigger, which is not possible in the current system.
Adding RPC/MDT detectors to the inner barrel will allow for three-station triggering. This will improve trigger efficiency from 65 to 95% at the HL-LHC.
Example: Higgs $\rightarrow 4\mu$

- Precision measurements in all channels needed to study small differences in the rate of Higgs boson production.

- The measurement precision of the $h\rightarrow 4\mu$ rate is driven by statistics (event acceptance).

- Without the HL-LHC upgrade, we cannot handle the increased trigger rates, and therefore can’t maintain the single muon $p_T$ threshold of 20 GeV.

- Raising the trigger threshold to 40 GeV, would decrease the $h\rightarrow 4\mu$ acceptance by factor of $\sim$2.
Monitored Drift Tubes (MDT)

- good space resolution ($\sim 100 \, \mu m$ per point) →
  - $\Delta p_t/p_t \approx 2-3\%$ @ $p_t < 200 GeV/c$
  - $\Delta p_t/p_t \approx 10\%$ @ $p_t \approx 1 TeV/c$

<table>
<thead>
<tr>
<th>Tubes per layer</th>
<th>BIL</th>
<th>BML</th>
<th>BOL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer per multilayer</td>
<td>24 o 36</td>
<td>56</td>
<td>72</td>
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<tr>
<td>Chamber length (mm)</td>
<td>1200</td>
<td>1680</td>
<td>2160</td>
</tr>
<tr>
<td>Chamber height (mm)</td>
<td>170</td>
<td>317</td>
<td>317</td>
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Monitored Drift Tubes (MDT)
FPGA-based CSM Design

- Key component is an FPGA with enough I/O to handle all 18 mezzanine cards at 320 Mbps
- Data processing with GBTx format FIFO
- Tx which can send out data @ 4.8 Gbps on 3 fibers
- Generate calibration pulses, encoded rest, fan-out JTAG information to mezzo

- Design Advantages
  - Flexibility in FPGA firmware design - for example, it will be easier to interface with any old mezzanine cards that cannot be replaced in Phase II
  - Can easily handle migration from Phase I triggered mode to phase II trigger-less

- Design Complications
  - Uncertainty about FPGA SEU performance in Phase II
  - Maintenance needed for firmware
GBTx-based CSM Design

- Based on three GBTx chips.

- Each GBTx chip:
  - Can utilize a maximum of 14 E-links at 320 Mbps.
  - 4.8 Gbps bi-directional output link.
  - Built-in clock manager.

- GBT-SCA will perform configuration and monitoring.

- Small service chip (asic) needed to interface with current mezzanine and fan out JTAG signals from GBT-SCA. Currently prototyping this with an FPGA.

- **Design Advantages**
  - Low cost, low power, radiation hard ASIC's from CERN
  - No firmware design/maintenance needed.

- **Design Complications**
  - Functionality fixed by GBTx chipset
  - Small additional chip needed for JTAG distribution
• Master GBTx:
  • Connected to VTRx. Responsible for 1 downlink (control) and 1 uplink (readout).
  • EC channel + 80 E-link connected with GBT-SCA.
  • Recover clock through downlink and distribute it to slave GBTx.

• Two Slave GBTx:
  • Connected with VTTx. Responsible for 2 uplinks (transmitter mode).
  • Controlled by the GBT-SCA I2C master serial bus.

• Four GBT-SCA:
  • Controlled via Master GBTx by 80 Mbps E-links.
  • Configures GBTx via I2C channels.
  • Monitoring all temperature, voltage information from 18 mezzanines.

• Service FPGA: JTAG fanout for Mezzanine and generates calibration pulses. Performs encoded reset.

• Power: FEAST ASIC Chips
Predicting Latency for the FE

- Adding worst case latency for each component
- A TDC multiplexer cut at 14 ticks gives 0.5% hit loss at 400 kHz/tube
- Deadtime cut at 800ns in 30mm tubes gives 24% hit loss at 400 kHz/tube

🌟 NOTE: GBT latency quoted in 2013 presentation is 254 ns but includes receiver time in FPGA - we assume this is roughly 90 ns and moved it from the GBTx CSM fixed latency to deserialization after the fiber.
On track to have both demonstrators evaluated by the end of October.