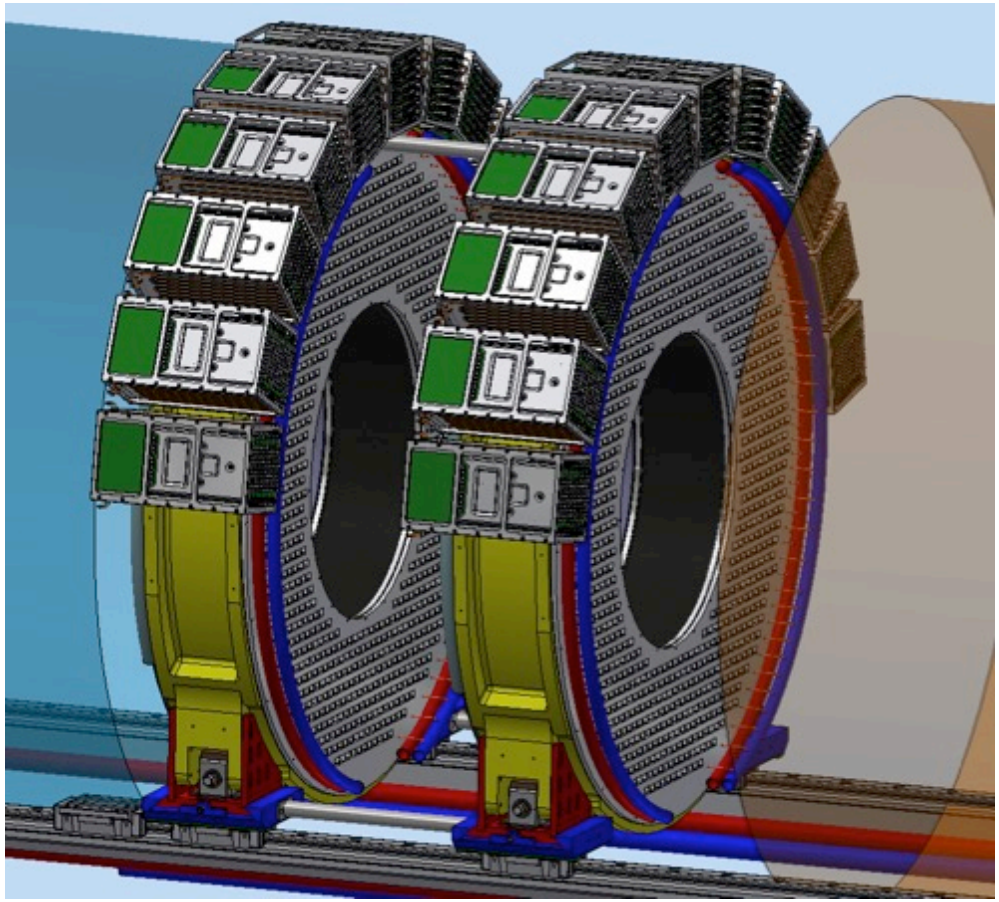
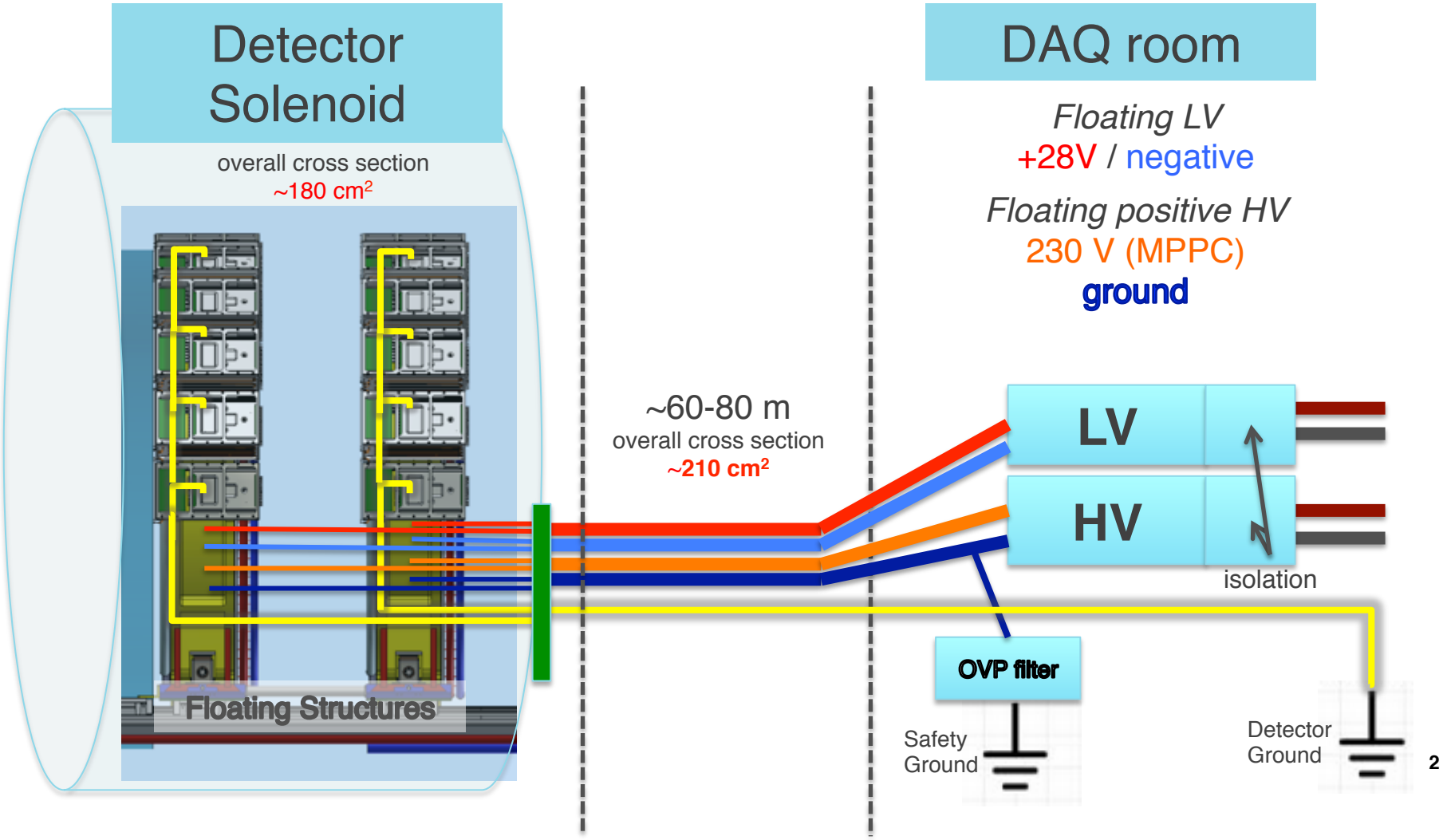
Mu2e Calorimeter

~ 680 CsI crystals (Square, side: 34 mm) for the first disk
~ 680 CsI crystals (Square, side: 34 mm) for the second disk
~ 1360*2 = 2720 SiPM photo-sensors

- 20 FADC channels per board
- 6/7 boards per crate
- 11 crates per the first disk
- 11 crates per the second disk

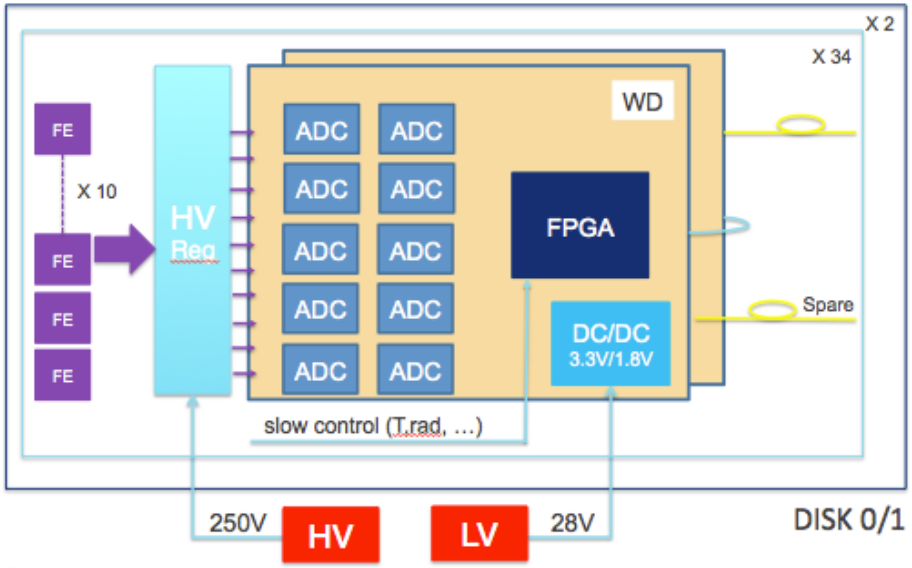


Calorimeter routing



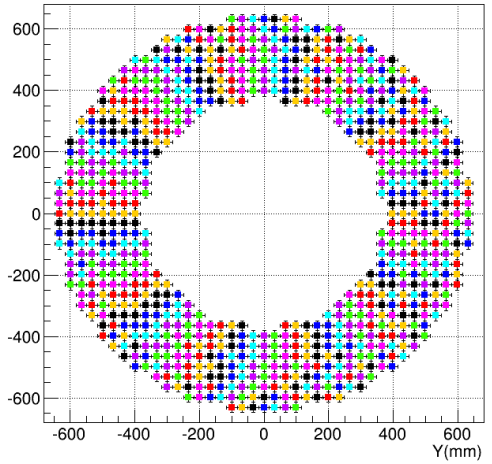
INSIDE the DS - Calorimeter Electronics Scheme

Overview of the calorimeter readout electronics:
each disk (~ 680 crystals per disk) is subdivided into 34 groups of 20 crystals.

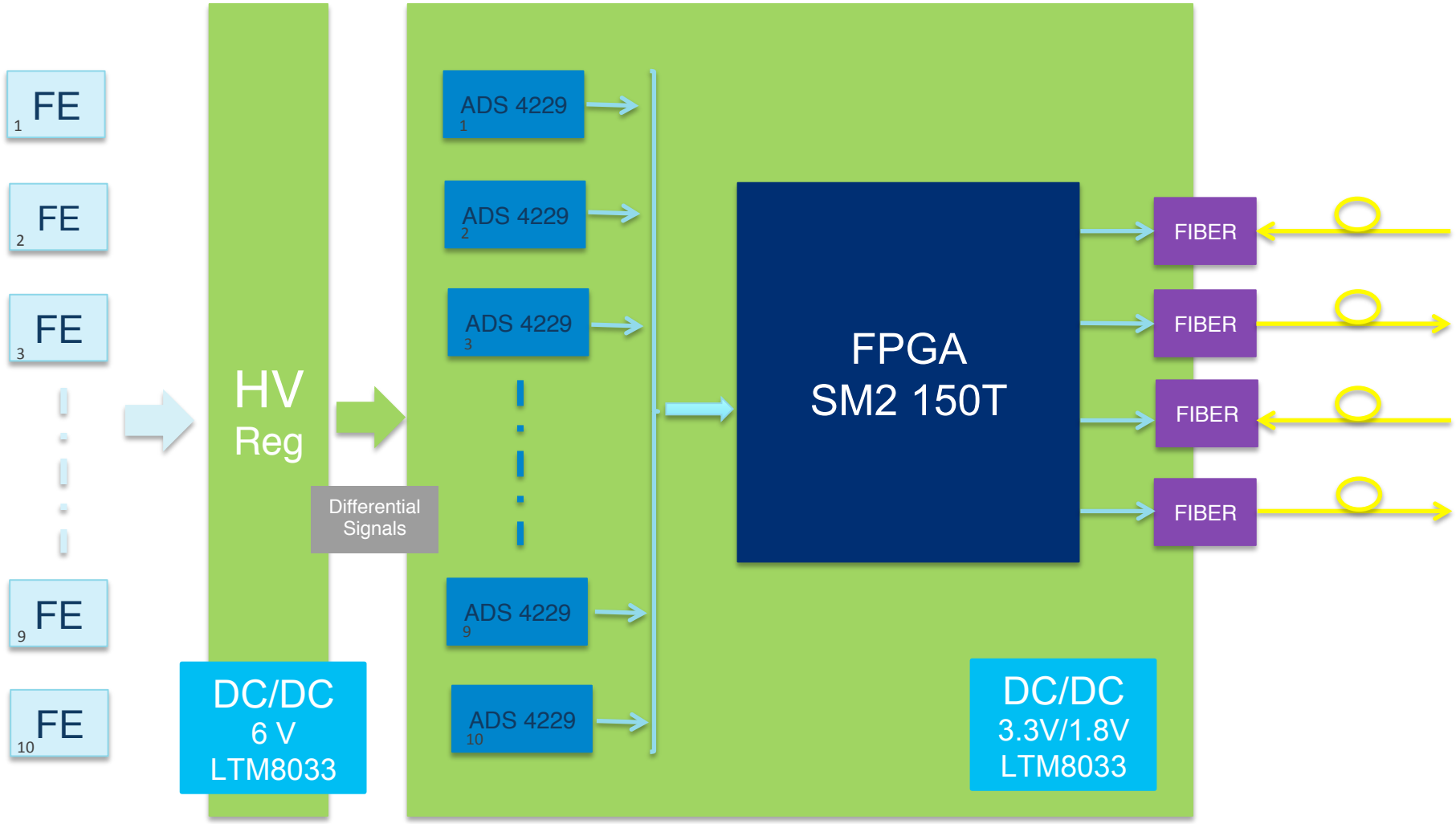


– Groups of 20 left (right) Amp-HV chips, controlled by a dedicated mezzanine board that distributes the LV and the HV reference value, while setting and reading back the locally regulated voltage

– Groups of 20 amplified signals are sent to a digitizer module where they are sampled and processed before being optically transferred to the DAQ system.

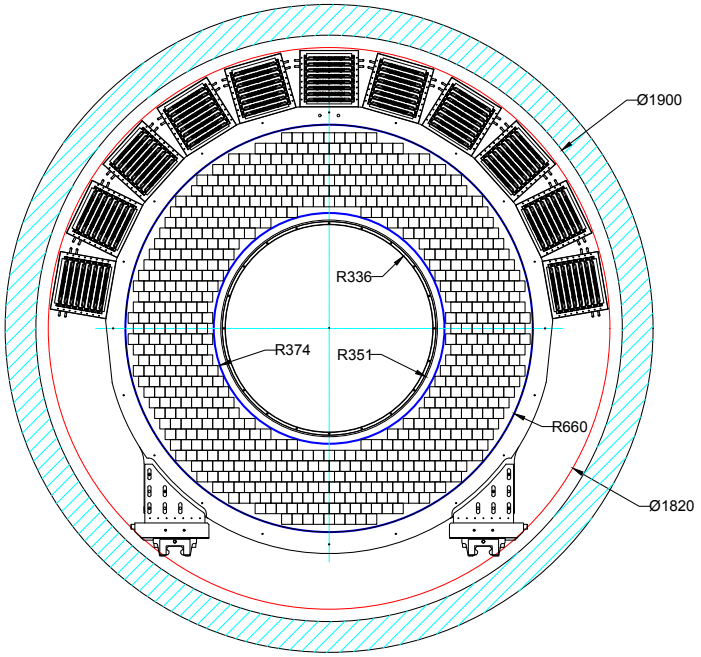


WD block diagram

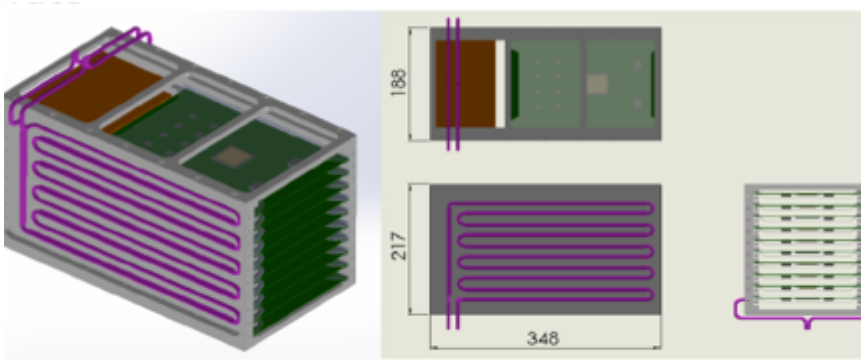


Calorimeter Crates

- There are therefore 11 crates per disk, hosting 6/7 sets of AMP-HV and WFD boards;
- The crates are placed in the outermost region of each disk;
- The crates are designed to provide heat dissipation for the electronics boards.

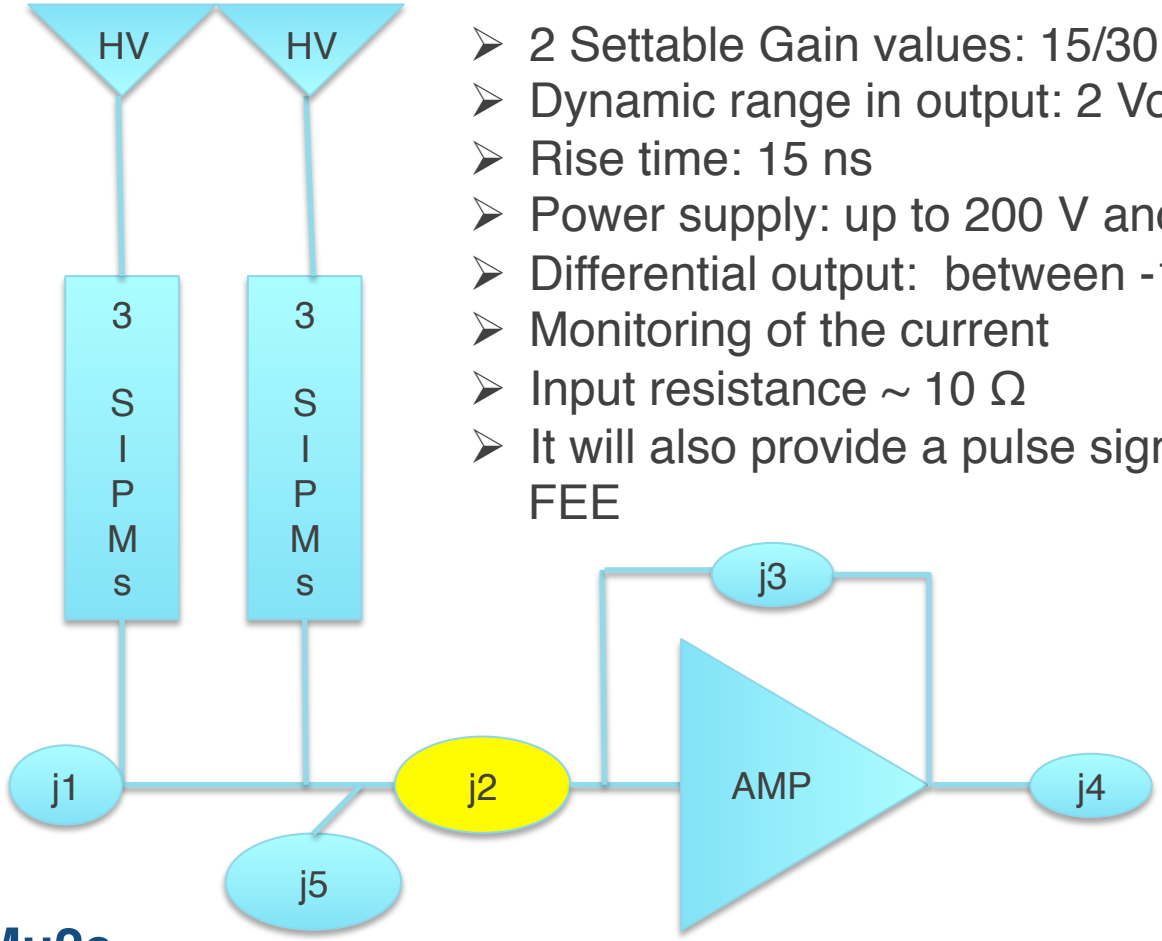


Crystal 34.3 mm x 34.3 mm (including wrapping 0,15 mm)
(34 mm + 0.15 mm + 0.15 mm) x (34 mm + 0,15 mm + 0.15 mm)
674 crystals



Calorimeter FEE

- Provide both the amplification stage and a local linear regulation for the Silicon photosensor bias voltage



- 2 Settable Gain values: 15/30
- Dynamic range in output: 2 Volt
- Rise time: 15 ns
- Power supply: up to 200 V and 3 mA
- Differential output: between -1 and +1 Volt
- Monitoring of the current
- Input resistance ~ 10 Ω
- It will also provide a pulse signal to test the FEE

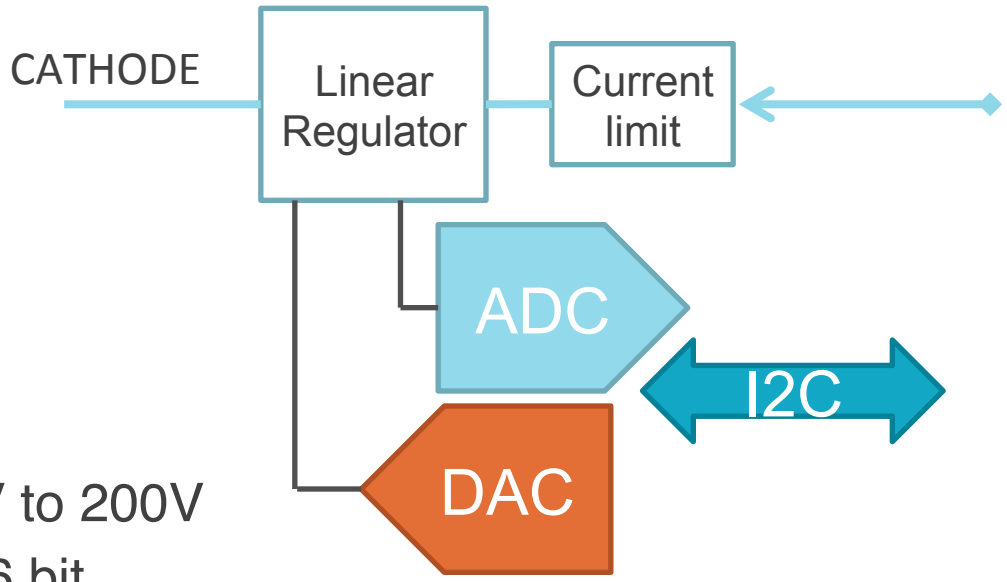
j1: Monitoring of the temperature
j2: Monitoring of the current
j3: Settable Gains
j4: Differential output
j5: Pulse Signal

Transimpedance Preamplifier

- Transimpedance 750Ω to 1.5KΩ
- Dynamic differential 2V
- Bandwidth 200Mhz
- Rise time 15ns
- Polarity Differential
- Output impedance 100 Ω
- Coupling output end source AC
- Filter Shaper 3-pole
- Noise, with source capacity 2 pC / channel

  → MEASURED with the Photosensors using cosmic rays test
- Power dissipation 20mW
- Power supply 6V
- Input Protector over-Voltage 10mJ

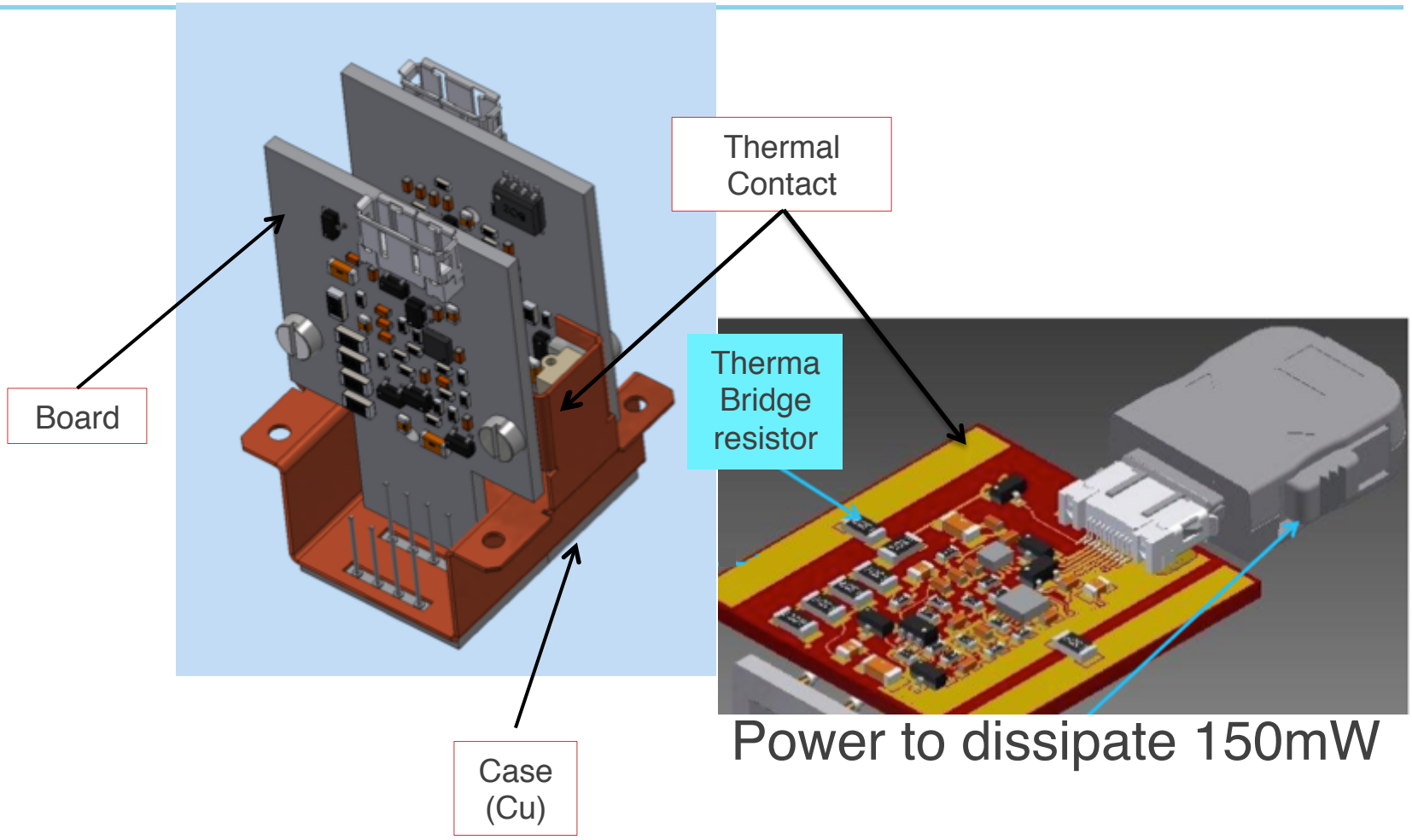
Linear Regulator shunt architecture.



- Adjustment range Vout 20V to 200V
- Accuracy, reading and writing, 16 bit
- Current limiter can be adjusted max. 3mA
- Noise tot. 2mVpp
- Long-term stability 100ppm
- Settling Time "local feedback" < 500 us ρ< 1
- Double filter high Voltage, attenuation 56db
- Temperature measurement -20 to 40°C

Engineering of the final packaging

SiPM Holder



Thermal conducting layer inserted in the SIPM package to cool them in vacuum

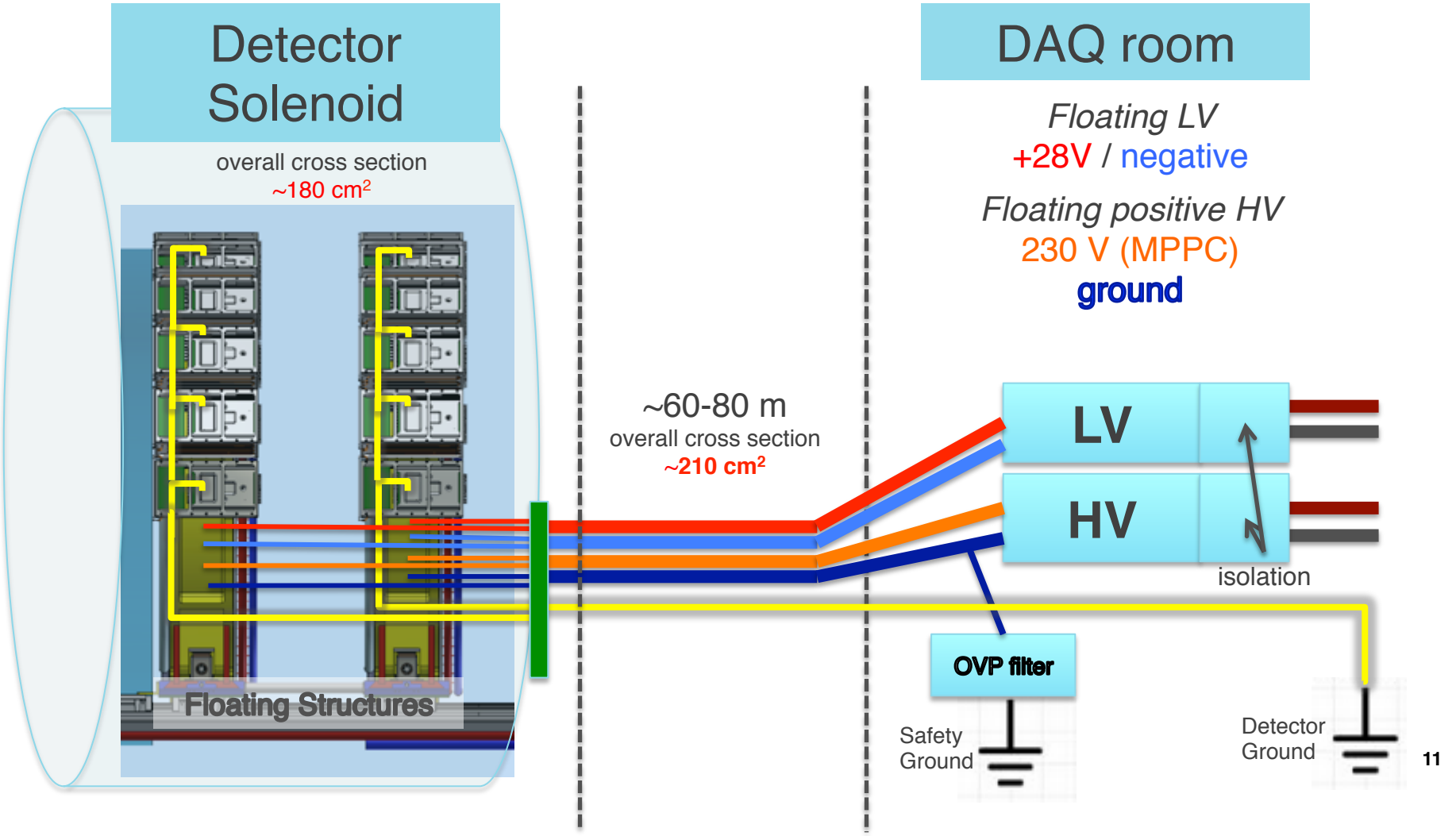
OUTSIDE the DS

- The high voltage required for the SiPMs is provided by power supplies that reside outside the detector in the DAQ room. Each supply generates a voltage of 230 V using low-noise switching technology. For each crate, there are four cables, resulting in 176 high voltage signal pairs (power and return) penetrating the cryostat.

- The low voltage power supplies for the detector will also reside also in the DAQ room. The supplies will be powered by 120V, 60 Hz main power. The outputs are +28 VDC, with isolated returns. The front-end electronics will use local point-of-load (POL) regulators to produce the voltages needed by individual circuit from the +28 V. Each crate will have eight low voltage connection, resulting in 352 low voltage signal pairs (power and return) penetrating the cryostat.

- The connector has not been specified, but may be multi-conductor.
- **The total power required, including a safety factor of 40%, is about 2 kW for the high voltage and about 4.5 kW for the low voltage.**

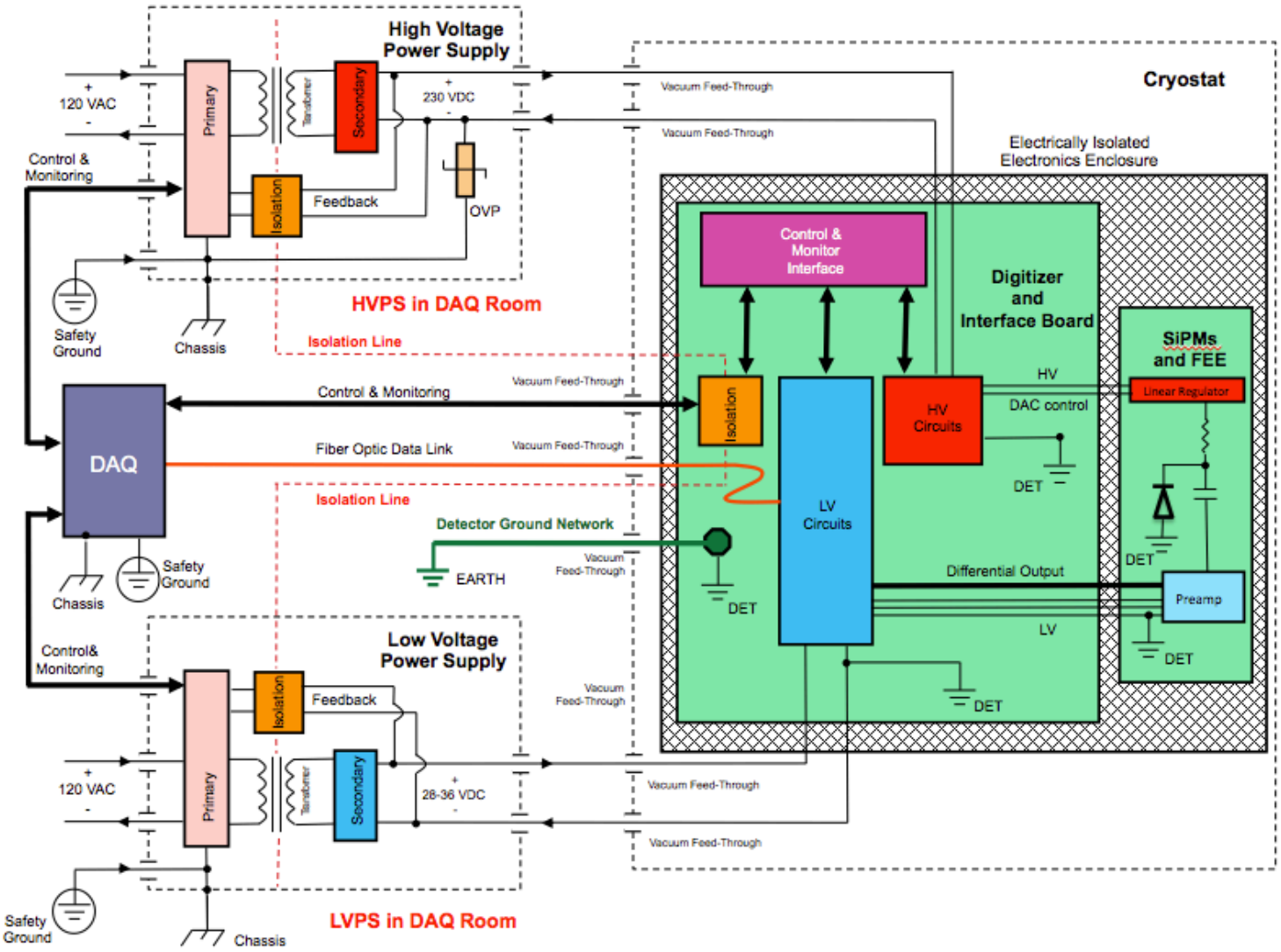
Calorimeter routing



Calorimeter Grounding - Conceptual Design -

- The calorimeter electronics will be isolated. The LV and HV will have isolated power returns at the supplies.
- They will also have isolated power returns at the supplies, using either active or passive over-voltage protection on the output power returns in the power supply unit to protect against abnormal faults. This will require approval from safety personnel. (Note that this is a backup protection scheme.)
- The ground reference for the high voltage power return will be made at the detector panel through the connection to Detector Ground.
- The power connections through the vacuum penetration will be electrically isolated from the detector support structure. Ground loops are eliminated by having isolated power supply outputs.

Calorimeter grounding diagram

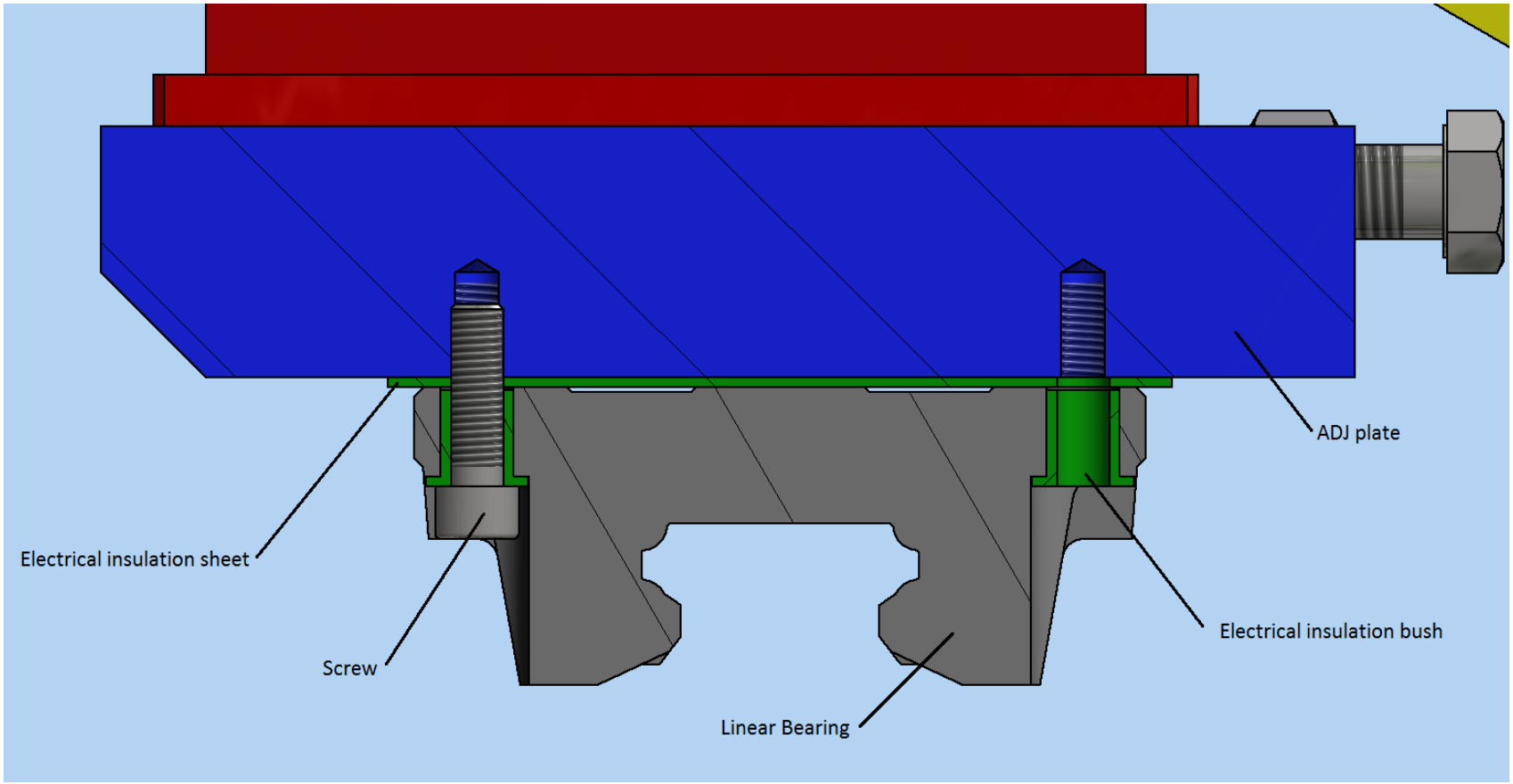


Grounding Connection

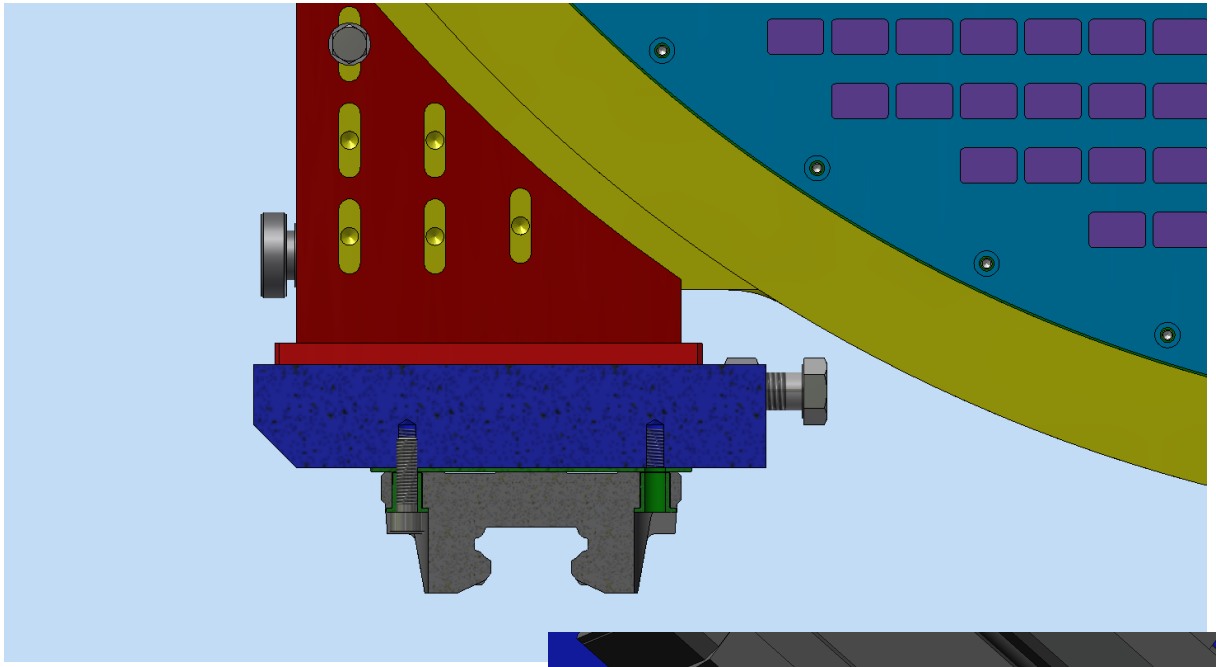
- The idea is to have two ground cables (one per disk), made of copper braid of 3 cm wide with an insulating jacket, going through the flange and then to connect them to the Ground Cable.
- The ground will be distributed on the disk using a copper braid going along the disk circumference. The copper braid will be connected to the ground cable (one for each disk) or directly or using a high power connector.
- The ground connection must pass through the vacuum flange. This will be accomplished using one of the hermetically-sealed 25-pin connectors (Positronics #XAVAC-25-M/S-I.0), the same type that will be used to pass the low voltage through the vacuum flange. The braids will be connected to the connector using all 25 pins, in a similar fashion as described for the tracker.
- Outside the flange, the 25 pins in the mating connector will be connected to an insulated braid, which in turn will connect to the Detector Ground main line.

Calorimeter Insulation -Feet-

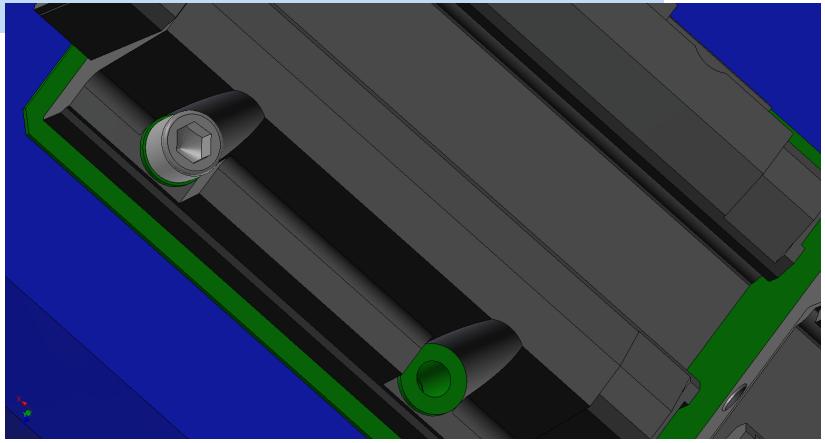
The calorimeter insulation will be done using insulation material in many sectors. The isolation material is the G11 with a thick of 2 mm.



Calorimeter Insulation - FEET 2 -

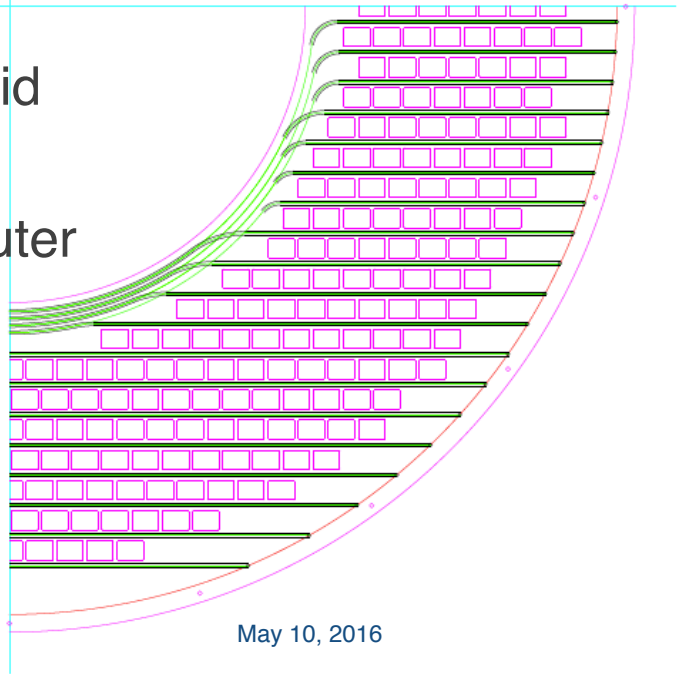


If we need to ground the structure we could remove the insulation at this level



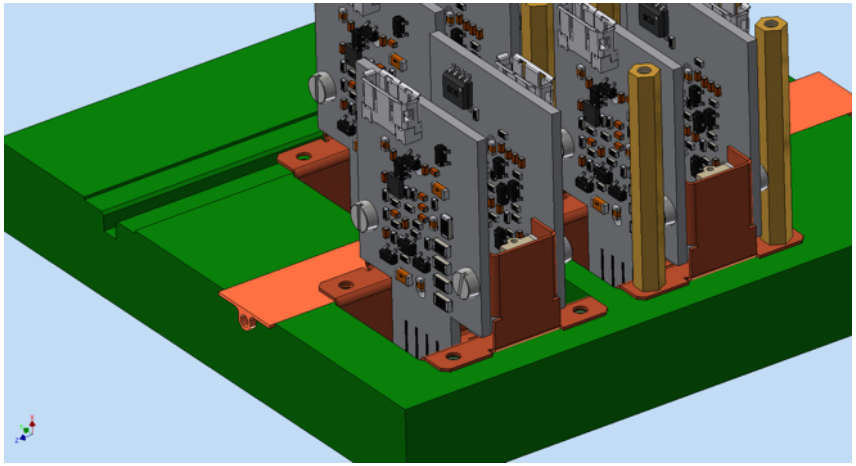
Calorimeter Insulation - Back plate -

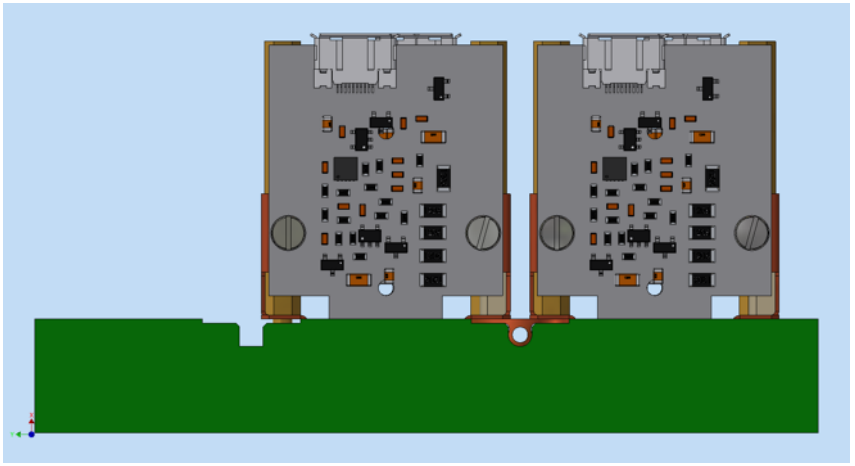
- The back plate houses the Front End electronics and SiPM holders and provides cooling.
- **Made of a supporting block of plastic material, FR4/PEEK**
- It embeds a series of conveniently shaped copper cooling pipe in the insulating supporting plate. Advantages with respect to use metal:
  - The cooling power is not wasted to cool down unneeded plate material
  - The plate is not going to expand and distort much
  - The plate can play a structural role being firmly connected to the cylinders
  - No risk of leaks since we are going to use pipes
- A dedicated calorimeter cooling station runs fluid at about -15° / 0° C.
- The back plate is thermally isolated from the outer ring and from the crystals (vacuum gap)
- The thermal resistances between the plate and the electronic holders are minimized



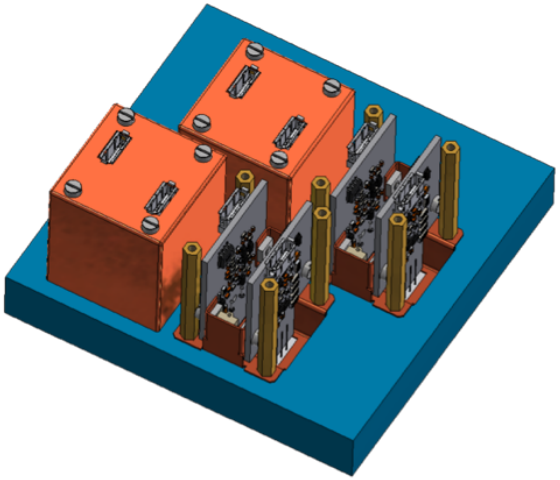
Cooling plate and Front End electronics

The front end electronic and the sensor are kept in place and cooled by a copper holder.





The design of the Faraday cage is under development.



Issues to deal with

The front-end electronics and the digitizer boards are under development:

- The radiation hardness study of the main components are already in progress → Results are more than satisfying.

The LV and HV power supplies must be still dimensioned and designed.

Extraction and intervention procedures on electronics are not yet fixed.

Summary

1. Does the Calorimeter address potential noise problems? Will the Calorimeter achieve desired performance?
– The electronics of the calorimeter has been tested in many test beam. Noise results are satisfying.

2. Is the design technically sound? Any outstanding issues?
– Isolation and commercial electronics are well understood. No known outstanding issues.

3. Significant risks? Mitigation plans?
– Environment in DAQ room must be reasonable for commercial electronics.

4. Safety concerns?
– Standard racks (208 VAC)

SPARES

Design Maturity and Path to Completion

- WD design components have already been selected and tested for radiation and high magnetic field immunity (docdb 6782)
  - FPGA: Smartfusion II SM2150T (qualified by producer)
  - ADC : ADS4229
  - DCDC : LTM 8033

- A first pre-prototype has been designed assembling demo boards and custom interconnecting boards. The obtained prototype is functionally identical to a single channel WD

- The design of the final WD is almost complete and the PCB is being laid out

- The first prototype of the 20 channels board is foreseen for end of July

Performance: FPGA

- The choice is almost unique (at moment)
- Microsemi SmartFusion2 family (SoC: FPGA + CPU)
  - Specs:
    - Flash (and not RAM) based
    - SEL free (see tables)
    - Configuration Flash SEU free(up to 90 MeV ions)
    - Data SEU low
    - Very low power

- We will use the largest and fastest one
- SM2150T-1 (1152 pins)

Table 1: Single Event Latch-Up Summary

Run	Device Tested	Number of Parts Tested	Test Facility	Test Temperature	Total Test Fluence	Number of SEL Events LET <= 20	Number of SEL Events LET > 20
1	M2S050	3	LBNL	Room Temperature	2.20×10^8	0	0
2	M2S050	3	LBNL	Room Temperature	4.09×10^8	0	0
3	M2S050	8	TAMU	100°C	4.41×10^8	0	2
Total		14			1.07×10^9	0	2

- In principle we do not need to qualify this part as a single element

5×10^{10} n/cm^2/y
5 Mbits RAM

1 SEU/board/hour
1 each 200000 events
(pessimistic)

Table 4: Configuration Single Event Upset Boundary of FIT rates

Environment	Upper Boundary of Configuration SEU FIT Rates
Ground Level (Sea Level, New York City)	Immune
Aviation (40,000 feet, New York City)	Immune
Space (Low Earth Orbit, 800 km circular, 85° inclination)	Immune

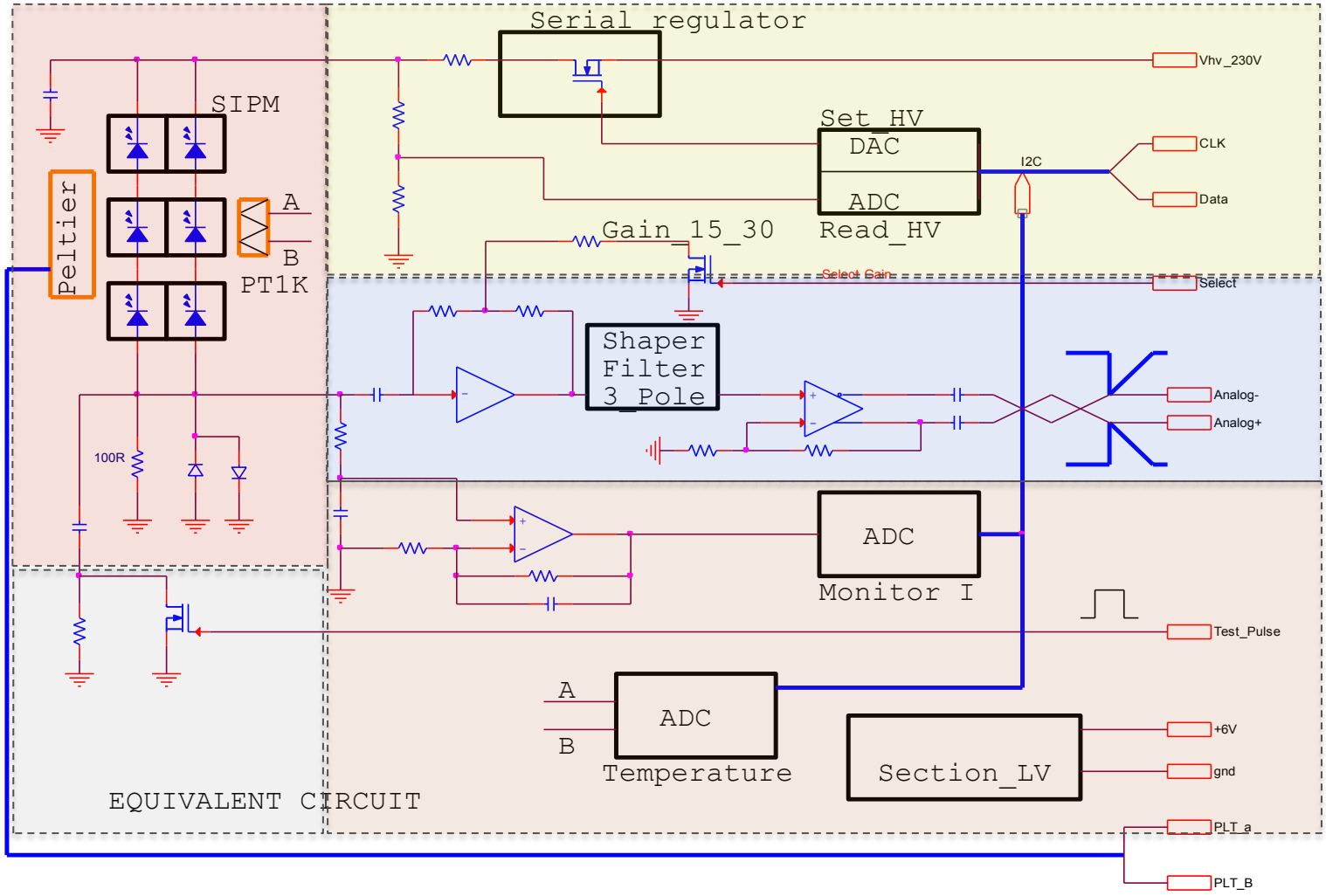
Table 5: Data SEU Summary (Single Bit Upsets)

Feature	Test Fluence (Neutrons/cm^2)	Error Rate Ground Level (Sea Level, NYC, FIT)	Error Rate Aviation (40,000', NYC, FIT)
Flip-flop	4.35×10^{11}	218.3 FIT / million flip-flops	1.13×10^5 FIT / million flip-flops
LSRAM	1.7×10^{11}	340.6 FIT / million bits	1.75×10^5 FIT / million bits
uSRAM	1.7×10^{11}	175.3 FIT / million bits	9.04×10^4 FIT / million bits

http://www.microsemi.com/document-portal/doc_view/134103-igloo2-and-smartfusion2-fpgas-interim-radiation-report

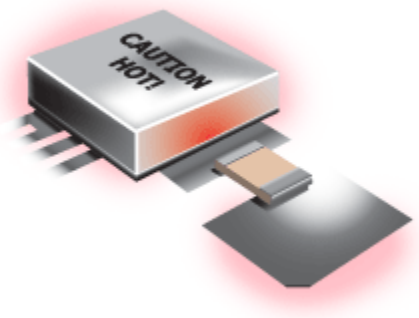
Architecture of Front-end

- ✓ Serial voltage regulator
- ✓ SiPMs polarization
- ✓ Amplifier
- ✓ Pulse signal
- ✓ Temperature and current monitoring



Cooling problem for Amp-HV

- We solve the problem of cooling in Vacuum by transferring the heat from the Amp-HV to the mechanical support, through a therma-Bridge
- An example is shown in the side view.
- The heat transfer must take place in isolation from common ground.

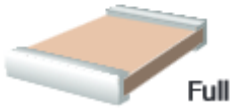


Therma-Bridge™ Electrically Isolated AlN Thermal Management Device

The ims Aluminum Nitride (AlN) **Therma-Bridge™** is a simple, cost effective device which aids in thermal management. Bridges are available in standard sizes and thicknesses. Custom sizes are also available on request. The **Therma-Bridge™** is designed to transport heat from one location to another. Simply attach one terminal to the heat source, and the other terminal to a thermal plane or heat sink. Popular application configurations are shown on the reverse side. The **Therma-Bridge™** has the following features:

- Electrically Isolated AlN substrate material
- Multiple sizes and thicknesses
- RoHS PtAg or Solder coated PtAg terminals for easy attachment

Terminal style:



Full wraparound

Terminal materials:

-3 ✓	PtAg (platinum silver) for epoxy or solder attachment
-C	Solder coated PtAg for solder attachment