35T Electronics Qa/Qc Overview

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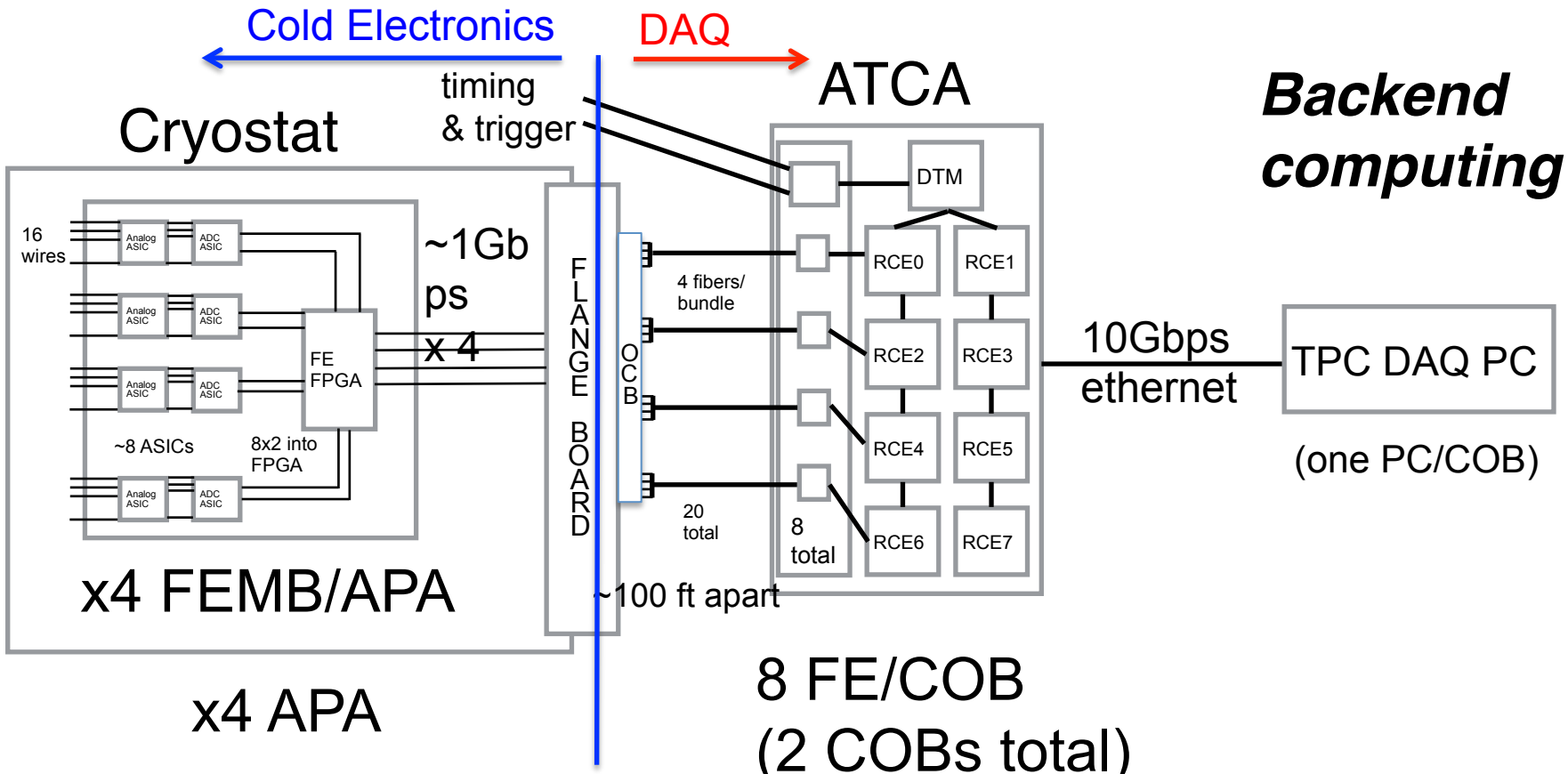
General Organization

- A brief description of the components and the test setup we used at DAB (D0 Assembly Building)
- The Qa/Qc that that was done for the major Electronics systems
  - Also known problems that we were coping with.
- I will mainly speak to the issues we had during the integration stage here at FNAL
  - Particularly comparing our Schedule to our reality
  - Try to understand where the discrepancy comes from
- Initial Testing using the evolving DAQ
- Noise in system

35t TPC Readout Chain



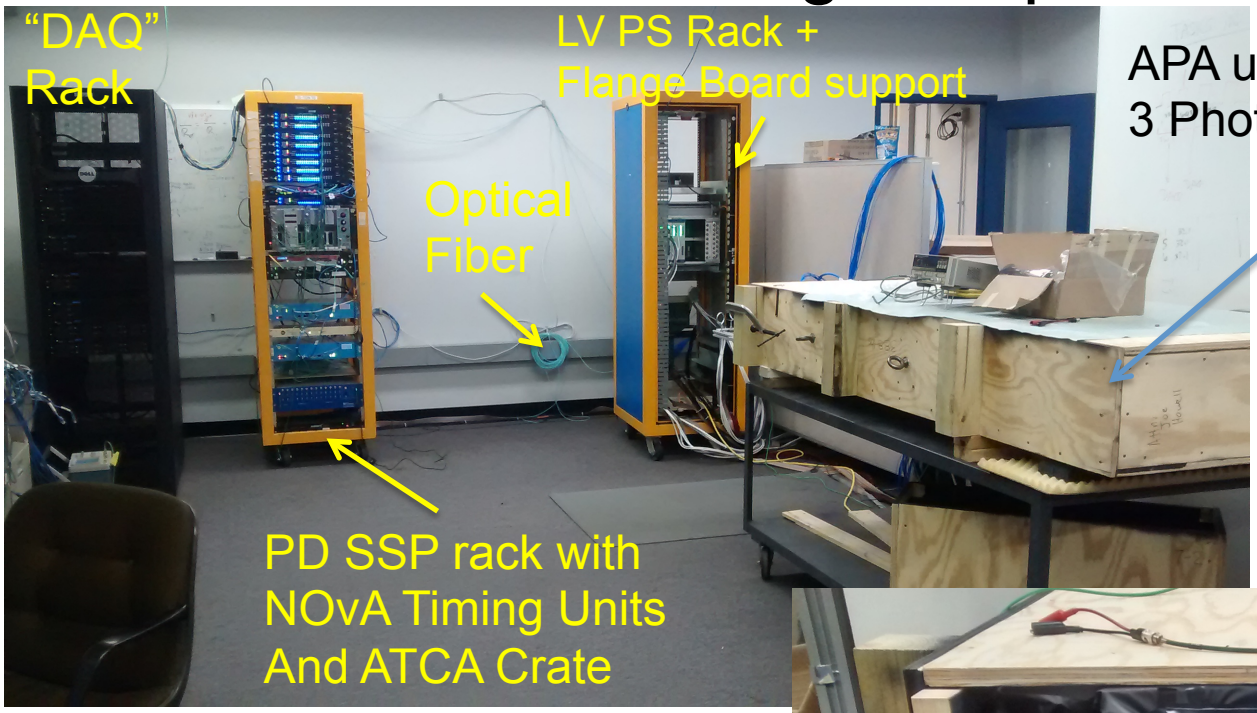
FE configuration & control done over same high-speed connections as signal, with dedicated I2C links as a backup

(from M.Graham LBNE DocDB 10886)

Photon Detector Readout

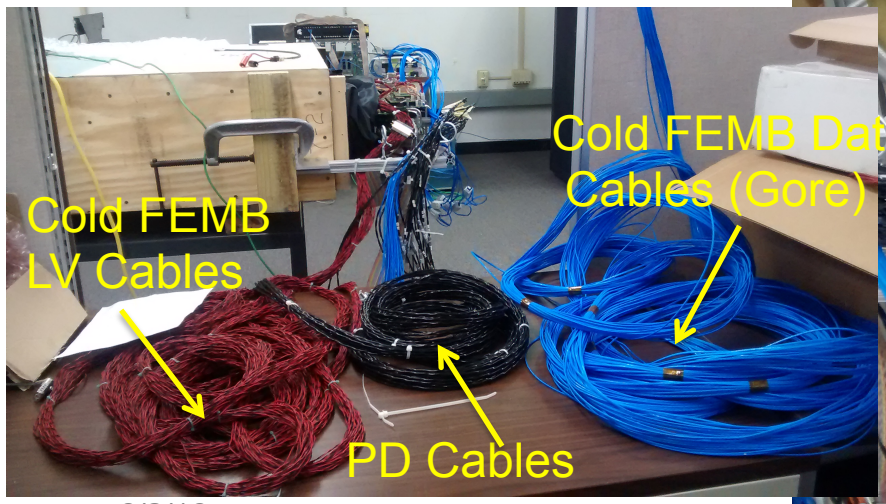
- SiPM Signal Processor (SSP) provides both the bias and digitation of SiPM signals
- Shielded twisted pair cables from individual SiPMs (up to 12 for each PD) plug into cold side of the Flange Board. Same type cables run from the warm side of the Flange Board to the SSPs which are located in a nearby rack.

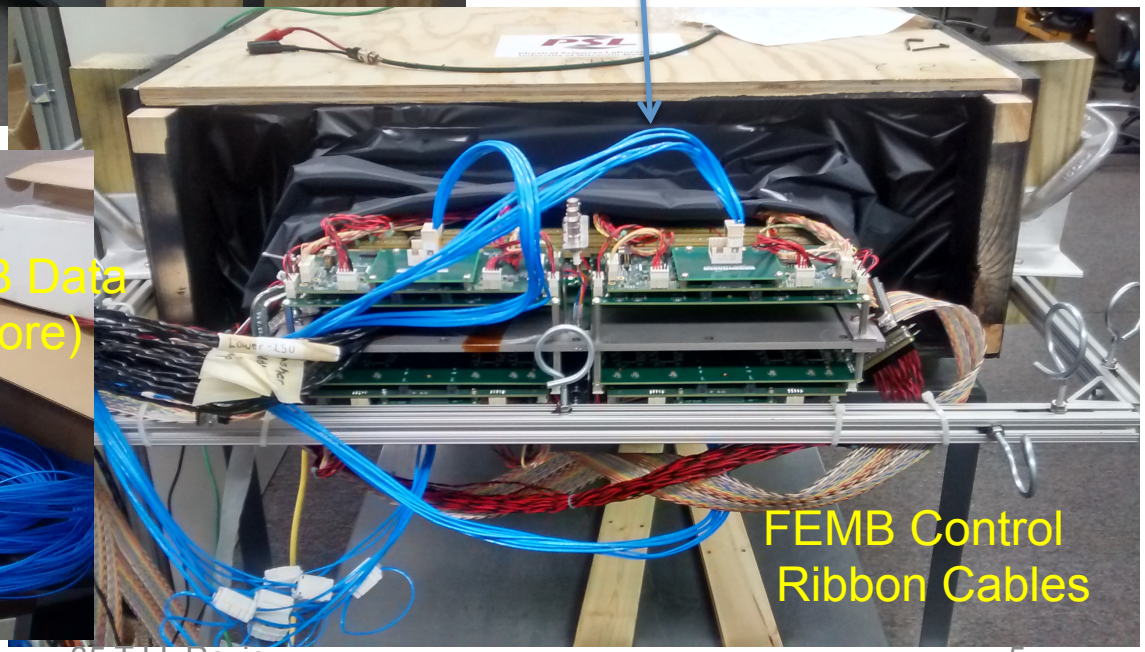
Testing Setup at DAB



APA under test with 4 FEMBs and 3 Photon Detectors

(Photos T.Shaw)





Component Qc/Qa at Production Sites

- APAs at PSL
- Front End Electronics at BNL
- Photon Detectors—various sites

APA Testing and QC at PSL

- Quality control tests:
  - Wire tension test of all wires in a layer after each wire layer is installed
  - Tension retest of 30 wires per layer after entire APA is wound
  - Electrical continuity test on each layer
  - After winding, hi-pot test, in air to 2kV, from each layer to all other layers and ground
  - Individual electrical test of pcbs
  - Cold test – LN2 immersion
    - Immersed hi - pot electrical test to 5kV
    - Examination for physical damage after cold test
    - Retest of wire tension and electrical parameters after cold test
- Travelers
  - Travelers have been used for the fabrication of all the 35T APAs
  - Each step is listed – with columns for date completed, person completing task and comments about anything unusual or otherwise noteworthy
- Log book

  A log book is kept where daily comments are written. These include good ideas, problems encountered, problems solved, reminders of things that should be included in future travelers, etc.

FEMB QC/QA at BNL

(B.Kirby, DocDB10882)

- 19 analog boards and 20 FPGA boards produced for 35t test
  - 16 required for full detector
- Extensive tests of FEMBs at room temperature and liquid nitrogen have been performed
- FEMBs validated in sequential tests:
  - On-board oscillator cryogenic screening prior to assembly
  - Post-assembly room temperature functionality test
  - Cryogenic functionality and performance validation
  - Final validation data-taking after cryogenic testing

Photon Detectors (D.Warner)

- All eight PDs have entries in DocDB.
  - PDs were put into APAs before APAs were wound with the wire planes
- Testing in Lab 3 in Village
  - (11/9/14) during VST period when all APAs were being stored at Lab3
- Testing consisted of the following:
  - Diode check with DVM to make sure electrical connection is still good
  - Flashing PD test LEDs for each PD bay and making sure all SiPMs respond (1 LED intensity, varied the bias voltage watching the output).
  - SiPM signals from the LED test were read out on a scope
- Summary:
- 74 total channels
- 71 checked out fine
- 1 checked out with inverted connector-- Repaired, now OK
- 1 failed-- good diode check, no photo response
- 1 failed-- bad diode check

Known Issues

- APAs
- FEMBs
- Flange Board (transition between cold and warm)

APA Wire Plane Known issues

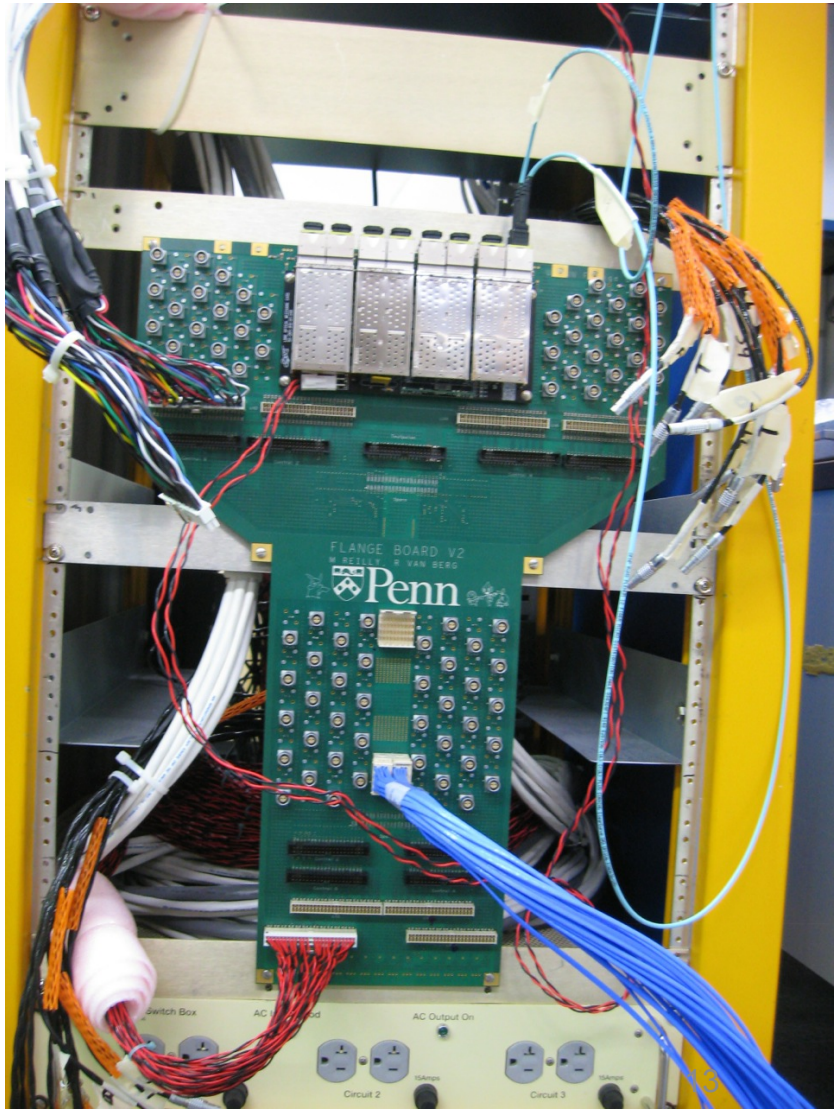
- # bad wires (broken/disconnected) (see Lee Greenler – DocDB 9399 for reason and for future mitigation)
  - 3 Bd 12
  - 4 Bd 2
  - 7 Bd -1 none
  - 7 Bd -2 8
- Issue here is there was no “easy” way at the time to check the APA for low noise channels---indicating no wire (of any length) was connected to the input.
  - Actual wire was still in place, just not connected to solder pad.
- Lessons Learned
  - Cooldown should be more gentle
  - Need to establish successful procedures before embarking on production runs
- Wire Map for APAs are very confusing
  - Partly due to overall symmetry, but also due to use of words like “left” and “right ”without a clear referenced observation points.
  - I had to write my own GUI to understand how to map physical wires to FEMB channels
  - Discovered error (one of consistency) in map. Unfortunately couldn’t get verification (or otherwise) from map producer.

FEMB known issues

- Sticky Bits
  - ADC 64 bit boundary has tendency to be wider than normal (~differential non-linearity)
  - Purportedly worse when at LAr Temps.
- Bad channels
  - From 7/27/15 Bad Channel Summary
    - 62 known bad channels (~3% of total)
      - Worst board has 16 bad channels (12.5%)
- Delivery schedule
  - First 2 production boards arrived DAB ~2/17/15
  - Next 4 on 4/10/15—replaced first 2
    - First time we had a APA with full complement FEMBs
  - Next 8 on 5/8/15
  - Next 6 on 7/10/15
  - Spare on 8/24/15 to replace FEMB with intermittent readout issues on some chips
- We went thorough several Firmware updates over this period that improved functionality with DAQ readout
- Found that pedestal level for Induction wires (bipolar signal) had worse noise than the pedestal level for the Collection Wires (unipolar)
- Synchronization of ADC bit readout was temperature dependent and had to be determined for each ADC chip.
  - This had to be done by expert.

Flange Board Known Issues

- Version 1 was not usable.
  - Could not use for VST
- Version 2, #1 & #2
  - Had some issues with solder mask, reworked
  - Finally available 4/6/15 (original V1 planned for VST on 11/14)
  - One chosen for actual use in 35T--its Bias HV lines had non-linear leakage currents
    - Had to abandon that functionality and make new ports/ feedthroughs for the 16 bias lines (12 for APAs, 2 for Deflectors, and 1 for the Field Cage termination Point Bias.
    - In addition, one bias line was shorted.
  - However other than these issues, the V2 FB performed well during the Run.



DAB Activities

- Installation Readiness reviews at end of August of 2014 established a "Baseline" schedule for the Phase 2 run.
  - This had us running Phase 2 at beginning of March 2015.
    - ***Actual run start was February 2016***
- We planned on having a "Vertical Slice Test" at DAB (D0 Assembly Building)
  - One APA + 4 FEMBs and Photon Detectors connected through Flange Board and readout through the complete DAQ.
  - Meant to also exercise the modes of running the DAQ
  - Baseline had all APAs equipped with FEMBs, tested, and installed in Cryostat in 4 weeks (12/3/14)
    - ***Actual was ~40 weeks from start of VST to final APA installed***
- Baseline had 6 months from APA installation to start of run
  - ***Actual was 5 months!***
- See Baseline Schedule and Actual Timelines in the Xtra Slides

What's Going on?

- This baseline schedule was coming from the various task managers
- After experiencing the reality, it is obvious that it just isn't credible to bring up a new DAQ with new hardware in 2 weeks
  - Even if you have all the experts available.
  - Now take away the experts after initial 2-3 week period and you get the result that simply getting the first APA "qualified" took 4 months.
    - Remaining 3 APAs just one month more!
- So from this point I will stop looking at the schedule.

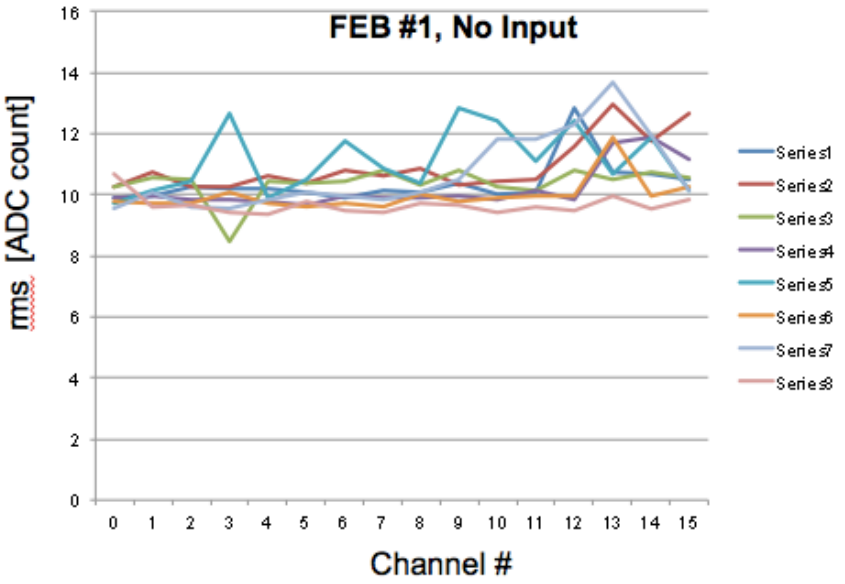
APA/FEMB Integration and Testing

- Pre-DAB tests
- DAB Integration

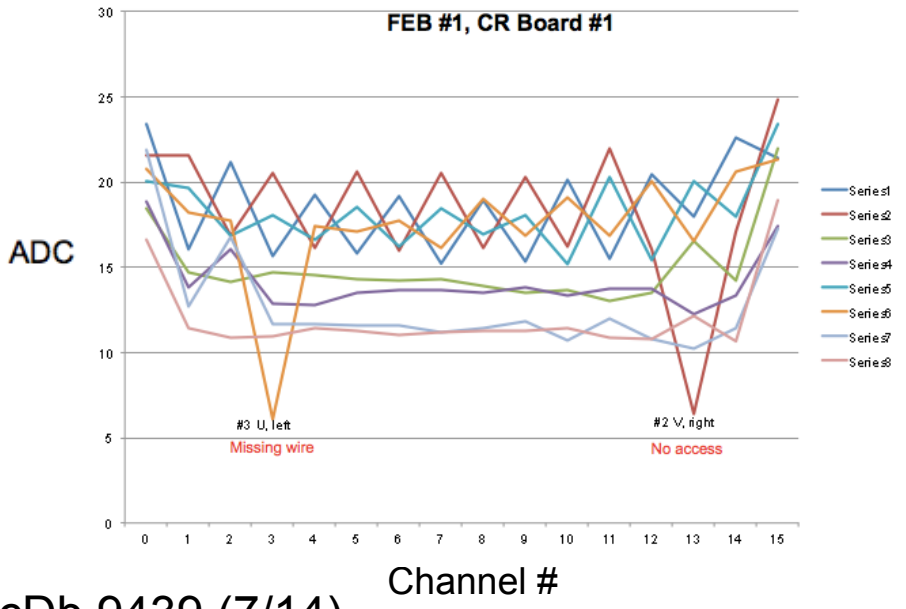
Integration and Testing of FEMBs with APAs

- Previously one APA (3 Bd) was shipped (6/14) to BNL to be checked out with preproduction FEMB.
- Found several wires on APA that were apparently not connected—fed back to PSL

Bare FEMB



FEMB on APA (Bare rms quad subtracted)



LBNE DocDb 9439 (7/14)

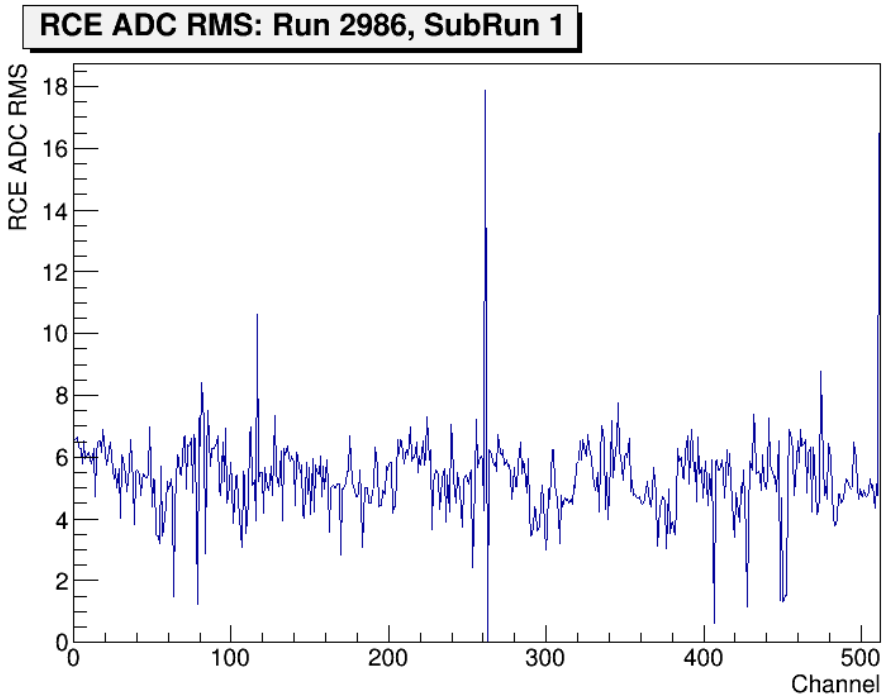
DAB Integration and Testing of FEMBs with APAs

- The criteria for acceptance were that after mounting the FEMBs on the APA:
  - FEMB could be read out.
    - Pedestals means and rms could be measured and were on the average the same between different FEMBs and APAs
    - As long as we had spare FEMBs, FEMBs with excessive broken channels would be swapped for better ones.
  - Chips on FEMB could be programmed
  - Photon Detectors in APA were responsive to LED flashers.
- We were unsure what the intrinsic noise level was in the open environment of DAB
- Any issues that were external to the cryostat would be not be considered "show stoppers".
  - e.g. items like the optical links which appeared to be very flaky would not disqualify the APA (or FEMBs on APA).
  - Assumption was that we would figure these things out later
    - Which is what did happen.
- In the end, all four APAs tended to look nominally the same noise-wise at the end of the DAB testing.
- Lack of on-site experts on electronics and the hardware side of the DAQ severely hampered progress
  - Runs were only a few minutes long since a crash would kill any data output
  - Many DAQ and hardware problems (not atypical for such a new system I think).
  - Everything (FEMB, ATCA components, SSPs) had multiple firmware upgrades.

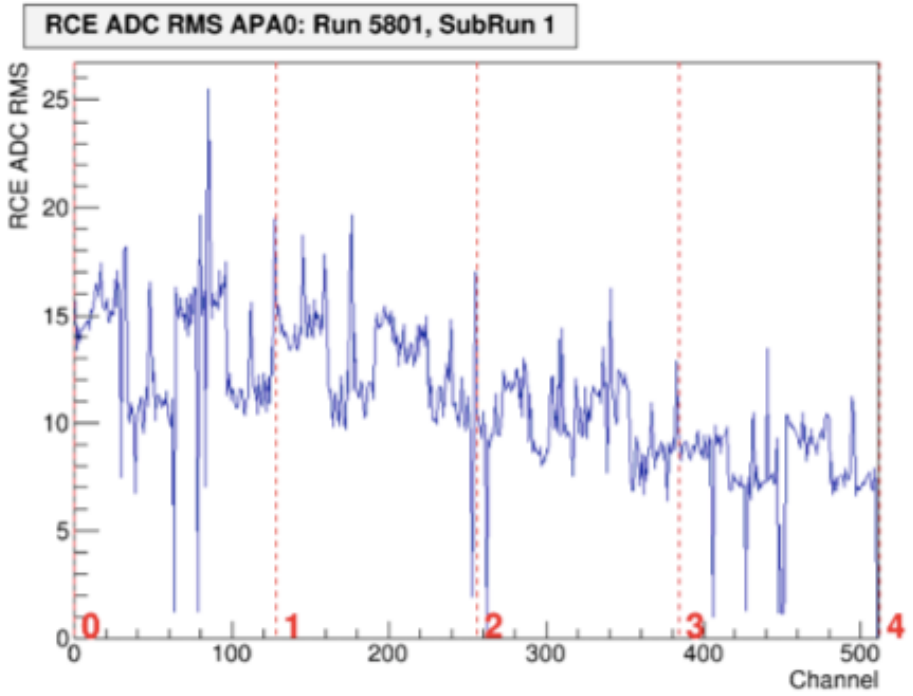
Installation of Detector In Cryostat

Comparing Noise in APA0 (7-1 APA) between DAB and Cryostat (Room Temp)

One FEMB



At DAB just before sending to PC4



After installation in cryostat ~12/16/15 while 35T is being leak-checked

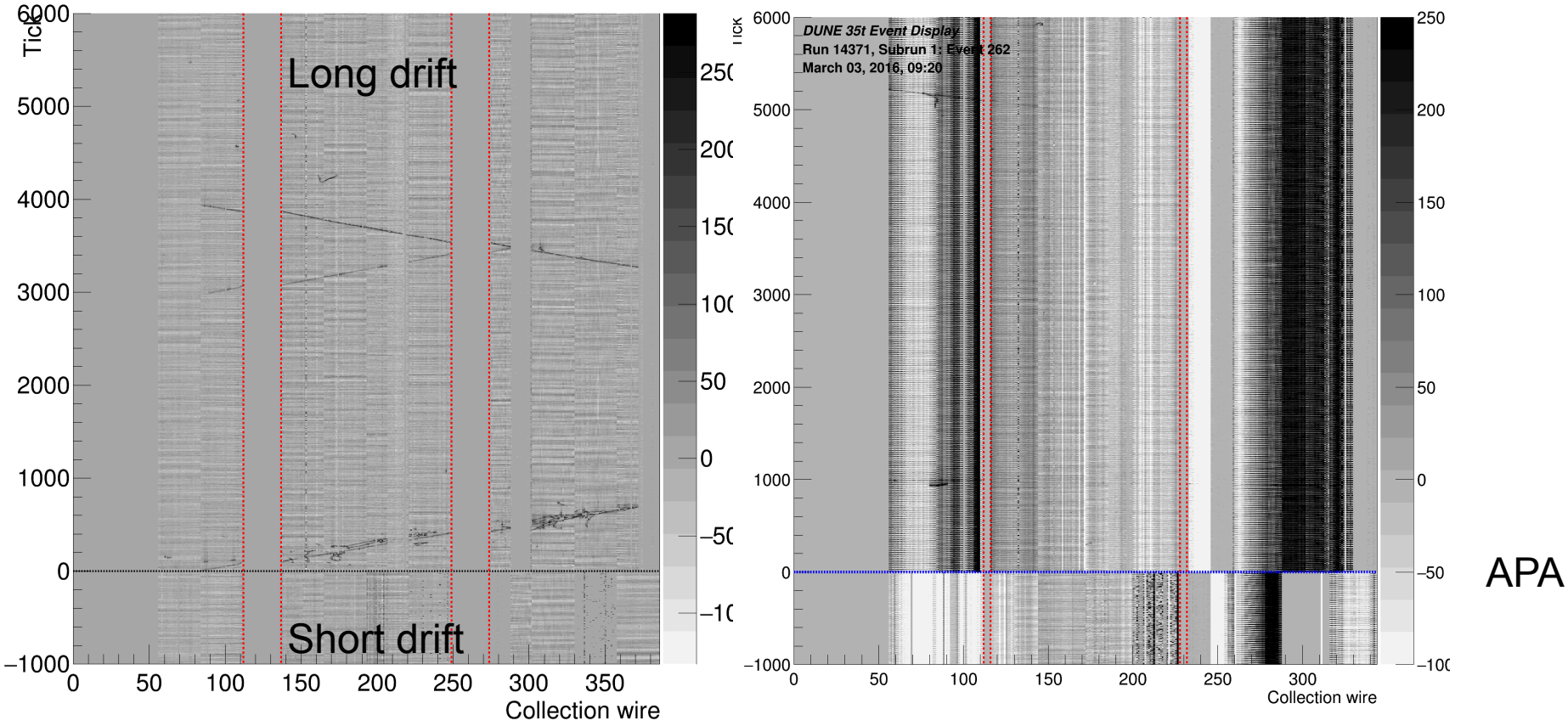
Noise

- The FEMBs + the APAs have been plagued by relatively high noise levels, correlated over many channes
  - These swamp the original specs that were based on thermal noise figures, as measured with capacitive loads
  - Clearly see noise influences that correlate to the individual wire planes
- Our “low noise” state includes this correlated noise.
- Since filling with LAr, we are often spontaneously triggered into an extremely high noise state that makes it impossible to use the data for anything (see next slide)
- Much work is being done now by Marvin Johnson, Brian Kirby, Linda Bagby, Steve Chappa… in trying to characterize this noise
  - Hope that understanding can be fed into the electronics/APA design/??? for ProtoDune

Online Event Display -Collection Plane
Top view of APA

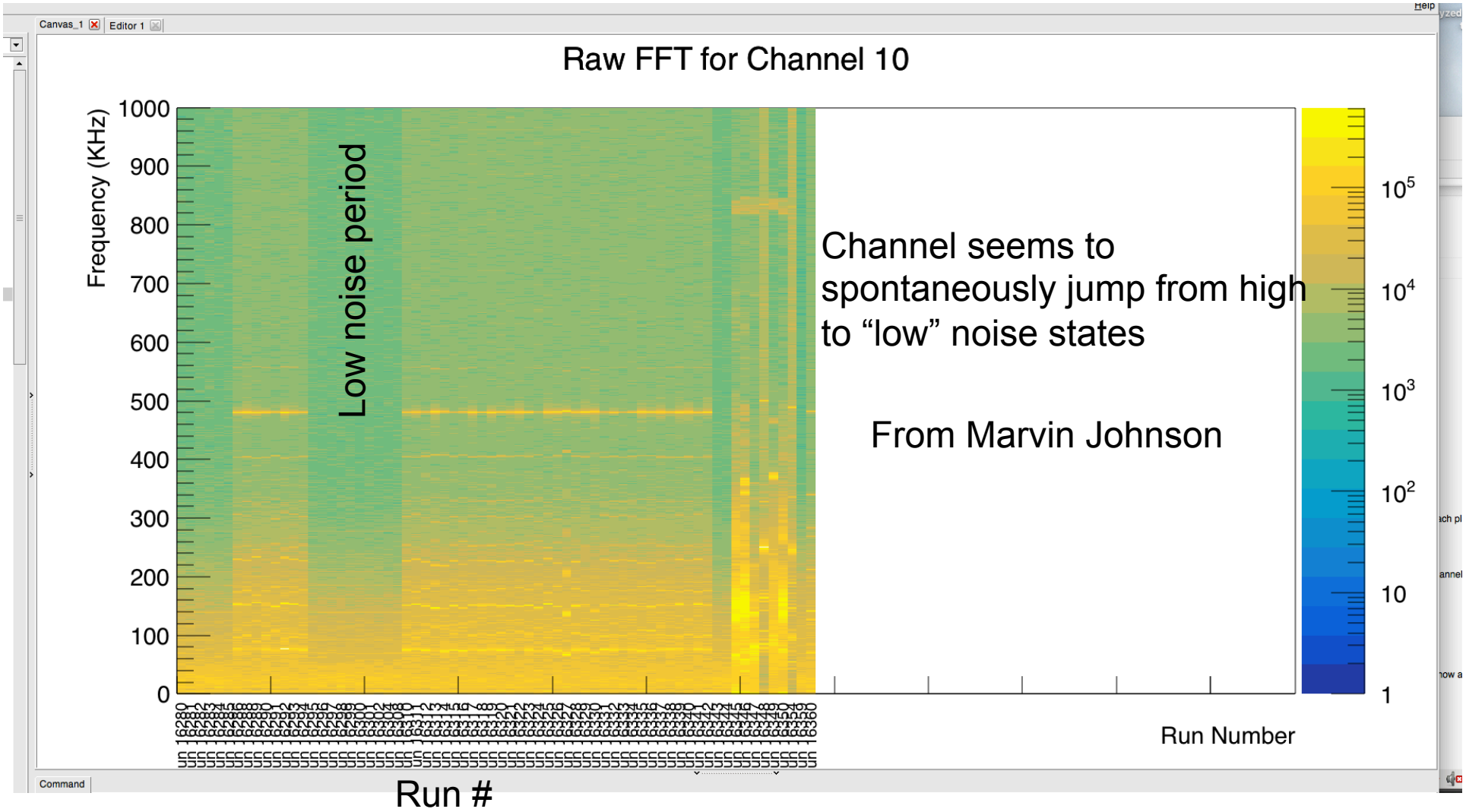
"Low" Noise State

Very High Noise State



APA

Looking a FFT of a single FEMB channel over a number of successive runs



Trying to find trigger/source of noise

- Several time we have stopped normal activity and turned off/unplugged hardware to see if we can find sources of noise.
- With respect to the trigger source for flipping into the very high noise state, turning off specific FEMBs sometimes helps.
- However even in the “low noise” state, the correlated noise dominates the thermal noise.
- Next slide is an attempt to strip off the correlated noise (11 kHz in this case) to see if we can see any hardware contributions.

Noise Hunting in 35T

(table from B.Kirby, 4/13/16 35T 11AM Meeting)

Noise Tests to Date - Non-TPC Noise Sources

- March 4 test: non-TPC systems turned on one at a time to measure contribution to noise, looking at "quiet" APA1

Run	Settings	Collection Noise (ENC)	Induction Noise (ENC)	Collection Noise 11kHz Subtracted	Induction Noise 11kHz Subtracted
14623	14mV/fC, 3us	1910e-	2430e-	610e-	1120e-
14628	14mV/fC, 3us SSPs on	2060e-	2540e-	670e-	1270e-
14629	14mV/fC, 3us Counters in	2060e-	2550e-	680e-	1280e-
14630	14mV/fC, 3us APA bias on	2070e-	2620e-	725e-	1430e-
14663	14mV/fC, 3us Drift on	2160e-	2760e-	740e-	1500e-

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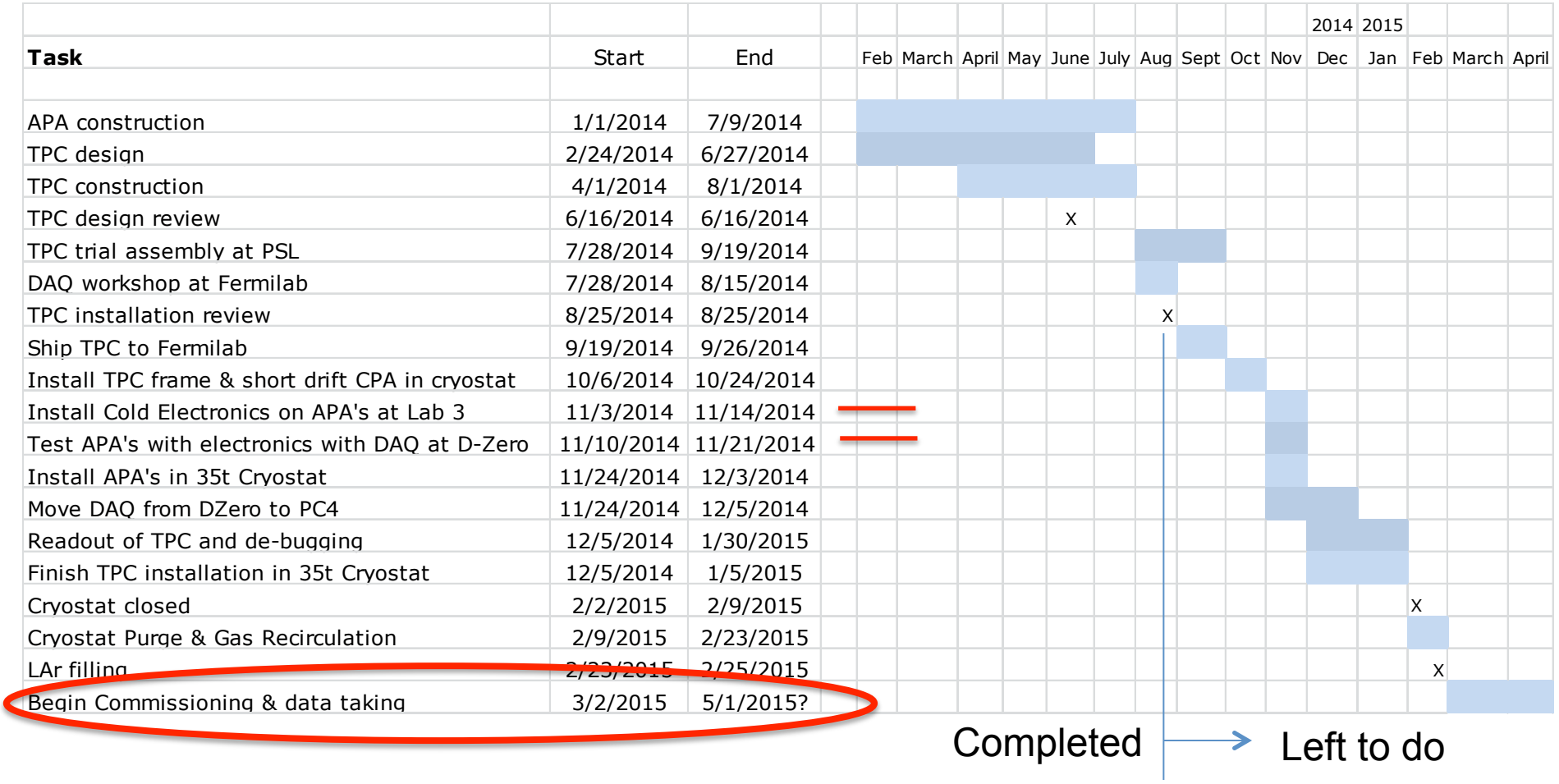
Xtra slides

From 35 Ton Installation Readiness Review 8/25/2014

High Level Summary Schedule
= “Baseline”

Task	Start	End
APA construction	1/1/2014	7/9/2014
TPC design	2/24/2014	6/27/2014
TPC construction	4/1/2014	8/1/2014
TPC design review	6/16/2014	6/16/2014
TPC trial assembly at PSL	7/28/2014	9/19/2014
DAQ workshop at Fermilab	7/28/2014	8/15/2014
TPC installation review	8/25/2014	8/25/2014
Ship TPC to Fermilab	9/19/2014	9/26/2014
Install TPC frame & short drift CPA in cryostat	10/6/2014	10/24/2014
Install Cold Electronics on APA's at Lab 3	11/3/2014	11/14/2014
Test APA's with electronics with DAQ at D-Zero	11/10/2014	11/21/2014
Install APA's in 35t Cryostat	11/24/2014	12/3/2014
Move DAQ from DZero to PC4	11/24/2014	12/5/2014
Readout of TPC and de-bugging	12/5/2014	1/30/2015
Finish TPC installation in 35t Cryostat	12/5/2014	1/5/2015
Cryostat closed	2/2/2015	2/9/2015
Cryostat Purge & Gas Recirculation	2/9/2015	2/23/2015
LAr filling	2/23/2015	2/25/2015
Begin Commissioning & data taking	3/2/2015	5/1/2015?



This schedule comes from the sub-detectorTask managers for these systems

35 Ton Phase 2 Actual Timeline

(as seen from “FNAL Integration Site” point of view)