# Front-end tests

2/6/2016

- Extensive discussions on grounding since the end of February with the help of Francois and dedicated meetings (last one on last Friday 27 March)

→ Definition of final grounding scheme being implemented by July 18th based on a common ground at the level of the cryostat and insulation transformers in order to decouple the ground of sensitive equipments

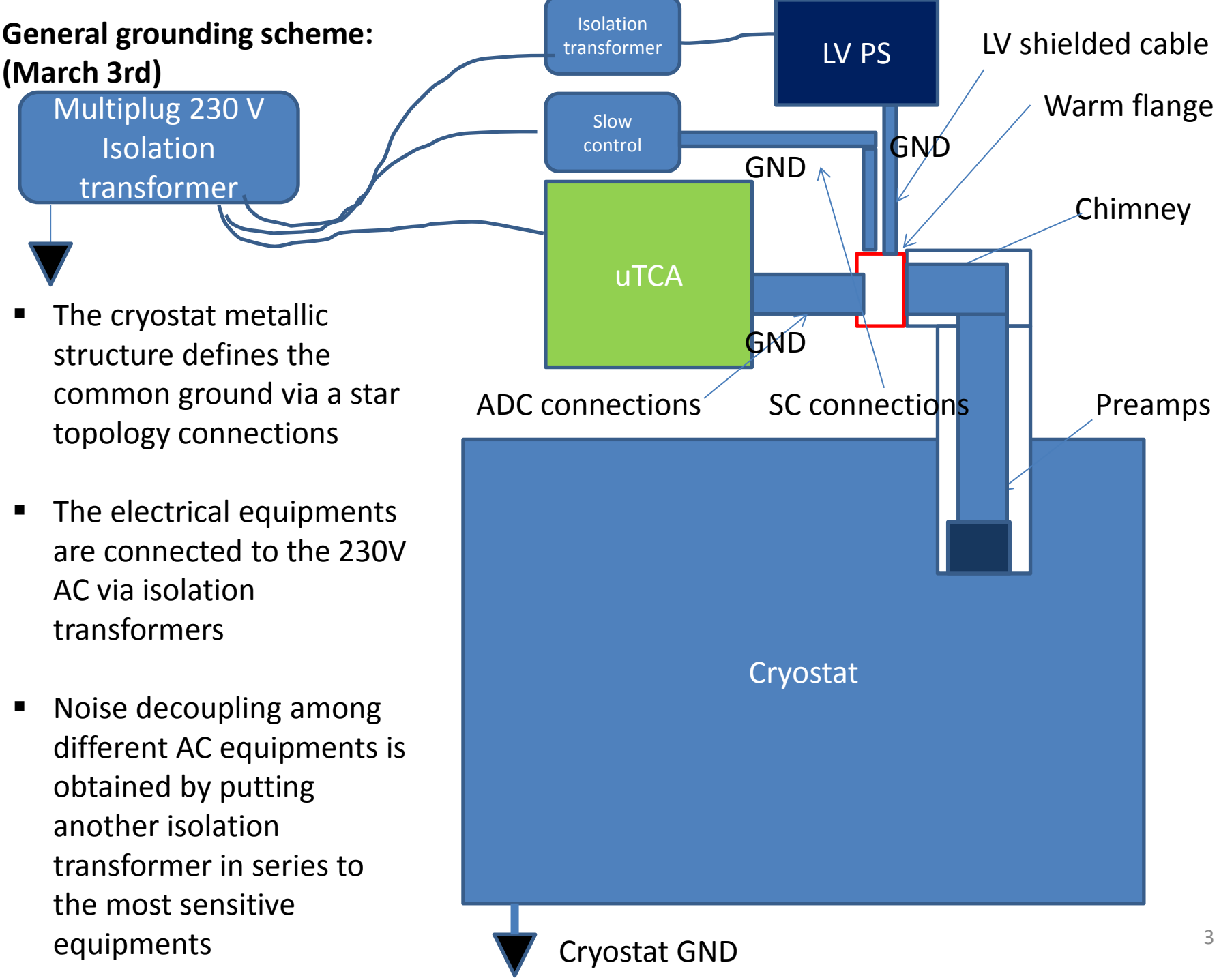
- Checks of all connection scheme from the anode planes to FE cards, chimney flanges, DAQ ADCs

→ Channels mapping, final design and production of FE cards with integration of decoupling and protection components on FE card (R bias, C decoupling and diode pairs) and warm flange (cleaner interface with grounding and shielding, had to be modified anyway since it, half of the pins of each connector were originally set to ground)

- Checks on mechanical compatibility of FE cards

→ **Further tests in situ on FE cards insertion and noise checks**

**General grounding scheme: (March 3rd)**




- The cryostat metallic structure defines the common ground via a star topology connections
- The electrical equipments are connected to the 230V AC via isolation transformers
- Noise decoupling among different AC equipments is obtained by putting another isolation transformer in series to the most sensitive equipments

legrand®

# Fiche e-catalogue

▶ Accéder à l'accueil e-catalogue

REF. 0 428 27

Télécharger le visuel

TRANSFO ISOLEMENT TRI PROTÉGÉ - PRIM 400 V/SEC 400 V + N - 16 KVA - ÉCRAN

**INFORMATION PRODUIT**
Découvrez nos solutions sur mesure dans l'onglet logiciel

| | |
|---|---|
| Tarif unitaire HT | 3 490,00 €* |
| Emballage (nombre d' unité) | 1 |
| Volume (dm³) | 229,00 |
| Poids (kg) | 103,00 |

>> Accéder au e-catalogue pour établir ma liste de matériel

>> Accéder au e-catalogue pour imprimer

## Caractéristiques générales

**Transformateurs triphasés - IP 21**

- Cuve RAL 7035

## Caractéristiques du produit

**Transformateurs d'isolement**

- Conformes à la norme IEC EN 60076-11
- Avec prises de réglage ± 5 % à partir de 50 kVA
- Avec écran électrostatique

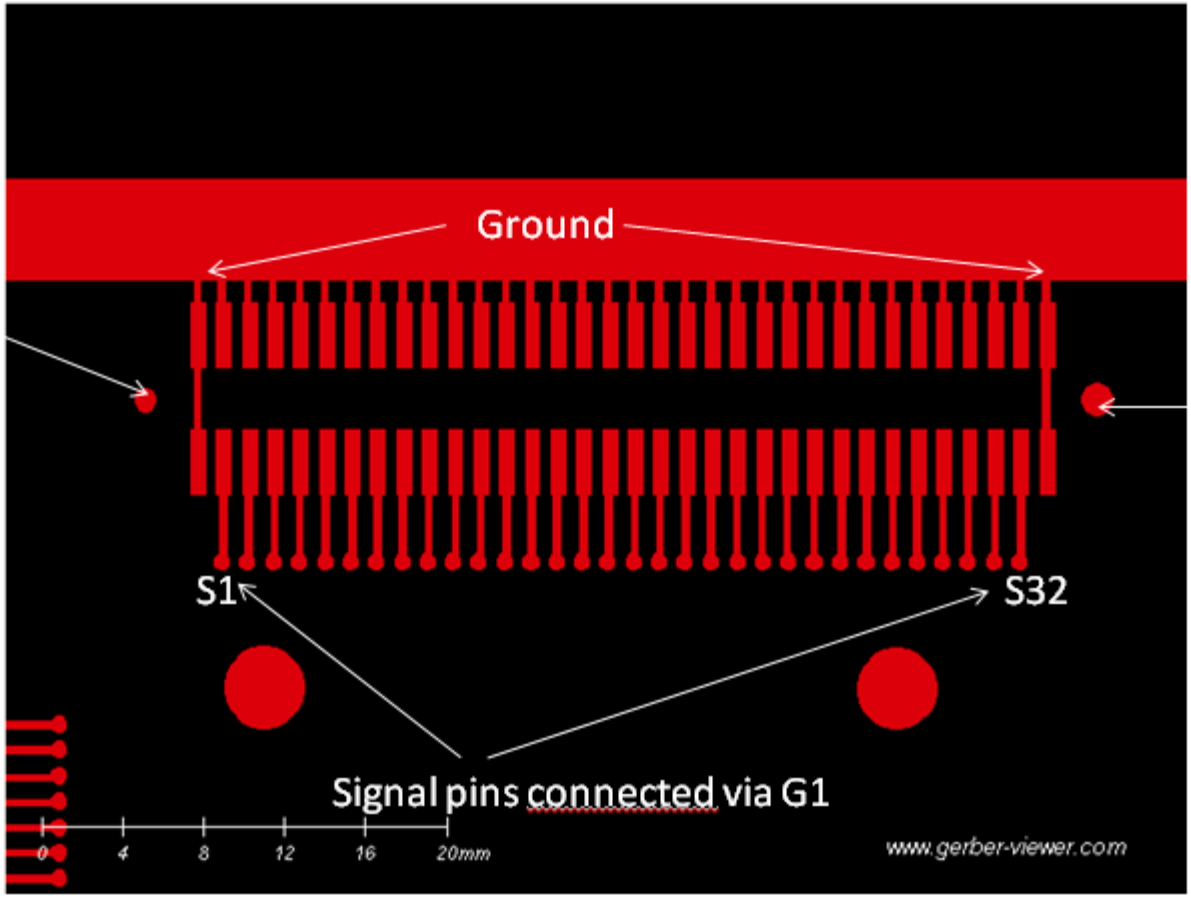
**Primaire : 400 V - Secondaire : 400 V + N**

- Puissance : 16 kVA
- Borne primaire câble souple section : 35 mm²
- Borne secondaire câble souple section : 35 mm²

Example of isolation transformer

Layer GTL,
zoom top corner, connector, 34 pairs connector, 34+2 GND, 32 signals

ANODE

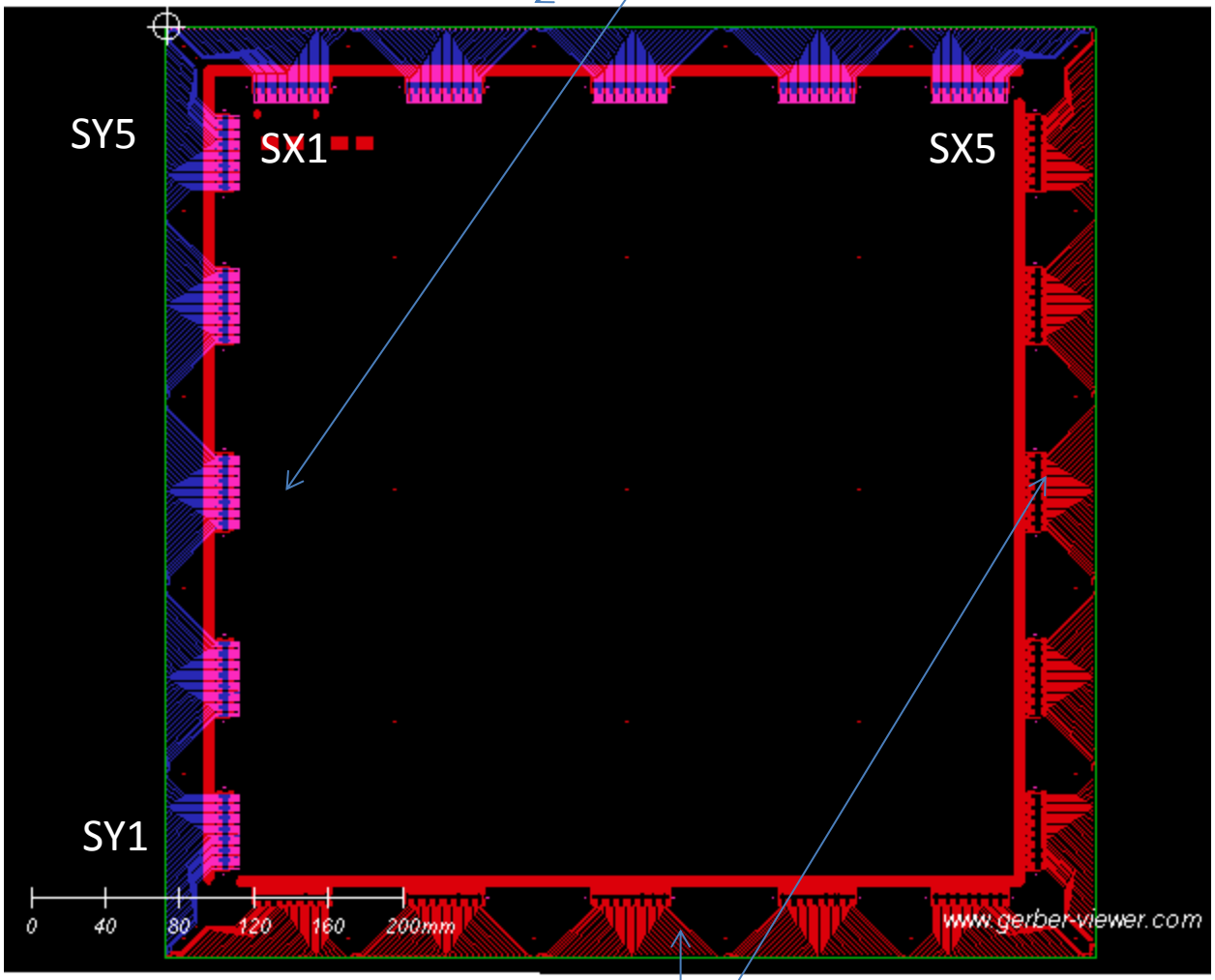



KEL 8913-068-178MS-A-F SMD mounting
Cable KEL8925-068-179-F

Layers G1 + GTL

Signal Connectors

Connectors have the small hole at right and the large one at left, so the numbering of channels 1-32 proceeds in the same sense (small hole to large hole).




**5 connectors of 32 channels per side:**

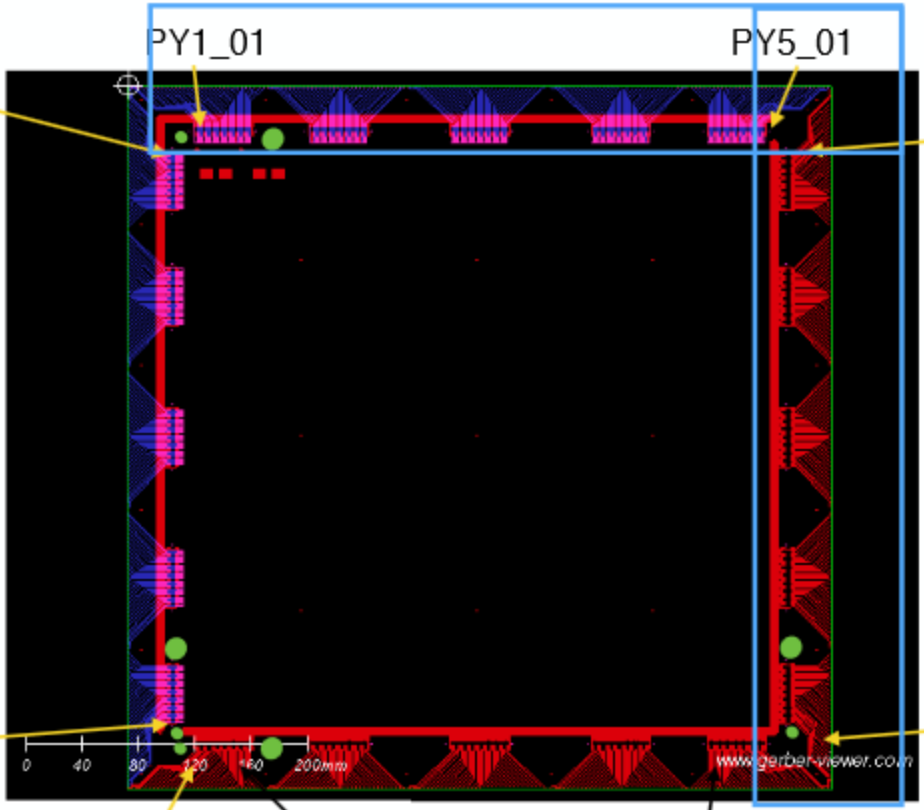
**SX1-5 Hor.**
**SY1-5 Vert.**

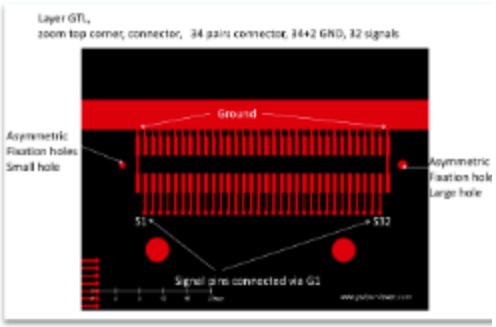
**For more than one anode we just continue the counting in next anodes**

**For 3x1x1:**
**SX1-SX20**
**SY1-SY10**

Also the naming of connectors on a side will do the same from the side of the small hole SX1 –SX5

Pulser or bridge connectors

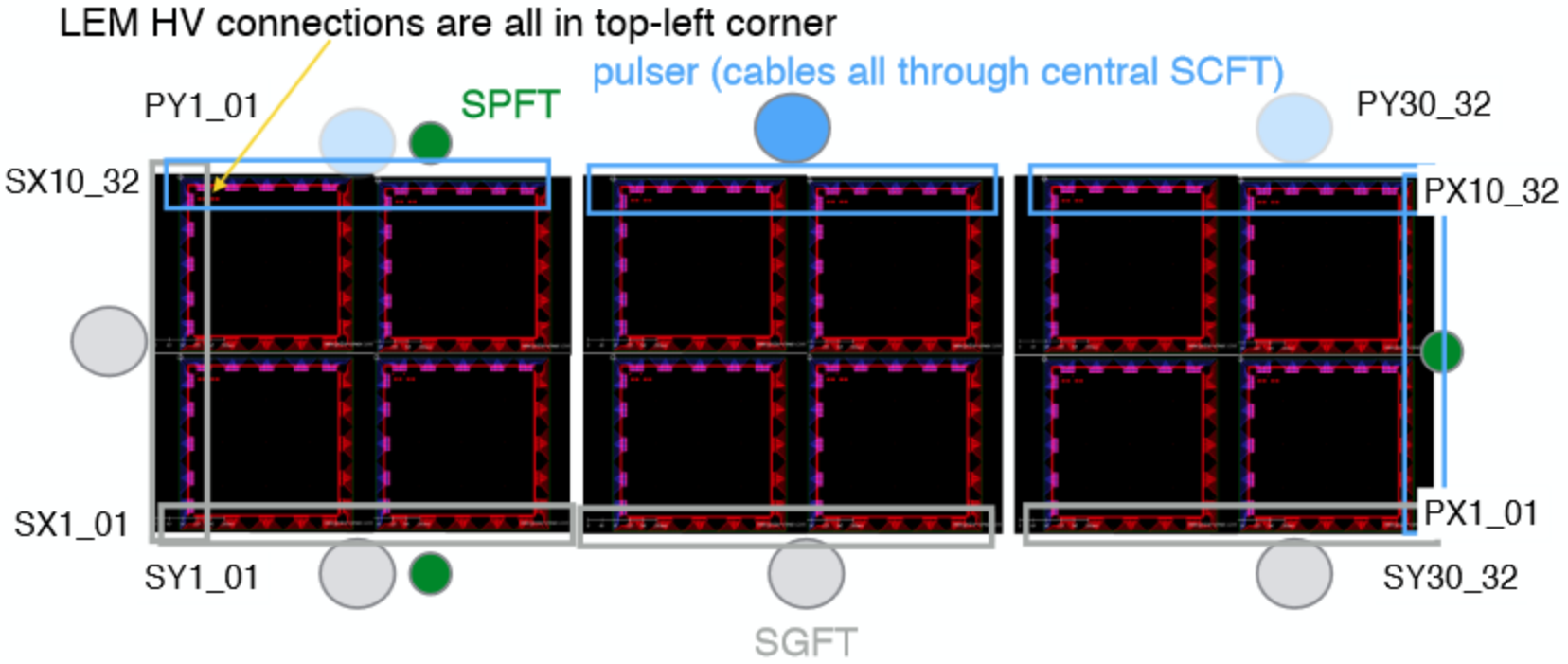


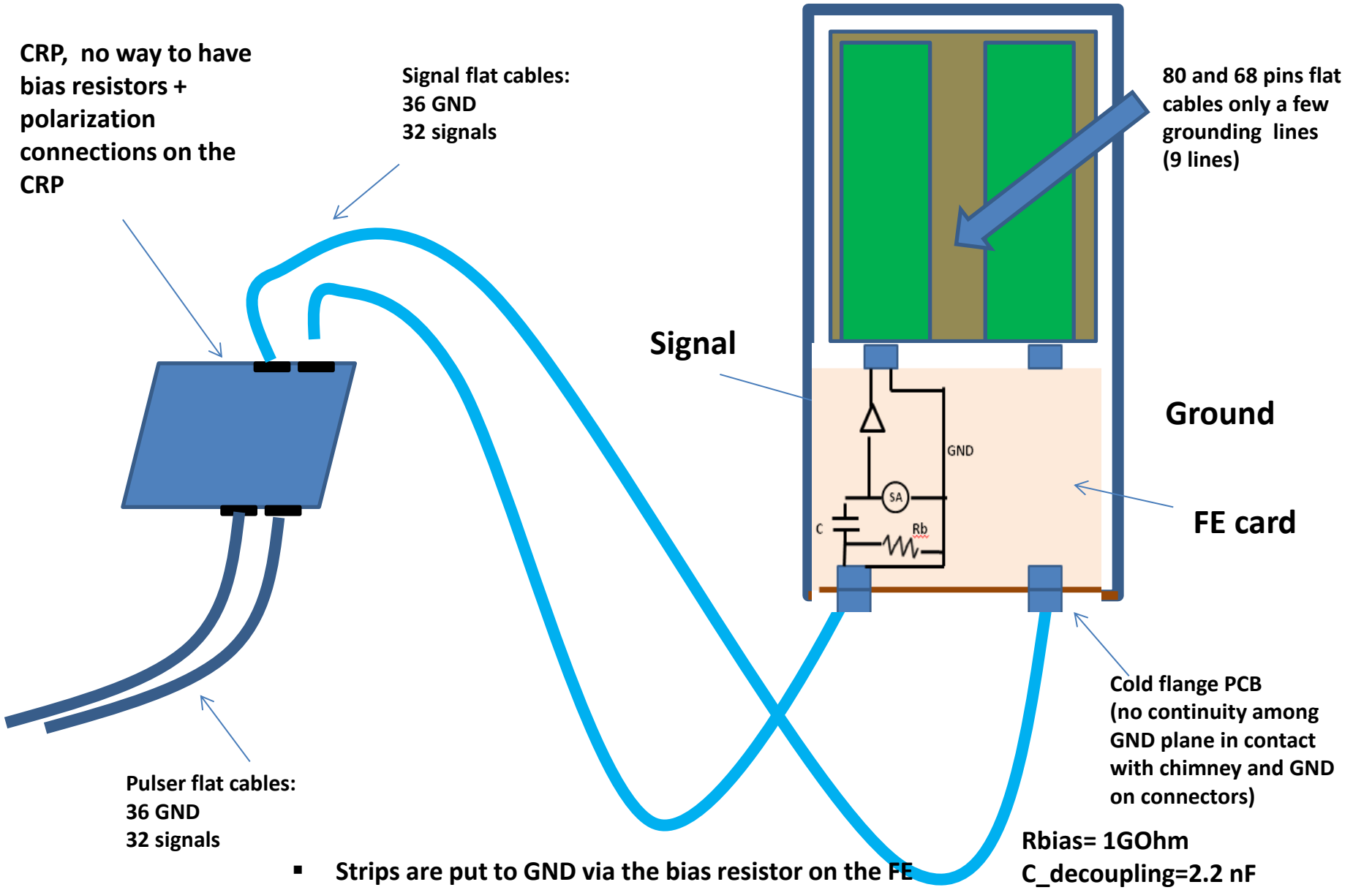

connectors have asymmetric holes to not make mistakes.
Ch 1 always starts on the small hole.

3x1x1 Meeting March 24th
and last on April 28th

This is how the CRP will be mounted and LEM-HV cables cut to match this layout.
After next week- No going back!

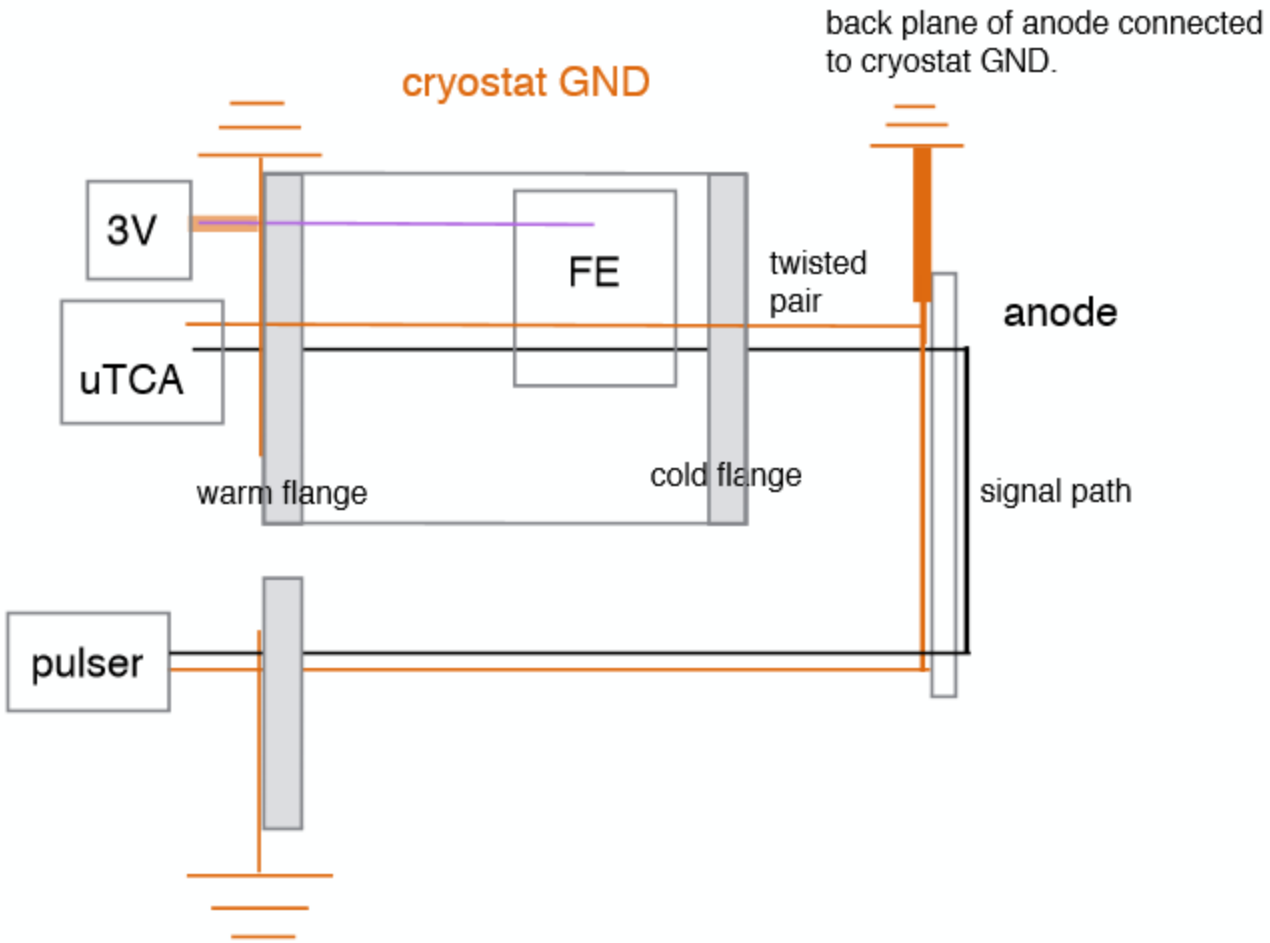



1. if we link the anode copper ground tracks as proposed in previous slide, then pulser/ signal have common GND
2. Do we agree on this layout and naming convention? (S,P)-(X,Y)-connector#_pin#




- Strips are put to GND via the bias resistor on the FE card
- Ground rings on anode grounded via a few conductors in the flat cables in the chimneys

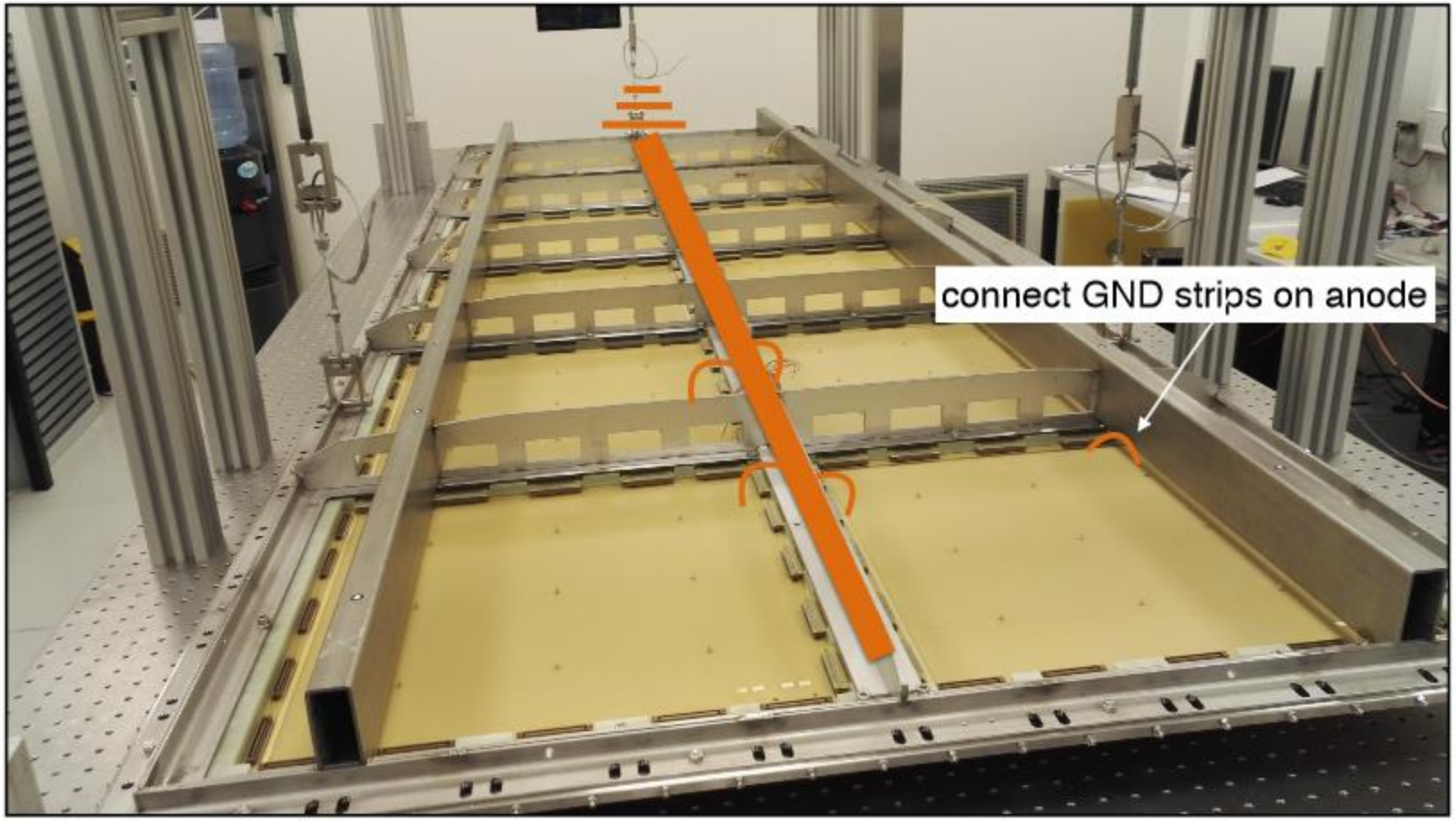
Rbias= 1GOhm
C_decoupling=2.2 nF
All HV rated
Diode pair as surge arrestors
(defined in past presentations)

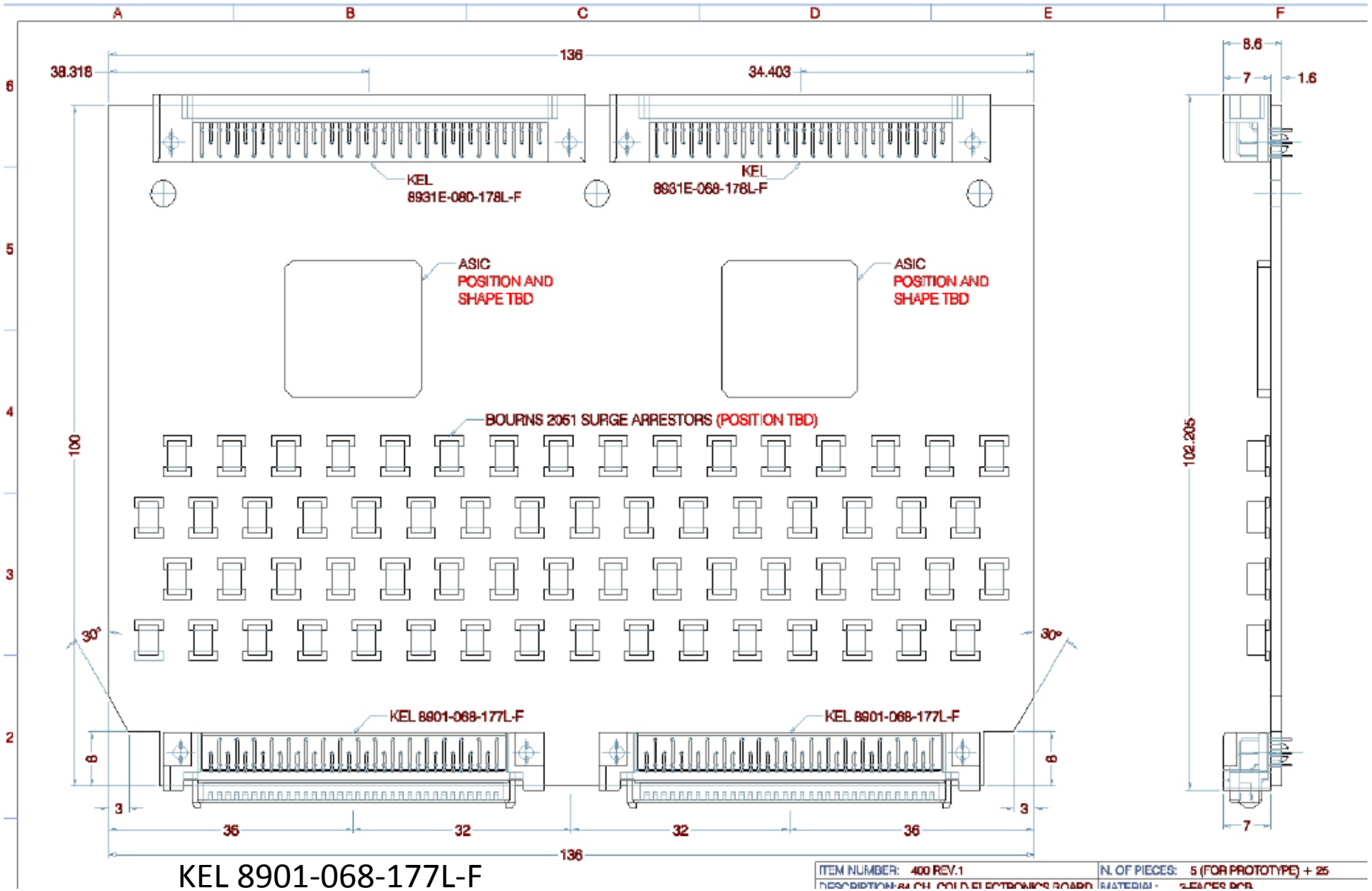

back plane of anode connected
to cryostat GND.
cryostat GND
3V
FE
twisted
pair
anode
uTCA
warm flange
cold flange
signal path
pulser

ETH

# copper strip on CRP

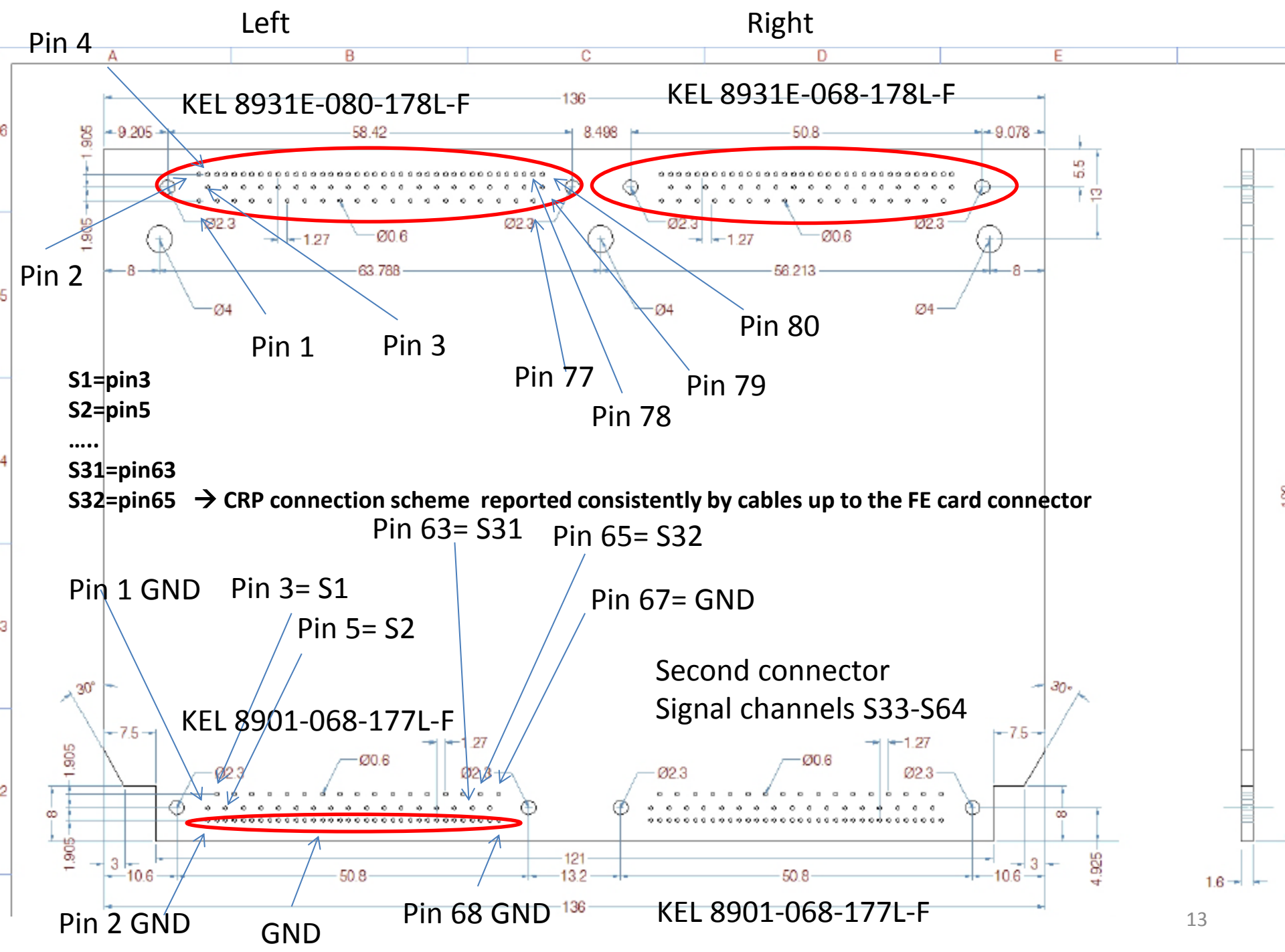
WA105



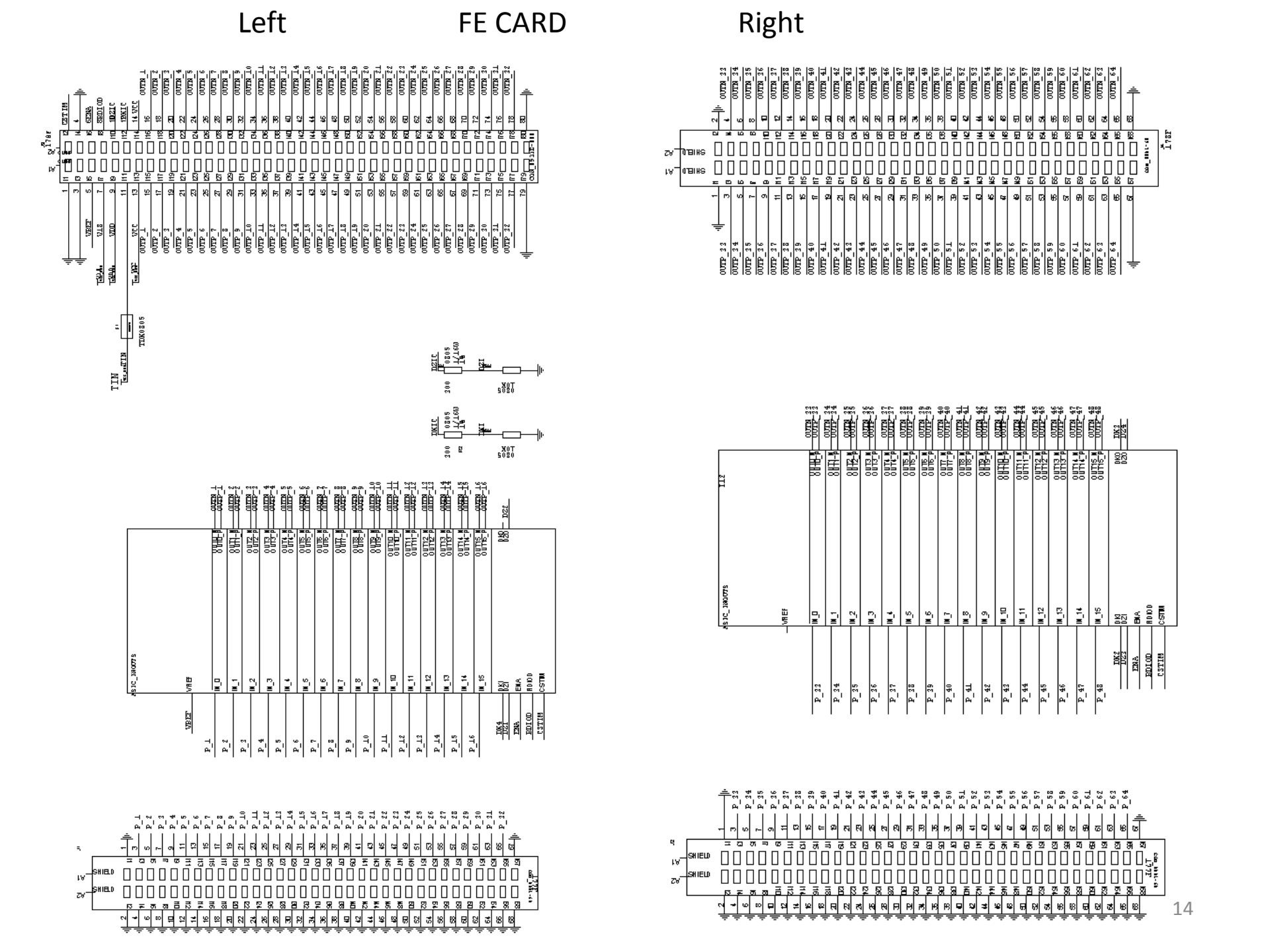



KEL 8901-068-177L-F

KEL 8901-068-177L-F

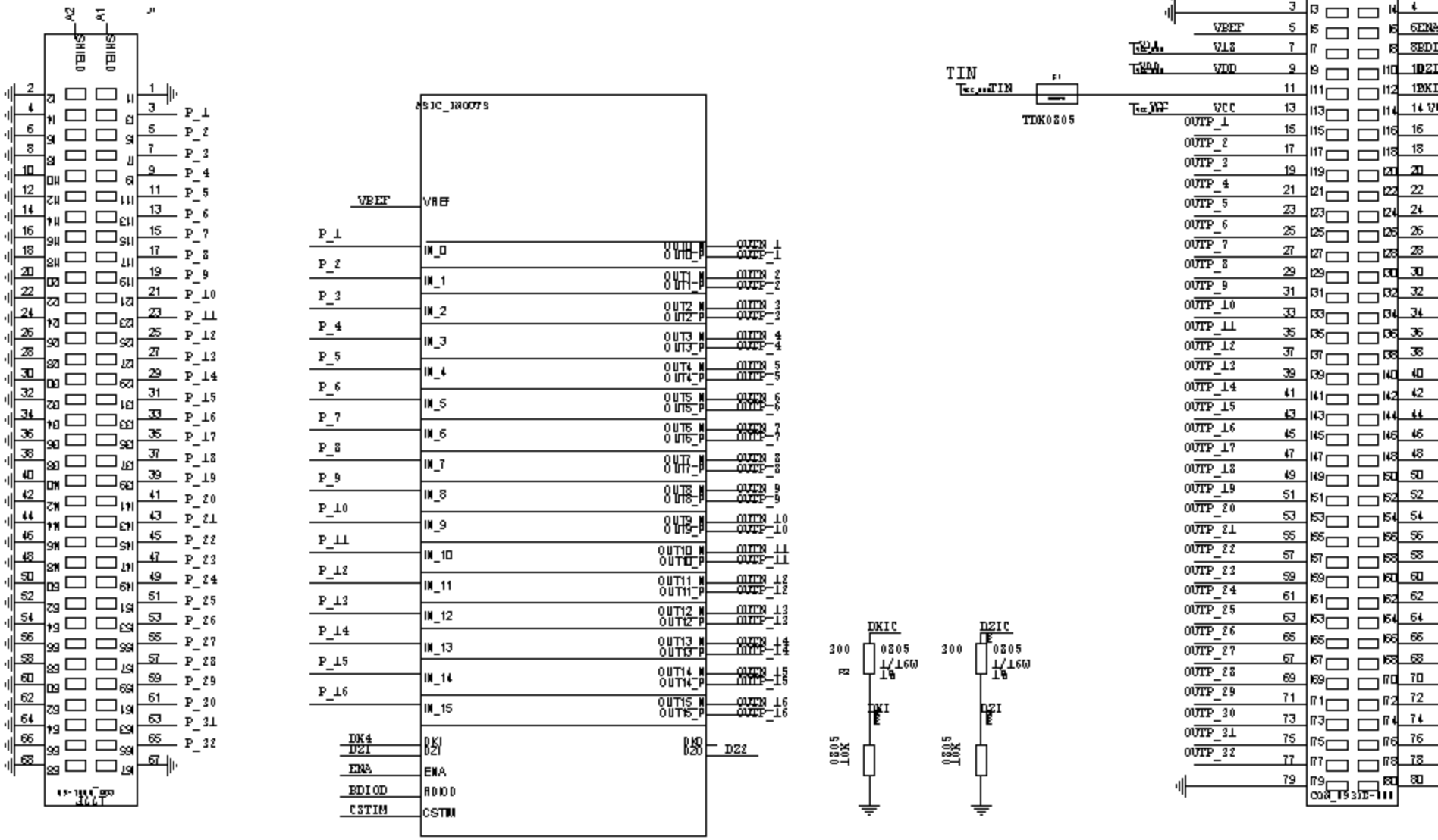

Left
Right
Pin 4
KEL 8931E-080-178L-F
KEL 8931E-068-178L-F
Pin 2
Pin 1
Pin 3
Pin 77
Pin 78
Pin 79
Pin 80
S1=pin3
S2=pin5
.....
S31=pin63
S32=pin65 → CRP connection scheme reported consistently by cables up to the FE card connector
Pin 63= S31
Pin 65= S32
Pin 1 GND
Pin 3= S1
Pin 5= S2
Pin 67= GND
Second connector
Signal channels S33-S64
KEL 8901-068-177L-F
Pin 2 GND
GND
Pin 68 GND
KEL 8901-068-177L-F

Left FE CARD Right



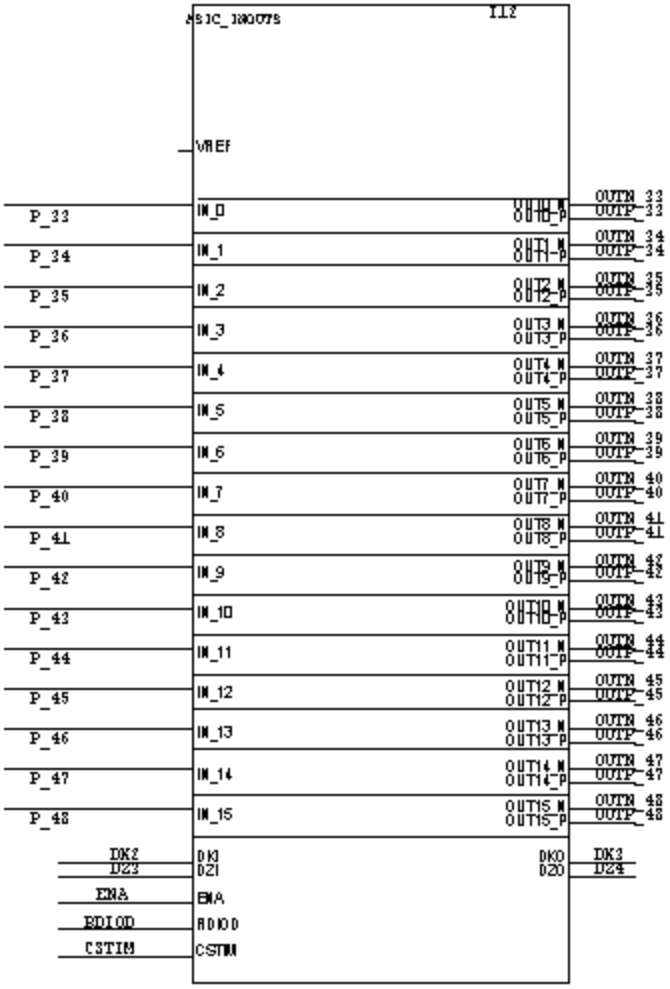
# FE CARD

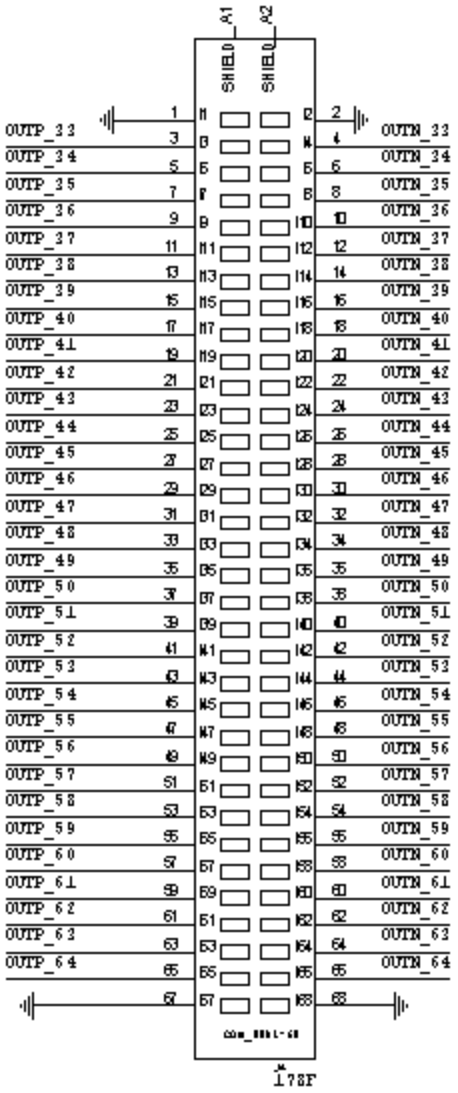
LEFT → to 80 pins flat cable



FE CARD

Right → to 68 pins flat cable

## Pin assignments on 80 pins output connector of FE card

1 GND
2 CSTIM (pulser)
3 GND
4 GND
5 VREF
6 ENA
7 V18
8 RDIOD
9 VDD
10 DZIC
11 TIN
12 DKIK
13 VCC
14 VCC

(Slow control, power block)
Pins 1-14

15 OUTP_1 differential out CH1
16 OUTN_1

17 OUTP_2
18 OUTN_2

19 OUTP_3
20 OUTN_3

....

75 OUTP_31
76 OUTN_31
77 OUTP_32
78 OUTN_32

79 GND
80 GND

## Pin assignments on 68 pins output connector of FE card

1 GND
2 GND

3 OUTP_33  differential out CH33
4 OUTN_33
5 OUTP_34
6 OUTN_34
……

63 OUTP_63
64 OUTN_63
65 OUTP_64
66 OUTN_64

67 GND
68 GND

# Summary of flat cable connectivity

**Pulser (80 pins flat cable):**
2 CSTIM (pulser signal for charge injection for the amplifier calibration), pulser connector should be connected to the GND plane too

**4 Controls (80 pins flat cable):**
6 ENA (Enable level: 0 or 3.3 V)
8 RDIOD (Feedback comp. diode level: 0 or 3.3 V)
10 DZIC (Slow control data spi-'like')
12 DKIK (Slow control clock spi-'like')

**6 Voltages (80 pins flat cable, fixed levels, provided by the filtered LV PS):**
5 VREF 1.4 V
9 VDD 3.3 V
7 V18 1.8 V
11 TIN 2.1 V
13 VCC 3.3 V
14 VCC 3.3 V (duplicated line due to the current consumption)

**5 Ground connections connector 80 pins:**
1 GND
3 GND
4 GND
79 GND
80 GND

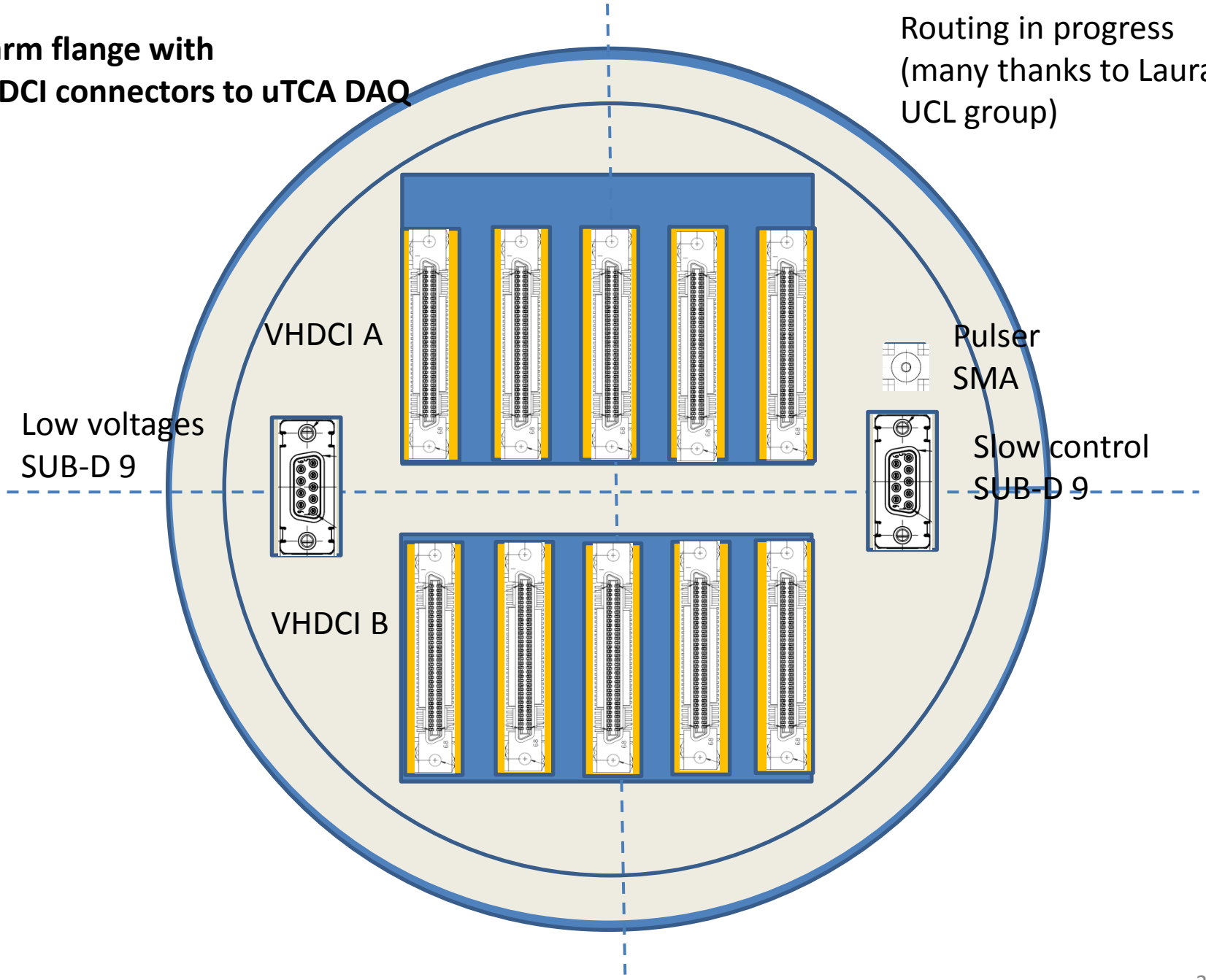
**4 Ground connections connector 68 pins:**
1 GND
2 GND
67 GND
68 GND

**128 signal differential lines (+/-):**
64 (80 pins connector) +64 (68 pins connector) =128

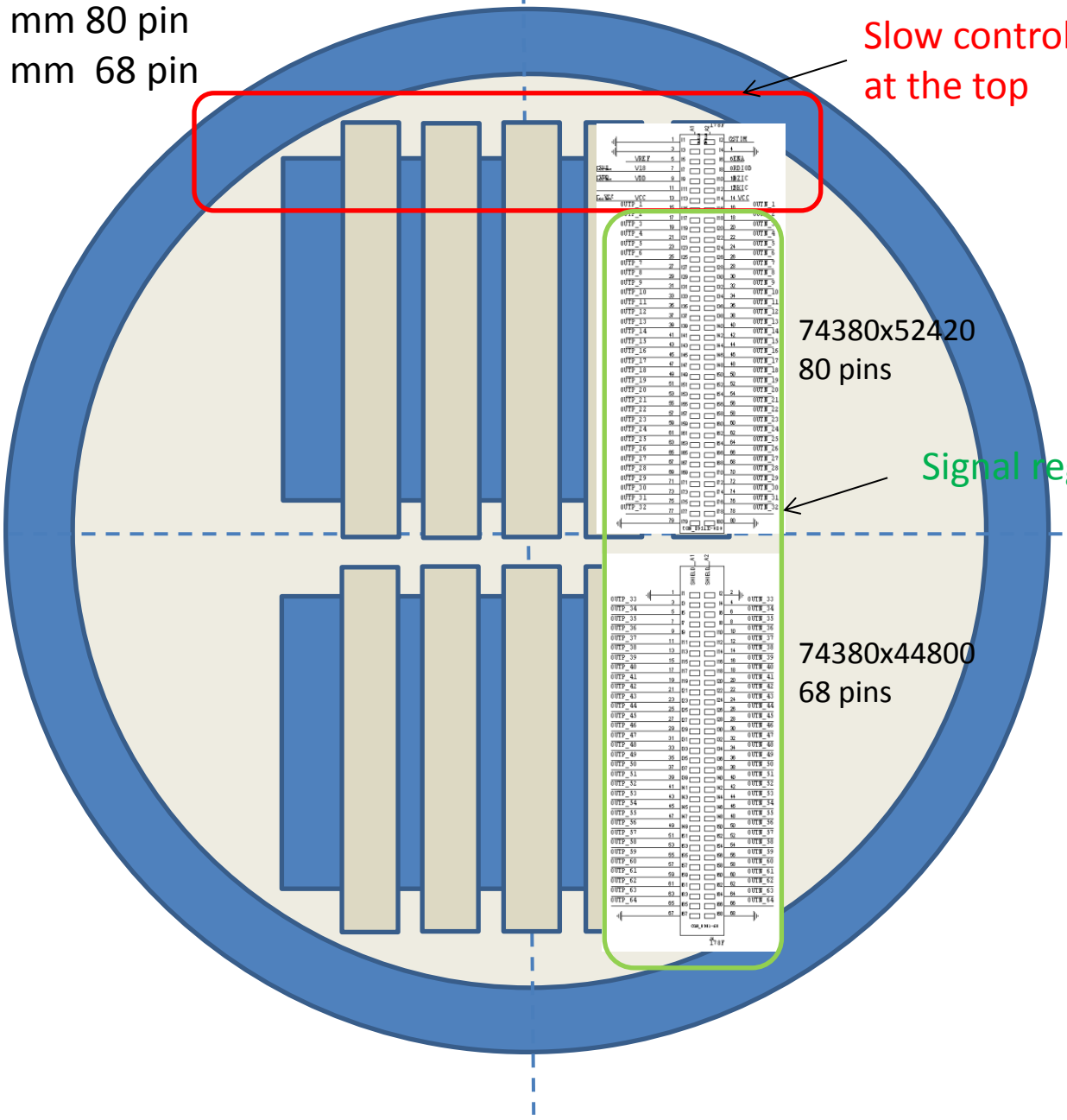
**Total number of lines (80+68)=148 = 1 pulser +4 SC +6 LV +5 GND +4 GND +128 Signals**

**Warm flange with VHDCI connectors to uTCA DAQ**

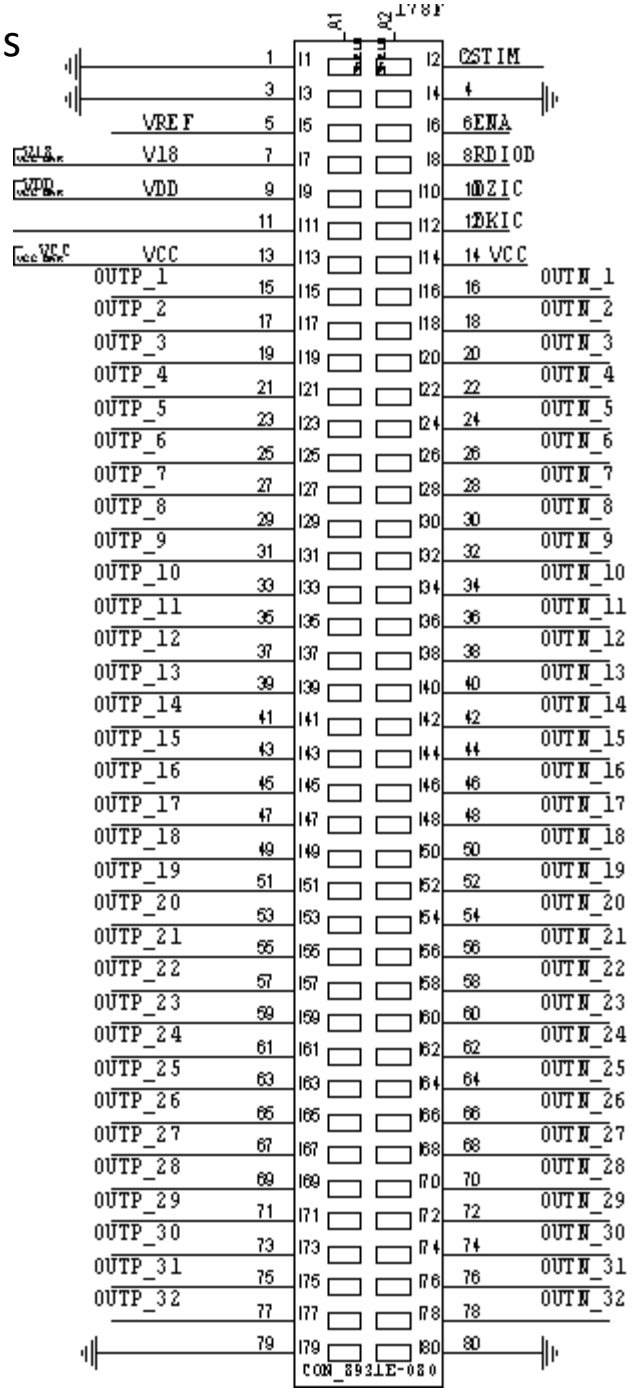
Routing in progress (many thanks to Laura and UCL group)



KEL connectors:
63.53 mm x 8.6 mm 80 pin
55.91 mm x 8.6 mm  68 pin
Pitch 13.2 mm

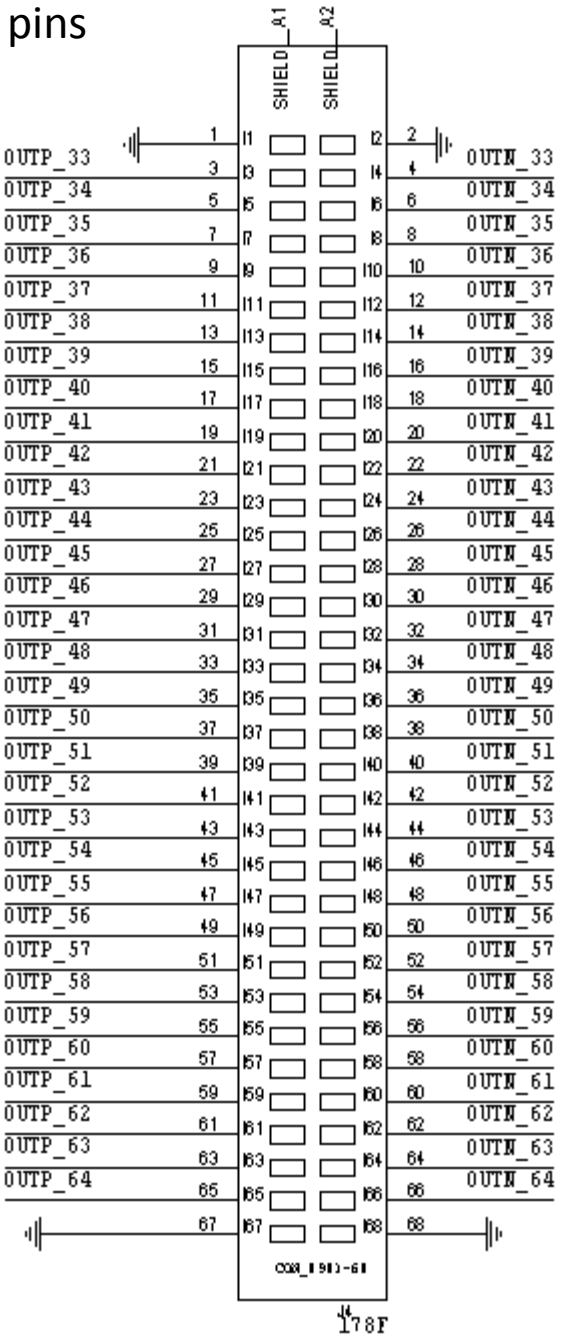


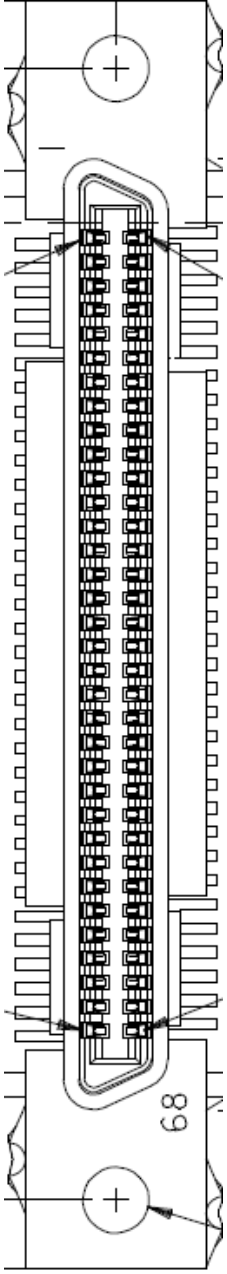
80 pins




KEL connectors

68 pins

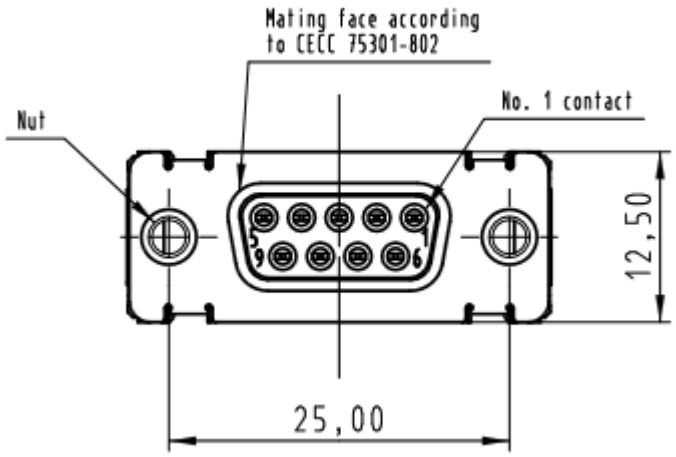





Molex to uTCA crate (32 channels)

| Pin | | Pin | |
|---|---|---|---|
| 1 | S1_P | 35 | S1_N |
| 2 | S2_P | 36 | S2_N |
| 3 | S3_P | 37 | S3_N |
| …. | | | |
| 16 | S16_P | 50 | S16_N |
| 17 | GND | 51 | GND |
| 18 | GND | 52 | GND |
| 19 | S17_P | 53 | S17_N |
| ….. | | | |
| 33 | S31_P | 67 | S31_N |
| 34 | S32_P | 68 | S32_N |

SUB-D9 Slow control

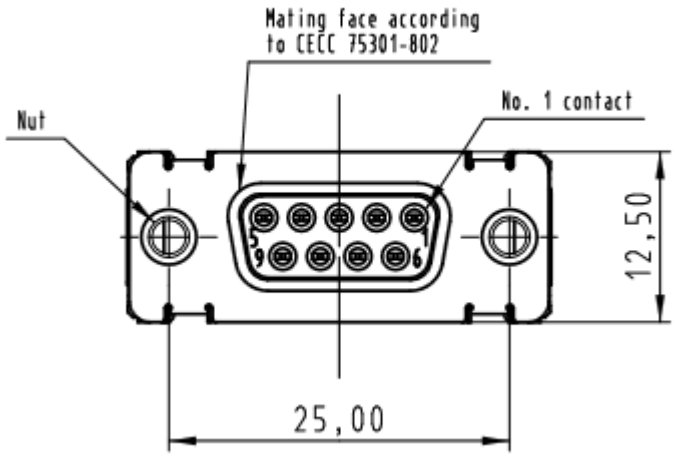



Pin1 →KEL80_6 ENA (Enable level: 0 or 3.3 V) (connector 1)
Pin2 →KEL80_6 ENA (Enable level: 0 or 3.3 V) (connector 2)
Pin 3→KEL80_6 ENA (Enable level: 0 or 3.3 V) (connector 3)
Pin 4→KEL80_6 ENA (Enable level: 0 or 3.3 V) (connector 4)
Pin 5→KEL80_6 ENA (Enable level: 0 or 3.3 V) (connector 5)
Pin 6→GND plane

Connection in parallel
To the 5 KEL80

Pin 7→KEL80_8 RDIOD (Feedback comp. diode level: 0 or 3.3 V)
Pin8 →KEL80_10 DZIC (Slow control data spi-‘like’)
Pin 9→KEL80_12 DKIK (Slow control clock spi-‘like’)
Shield → GND plane

# SUB-D9 Low voltages




Pin1 → KEL80_5 VREF 1.4 V
Pin2 → KEL80_9 VDD 3.3 V
Pin3 → KEL80_7 V18 1.8 V
Pin4 → KEL80_11 TIN 2.1 V
Pin5 → KEL80_13 VCC 3.3 V
Pin6 → KEL80_14 VCC 3.3 V (duplicated line due to the current consumption)
Pins7-9 → GND plane
Shield → GND plane

Connection in parallel to the 5 KEL80

**List of electrical equipments:**

**Heinzinger HV PS for cathode:** ground defined by the cryostat by connecting the GND of the cable to the cryostat, ripple filter in series to the cable

**LEM HV PS:** similar to cathode HV PS

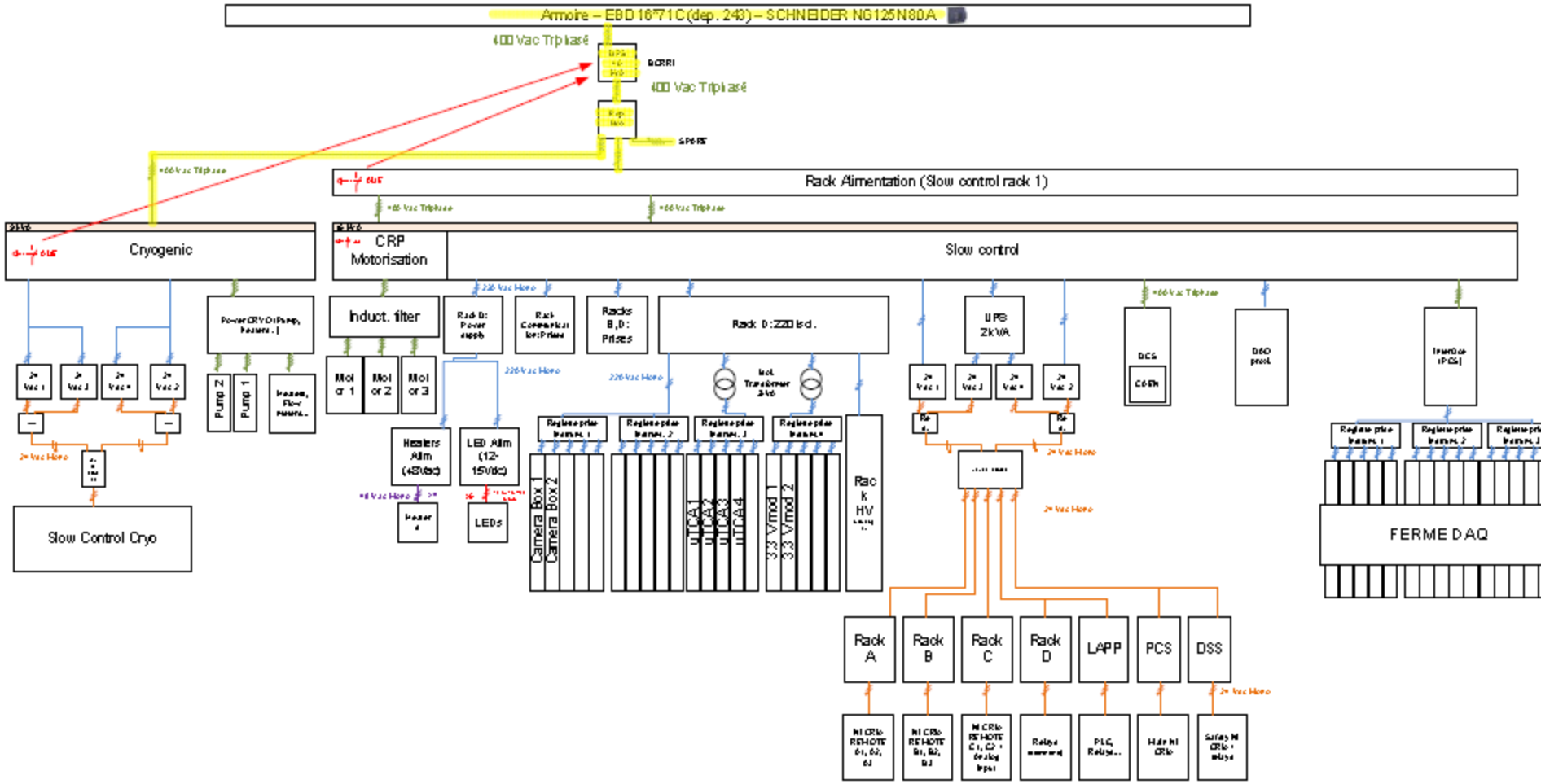
**Cold Electronics PS x2:** 230V, 350W, from dedicated multiplug isolation transformer to remove noise from other equipments connected to the same main, PS connected via shielded cables to chimneys patch boxes, GND and shield of the cables connected to cryostat

**uTCA crates x4:** 230V, 300 W from multiplug isolation transformer, ADC differential connections to patch box. GND defined via shield of the cables to the cryostat. ADC output via optical connections only. uTCA crate contains cards reading 64 ADCs each.

**Pulser:** pulser for calibrations of ASICS and strips, W from multiplug isolation transformer, 230V, 300W

**Slow control equipments:** GND referred to cryostat

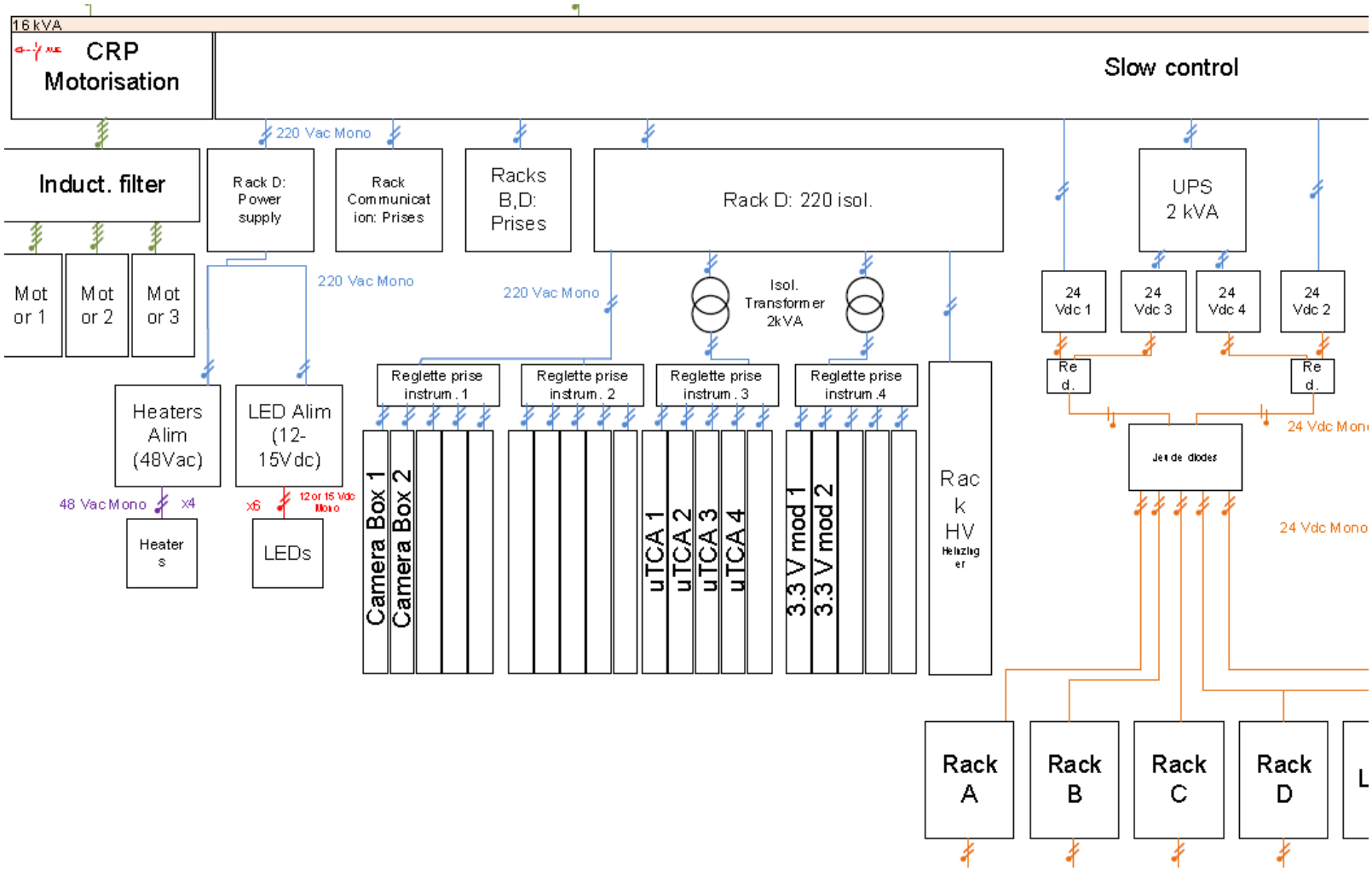
Final scheme defined last Friday, under implementation by July 18th



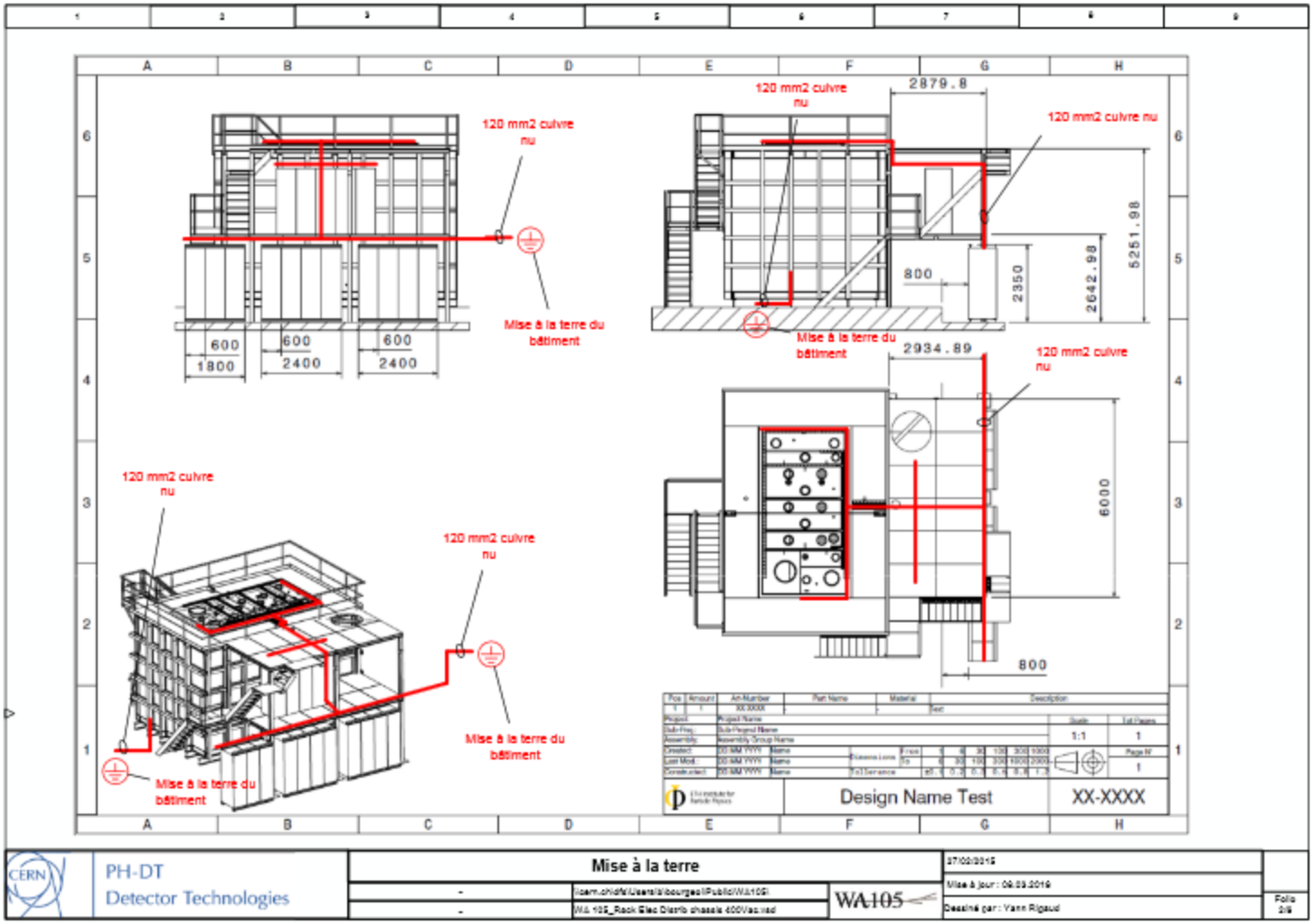
Two separate isolation transformers:

a) For the LV PS (the most critical part of the system)

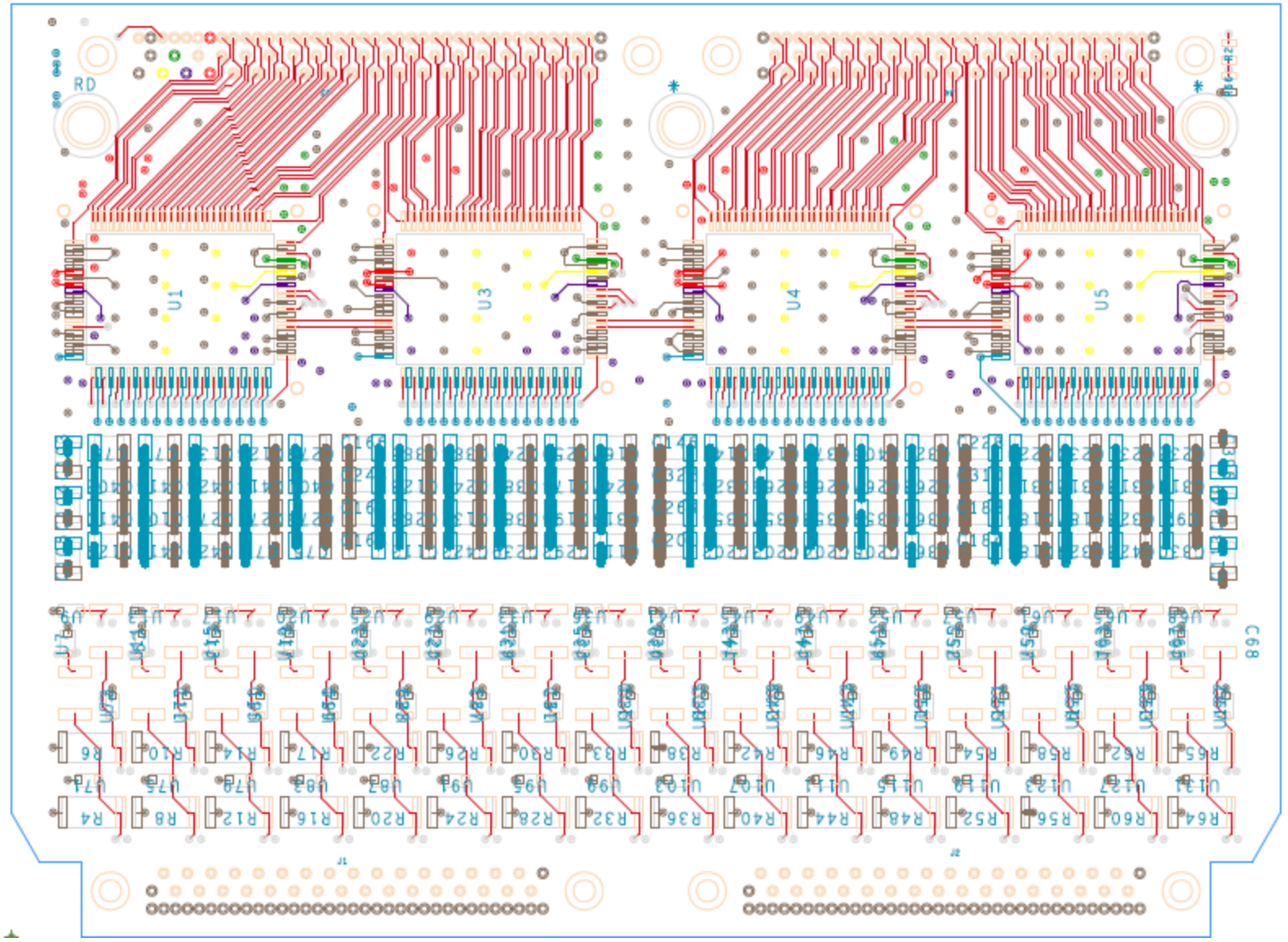
b) For the other FE equipments on the roof of the cryostat (uTCA crates, pulser etc ..)



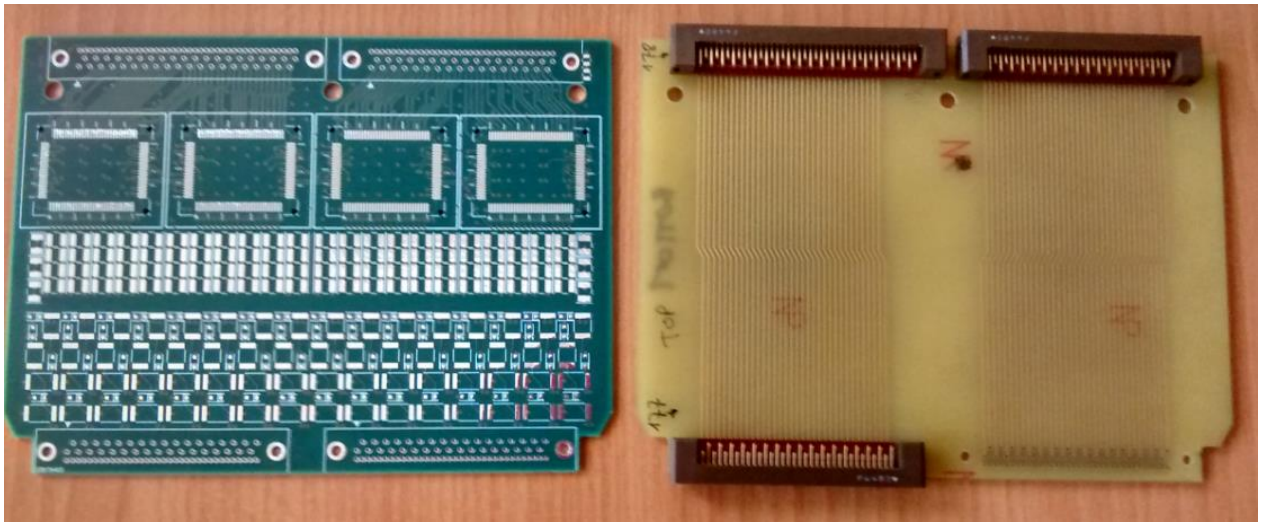
# GND copper layout scheme from Bourgeois



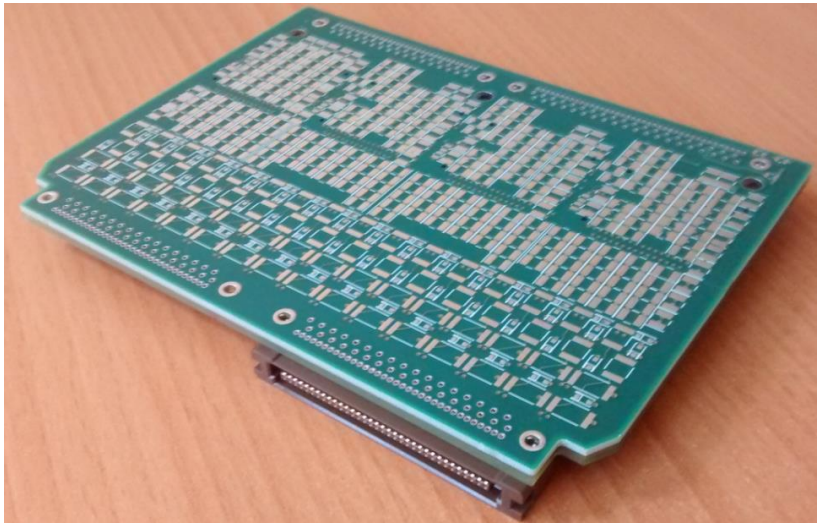
FE cards, already produced in a pre-batch for the 4 chimneys of 3x1

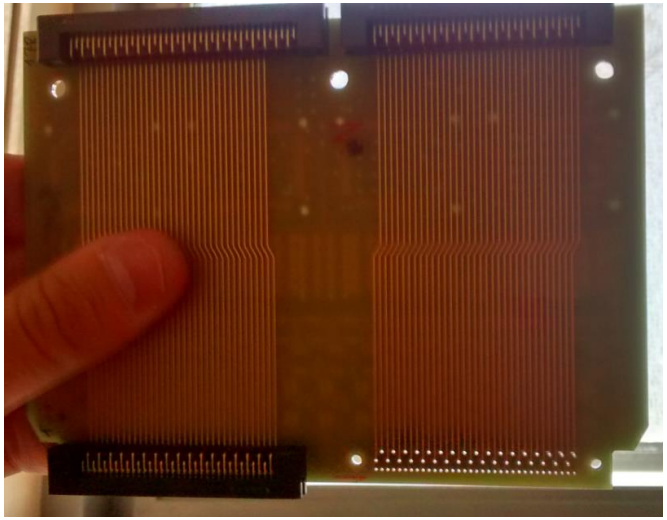


**The final FE card has extactly the same mechanical layout of the fake FE → no problems expected at the level of the insertion**



The two layouts and all patterns of holes for the connectors correspond perfectly. When superimposing the two cards the connectors can be inserted with their pins easily crossing the two cards in a row and there is no difference on all the card borders.





# Next tests:

1) Week of June 20:
insertion tests of FE cards
check with diodes: small plug with a battery which uses one of the 9 GND lines and check the return of voltage on the other 8 GND lines by lighting diodes: the topology is such as the GND lines are always at the extremities of the connectors, so if they are in good contact the entire connector is well inserted

2)Possible continuity tests after moving the end-cap to the cryostat of all anodes (if anode pulser is functional) by using the fake FE cards → use of a small DAQ system (raspberry pi) with a relays switchbox to systematically acquire all the pulser waveforms on a digital scope

July4th: movement of the end-cap.
July 18th: grounding and electrical connections ready

3) After July 18$^{th}$: Extensive noise tests of the FE electronics + grounding system after cryostat closure and grounding system implementation (in between July 18th and July 30th) → need the warm flange and grounding scheme in place