Photon Detector Readout Plan

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Outline of Talk

- Introduction
- Readout System Requirements
- Overview of Current SSP Module
  - Performance Attributes
  - Overview of Architecture
  - Production to Date
  - A Few Performance Results
  - Lessons Learned
- Changes for ProtoDUNE
  - New Cables, Connectors, Cable plant
  - Timing System Changes
  - Power System Changes
  - Minor Modifications for Grounding Plan
  - New Flange Board
- Status & Schedule
- Summary

Introduction

- **The Following Review Questions will be addressed (from the Charge):**

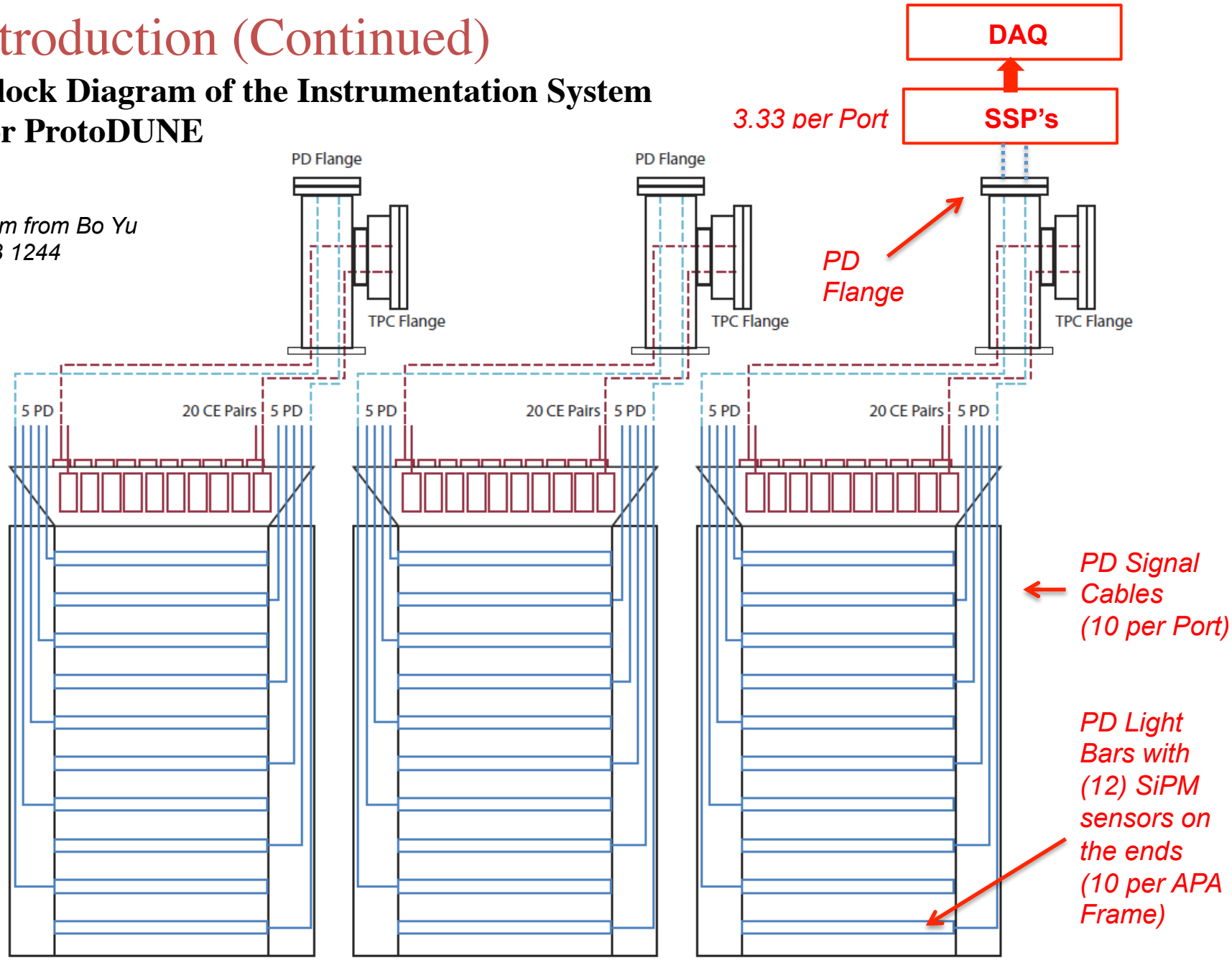
1. **Does the Photon Detector System design enable validation and refinement of the DUNE photon detector requirements?**
2. **Are Photon Detector System risks captured and is there a plan for managing and mitigating these risks?**
3. **Does the design lead to a reasonable production schedule, including QA, transport, installation and commissioning?**
4. **Does the documentation of the Photon Detector System technical design provide sufficiently comprehensive analysis and justification for the Photon Detector System design adopted?**
5. **Is the Photon Detector system scope well defined and complete? Are all Photon Detector System interfaces to other detector components: APA, cryostat and DAQ systems documented, clearly identified and complete? Do the electronics feedthrough port and TPC integrated 3D models adequately represent the mechanical, electrical and electronic interfaces to the Photon Detector System? Is the cabling, power and calibration well defined and understood? Is the grounding and shielding understood and adequate?**
6. Are the Photon Detector System 3D model(s), top level assembly drawings, detail/part drawings and material and process specifications sufficiently complete to demonstrate that the design can be constructed and installed?
7. **Are operation conditions listed, understood and comprehensive? Is there an adequate calibration plan?**
8. Are the Photon Detector System engineering analyses sufficiently comprehensive for safe handling, installation and operation at the CERN Neutrino Platform? Is the installation plan sufficiently well developed? Is the design for installation tooling adequate for installing the photon system?
9. **Have applicable lessons-learned from previous LArTPC devices been documented and implemented into the QA plan? Are the Photon Detector System quality control test plans and inspection regimes sufficiently comprehensive to assure efficient commissioning and adequate operational performance of the NP04 experiment?**

(Green = Will cover in this Talk; Blue = Will mention in this Talk)

Introduction (Continued)

- **Block Diagram of the Instrumentation System for ProtoDUNE**

Diagram from Bo Yu DocDB 1244



⇨ *No Cold Electronics in the PD system!*

Initial Readout Requirements

- **Initial PD Readout Electronics Requirements developed with idea to build a very high-performance readout system, to validate the detector development**
  - Initially, performance requirements were vague; Few simulations had been done
  - Goal was to support a wide range of R&D to help define the ultimate requirements
    - ⇨ *35 ton Detector, TallBo, University R&D…*
  - For the 35-ton Detector, read out one SiPM per channel (more later…)

Performance Parameter	Initial Target	Achieved (35-ton)
Time Resolution	< 30 nS wrt T0	~2-3 nS on single pe
Charge Resolution	0.25% pe equiv.	66 nA @ 150 MSPS
Dynamic Range	1000:1 (pe equiv)	14-bit
Linearity	Sufficient to resolve 1 pe	< 1 % INL; < 1 ADC count DNL
Multi-Hit Capability	Sufficient to measure Triplet (late) photons	Continuous waveform sampling, 13 uS buffer @ 150 MSPS
Dead Time	Live up to 2 drift times either side of beam spill	No dead time up to 30 KHz/ch (1000 samples/event)
Bias Control	0.1V resolution up to 30V per channel	0.1V resolution up to 30V per channel
Calibration	On-board charge injection	On-board charge injection
Timing Interface	Time-stamp events	NOvA Timing System interface

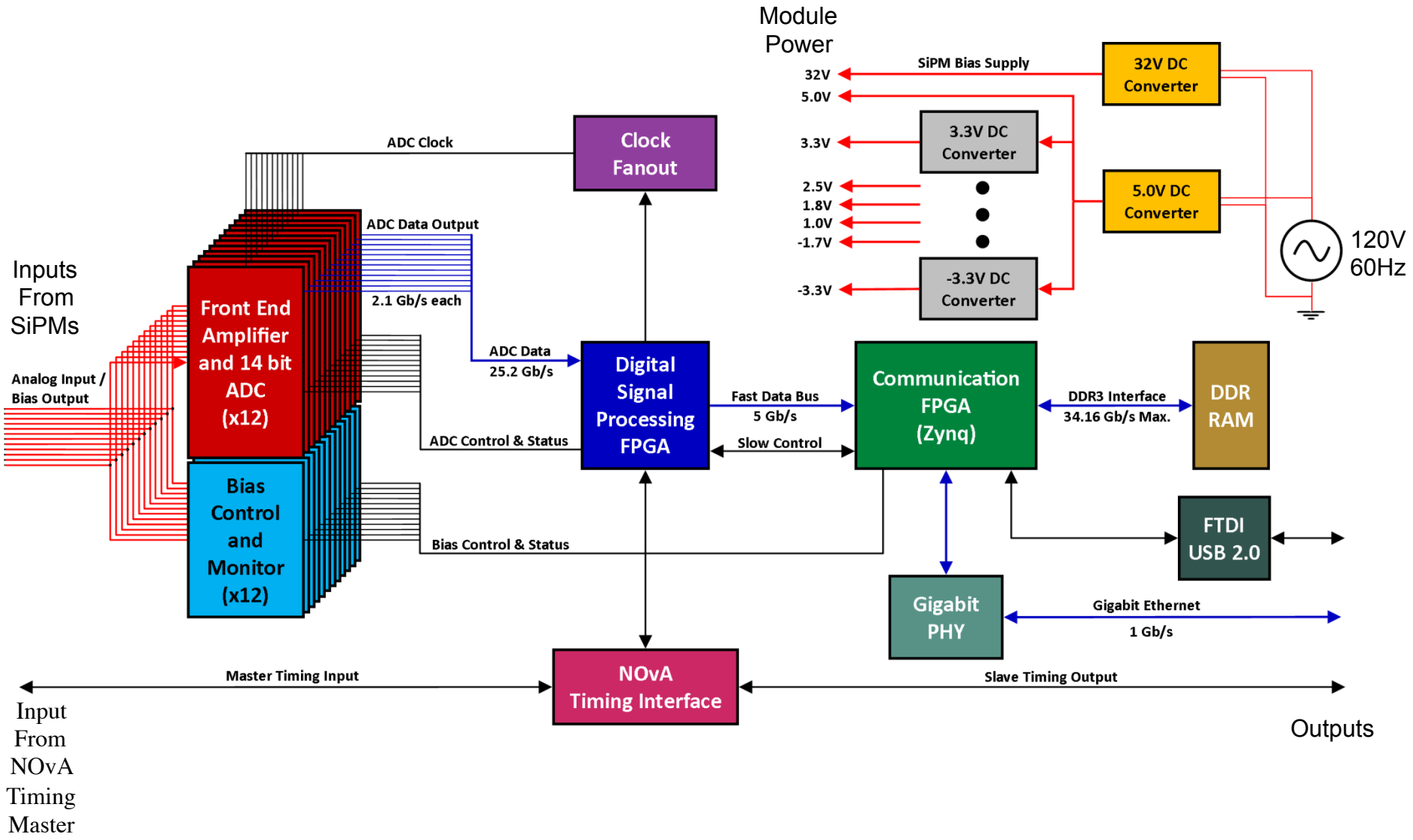
Details on requirements given in the LBNE docdb-7605, "Working Draft of Photon Detection System Electronics Requirements", N. Buchanan, Z. Djurcic, G. Drake, M. Johnson, B. Jones, J. Klein, J. Musser, S. Seibert.

Overview of the Current SSP Module

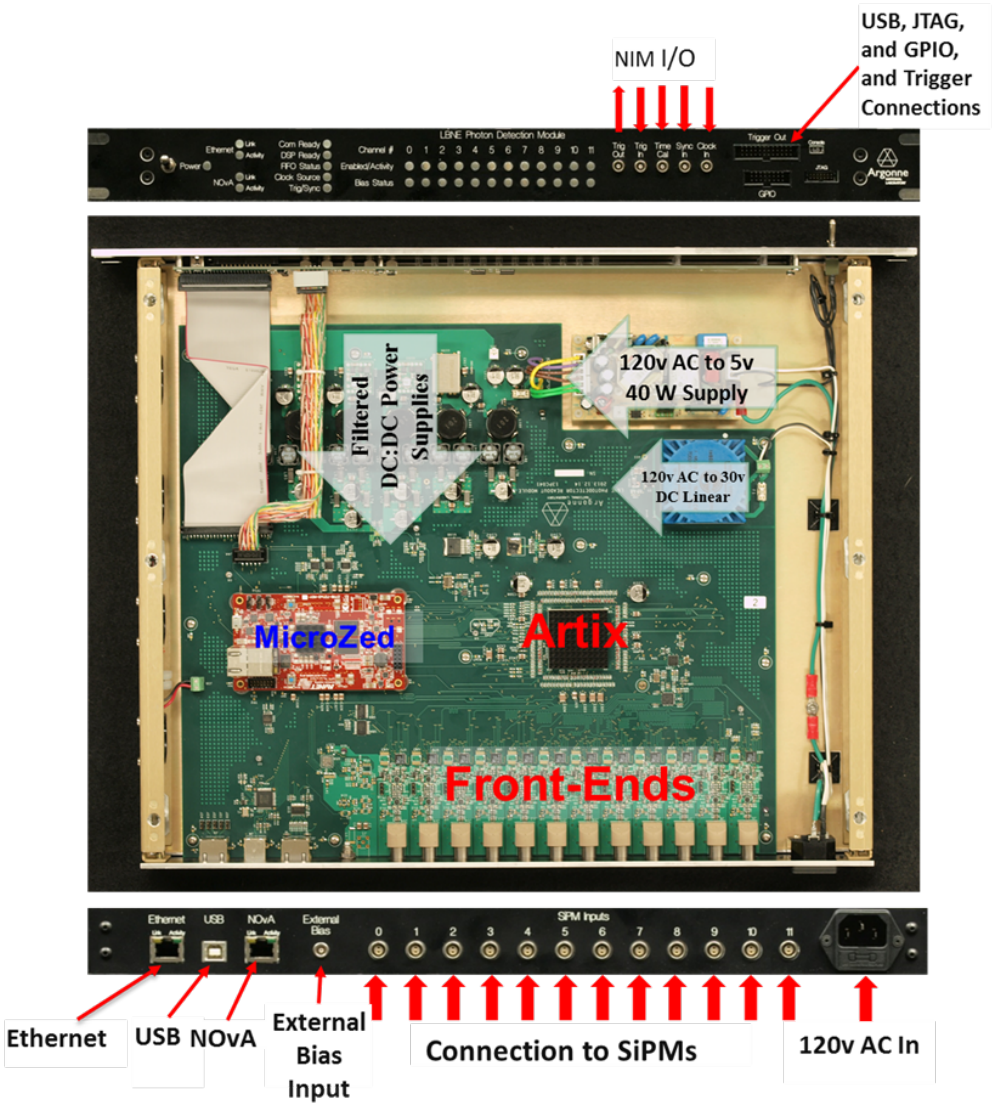
- **The Silicon Photo-multiplier Signal Processor (SSP) prototype module:**
  - High-speed waveform digitizer
  - ***Current sensitive, differential input amplifiers*** → Good noise performance over long cables
  - Each channel has a ***14-bit, 150 MSPS ADC***
  - ***Timing*** obtained using signal processing techniques on leading edge of SiPM signal (CFD)
  - 12 channels per module
  - Uses Artix FPGA for sig. proc.
  - Has NOvA Timing Interface
  - ***Uses 120VAC; On-board LV power***
  - Has internal prog. SiPM bias (30V)
  - Trigger: self or external
  - ***Has Trigger Out signal***
  - Deep data buffering – 13 μsec
  - ***No dead-time*** (up to 30 KHz/ch)
  - Programmable DAQ interface
  - ***USB & GbE communications***
  - Internal charge injection
  - Internal bias monitoring

- ⇨ ***1U rack-mounted unit***
- ⇨ ***Completely self-contained: Plug & Play***
  - ⇨ ***No crates needed***
  - ⇨ ***No external power supplies needed***
  - ⇨ ***No processor needed on front-end***

Block Diagram of Current SSP



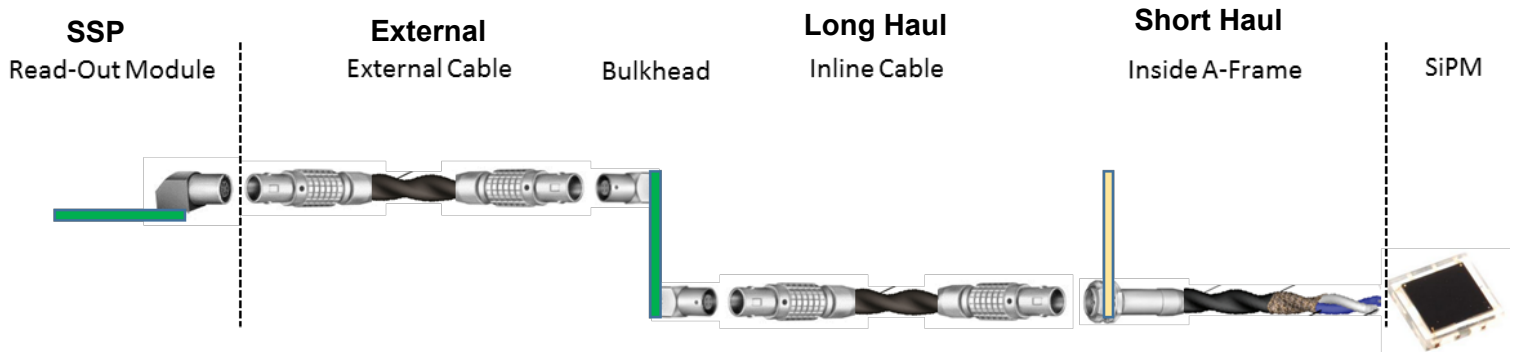
Overview of the Current SSP Module (Continued)



The Current SiPM Signal Cable Plant

- **The Current SSPs have one SiPM per readout channel**
  - Was done to ensure good performance over a long distance (~20 m)
  - Due to schedule constraints and attempt to reduce development costs, wanted to avoid use of cold electronics for this system
- **Current cable plant**
  - Gore cable: differential pair with shield & PTFE outer jacket
  - LEMO differential connectors
  - 3-segment plant: Short Haul; Long Haul; External

⇨ ***Total length for the 35-ton Detector: 20 meters***



⇨ ***We will be changing this for ProtoDUNE (more later…)***

Current Status

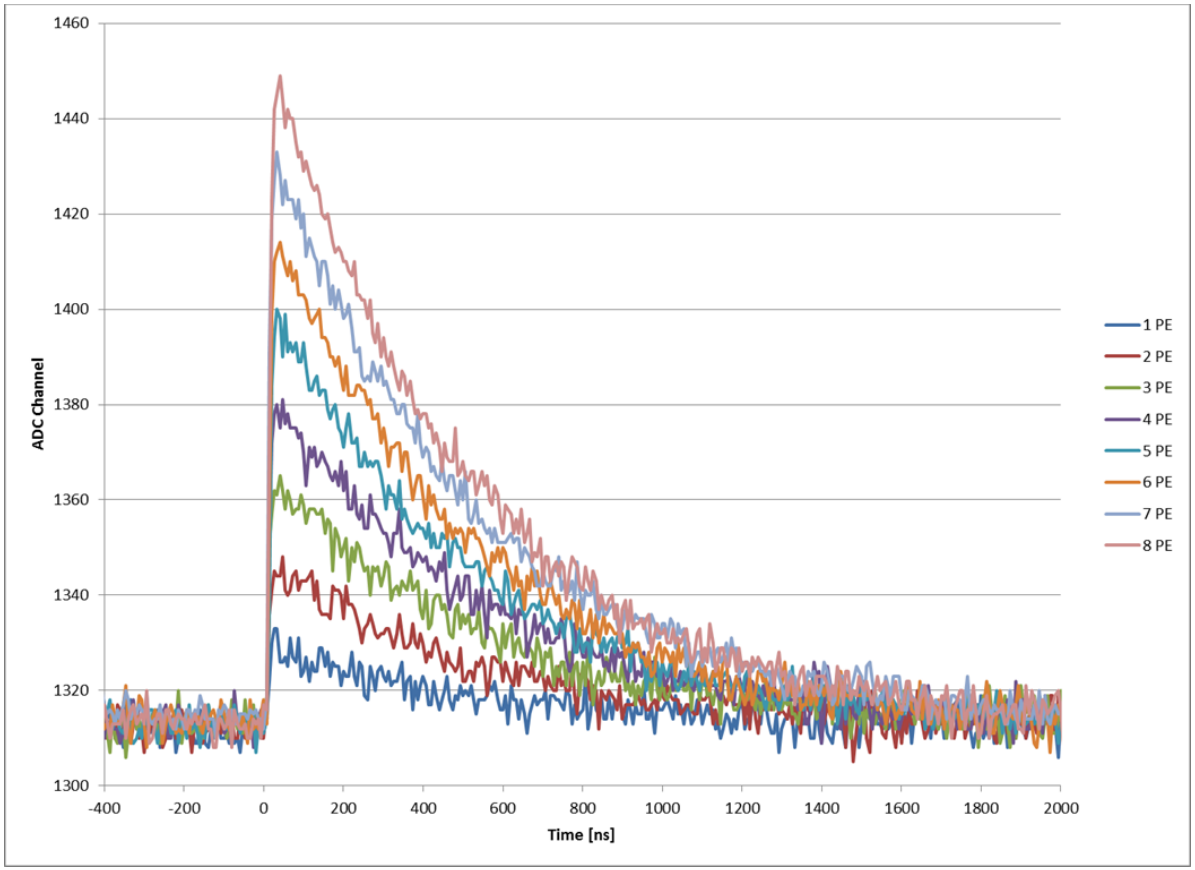
- **(4) prototype units manufactured and assembled**
  - Currently in use at: (2) IU, (1) CSU, and (1) Warwick
- **(12+) small production version units manufactured and assembled**
  - 7 installed with 35t + 1 spare at DAB
  - (1) CSU, (1) LSU, (2) ANL
  - Also, (1) used as a platform for the Calibration Module
- **Firmware development performed with 35 ton**
  - Full ADC waveforms can be read out; ADC data processing firmware is complete
  - Have implemented CF timing, peak measurement, & total charge calculations
  - USB & GbE communication interfaces fully functional
  - Control & monitoring firmware is in place, including SiPM bias control & monitoring
  - NOvA Timing interface fully functional

⇨ ***~ 2 years of experience with the system to date***

⇨ ***Several TallBo runs, Readout with the 35-ton Detector, Supported University R&D***

Performance Tests (1)

- **Digitize Spontaneous Photo-Electrons from a SiPM**
  - SiPM immersed in LN2; Cable length 5 meters



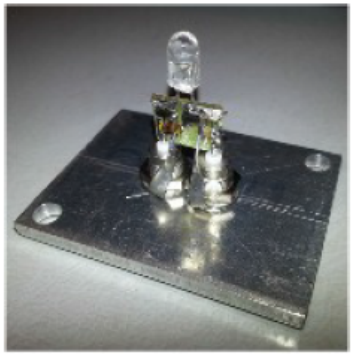
Waveform capture of SiPM signals using an SSP

(Results are similar for 20 meters)

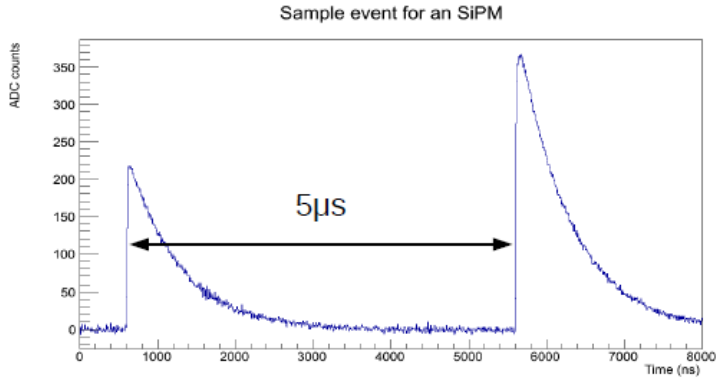
⇨ ***Good Signal-to-Noise performance ~7 for a single pe***
⇨ ***Can clearly see single pe's***
⇨ ***Good separation between multiple photo-electron peaks***

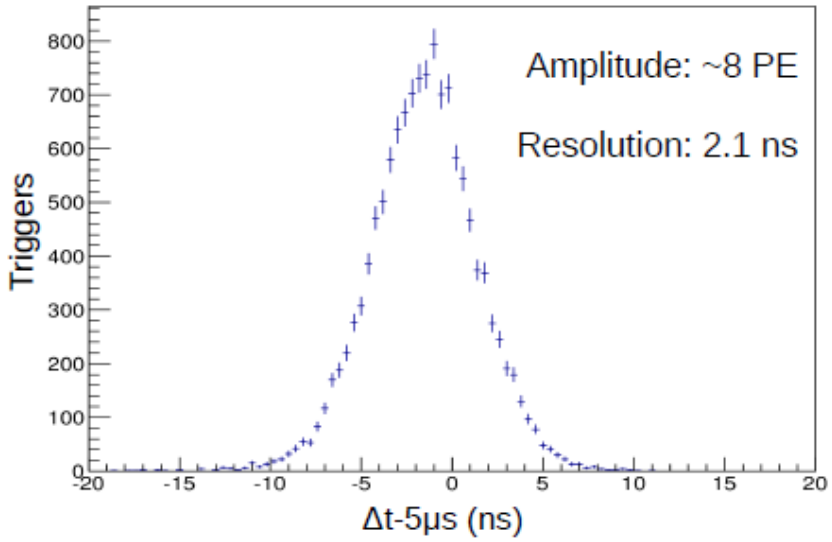
Performance Tests (2)

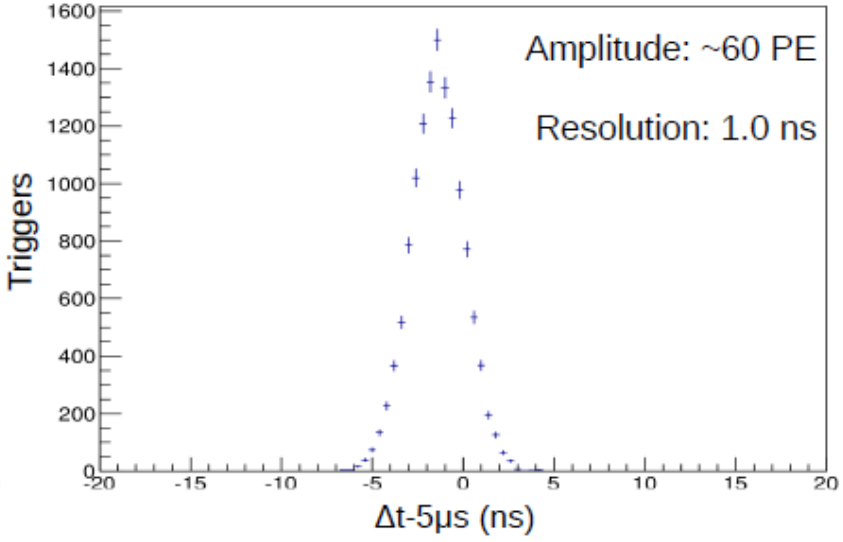
- **Timing Resolution Study using 2 LED pulses (B. Howard, IU – DocDB 10307)**
  - SiPM immersed in LN2; Cable length 5 meters



370 nm LED with pulser circuit



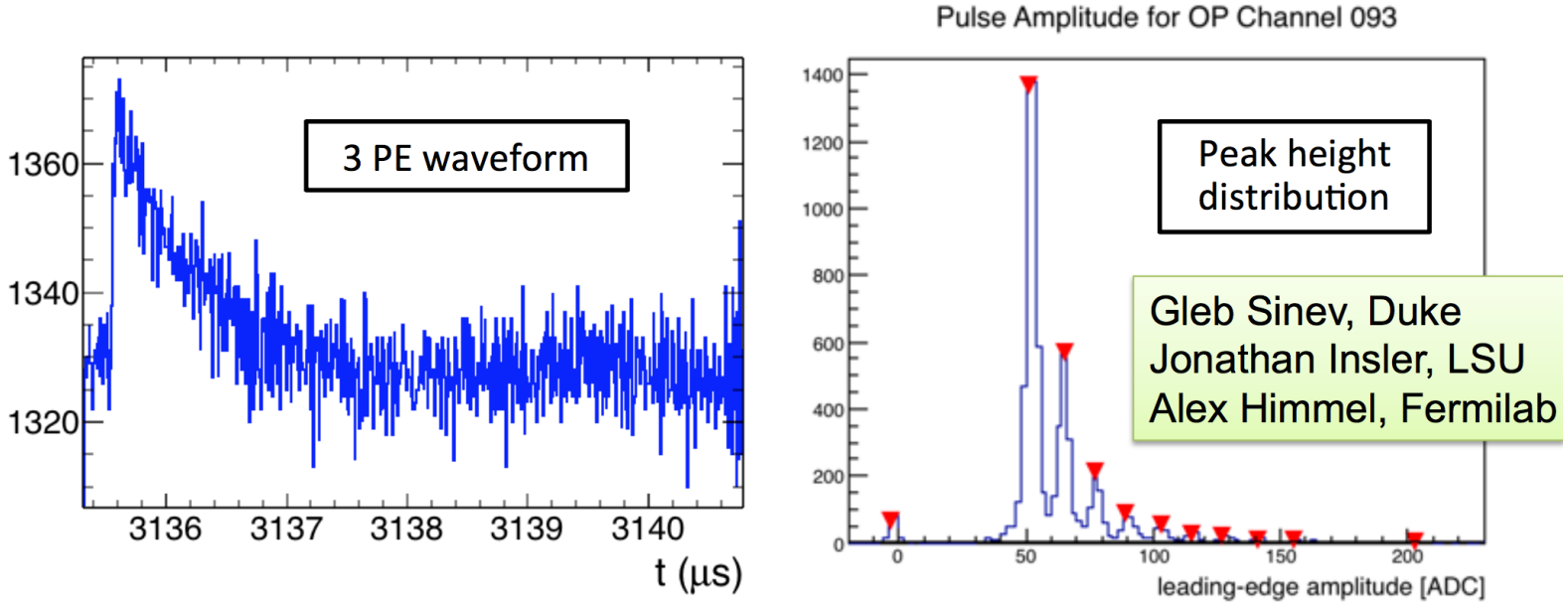




⇨ ***Uses CFD in Firmware; Need > 3 points on leading edge, @ 150 MSPS***

Performance Tests (3)

- **Results from the 35-ton Detector**
  - PDs were noisier than expected
    - Amount of noise varies by channel.
    - Primary noise source is pick-up from the TPC electronics (see below)
    - Threshold was set to 2-3 pe instead of the desired 0.5 pe
    - One third of the channels were turned off or suppressed due to high noise
  - However, on well-behaved channels, signals of a few pe can still be seen

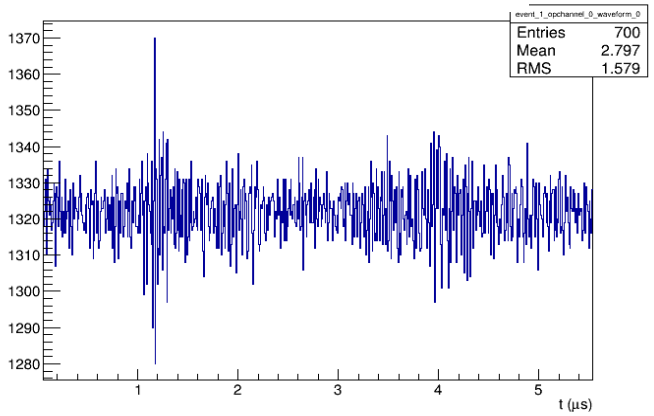


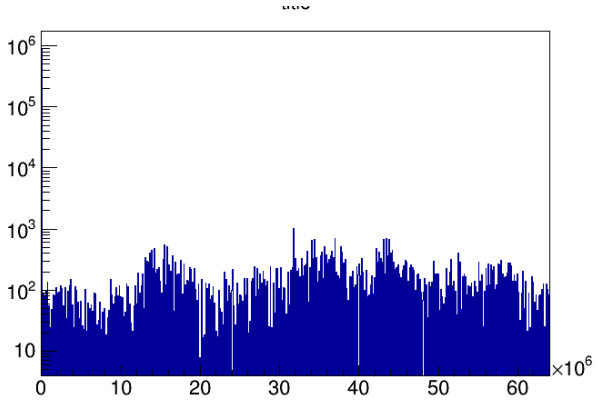
Plots originally presented by Michelle Stancari

Performance Tests (3) (Continued)

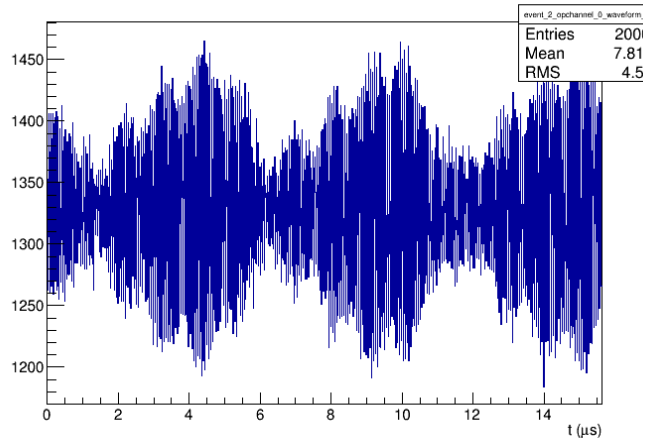
- **Results from the 35-ton Detector (Cont.)**
  - Study of noise pick-up

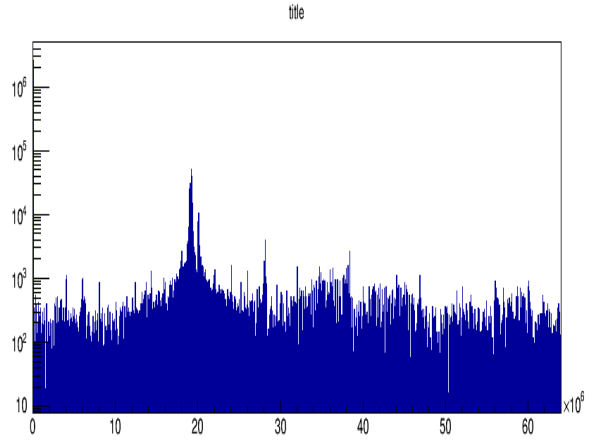
Waveforms: **FFTs:**





TPC Electronics OFF





TPC Electronics ON

⇨ ***Intrinsic noise performance of the SSPs looks OK***

⇨ ***Primary noise source was pick-up from the TPC***

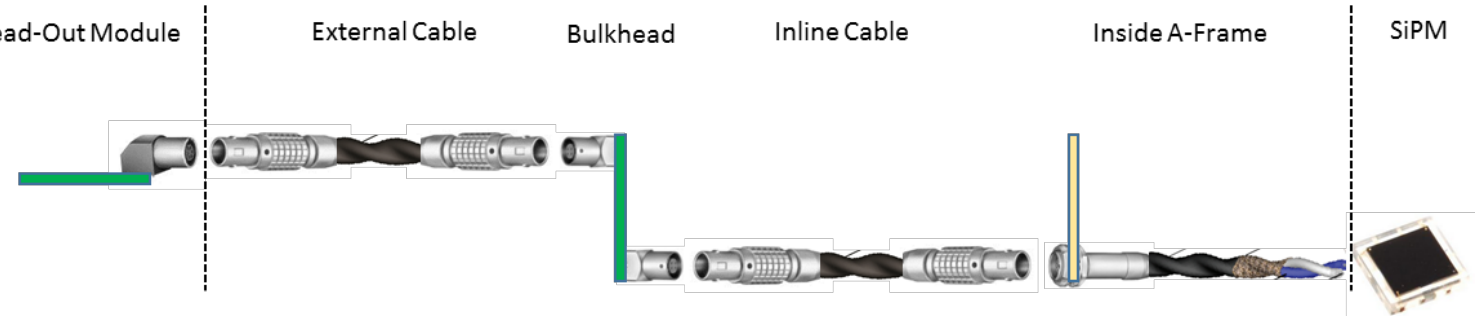
Summary of Current Performance Attributes

- **ADC Resolution**
  - 66 nA (→ dq/dt = 0.44 fC * 150 MSPS)
- **Differential Signal Input**
  - >60 db common mode rejection
- **Charge Measurement Accuracy**
  - Channel gains matched to 1% in a module, 2% overall
- **Electronics Noise**
  - 2.2 ADC counts RMS @ pedestal.
- **Charge Measurement Dynamic Range**
  - 14 bits
- **Linearity**
  - Integral: ≤ 1%; Diff: ≤1 count
- **Calibrations**
  - On-board charge injection, 1% caps, 14-bit DAC
- **Timing Resolution/Accuracy**
  - ~3 ns for single pe's (4 samples)
- **Dead Time**
  - No Dead Time up to 30k events/s @ 100 samples per event (per ch)
- **Multi-Hit Capable**
  - Resolve two pulses separated by <100ns as separate hits
- **Detection of Triplet (late) photons**
  - Waveform storage up to 2048 samples per event per channel possible
  - Deep buffers capture both prompt and late light
- **Trigger Interface**
  - Two modes, ***External*** and ***Internal***
  - ***External***: Read out programmable window of samples upon receipt of trigger.
  - ***Internal***: Firmware reads out automatically, sensing edges based on firmware constant-fraction discriminator.
- **SiPM Bias Control**
  - 30V bias for individual channels, with voltage monitor read back

⇨ ***Assume that we will retain this performance for PotoDUNE…***

Lessons Learned

- **The current readout system can easily digitize single pe waveforms over 20 meters of cable**
  - No cold electronics needed, if cables of sufficient quality, and not too long…
- **The intrinsic noise performance in LAr is good**
  - ADC RMS values 2-3 ADC counts (120 – 200 nA) over 20 m of cable
- **The timing performance is good**
  - Timing resolution on single pe's ~2-3 ns over 20 m of cable
- **The internal bias & other features worked well**
- **The module was fairly robust, with few problems during operation**
- **Problems with the Cable Plant: The cables worked well, but…:**
  - The cables & connectors were expensive, difficult to fabricate, difficult to install
  - Have 240 SiPMs for ProtoDUNE, so much larger cable plant

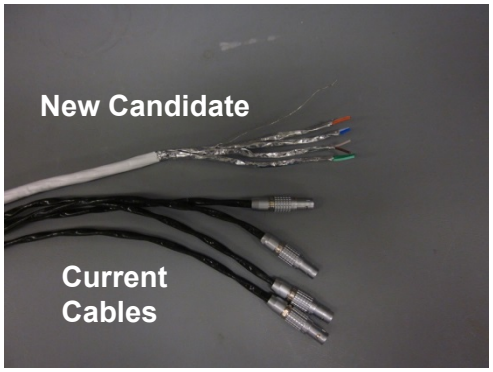


⇨ ***It is desirable to change this for ProtoDUNE***

Requirements & Changes for ProtoDUNE (1)

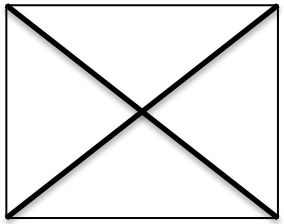
- **Change Signal Cables & Connectors: Will use CAT6 Cables**
  - (4) individually-shielded, twisted pairs
  - Mass-terminated, RJ45 Connectors on SiPM board & SSP; Possible alt. for Flange
  - 2 Cable Segments: Inside cryostat (”cryo” cables); Outside cryostat (“warm” cables)
  - Estimated length: 25 meters

⇨ ***Requires change to SSP: addition of connector Daughter Board & new back panel***

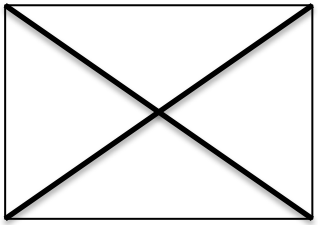


Top: 4-pair CAT6A STP cable - Superior Essex
Bottom: (4) 1-pair cables - Gore

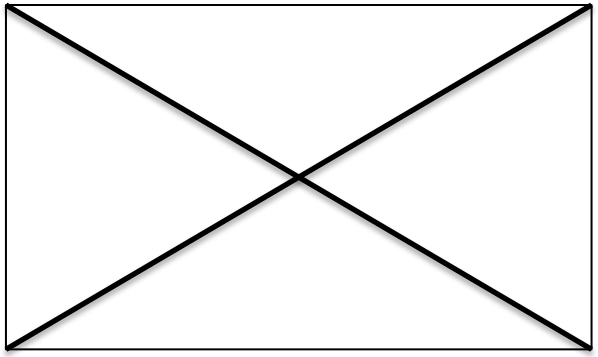
Candidate CAT6A connector
4 pairs with shield (for Flange)



Completed new cable



SSP Daughter Board

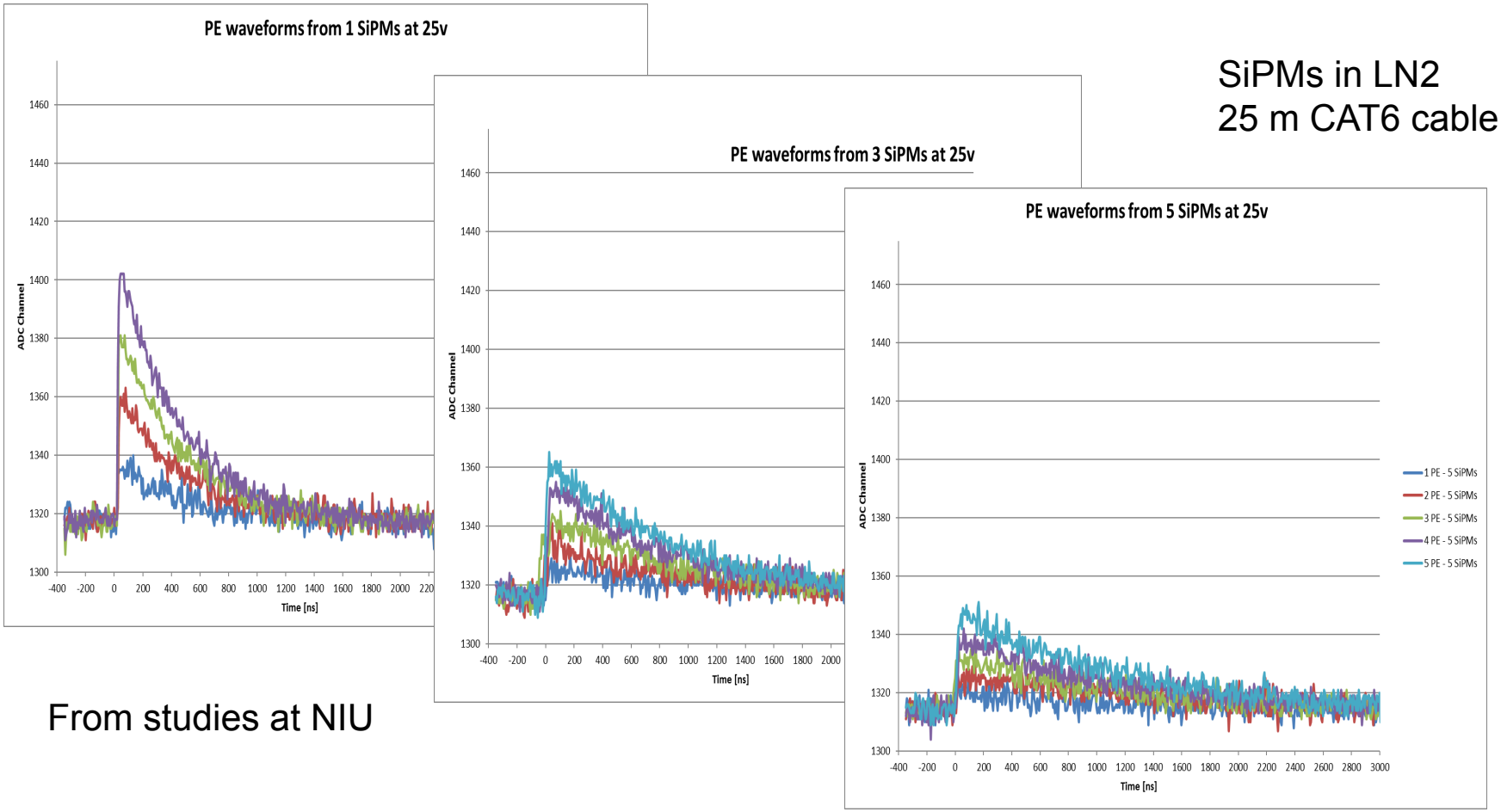


Modification to the SSP

⇨ ***Significant saving in cost & ease of fabrication & installation***

Requirements & Changes for ProtoDUNE (2)

- **Sum (3) SiPM outputs together**
  - Goal: further reduce cable plant costs & cable plant size
- **Study: See reduced pulse height & longer tail as more SiPMs ganged together**



SiPMs in LN2
25 m CAT6 cable

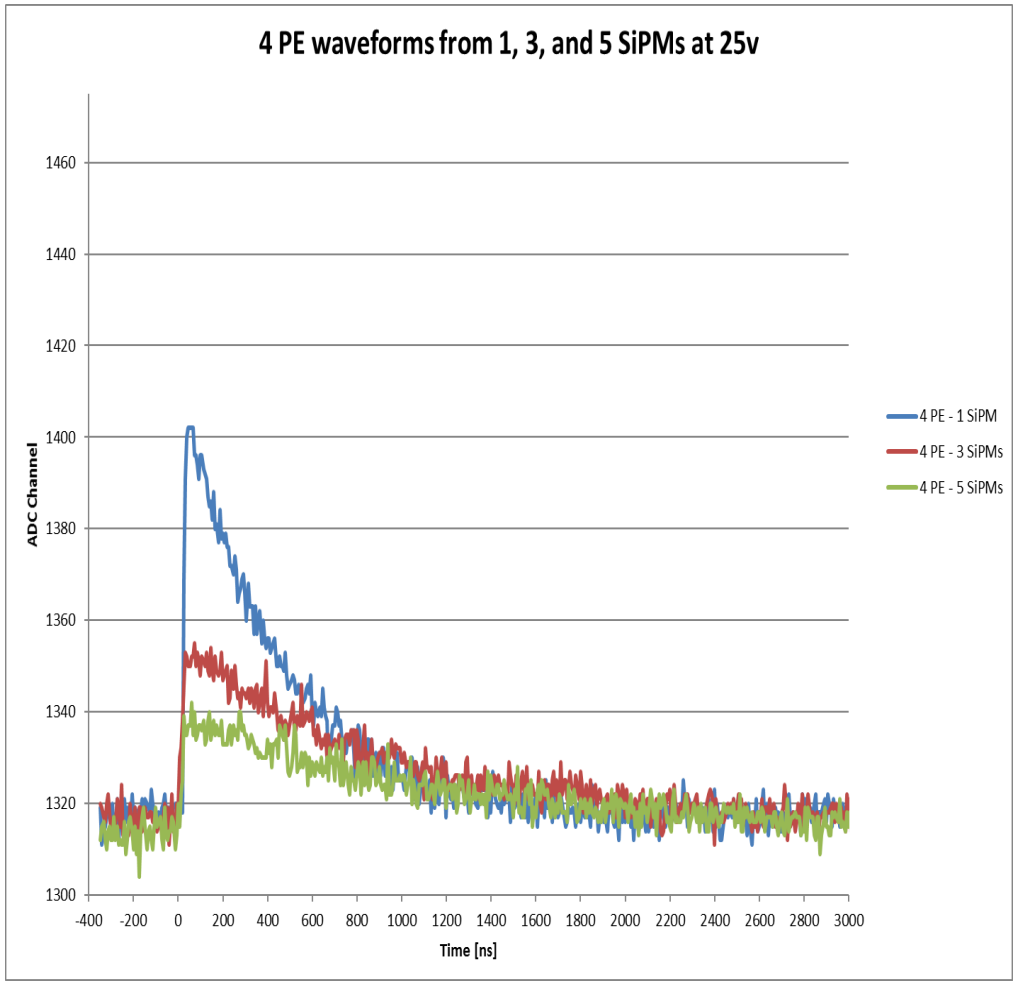
From studies at NIU

⇨ ***Conclusion: Gang 3 SiPMs @ 25 meters should give adequate S/N, if environmental noise is low***

⇨ ***Marginal S/N if cables longer, or gang more SiPMs together***

Requirements & Changes for ProtoDUNE (2) (Cont.)

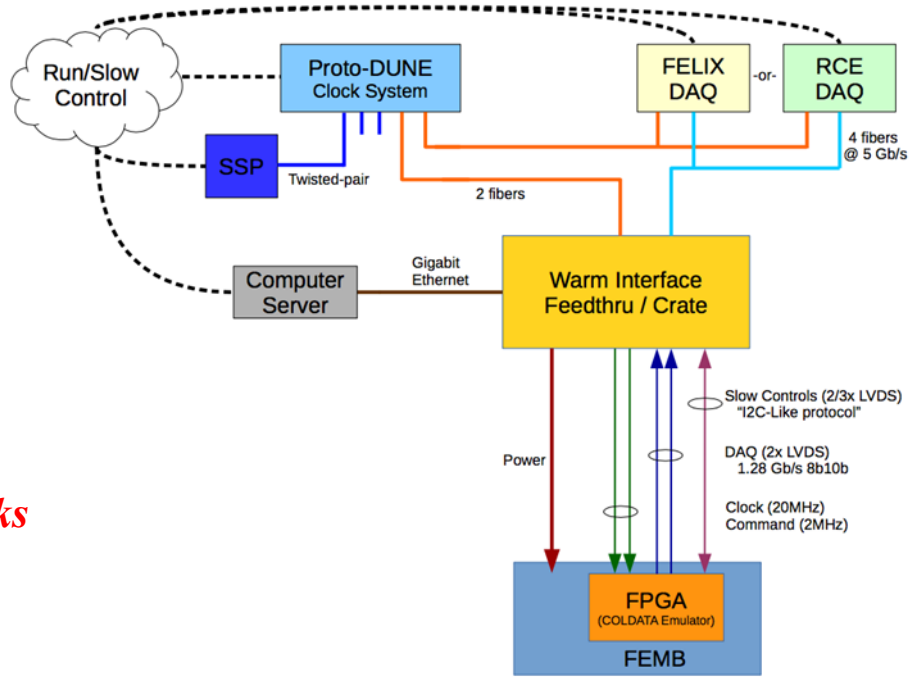
- **Sum (3) SiPM outputs together (Cont.)**



Test Condition	1 PE Peak (ADC Counts)	Decay Time (ns)
1 SiPM at 25v	16.8	560
3 SiPMs at 25v	10	1132
5 SiPMs at 25v	6.8	1172
5 SiPMs at 28v	10.2	1192

Requirements & Changes for ProtoDUNE (3)

- **Changes to Timing System**
  - SSPs currently interface to the NOvA Timing System.
  - ProtoDUNE will use something different:
    "DAQ to Cold Electronics Protocol and Timing for the ProtoDUNE TPC", DUNE-doc-1394,
  - Timing system still under development
  - Depending on outcome, options:
    - Incorporate changes directly into the SSPs (preferred)
    - Develop intermediate interface between new timing system and SSPs to produce "NOvA-like" timing



⇨ ***Must evaluate options in terms of development costs, schedule, & robustness***

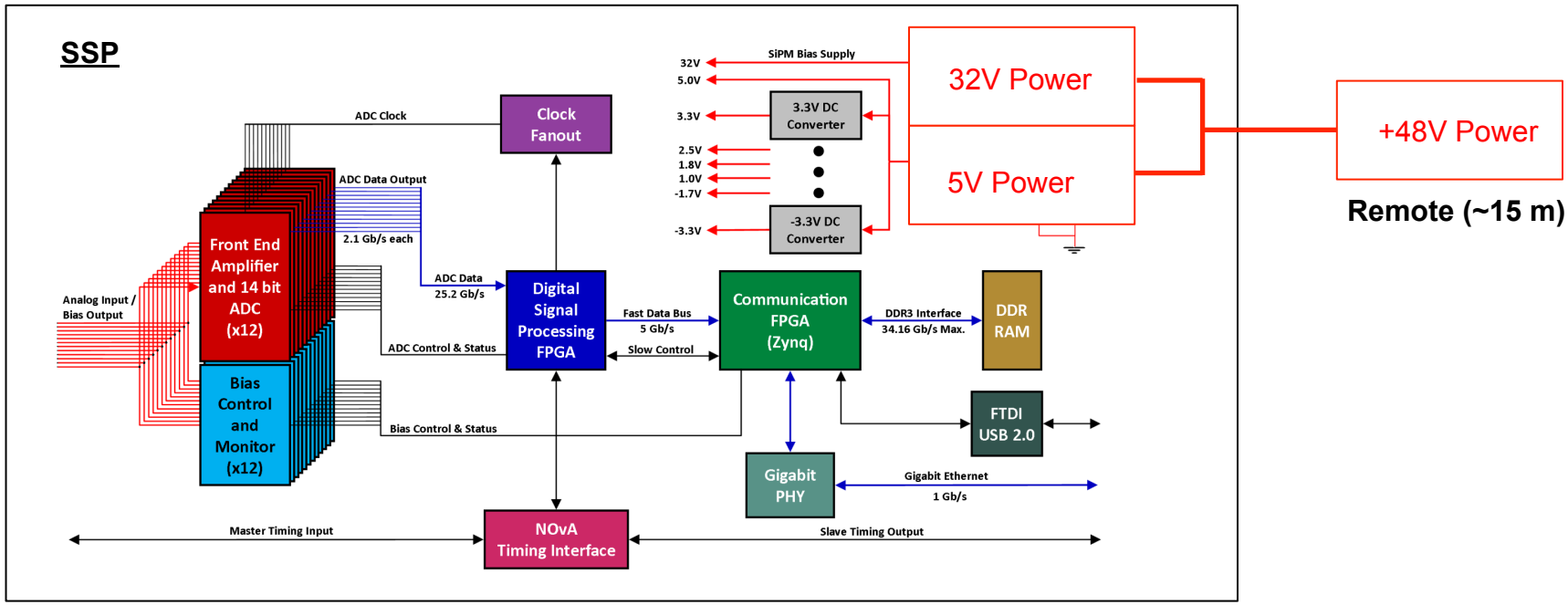
⇨ ***Timescale for decision: ~Next few weeks***

Requirements & Changes for ProtoDUNE (4)

- **Changes to the Power System**
  - SSPs currently receive input power from 120V, 60 Hz AC
  - At a minimum: changes needed to interface to Swiss power (240V, 50 Hz)
  - Another constraint: Cable length ~ 30 meters if SSPs installed at closest point of available AC power

⇨ ***This exceeds out comfort level in S/N due to long cable lengths***

⇨ ***Solution: Provide +48V Power to SSPs (reauires modification to design…)***



⇨ ***If we do this, SSPs can be mounted on top of Cryostat; Total cable length: 18 meters***

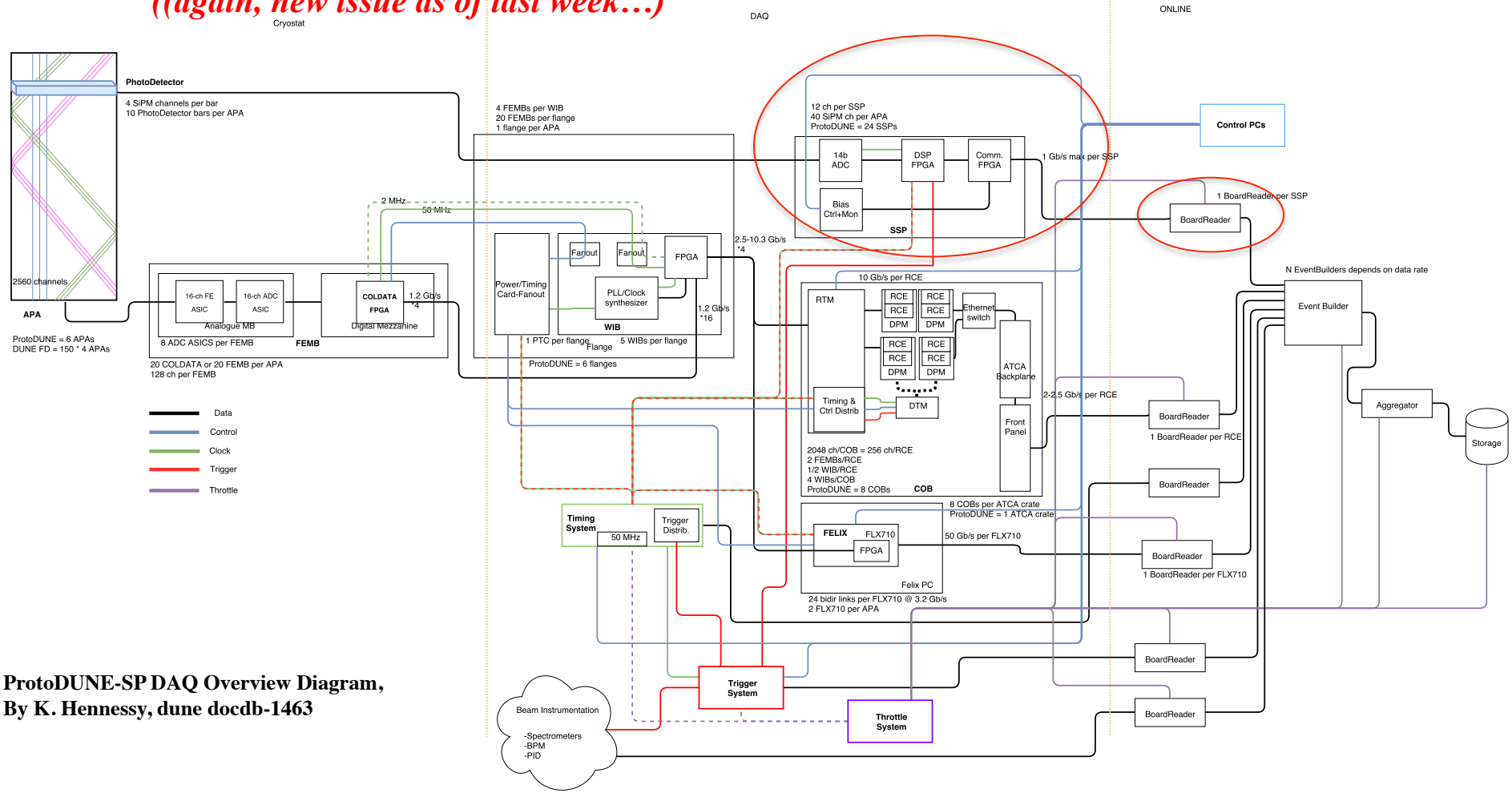
⇨ ***Strong motivation to do this to reduce risk of S/N problems***

⇨ ***Design change is under development (this issue arose only last week…)***

Requirements & Changes for ProtoDUNE (5)

- **Changes to DAQ System: 2 Modes of Operation**
  - In spill: Collect full waveforms for beam triggers
  - Out of Spill: For muons, collect either waveforms or header info only

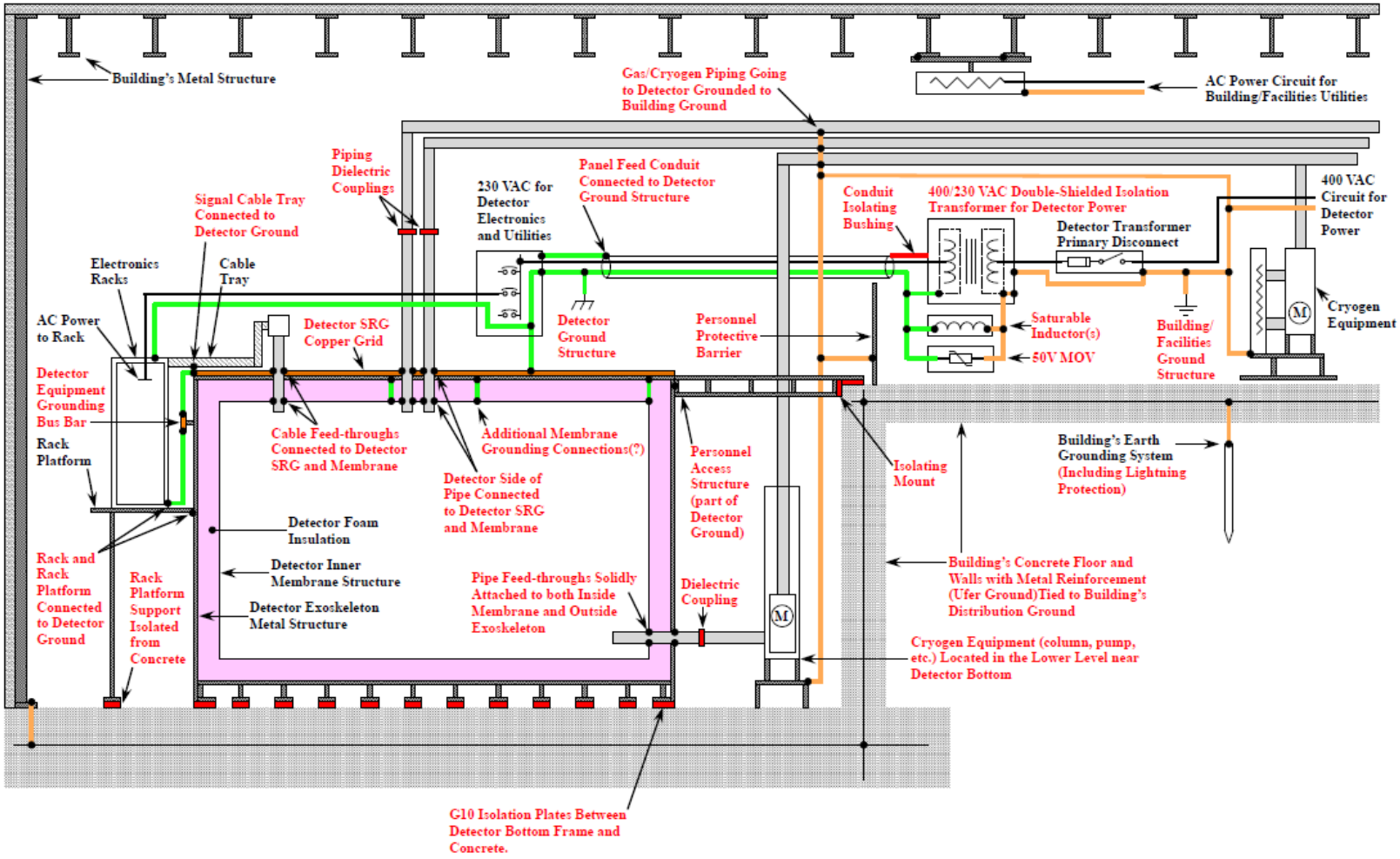
⇨ ***Change is mostly firmware, although spill signal may be part of timing system… ((again, new issue as of last week…)***



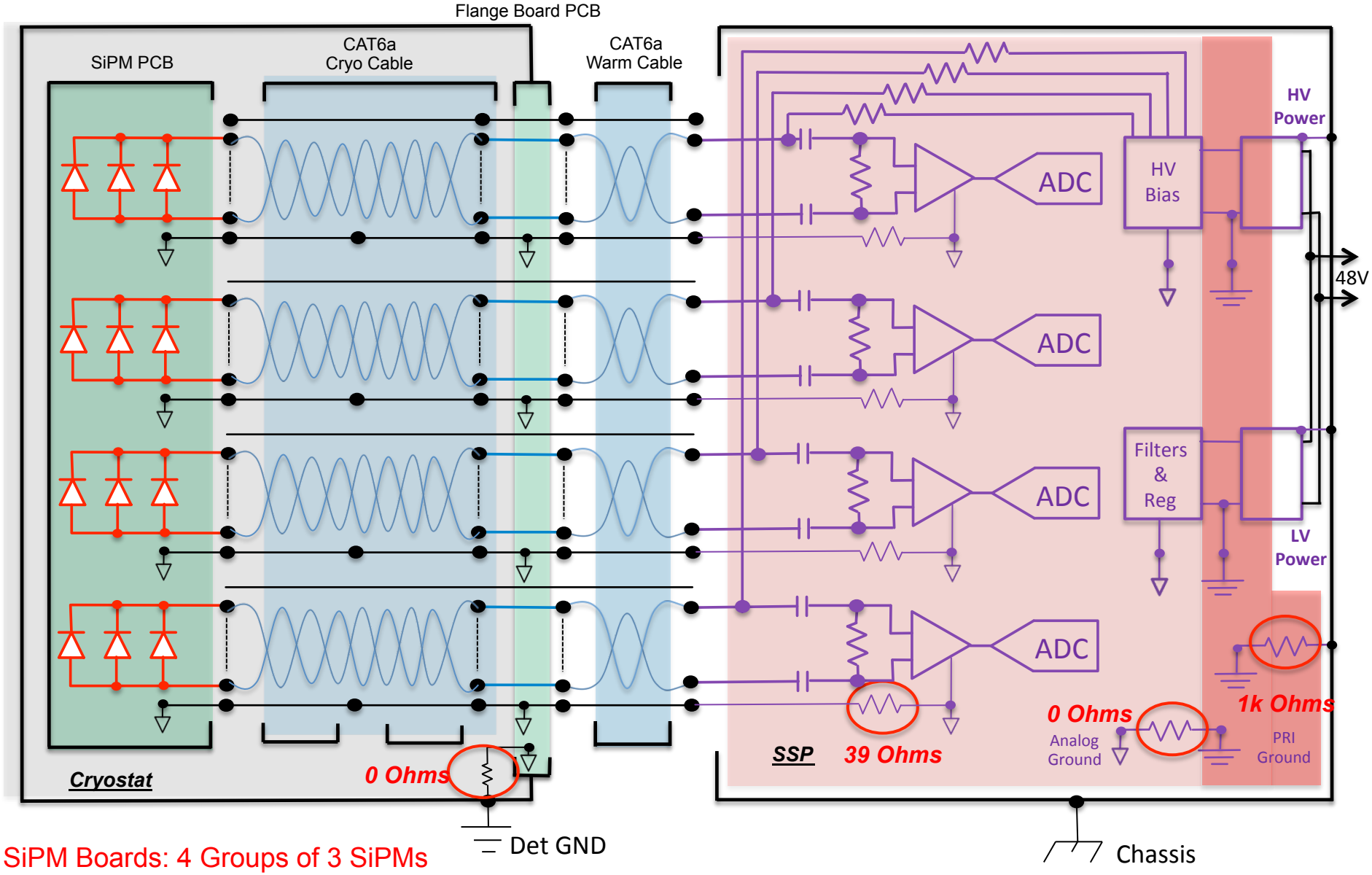
ProtoDUNE-SP DAQ Overview Diagram, By K. Hennessy, dune docdb-1463

Requirements & Changes for ProtoDUNE (6)

- Grounding and Shielding requirements:
  - DocDB 879
  - DocDB 1330



SSP Grounding Plan for ProtoDUNE



SiPM Boards: 4 Groups of 3 SiPMs

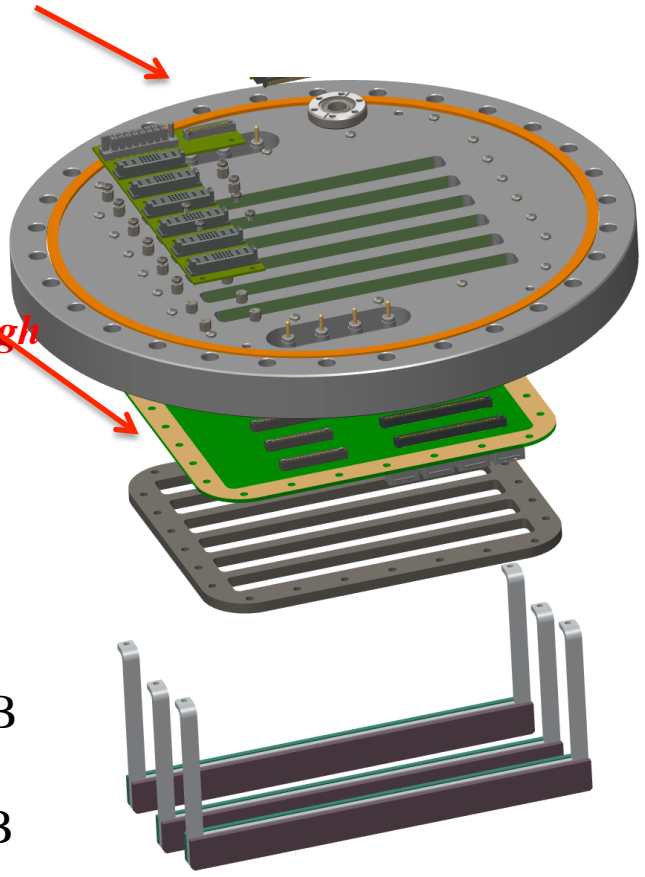
Signal Cables: 4 individually-Shielded Twisted Pairs

SSP Electronics (12 Ch per Module)

Requirements & Changes for ProtoDUNE (7)

Candidate Connector

- **Flange Board (Warm Interface)**
  - PD Flange Board will be passive, serving only as a feed-through for the analog SiPM signals
  - Design will use mechanics being developed for the cold electronics (mechanical design of flange)
  - Design will have custom PCB for feeding signals through the flange
    - Strain relief of the cables is important
    - Integrity of connector is important
    - Candidate connector being evaluated
  - ⇨ ***BNL responsible for a mechanical portion of the feedthrough (flange, seal, strain relief) design.***
  - ⇨ ***ANL responsible for Printed Circuit Board (PCB) Feed-through for Photon-Detector.***
  - 3D CAD model of the CE flange, key drawings, and the fabrication package of a prototype CE flange PCB exist.
  - ANL will provide BNL an initial PD flange board PCB connector layout with minimum connector spacing
  - BNL will be responsible for the integration of the PCB into the flange and leak checking.
  - We have yet to define the electrical testing protocol.



Example of CE flange/ feedthrough design

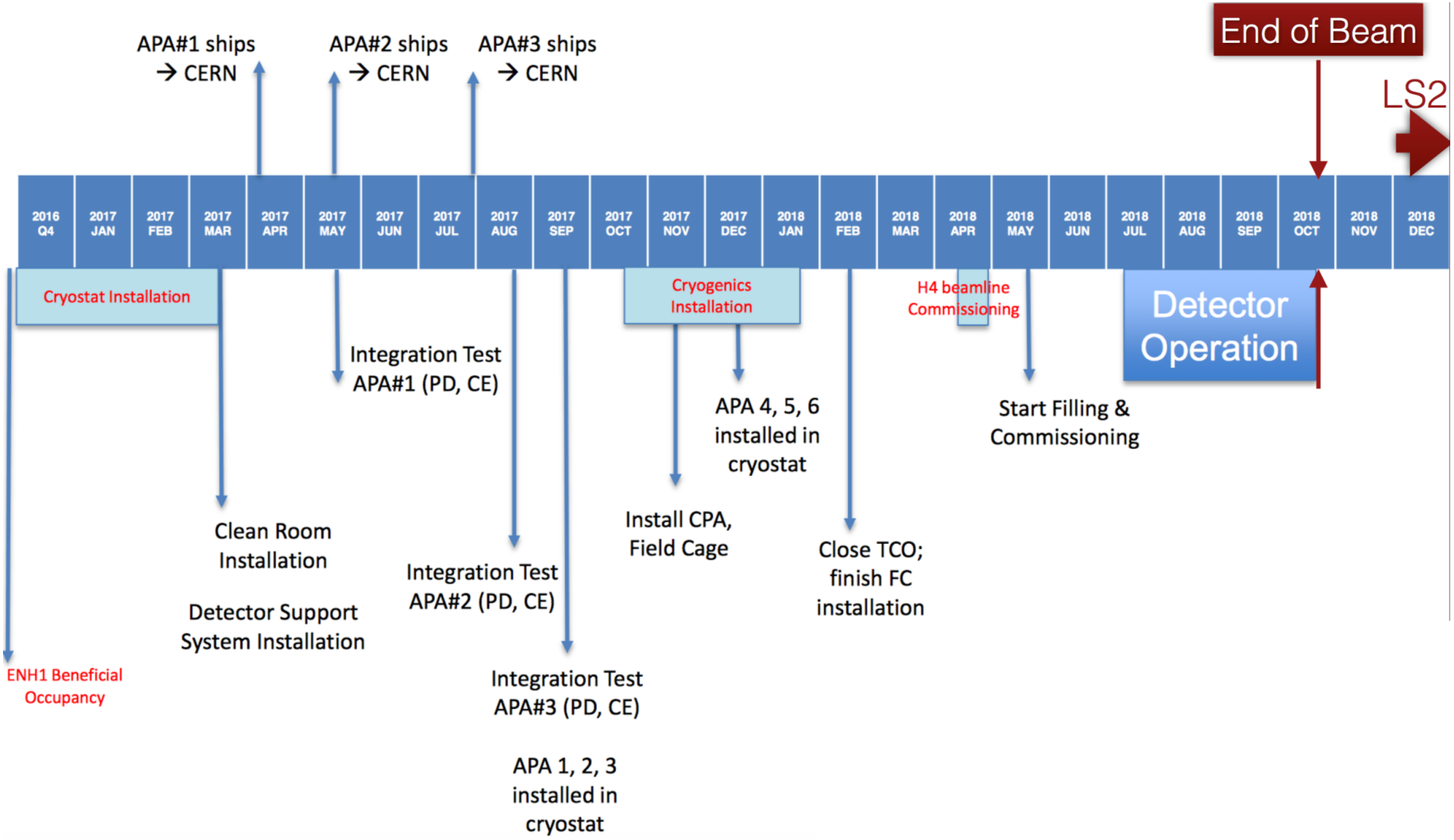
Requirements & Changes for ProtoDUNE

- **Summary of Interfaces**
  - PD Mechanics
  - PD Installation
  - Timing System
  - DAQ System
  - Grounding & Shielding
  - TPC Mechanics

Requirements & Changes for ProtoDUNE

- **Summary of Risks**
  - S/N is worse than expected; Several possible factors:
    - Longer cable lengths (i.e., SSPs cannot be mounted on top of cryostat)
    - Noise pick-up from other sources

Schedule of Activities at CERN



- Schedule developed to address system testing, integration, installation, commissioning.
- PD readout activities start with a vertical slice test at CERN in Dec16 – Jan17.

Status & Plan

- **Overall Plan**
  - Complete development of required design changes to SSP
  - Complete design & layout of Flange PCB
  - Develop plan for retro-fitting 8 SSP modules from the 35-ton Detector
  - Initiate small production run of 16 more SSPs to complete quantity needed
  - Initiate procurement of SSP signal cables
  - ANL will participate in Vertical Slice Tests, Integration Tests, installation, & commissioning at CERN
- **Current Status**
  - Cable design is complete
  - Connector modifications to SSPs designed & prototype built & tested
  - Beginning development of power system changes
  - Beginning layout of Flange PCB
  - Discussions continuing on DAQ & Timing System
- **Milestones**
  - One fully-functional SSP for Vertical Slice Tests ~Dec. 2016
  - Begin SSP production ~Feb., 2017 ⇨ ***Production planning in progress…***
  - Cable fabrication complete by Spring, 2017
  - Begin Integration Tests ~May, 2017
  - Installation & commissioning complete ~Sept., 2017

Summary

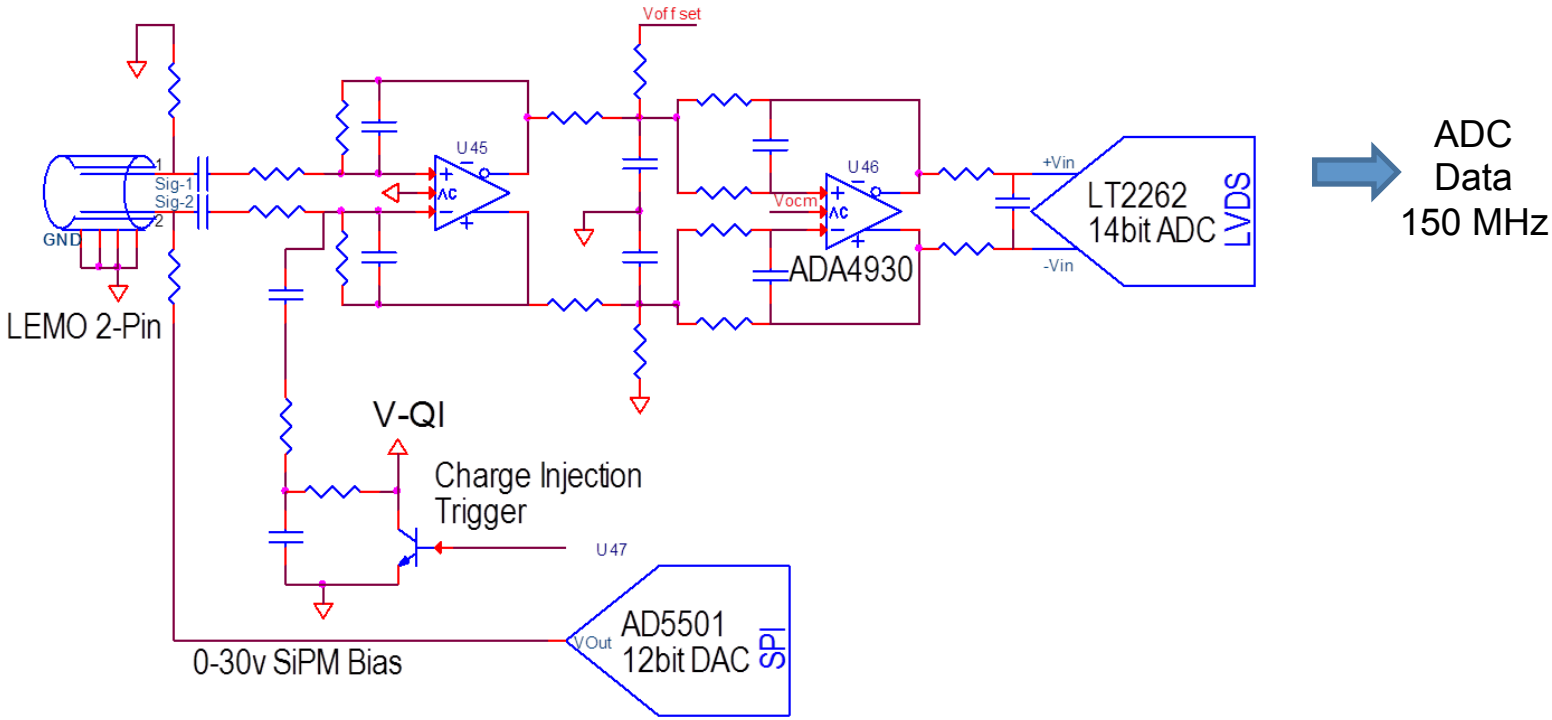
- **SSPs have been developed over the last 2-3 years**
  - Mature design: (1) prototype cycle; (1) small production run to date
  - Performance in TallBo tests & University R&D have been very good
  - Performance in the 35-ton detector was marginalized by noise pick-up, but indications are that the performance meets or exceeds the physics requirements
- **Design changes for ProtoDUNE mostly understood; Some work yet to do:**
  - Design changes for cable plant (mostly) complete
  - Design changes for power system in progress
  - Design changes for Timing System in discussion
  - Design changes for DAQ in discussion
  - Design of PD Flange Board understood; Connector selection in progress
- **Milestones & Goals**
  - One fully-functional SSP for Vertical Slice Tests ~Dec. 2016
  - Begin SSP production ~Feb., 2017
  - Cable fabrication complete by Spring, 2017
  - Begin Integration Tests ~May, 2017
  - Installation & commissioning complete ~Sept., 2017

    ⇨ ***Requirements are understood (DAQ & Timing coming…)***
    ⇨ ***Scope of project is understood***
    ⇨ ***Interfaces are understood & work in progress to complete design***
    ⇨ ***ANL responsibilities are understood***
    ⇨ ***Risks are manageable, but change to the power system is necessary***
    ⇨ ***Schedule is understood; Production planning in progress***

Backups

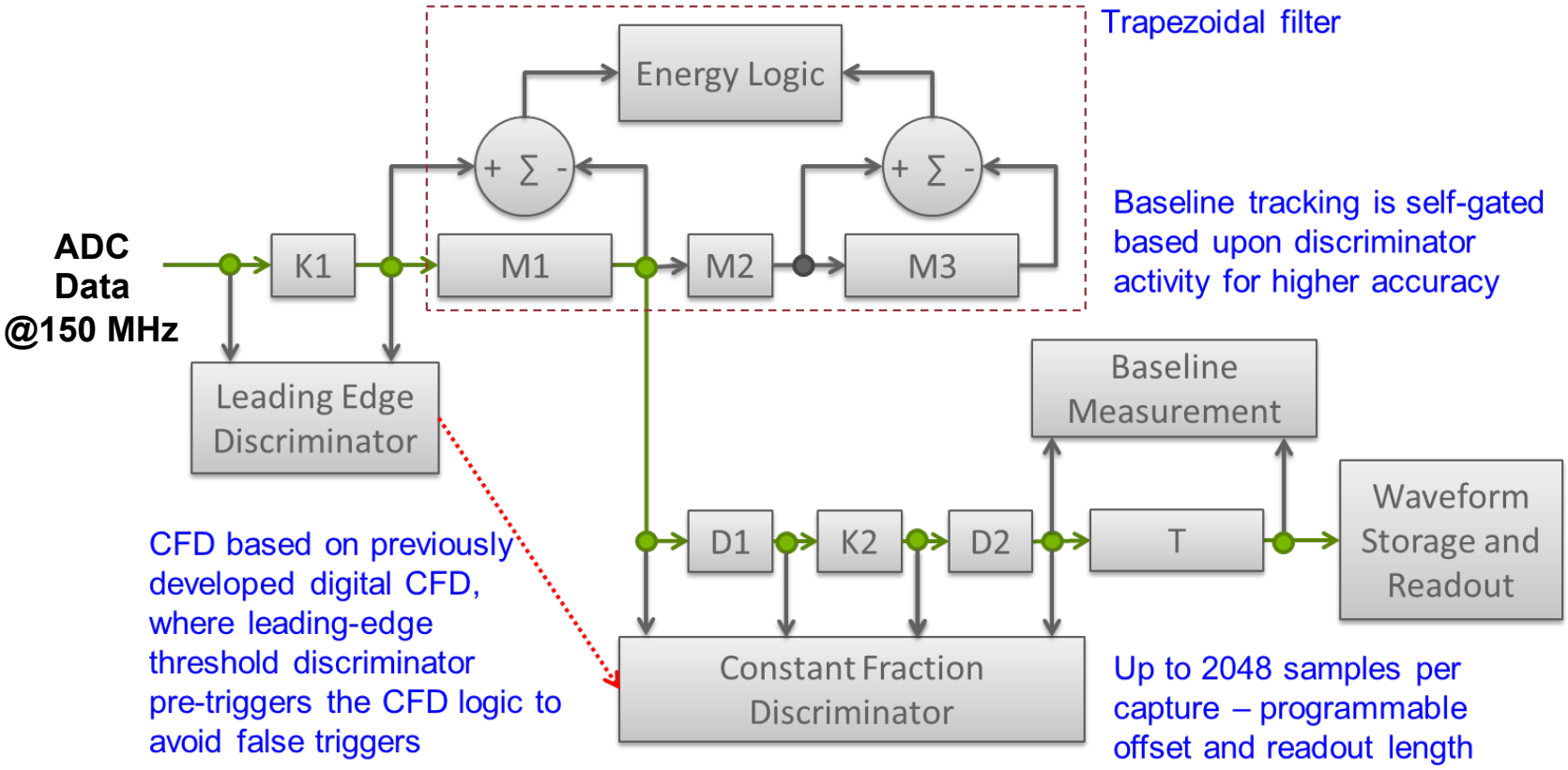
Overview of the SSP Module

- **Front End Amplifiers & ADCs in the SSP**
  - Inputs use shielded twisted-pair cable & connectors
  - Fully differential analog signal processing, ~60db common mode rejection
    - ⇨ ***Needed to process single pe signals over 25 m cable (→ 40 m)***
  - Individual programmable bias for the SiPMs included



Overview of the SSP Module

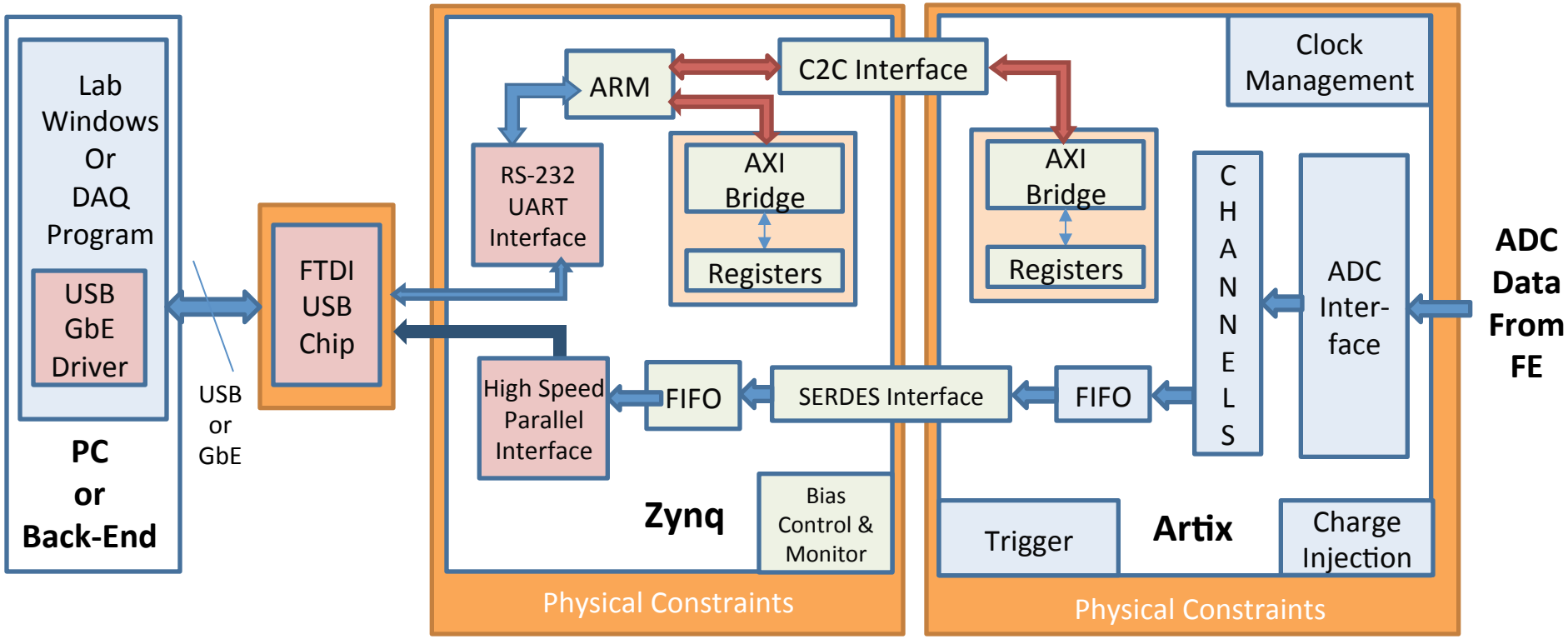
- **Processing of Digitized Data in the Artix FPGA**



⇨ ***Can perform waveform analysis in front-ends using digital signal processing***
⇨ ***Can also (in addition) read out full waveform data (default, baseline)***

Overview of the SSP Module

- **Signal Processing & Readout of Data**
  - The Artix FPGA collects and processes serial data streams from all 12 ADCs
  - The Zynq FPGA interfaces data I/O to USB and GbE
  - Control & monitoring interface is through the Zynq ARM processor



Timing and Triggering

- Connection to the NOvA timing system is supported
- Module supports two modes of triggering:
  - In the Post-Trigger mode, a NIM input is used from an external trigger source. Registers within the ANL digitizer select *how far before the trigger* readout will start (look-back time) and *how many ADC samples* will be read out (readout length).
  - In the Self-Trigger mode, the internal discriminator of each channel is used as the trigger for each channel. Registers select *how far before the discriminator firing* readout will start (pre-trigger) and *how many ADC samples in total* will be read out (readout length).

- **Data buffer depth (13us) is more than sufficient to capture late light!**

Communications – Event Format

Each event's ADC samples (waveform data) are preceded by an event header containing event size, event timestamp and various parameters calculated by the firmware describing the timing and energy of the event. We envision that, as event rates are increased, full waveform readout will slowly be replaced by readout of just these headers with little to no waveform data needed.

	bit ==>															
word #	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	Packet Length															
1	Header Type				PU flag	0	0	0	Trigger Type							
2	Trigger ID															
3	Channel ID				Module ID											
4	Fractional Timestamp(0:15)															
5	Event Timestamp(0:15)															
6	Event Timestamp(16:31)															
7	Event Timestamp(32:47)															
8	Event Peak Sum (0:15)															
9	Event Peak Sum(16:23)								Event Peak Offset(0:7)							
10	Event Pre Sum(0:15)															
11	Event Pre Sum(16:23)								Reserved							
12	Baseline(0:15)															
13	Reserved															
14	CFD Sample 0															
15	CFD Sample 1															
16	CFD Sample 2															
17	CFD Sample 3															
18	Waveform Sample 0														Markers	
19	Waveform Sample 1														Markers	
...	...														...	
n	Waveform Sample m														Markers	

Event Header Format

← Event ID

← Timing

← Energy

← Timing Interpolation

← Waveform

Results from 35-Ton Detector

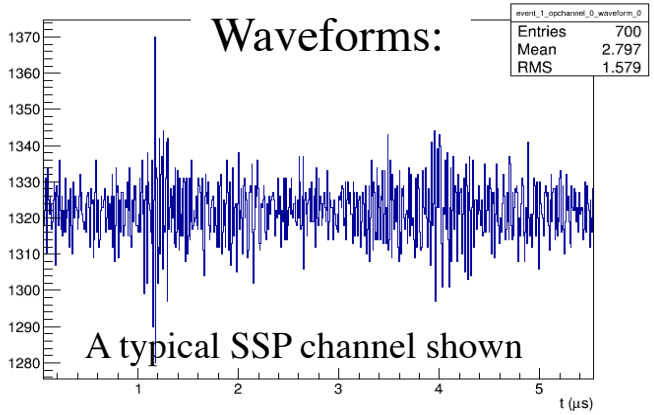
- Photo-detector/APA noise tests performed at 35-ton

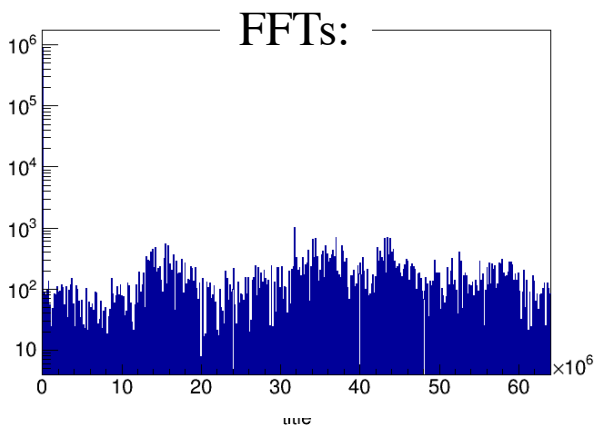
- Photon-detector noise study is performed based on SSPs pedestal runs with the SSPs in the following cases:
  a) the TPC turned off
  b) the TPC turned on but not taking data; and
  c) the TPC turned on and operating;

- Tests a)-c) are susceptibility tests, to see if the SSP is picking up noise from the TPC.
  - From a), observe noise of the SSP system with no TPC noise sources present. This is presumably the best noise performance that the SSP system can do, although there may be other noise sources that we pick up that make it worse than expected.
  - From b), observe the noise of the SSP system with the TPC powered but not reading out. Might be able to say something about the source of the noise from this.
  - From c), observe noise of SSP system with TPC powered and reading out. This should be the worst case.

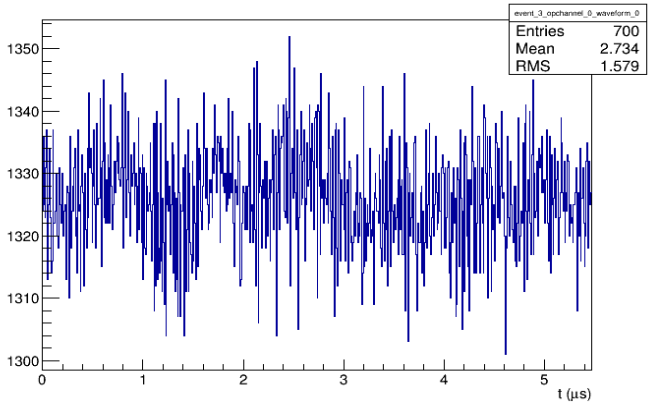
Results from 35-Ton Detector

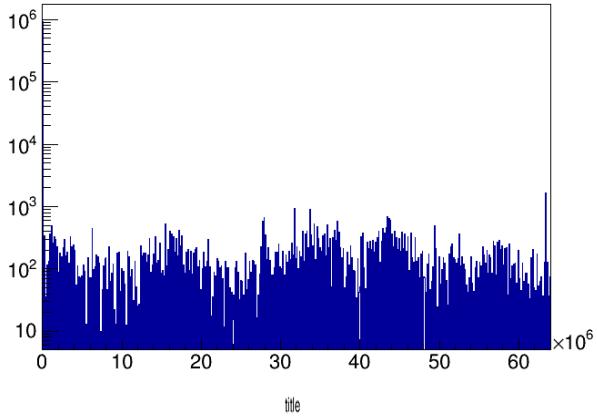
Case A)



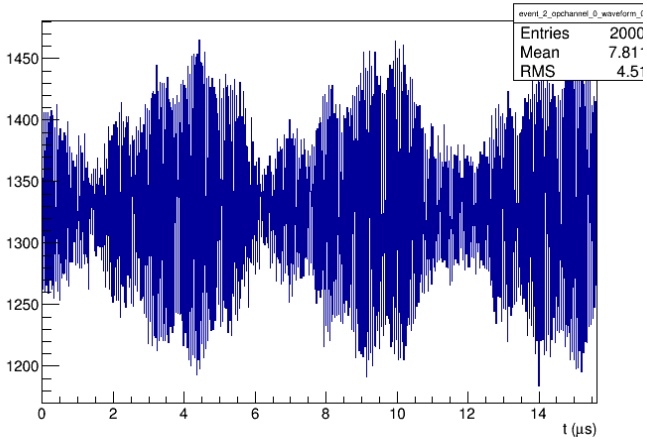


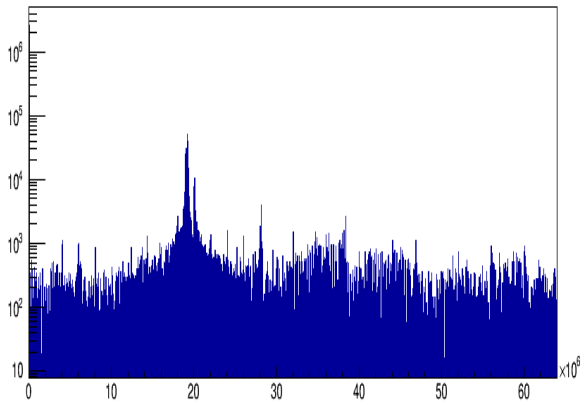
Case B)





Case C)





Shows that photon detector picks a noise from APA, but is not a significant source of noise on its own.