Photon Detector Readout Plan

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Introduction

- The Following Review Questions will be addressed:

1. Does the Photon Detector System design enable validation and refinement of the DUNE photon detector requirements? ✔
2. Are Photon Detector System risks captured and is there a plan for managing and mitigating these risks?
3. Does the design lead to a reasonable production schedule, including QA, transport, installation and commissioning? ✔
4. Does the documentation of the Photon Detector System technical design provide sufficiently comprehensive analysis and justification for the Photon Detector System design adopted? ✔
5. Is the Photon Detector system scope well defined and complete? Are all Photon Detector System interfaces to other detector components: APA, cryostat and DAQ systems documented, clearly identified and complete? Do the electronics feedthrough port and TPC integrated 3D models adequately represent the mechanical, electrical and electronic interfaces to the Photon Detector System? Is the cabling, power and calibration well defined and understood? Is the grounding and shielding understood and adequate? ✔
6. Are the Photon Detector System 3D model(s), top level assembly drawings, detail/part drawings and material and process specifications sufficiently complete to demonstrate that the design can be constructed and installed?
7. Are operation conditions listed, understood and comprehensive? Is there an adequate calibration plan? ✔
8. Are the Photon Detector System engineering analyses sufficiently comprehensive for safe handling, installation and operation at the CERN Neutrino Platform? Is the installation plan sufficiently well developed? Is the design for installation tooling adequate for installing the photon system?
9. Have applicable lessons-learned from previous LArTPC devices been documented and implemented into the QA plan? Are the Photon Detector System quality control test plans and inspection regimes sufficiently comprehensive to assure efficient commissioning and adequate operational performance of the NP04 experiment?

Readout Philosophy

- Initial PD Readout Electronics Requirements developed with idea to have extremely high-performance readout system
  - -address a wide range of R&D issues
  - -enable validation and refinement of the DUNE photon detector requirements

Performance Parameter	Target
Time Resolution	Better than 30 ns wrt event time zero ("t0")
Charge Resolution	0.25% photo-electron equivalent
Dynamic Range	$\sim$ x10 better than detector (1000:1)
Linearity	Sufficient to resolve 1 photo-electron signals
Multi-Hit Capability	Sufficient to measure Triplet (late) Photons
Dead Time	Live up to 2 drift times either side of beam spill
Bias Control	0.1 V resolution up to 30 V per channel
Calibration	On-board Charge Injection
Timing	Events time-stamped using NOνA Timing or equivalent syst.

Details on requirements given in the LBNE docdb-7605, "Working Draft of Photon Detection System Electronics Requirements", N. Buchanan, Z. Djurcic, G. Drake, M. Johnson, B. Jones, J. Klein, J. Musser, S. Seibert.

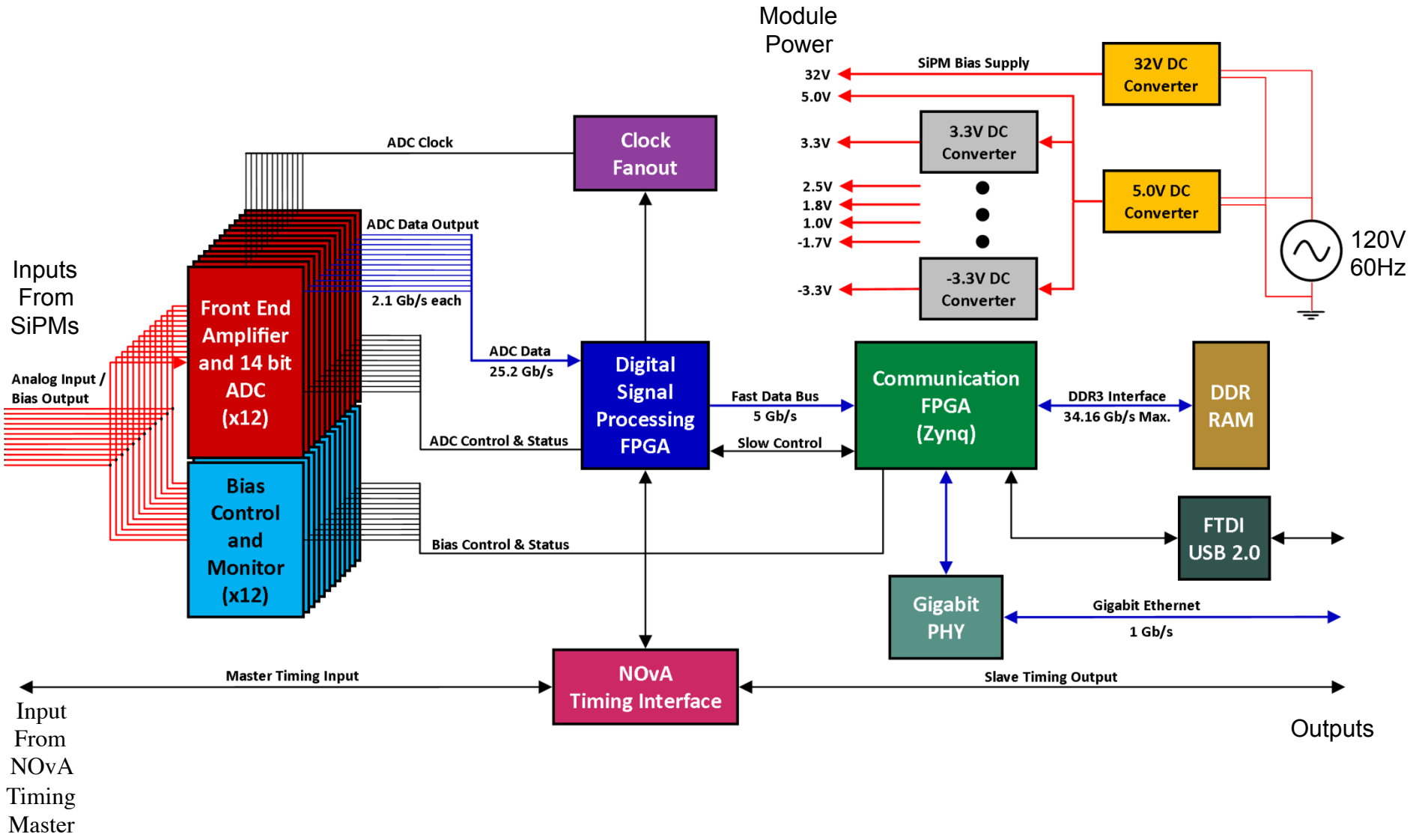
- These requirements incorporated to Silicon Photo-multiplier Signal Processor (SSP) prototype module

Overview of the SSP Module

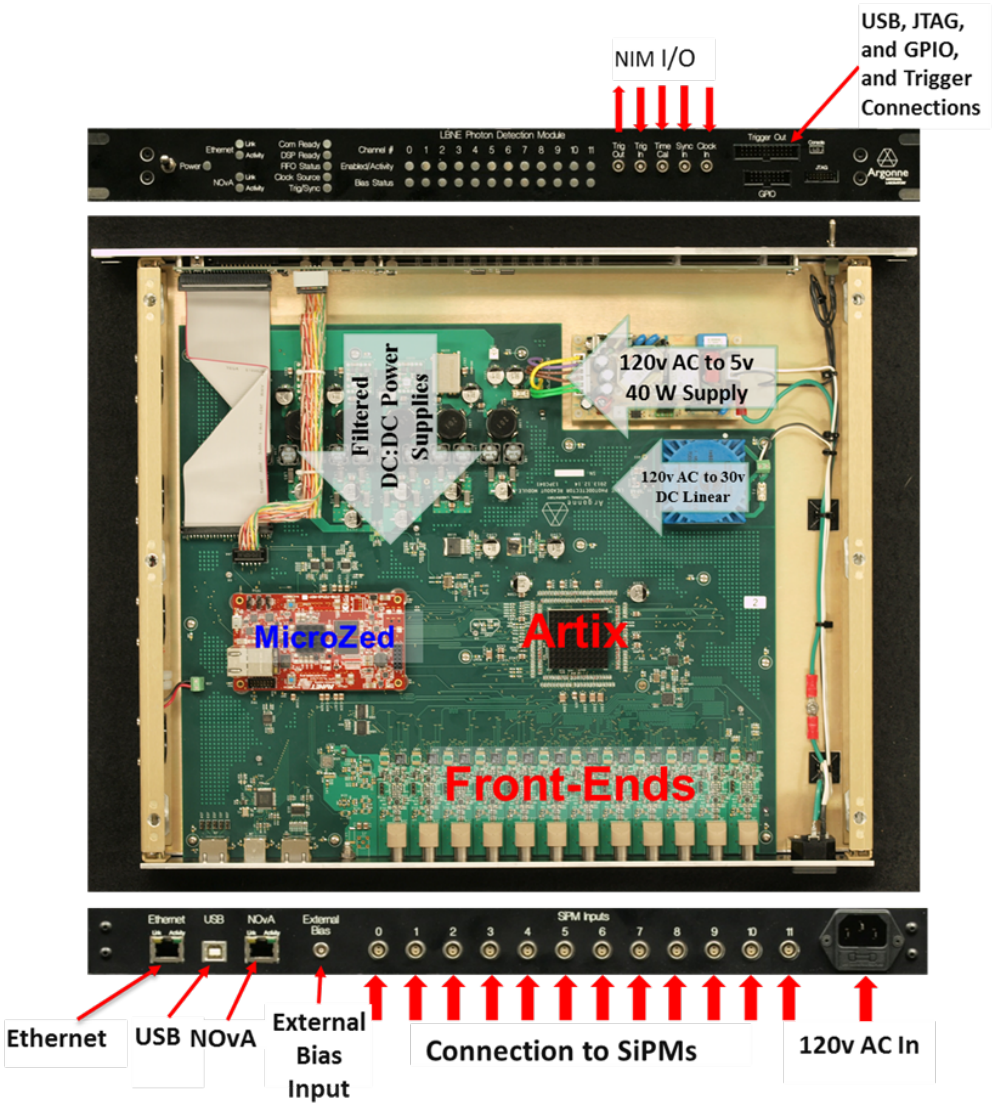
- **The Silicon Photo-multiplier Signal Processor (SSP) prototype module:**
  - High-speed waveform digitizer
  - ***Current sensitive, differential input amplifiers*** → Good noise performance over long cables
  - Each channel has a ***14-bit, 150 MSPS ADC***
  - ***Timing*** obtained using signal processing techniques on leading edge of SiPM signal (CFD)
  - 12 channels per module
  - Uses Artix FPGA for sig. proc.
  - Has NOvA Timing Interface
  - ***Uses 120VAC; On-board LV power***
  - Has internal prog. SiPM bias (30V)
  - Trigger: self or external
  - ***Has Trigger Out signal***
  - Deep data buffering – 13 μsec
  - ***No dead-time*** (up to 30 KHz/ch)
  - Programmable DAQ interface
  - ***USB & GbE communications***
  - Internal charge injection
  - Internal bias monitoring

- ⇨ ***1U rack-mounted unit***
- ⇨ ***Completely self-contained: Plug & Play***
  - ⇨ ***No crates needed***
  - ⇨ ***No external power supplies needed***
  - ⇨ ***No processor needed on front-end***

Block Diagram of SSP



Overview of the SSP Module



Summary of Current Performance Attributes

- **ADC Resolution**
  - 66 nA (1pe ≈ 160 fC at 1E6 gain)
- **Differential Signal Input**
  - >60 db common mode rejection
- **Charge Measurement Accuracy**
  - Channel gains matched to 1% in a module, 2% overall
- **Electronics Noise**
  - 2.2 ADC counts RMS @ pedestal.
- **Charge Measurement Dynamic range**
  - 14 bits
- **Linearity**
  - Integral: ≤ 1%; Diff: ≤1 count
- **Calibrations**
  - On-board charge injection, 1% caps, 14-bit DAC
- **Timing Resolution/Accuracy**
  - ~3 ns for single pe's (4 samples)
- **Dead Time**
  - No Dead Time up to 30k events/s @ 100 samples per event (per ch)
- **Multi-Hit Capable**
  - Resolve two pulses separated by <100ns as separate hits
- **Detection of Triplet (late) photons**
  - Waveform storage up to 2048 samples per event per channel possible
  - Deep buffers capture both prompt and late light
- **Trigger Interface**
  - Two modes, ***External*** and ***Internal***
  - ***External***: Read out programmable window of samples upon receipt of trigger.
  - ***Internal***: Firmware reads out automatically, sensing edges based on firmware constant-fraction discriminator.
- **SiPM Bias Control**
  - 30V bias for individual channels, with voltage monitor read back

⇨ ***Assume that we want to retain (most of) this performance going forward…***

⇨ ***A review of the required specs is needed***

Current Status

- **(4) prototype units manufactured and assembled**
  - Currently in use at: (2) IU, (1) CSU, and (1) Warwick

- **(12+) small production version units manufactured and assembled**
  - 7 installed with 35t + 1 spare at DAB
  - (1) CSU, (1) LSU, (2) ANL
  - Also, (1) used as a platform for the Calibration Module

- **Firmware development performed with 35 ton**
  - Full ADC waveforms can be read out; ADC data processing firmware is complete
  - Have implemented CF timing, peak measurement, & total charge calculations
  - USB & GbE communication interfaces fully functional
  - Control & monitoring firmware is in place, including SiPM bias control & monitoring
  - NOvA Timing interface fully functional

- **Tests of analog performance meet specifications**
  - Measurements of front-end show <300mV of noise in amplifier
  - ADC tests show <3 counts of total noise (~0.3 pe)
  - Single pe timing resolution ~3 ns
  - ⇨ ***Can measure single pe's over ~25 meters of cable → No cold electronics needed***

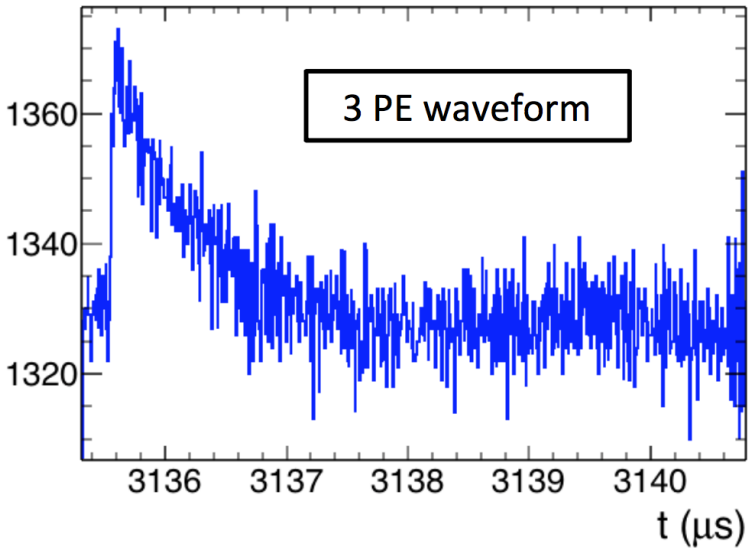
Performance Tests

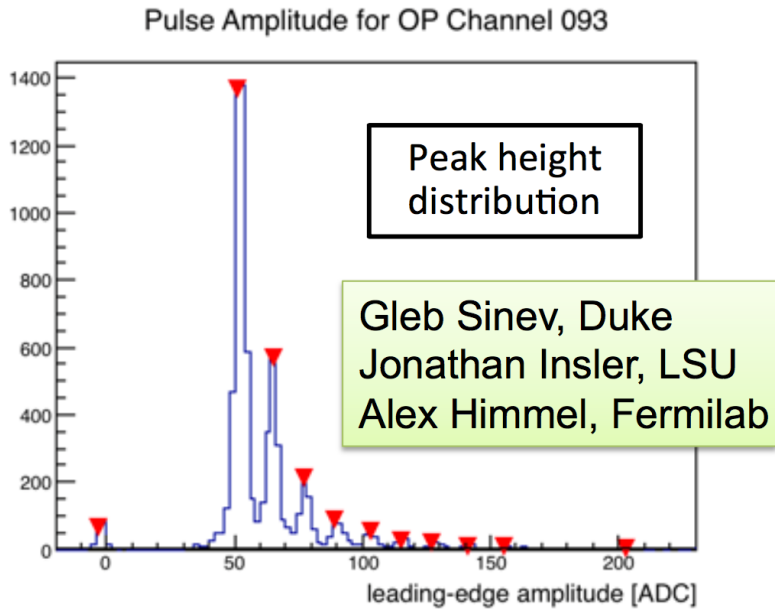
(show performance over a short/long cable in small dewars, time-resolution etc
=> some of it shown in other talks)

Results from 35-Ton Detector

Originally presented by Michelle Stancari

- PDs were noisier than originally anticipated.
  - Amount of noise varies by channel.
  - Some of the noise is feeding in from TPC electronics
- We see the PD trigger rate shoot up when the TPC is in a high-noise state.
  - Readout threshold was set to 2.2 PE or 3.3 PE (depending on readout mode) instead of the desired 0.5 PE.
  - One third of the channels were turned off or suppressed with higher thresholds because of excess noise.
- On well-behaved channels, signals of a few PE can still be seen clearly.





Gleb Sinev, Duke
Jonathan Insler, LSU
Alex Himmel, Fermilab

Results from 35-Ton Detector

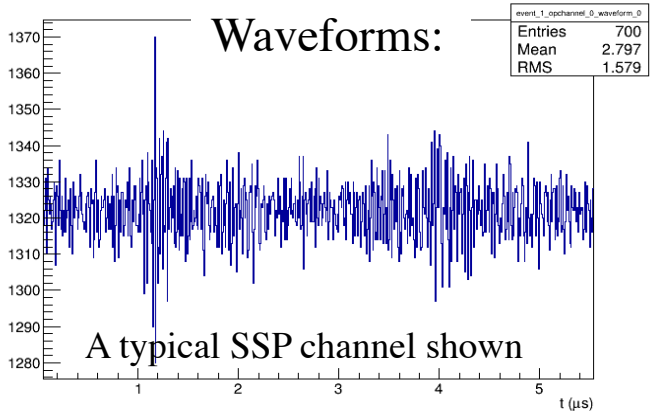
- Photo-detector/APA noise tests performed at 35-ton

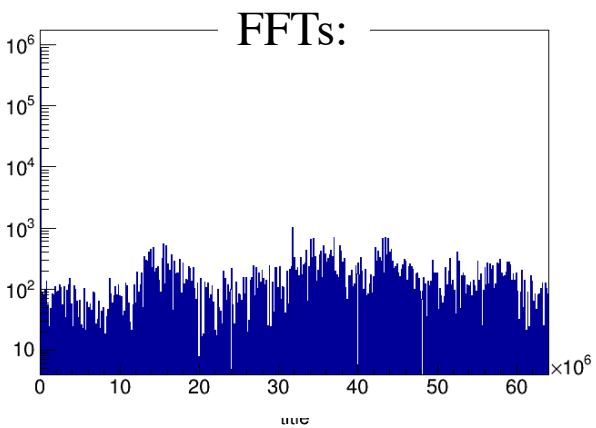
- Photon-detector noise study is performed based on SSPs pedestal runs with the SSPs in the following cases:
  a) the TPC turned off
  b) the TPC turned on but not taking data; and
  c) the TPC turned on and operating;

- Tests a)-c) are susceptibility tests, to see if the SSP is picking up noise from the TPC.
  - From a), observe noise of the SSP system with no TPC noise sources present. This is presumably the best noise performance that the SSP system can do, although there may be other noise sources that we pick up that make it worse than expected.
  - From b), observe the noise of the SSP system with the TPC powered but not reading out. Might be able to say something about the source of the noise from this.
  - From c), observe noise of SSP system with TPC powered and reading out. This should be the worst case.

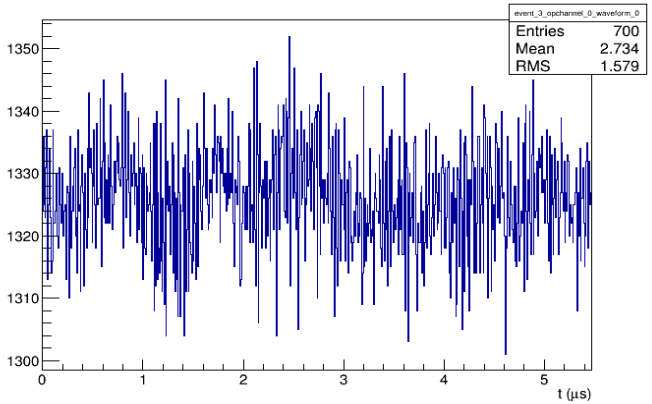
Results from 35-Ton Detector

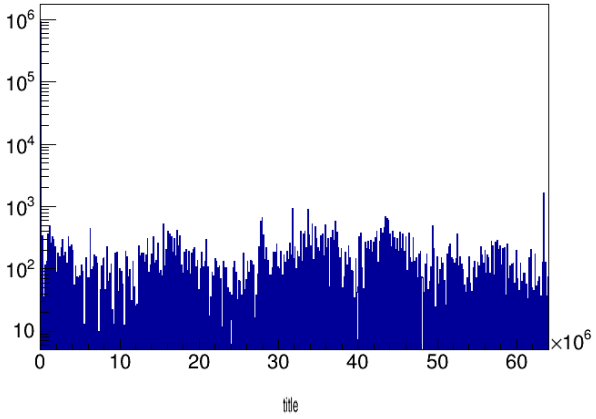
Case A)



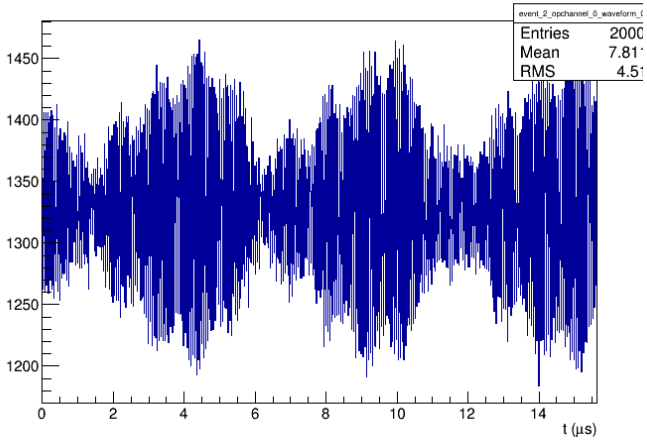


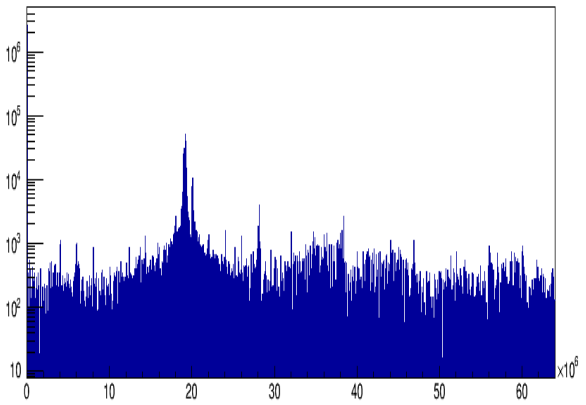
Case B)





Case C)



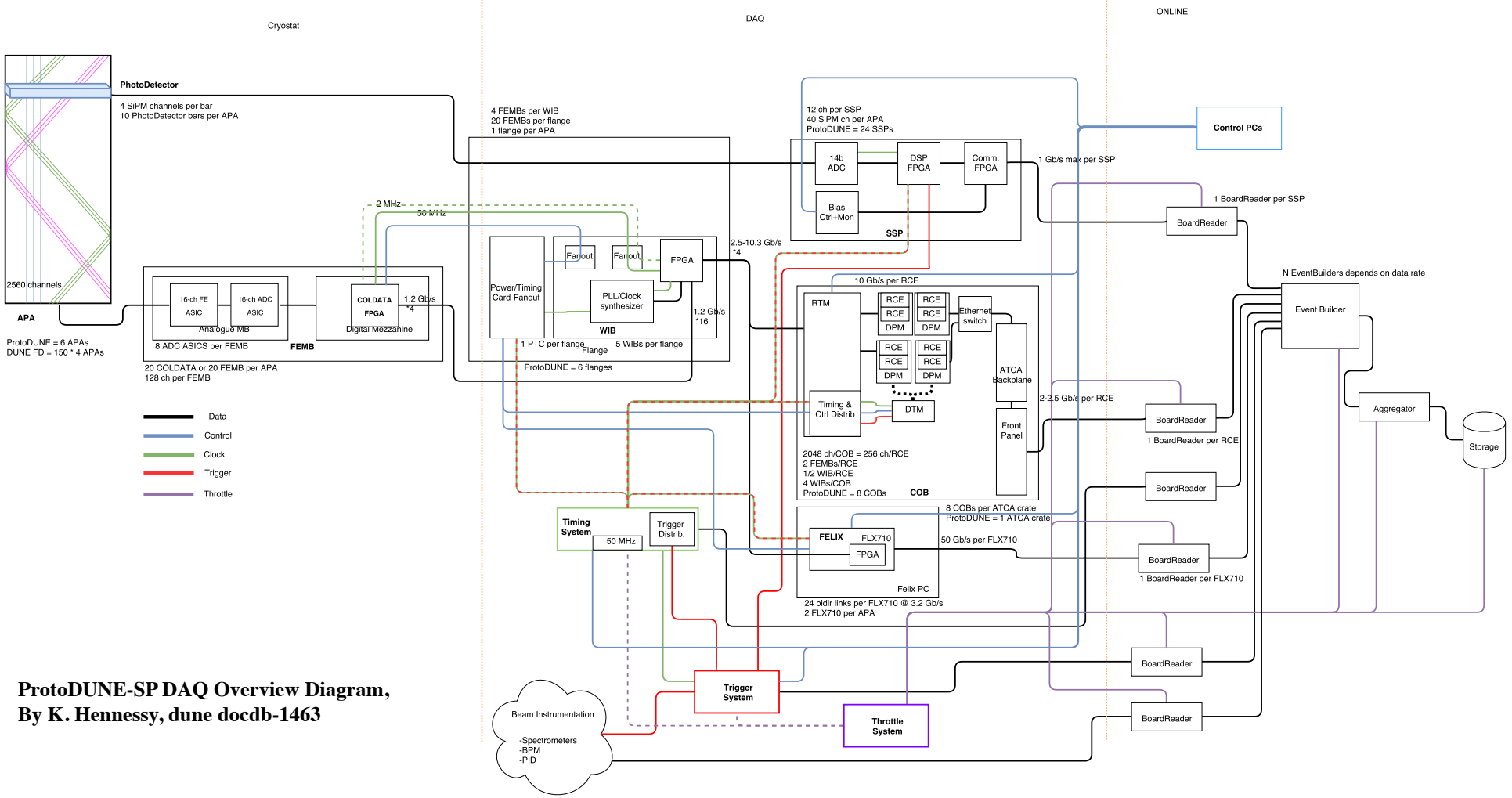


Shows that photon detector picks a noise from APA, but is not a significant source of noise on its own.

PD Electronics Activities & Plans

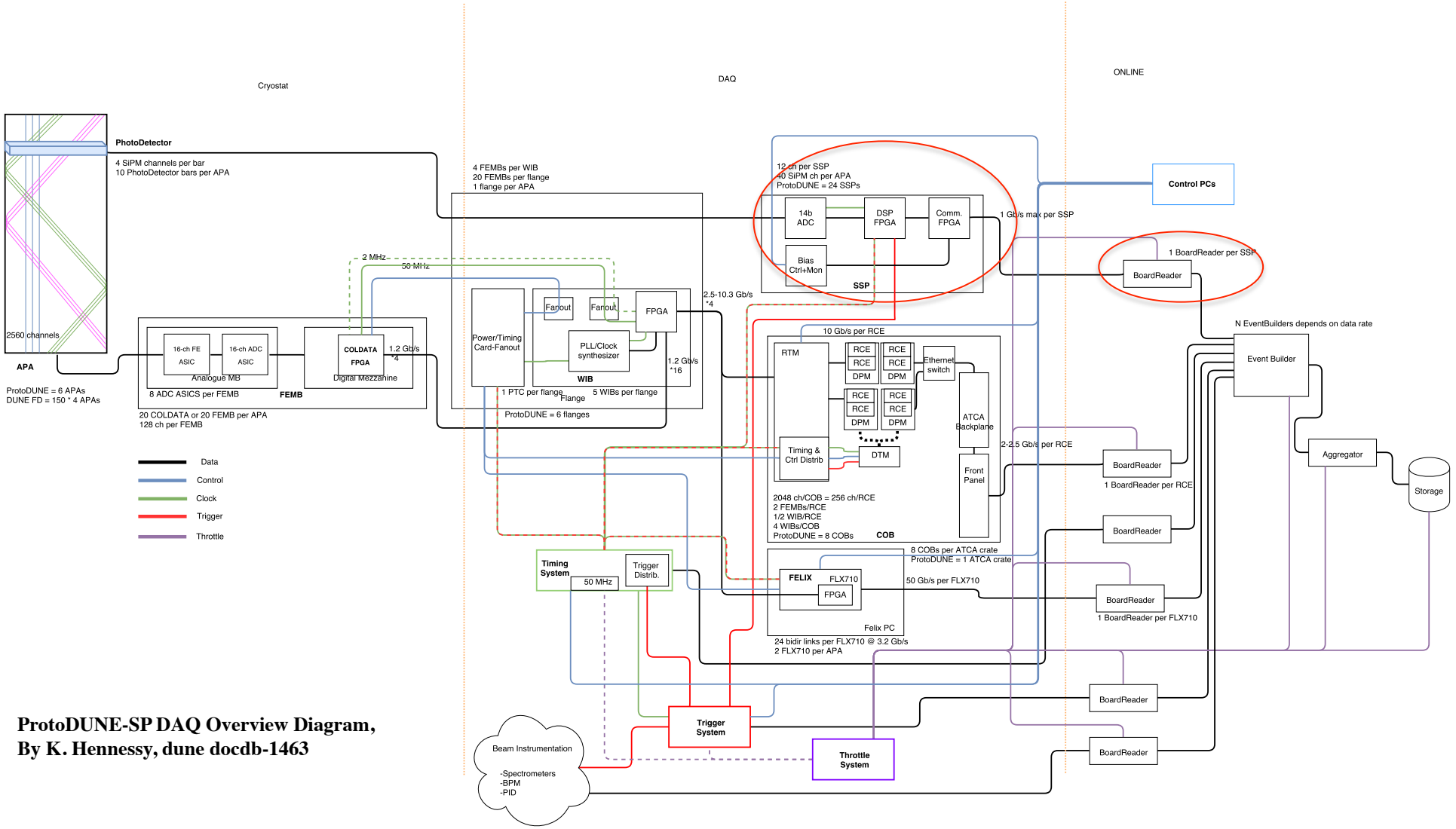
- **Recent Activities**
  - Implement and support readout of the 35-Ton Detector @ FNAL
  - SiPM ganging studies
  - Signal cable selection & tests
  - Associated connector selection
- **Current Activities (this fiscal year)**
  - Development of a prototype SSP with new connectors and cables
  - Tests with new SiPM mounting/ganging board
- **Next Steps: ProtoDUNE**
  - Incorporate design changes to meet protoDUNE requirements
    - DAQ
    - Timing
    - Power
    - Photon-Detector Feedthrough (APA Interface)
    - Grounding and Shielding
  - Fabricate SSP modules for protoDUNE

ProtoDUNE-SP DAQ Overview



ProtoDUNE-SP DAQ Overview Diagram, By K. Hennessy, dune docdb-1463

ProtoDUNE-SP DAQ Overview



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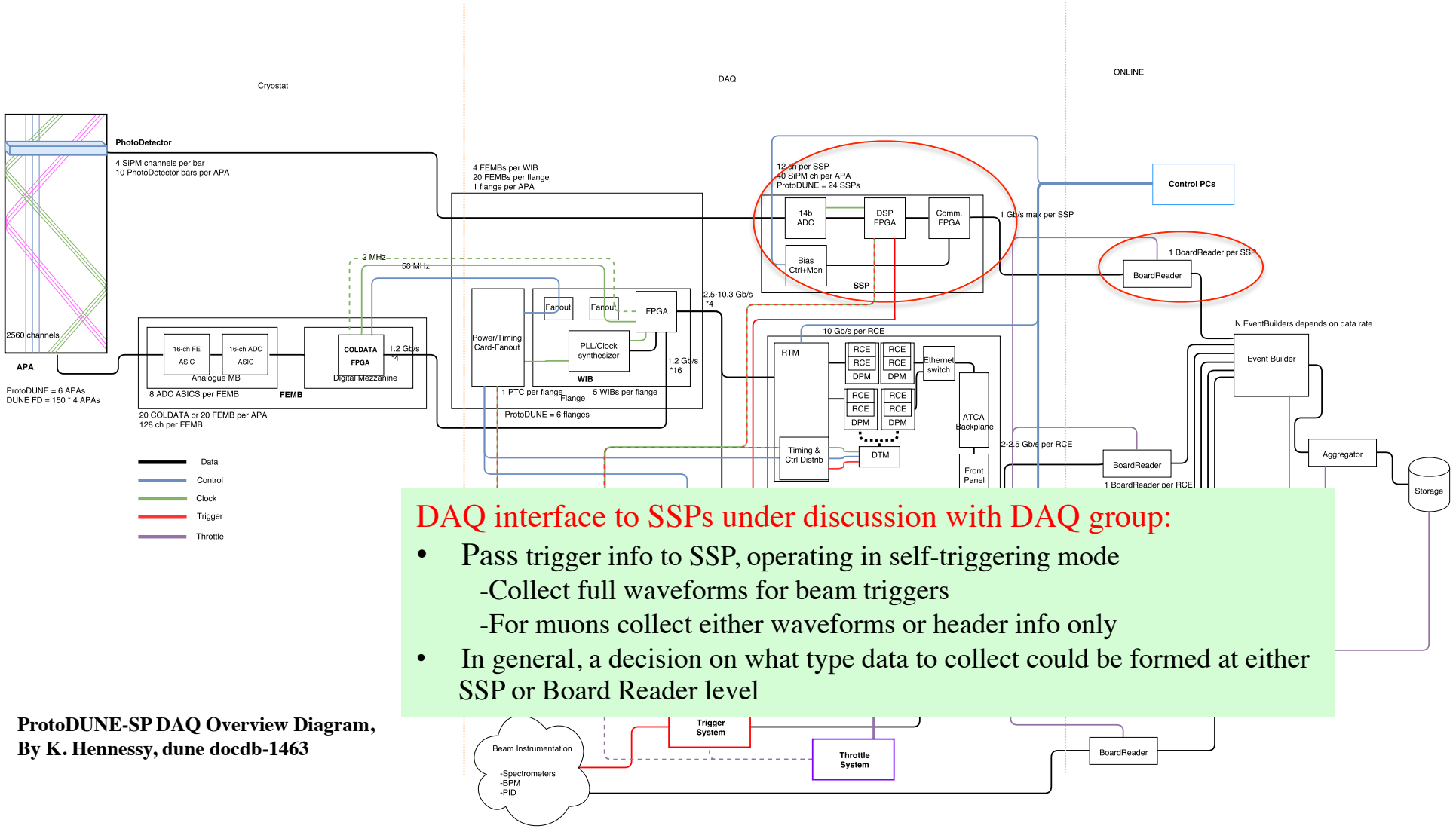
ProtoDUNE-SP DAQ Overview



DAQ interface to SSPs under discussion with DAQ group:

- Pass trigger info to SSP, operating in self-triggering mode
  - -Collect full waveforms for beam triggers
  - -For muons collect either waveforms or header info only
- In general, a decision on what type data to collect could be formed at either SSP or Board Reader level

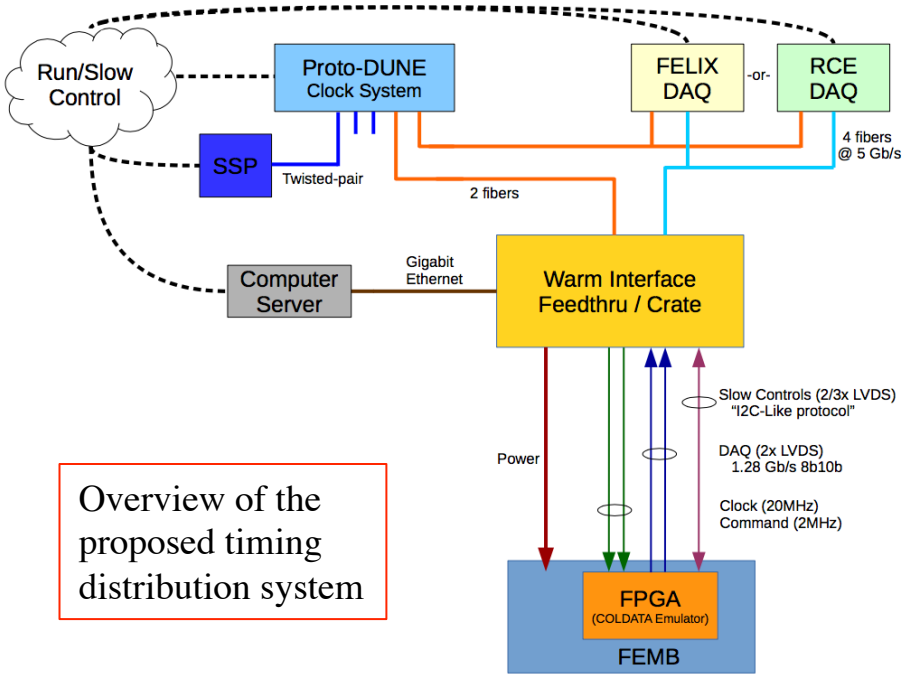
ProtoDUNE-SP DAQ Overview Diagram, By K. Hennessy, dune docdb-1463

Timing Interface

- The SSP clock management logic allows the ADCs in the SSP to be clocked to the NOvA timing system (or provide an external clock to the front panel)

- "DAQ to Cold Electronics Protocol and Timing for the ProtoDUNE TPC", DUNE-doc-1394, under development.
  -different from NOvA System

- New timing system would ideally use existing NOvA timing physical link at SSPs, but the protocol will change
  -will require modifications to the SSP firmware



Overview of the proposed timing distribution system

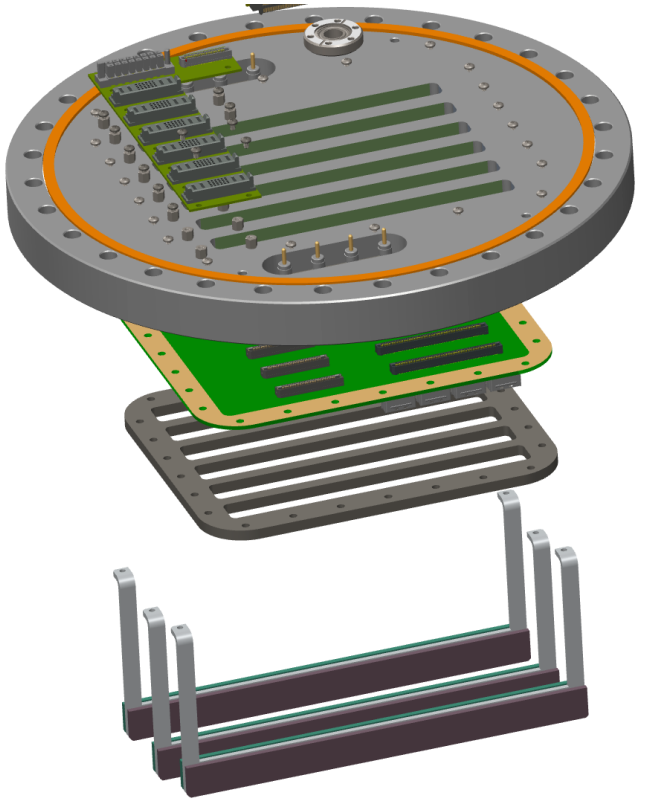
Photon-Detector Feedthrough

- BNL responsible for a mechanical portion of the feedthrough (flange, seal, strain relief) design.

- ANL responsible for Printed Circuit Board (PCB) Feed-through for Photon-Detector.

- 3D CAD model of the CE flange, key drawings, and the fabrication package of a prototype CE flange PCB exists.
  - -ANL will provide BNL an initial PD flange board PCB connector layout with minimum connector spacing.
  - -BNL will try to fit this layout to the existing CE flange design (14" CF), and iterate with ANL to get to the final PCB.
  - -BNL will be responsible for the integration of the PCB

- We have yet to define the electrical testing protocol.



Example of CE flange/ feedthrough design

Grounding and Shielding Approach

- Grounding and Shielding requirements:

- Describe modified SSP cable connector/cable plant …

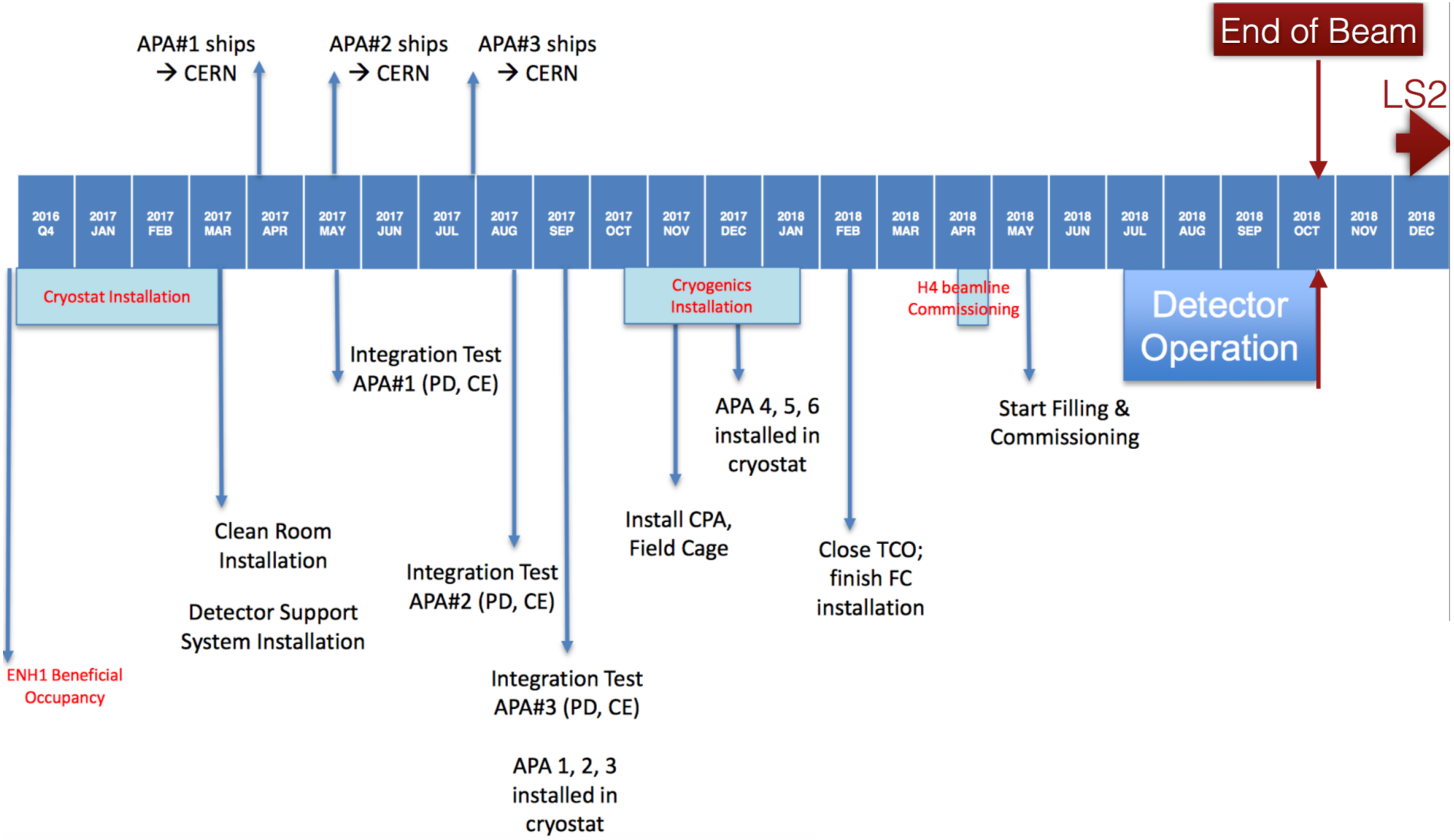
- There will be no AC distribution on top of the protoDUNE cryostat. Any equipment located on the top should be run with DC voltage
  -Requires DC-DC modification to SSPs power supply
  -DC powered SSPs may be located on top of the detector close to the feedthroughs

(-Other electrical interfaces described as well
-want to include SiPM board schematics and drawings
-etc.)

Next Steps

(describe how/when design changes will be incorporated, tested)

Schedule of Activities at CERN



- Schedule developed to address system testing, integration, installation, commissioning.
- PD readout activities start with a vertical slice test at CERN in Dec16 – Jan17.

Schedule of Activities at CERN

Summary

Backups