Warm Interface Electronics

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Representing work of Jack Fried, Hucheng Chen, Hans Berns and many others

Charge Questions

1. Are the requirements for the proposed ProtoDUNE-SP and SBND CE systems sufficiently complete and clear?

2. Does the conceptual design for the CE systems meet the requirements?

3. Are justifications for each of the specific technical design choices sufficiently documented?

4. Does the design as presented represent a good development path toward DUNE and are there opportunities for incorporating potential advances in the CMOS technology over the DUNE time scale?

5. Are the CE interfaces to other detector subsystems including TPC, DAQ, and cryostat well defined and documented?

6. Is the grounding and shielding plan for the detectors and its impact on the CE systems understood and adequate?

7. Does the proposed CE design adequately address potential catastrophic failure modes, such as large HV discharges?

8. Are the proposed integrated system tests sufficient to assure that the systems will meet the performance requirements for ProtoDUNE-SP and SBND? Have applicable lessons-learned from previous LArTPC detectors been documented and implemented into the QA plan?

9. Is the CE design robust enough and the quality control plan and testing program sufficiently comprehensive to assure the dead/bad channel requirements for ProtoDUNE-SP and SBND are achieved

This talk will primarily address question 5, but many others will be addressed in part

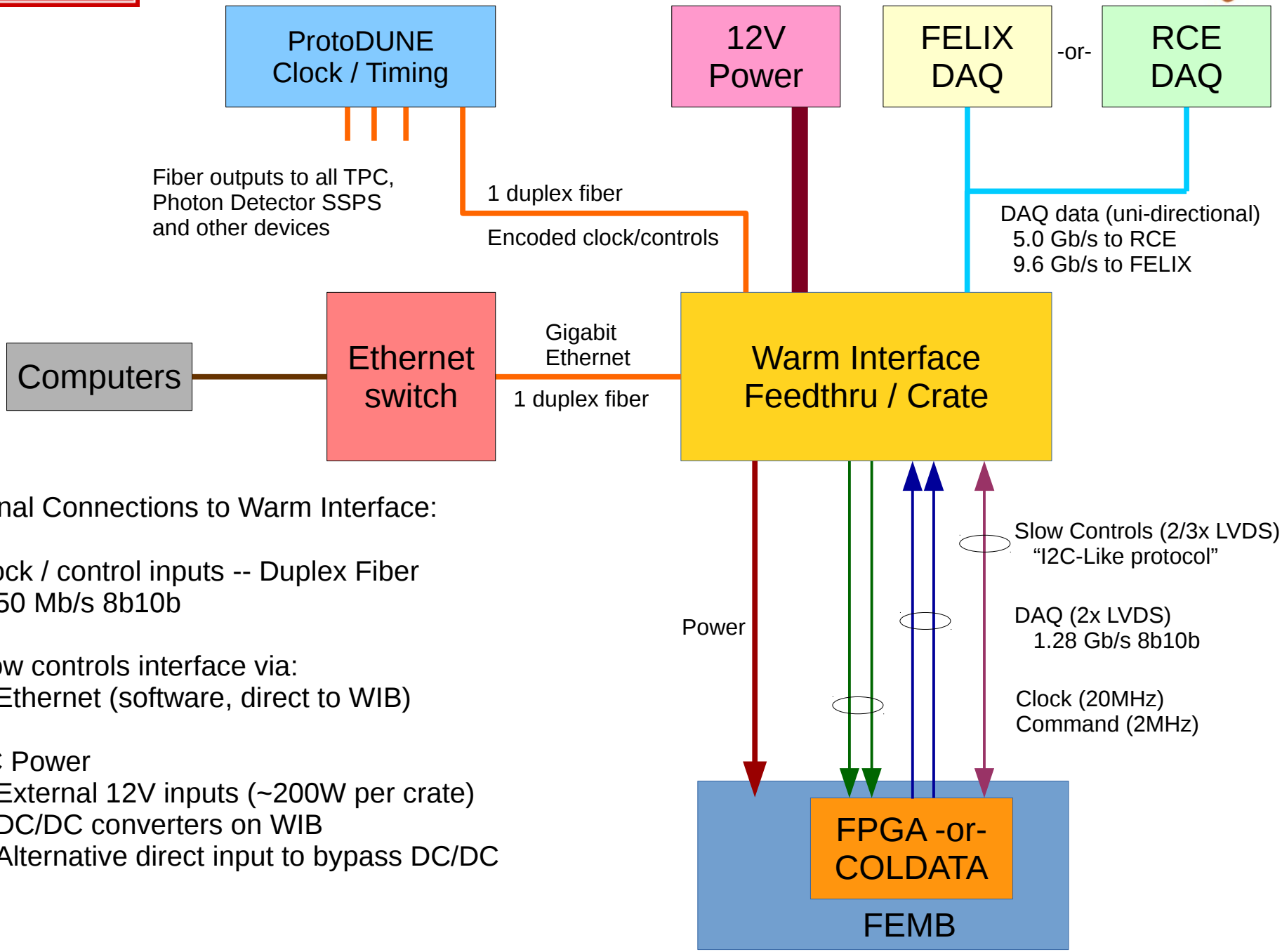
Outline

- Requirements
- Warm electronics overview
- Timing system
- Warm Interface Board
- Power and Timing Card
- Status and Schedule

Warm Electronics Requirements

- Supply DC power (~ 200W per flange) to cold
- Supply clock and control signals to cold
  - 50 MHz clock, RESET, SYNC commands [per COLDATA spec]
- Provide slow control interface (“I2C-like”)
- Receive data on Cu links at 1.28 Gb/s
- Check data for errors and transmit to DAQ:
  - RCE system at 5.0 Gb/s
  - FELIX system at 9.6 Gb/s
- Provide monitoring and “local DAQ” for testing via Gigabit Ethernet

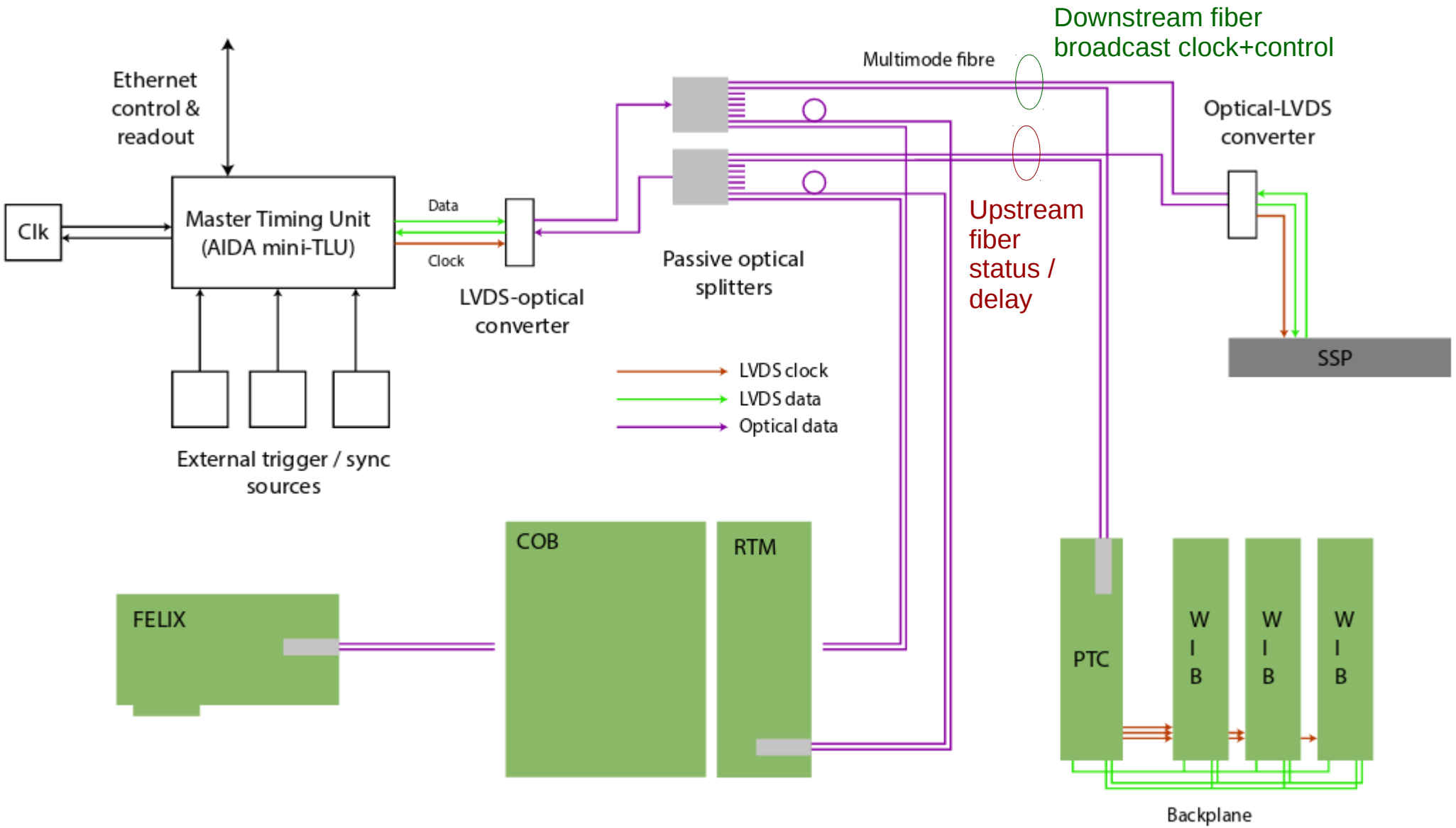
ProtoDUNE Single Phase TPC Electronics



External Connections to Warm Interface:

- Clock / control inputs -- Duplex Fiber
  - 50 Mb/s 8b10b
- Slow controls interface via:
  - Ethernet (software, direct to WIB)
- DC Power
  - External 12V inputs (~200W per crate) DC/DC converters on WIB
  - Alternative direct input to bypass DC/DC

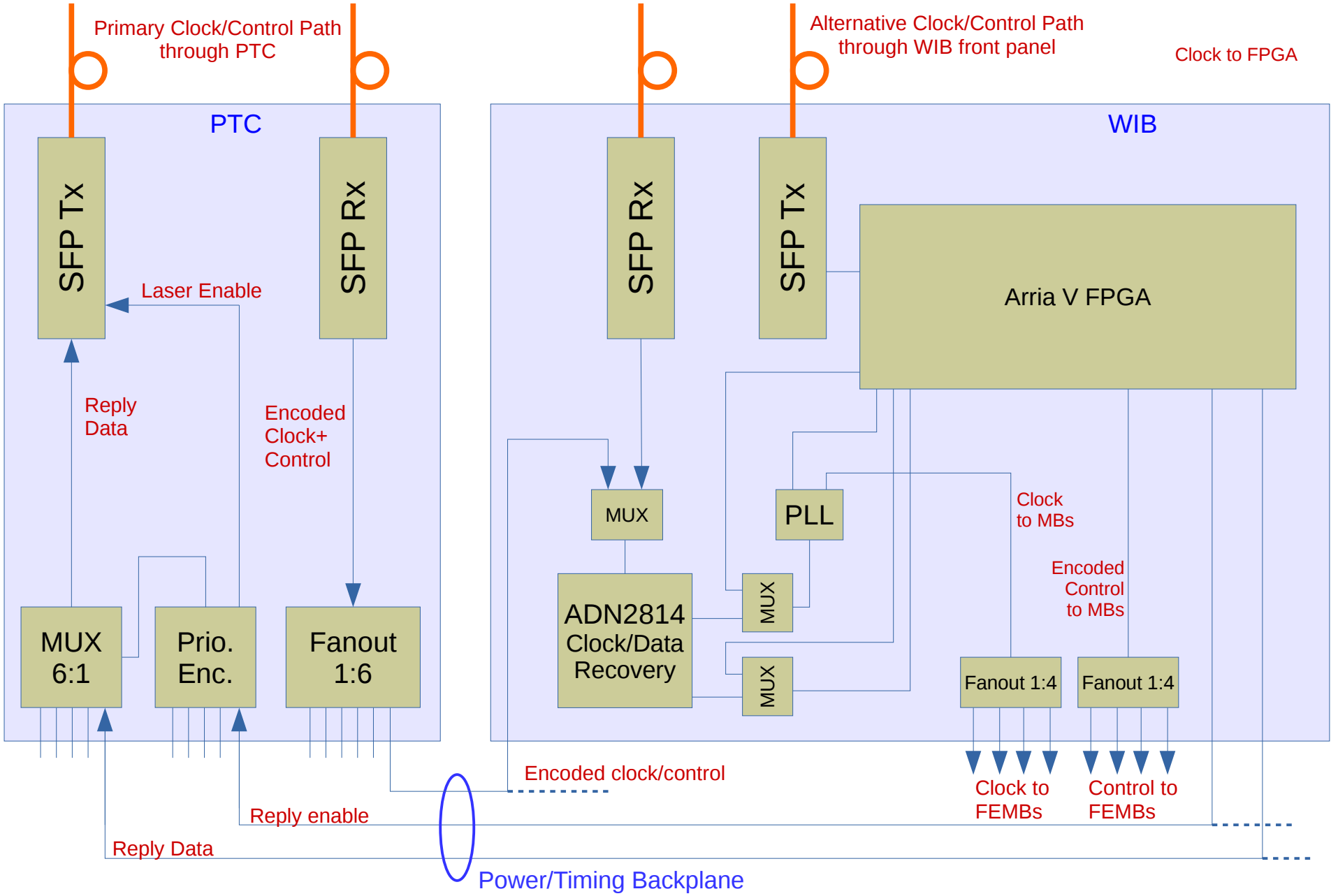
ProtoDUNE Timing System



Timing System Functions

- Master timing unit functions
  - Receive from GPS:
    - Master clock (10 Mhz), 1pps, time-of-day
  - Receive from other sources:
    - Beam timing signals
    - Triggers
  - Transmit (broadcast) on single fiber:
    - 50 MHz master clock
    - Encoded synchronous commands
      - CONVERT, SYNC, RESET, etc
    - Encoded asynchronous commands
      - Read error registers, etc (individually addressed)
- Timing endpoint functions
  - Receive and extract master clock
  - Receive synchronous commands (timing good to 1 clock tick)
  - Receive asynchronous commands and respond if required

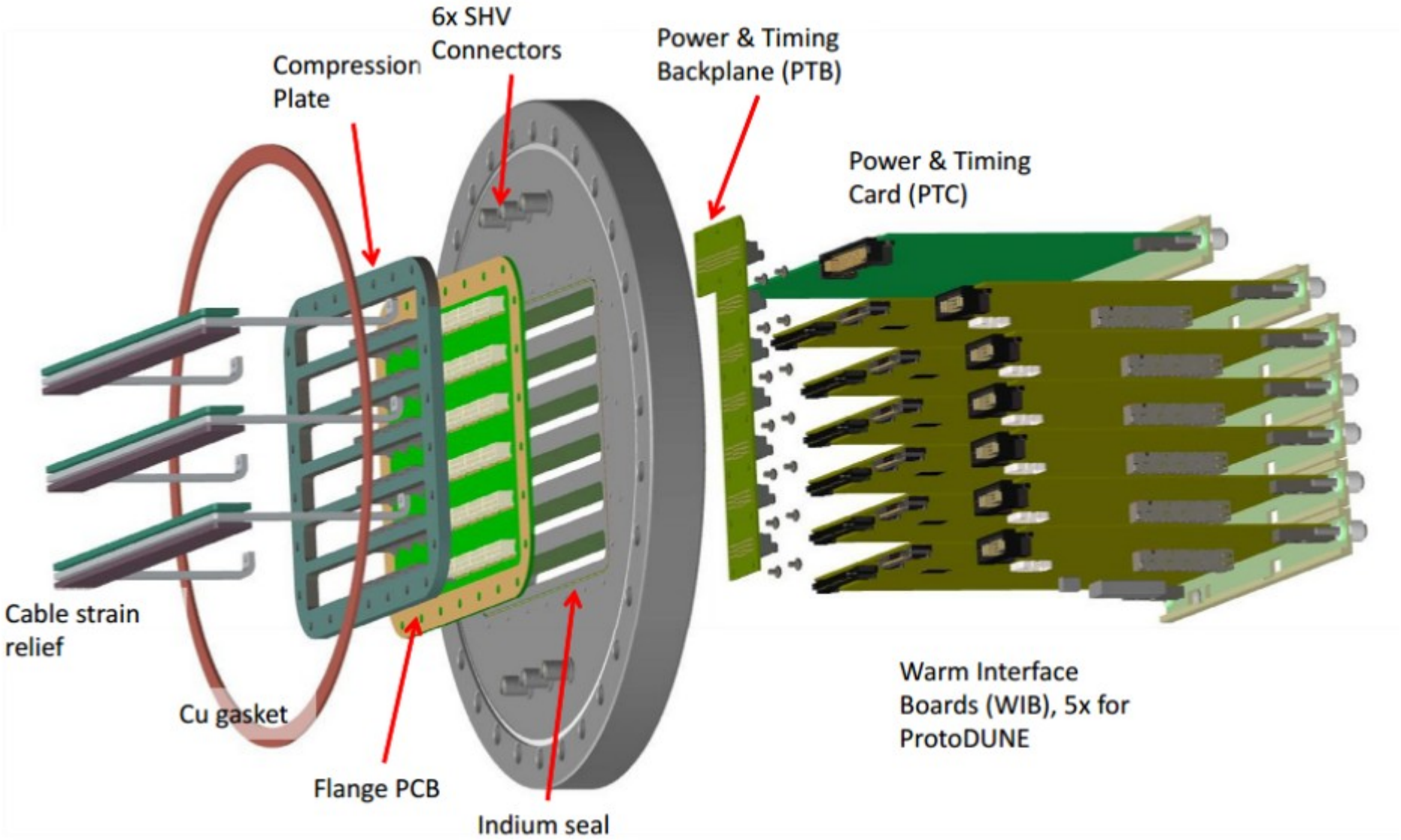
Warm Interface Crate Timing and Control



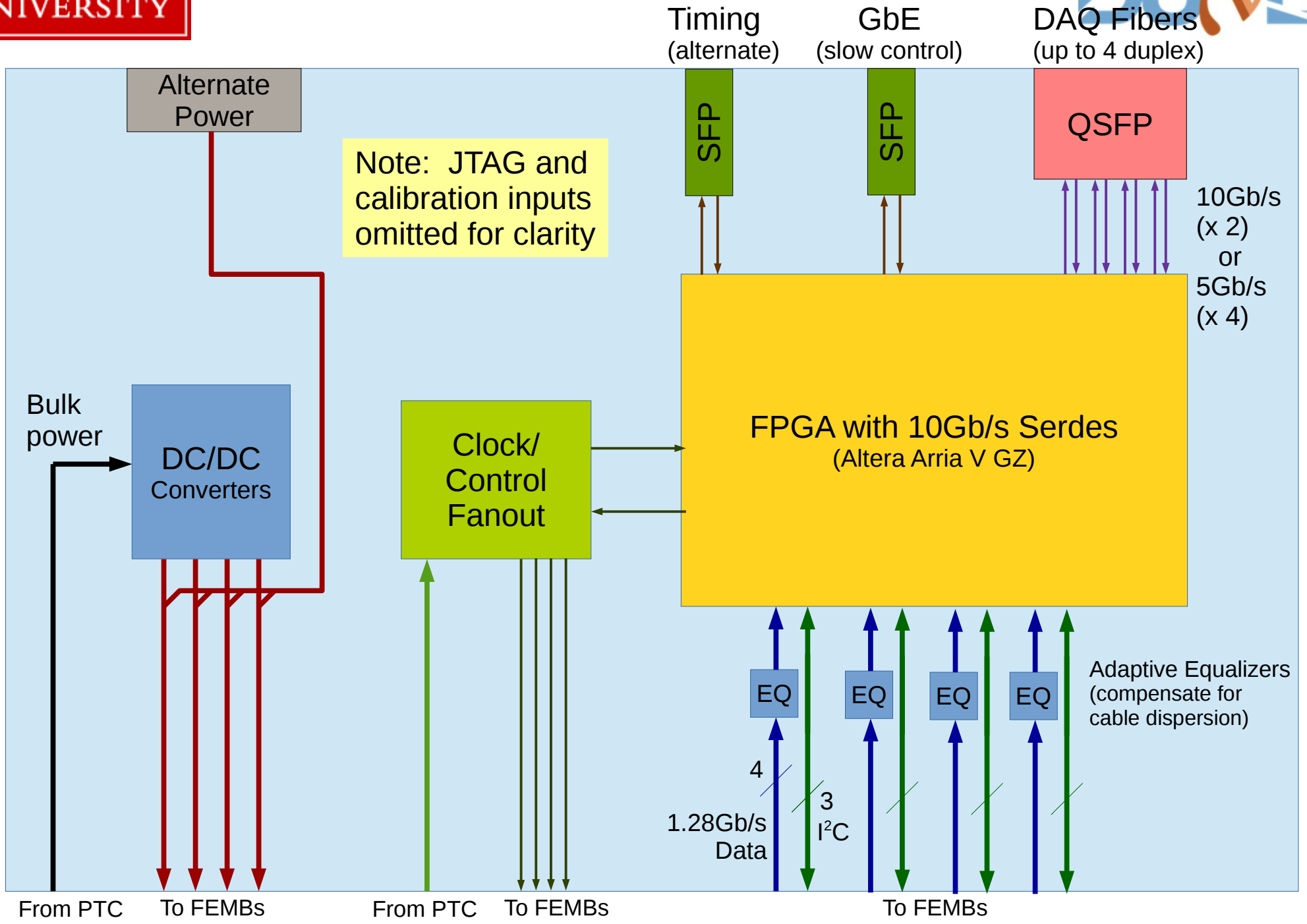
Timing Modes

- Normal Mode:
  - Encoded clock/controls from timing system via PTC fanned out on backplane to WIBs
- Individual WIB Mode:
  - Encoded clock/controls from timing system to WIB for bench tests or other special conditions
- Stand-alone Mode:
  - Clock and controls generated by FPGA based on on-board crystal oscillator

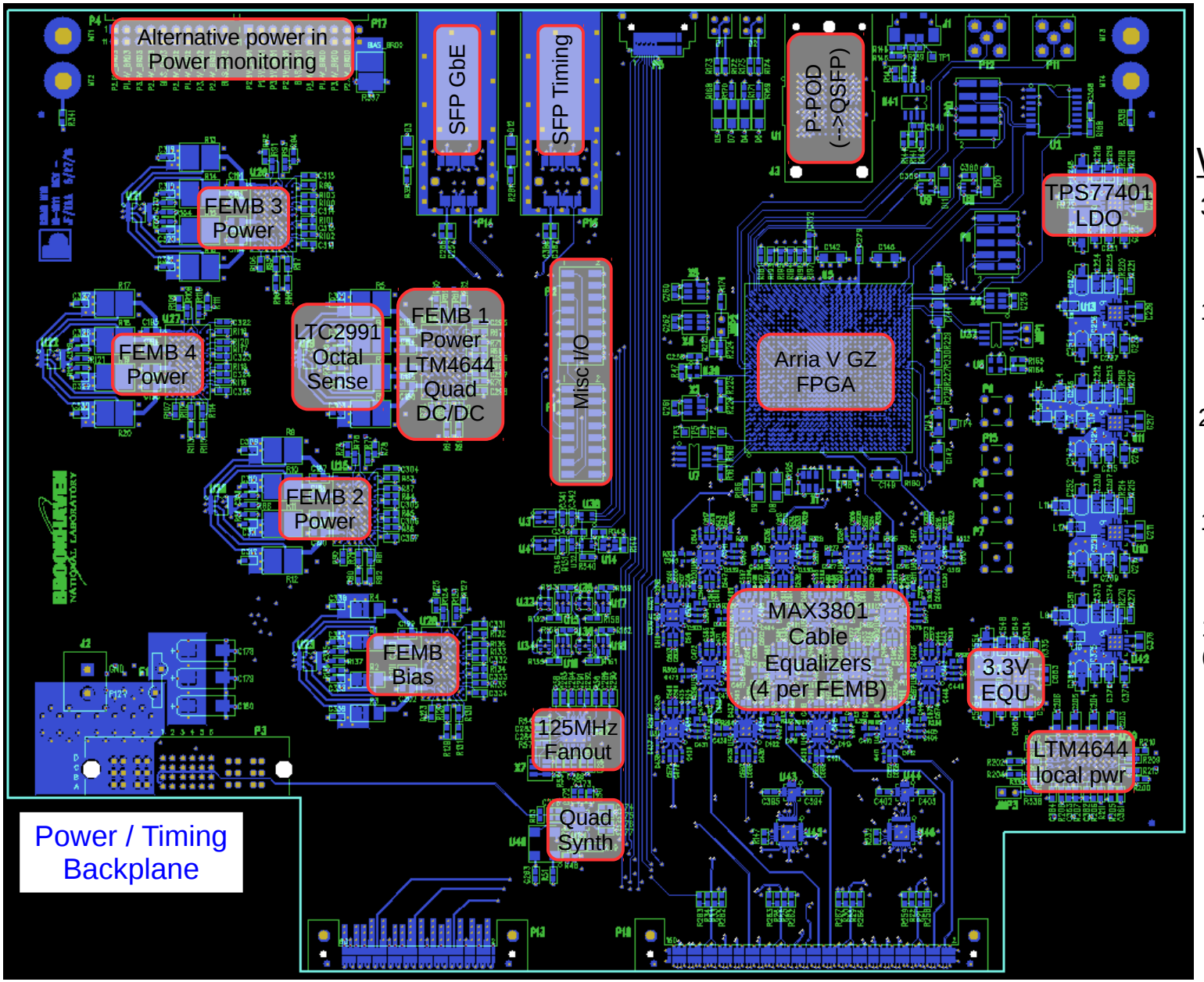
Warm Interface



ProtoDUNE WiB Block Diagram



(SBND) WIB Layout



WIB power

3.3V

1.5V

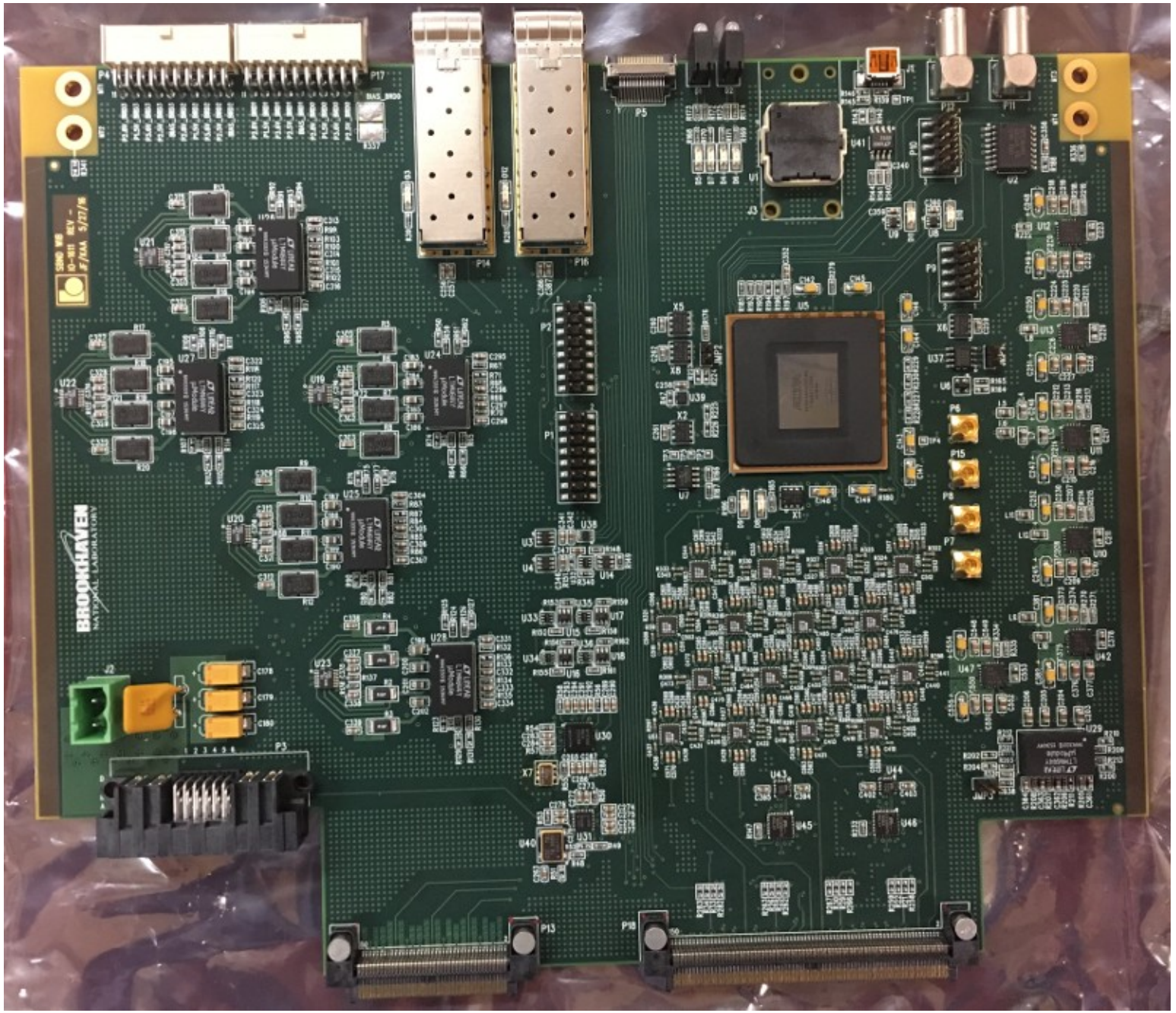
2.5V

1.1V

1.15V
(FPGA GXB)

5V
3.6V
2.8V
1.8V

SBND WIB

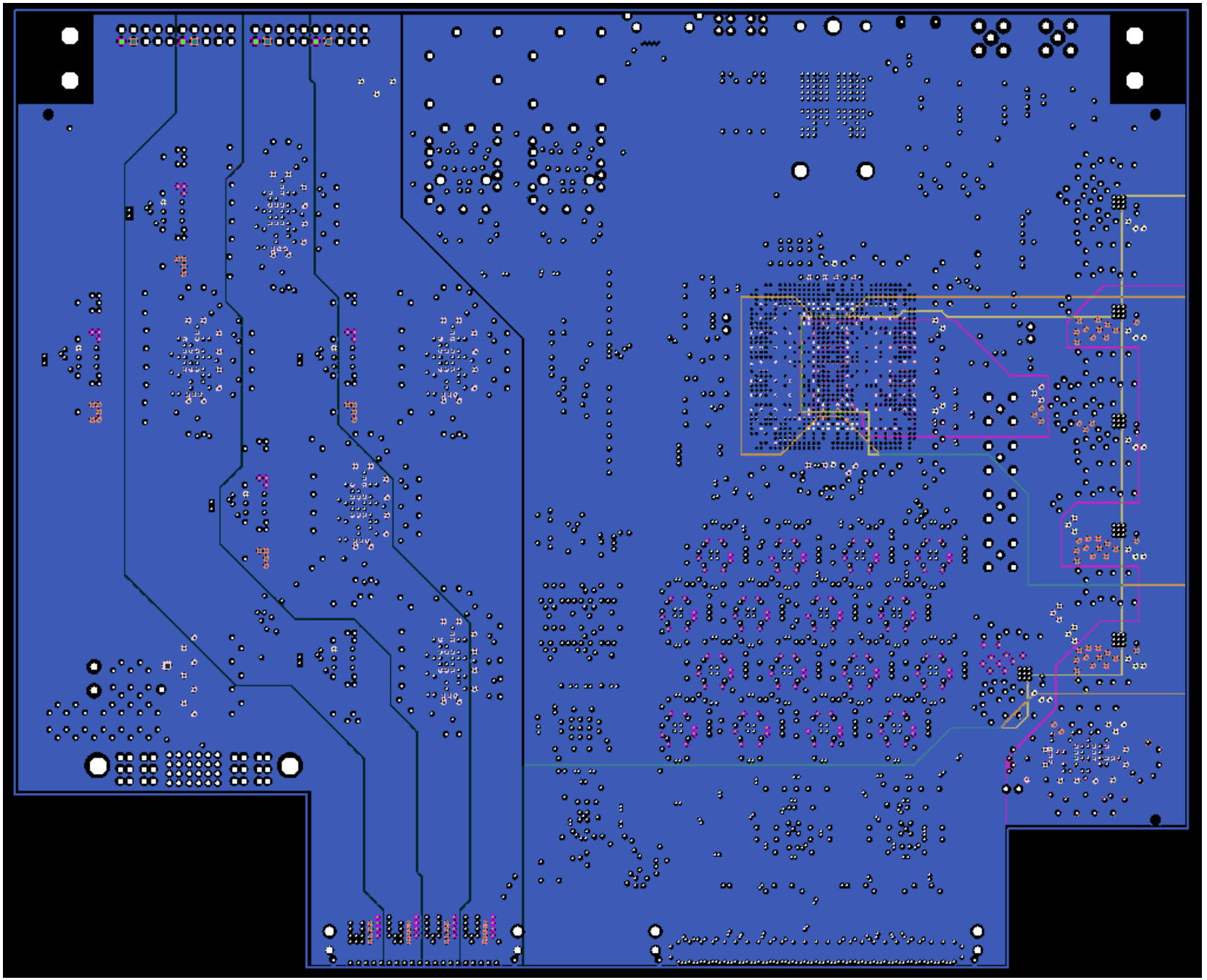


(SBND) WIB Layout

(4) split planes provide voltages to each FEMB

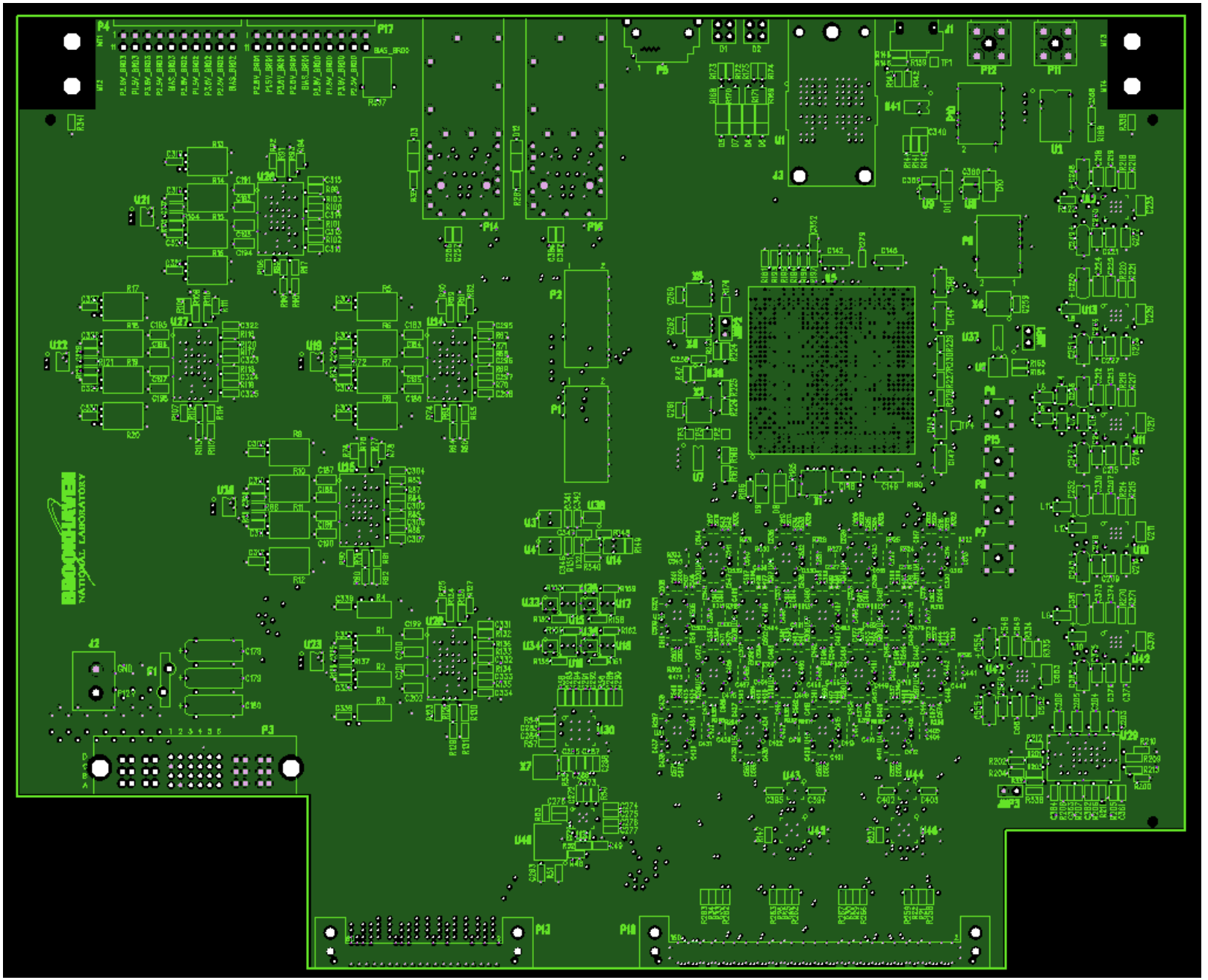
2.5V ~1A
1.5V < 0.3A
2.8V < 0.3A
3.6V < 0.3A
(per FEMB)

Supply are isolated between FEMBs (common GND)

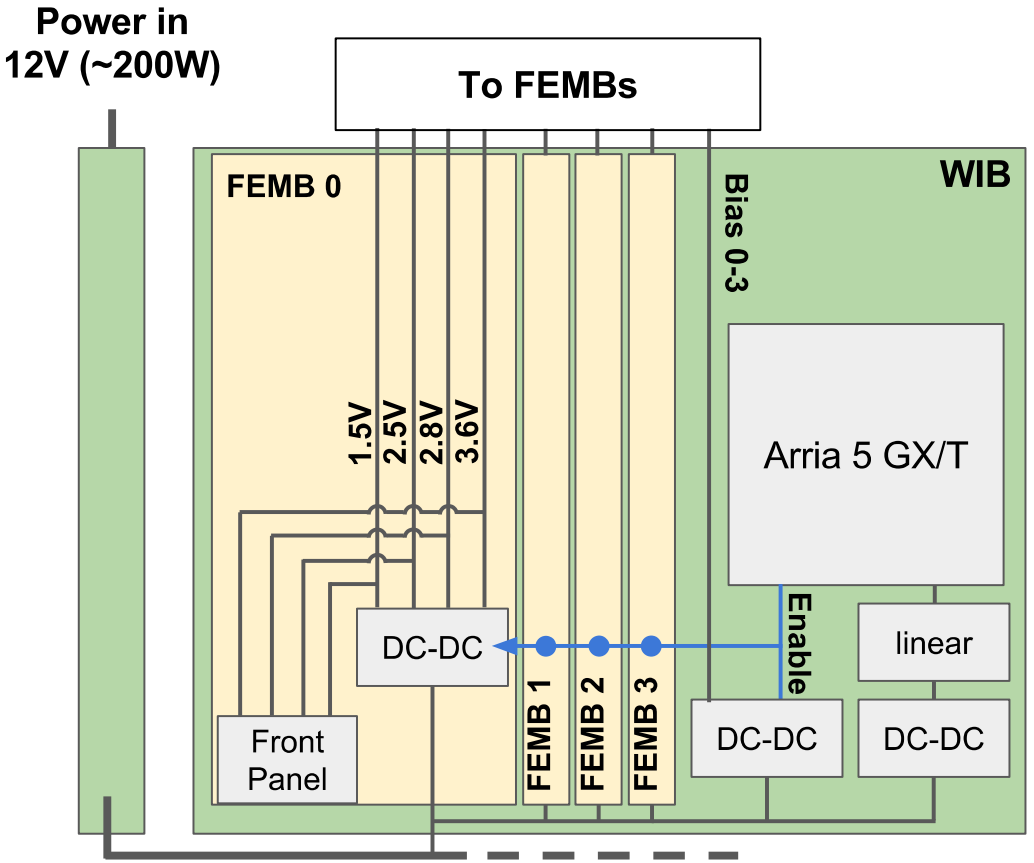


(SBND) WIB Layout

Single GND plane (GND common on feedthru board too)

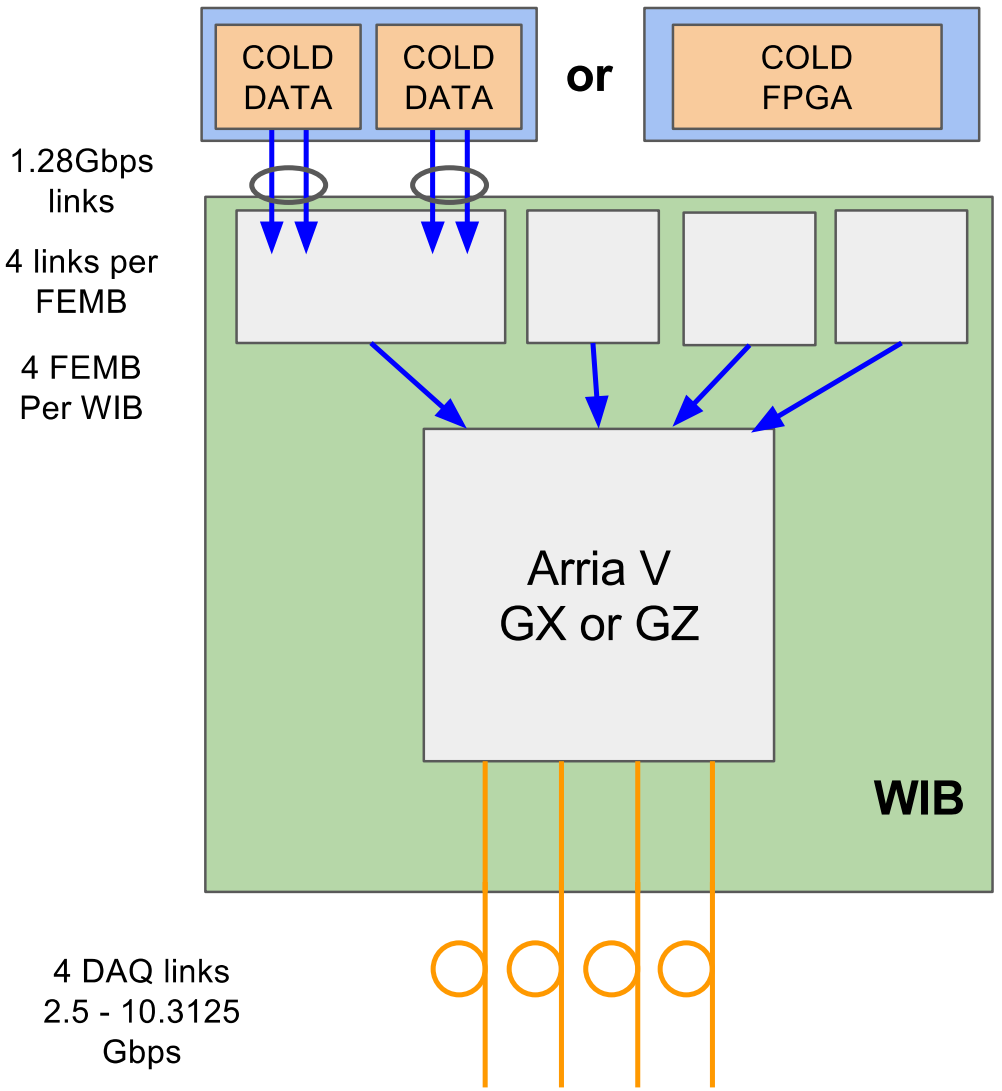


WIB Power



- Power for cold:
  - Each FEMB requires 1.5V, 2.5V, 2.8V, 3.6V and bias
  - Primary power path:
    - External 12V distributed through PTC, backplane
    - Each WIB uses LTM4644 quad DC/DC converters to generate required voltages
  - Alternate power path:
    - Front panel connector receives regulated cold power directly

WIB DAQ links



- FEMB source
  - ProtoDUNE FEMB has one FPGA simulating two COLDATA ASICS
  - Each ASIC sends two 1.28Gb/s LVDS streams
  - Each stream sends 56 bytes per 500ns
  - About 3.6 Gb/s payload per FEMB
- WIB
  - Multiplex data from 4 FEMB
  - Output to FELIX or RCE (2x 9.6Gb/s or 4x 5.0Gb/s)

Data Format
WIB → RCE

WIB firmware performs extensive error/consistency checking on input data.

Errors are flagged.

Entire frame is protected with a CRC-32.

PRELIMINARY WIB-RCE Data format @ 5.0 Gb/s

Word	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	COLDATA_Timestamp[7:0]								K28.5								WIB Header (6 words)
2	Timestamp Extension [23:16]								COLDATA Timestamp [15:8]								
3	Timestamp Extension [39:24]																
4	Error-Bits								ASIC[B]				Capture[A]				
5	WIB_Timestamp[15:0]																
6	Format Version					FiberNo			SlotNo				CrateNo				
7	Reserved								Stream_2_Err[C]				Stream_1_Err[C]				
	Checksum_B[7:0]								Checksum_A[7:0]								COLDATA 1 (56 Words)
	…																
62	S8 [99:84]																
63	Reserved								Stream_2_Err[C]				Stream_1_Err[C]				
	Checksum_B[7:0]								Checksum_A[7:0]								COLDATA 2
	…																
118	S8 [99:84]																
119	CRC-32 [15:0]																WIB Trailer (2 words)
120	CRC-32 [31:16]																
121	K28.2								K28.1								Padding
122	K28.2								K28.1								
123	K28.2								K28.1								
124	K28.2								K28.1								
125	K28.2								K28.1								

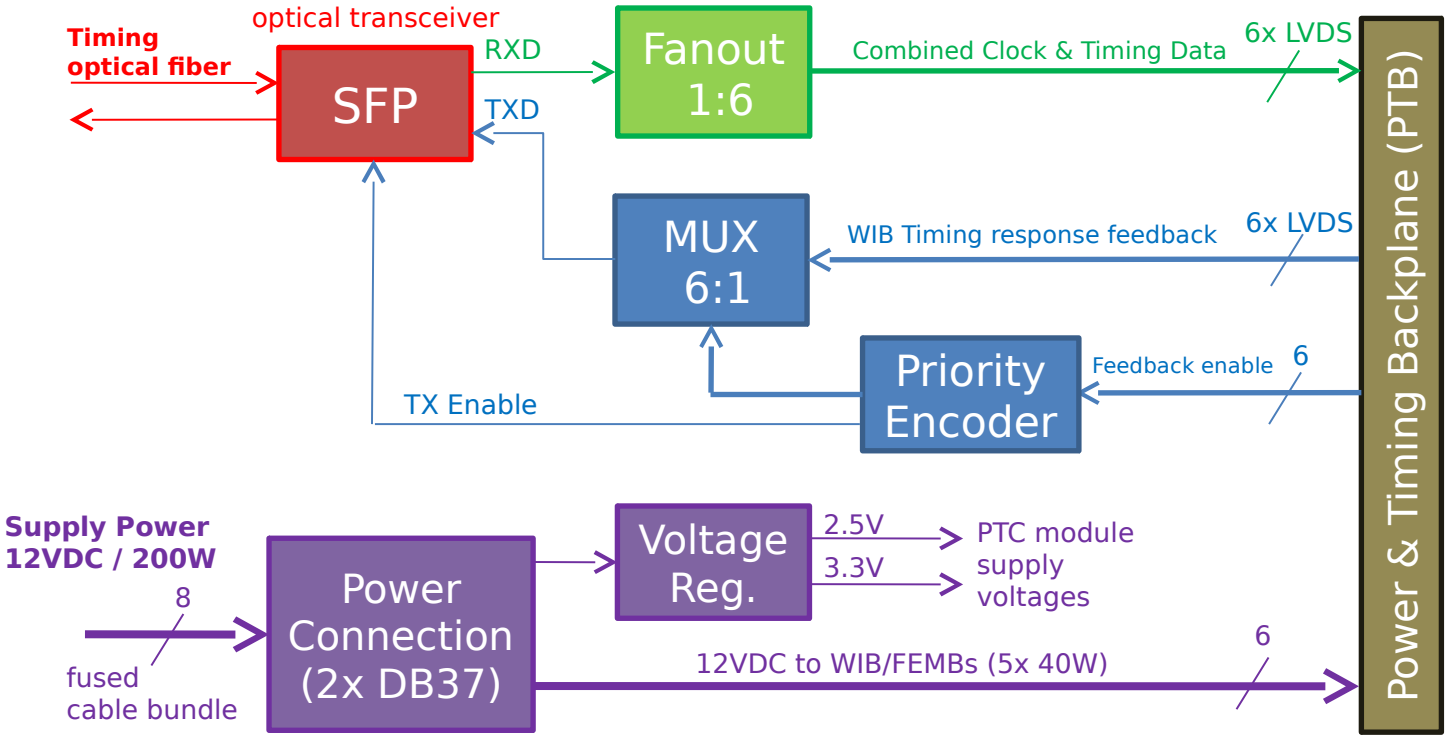
SBND/ProtoDUNE WIB Changes

- Replace PPOD with QSFP
  - Rearrange FPGA transceiver pins to support 10Gb/s
- Modify MPTC backplane connector to work with new ProtoDUNE PTC design
  - Support LVDS output signals for timing system feedback
- Add Si5338 clock synthesizer for 10Gb link reference clock
- Add ADN2184 clock/data recovery IC for timing system
  - Also add SY89847U ultra-low jitter mux to select timing input (front panel vs backplane via PTC)

Power & Timing Card (PTC) for ProtoDUNE

- Plugs into the Power & Timing Backplane (PTB) of the Warm Interface Electronics
- Receives 12V DC Low Voltage Power for the Entire Cold & Warm Electronics of a Flange
  - Approx. 200W for 5x WIB, 50x FEMB
  - LV fanned out to each WIB over PTB
- Bidirectional fiber interface between the ProtoDUNE Clock System and WIB modules
  - Combined Clock/Data signal from Clock System fanned out to WIBs via differential LVDS signals over the PTB Backplane
  - WIB Timing Response Feedback via the PTB Backplane multiplexed to the ProtoDUNE Clock System

Power & Timing Card (PTC) for ProtoDUNE

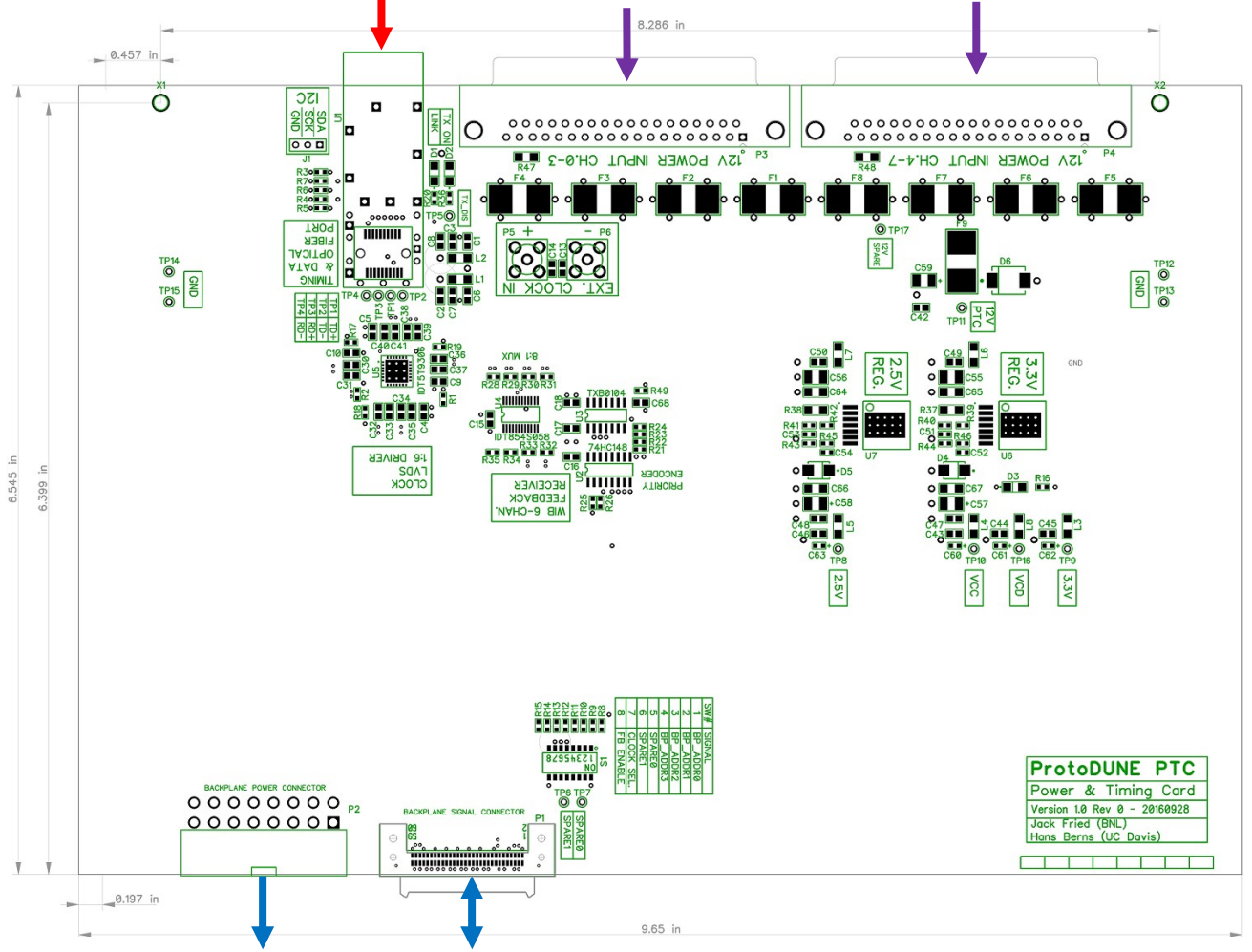


Note: 6 channels wired for SBND PTB backplane compatibility
5 channels used for ProtoDUNE

PTC Preliminary Layout and Dimensions

Optical Fiber

12V Power Input (2x DB37 conn.)



Backplane Connectors: Power + Signals to/from WIBs

Status / Schedule

WIB P1 (SBND) under test

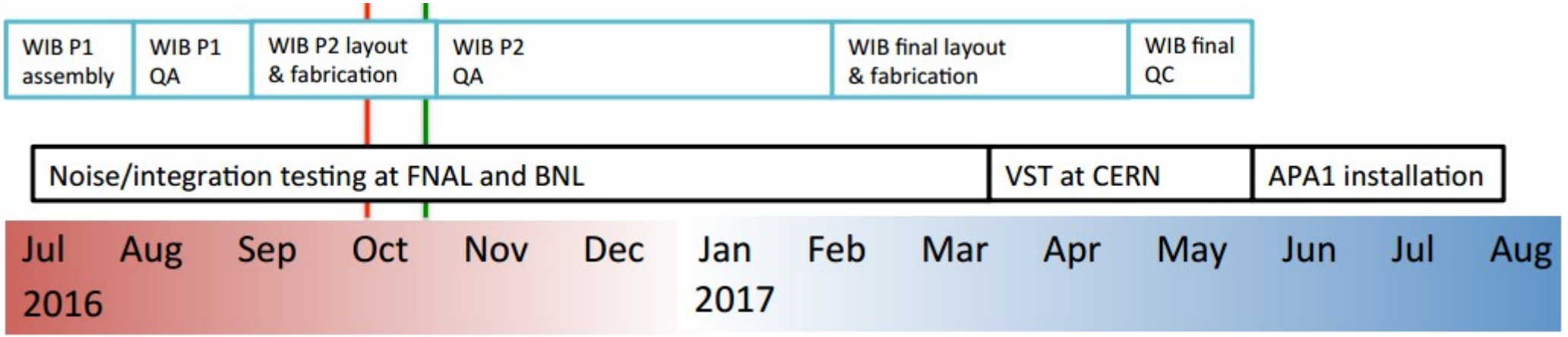
Firmware developed at Boston / have WIB and RCE setup and ready for integration

WIB P2 (ProtoDUNE) design changes underway

PTC layout underway

PTB identical to SBND so no changes required

Prototype Development		Design	Fabrication	Test
Warm Electronics	WIB	P1 ✔ P2 ongoing	P1 ✔ P2 October	P1 ongoing P2 November
	PTB	✔	October	November
	PTC	✔	October	November



Backup Slides

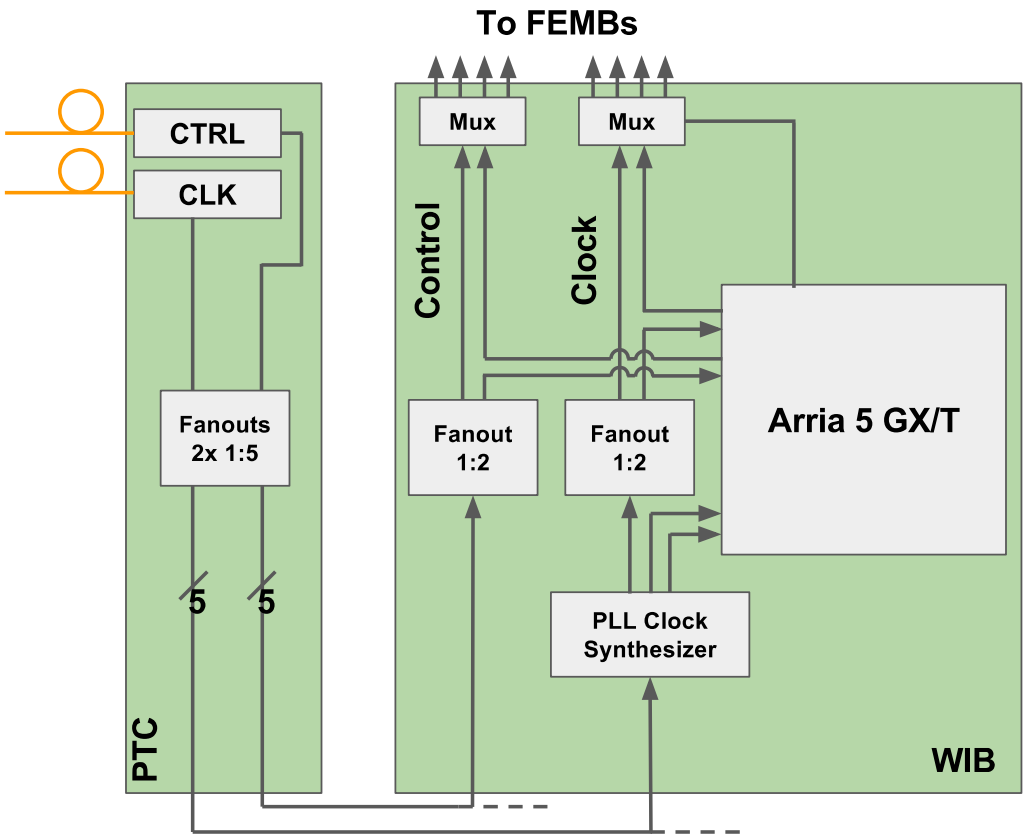
Timing System Details

- Low-level protocol is 50 or 100 Mb/s (*t.b.d)* straight binary using 8b10b coding
- Two command types:
  - Synchronous packet: 3 symbols (15 clocks)
    - Header (8b10b comma sequence)
    - Command byte
    - Time offset byte (allows alignment of command)
  - Asynchronous packet: 8+n symbols
    - Header (8b10b comma sequence)
    - Address (2 bytes)
    - Command byte
    - Data bytes
    - Checksum/CRC (2 bytes)
    - Trailer (8b10b control sequence)

Timing System Details

- Phase Adjustment
  - Adjust phase of each endpoint so all are within 1 clock tick
  - Adjustment procedure:
    - Enable endpoint transmission (via command)
    - Wait for CDR lock and measure clock phase
    - Request status packet
    - Measure whole-cycle offset to establish roundtrip time
    - Issue delay / phase adjustment command
    - Verify correct alignment
    - Disable endpoint transmission
  - This procedure is estimated to talke ~10ms per endpoint

WIB Timing + Control



- PTC → WIB
  - Two fibers/pairs with clock, encoded control
  - Fanned out to each WIB
- On WIB:
  - PTC clock used to synthesize clocks for FPGA and cold
  - Incoming clock/control fanned out to FPGA
  - Clock/control source selectable FPGA or external
- Limitations of current design:
  - Only external clock goes thru PLL
  - Third (return) fiber/pair used in NoVA system not yet included

Warm Electronics Status

- SBND versions under test
  - (BNL Talk)
- Development / integration of firmware for ProtoDUNE underway in Boston
  - We have a WIB and RCE
  - Initial firmware is running on Altera dev board with loop-back
  - Expect to commission the WIB to RCE link soon
  - Integration with FEMB is the next step
- Expect to complete ProtoDUNE version of WIB this fall and port the firmware (should be a minor job)