SBND Warm Electronics Design and Integration Test with DAQ System

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Cold Electronics Review

October 13, 2016

BROOKHAVEN NATIONAL LABORATORY

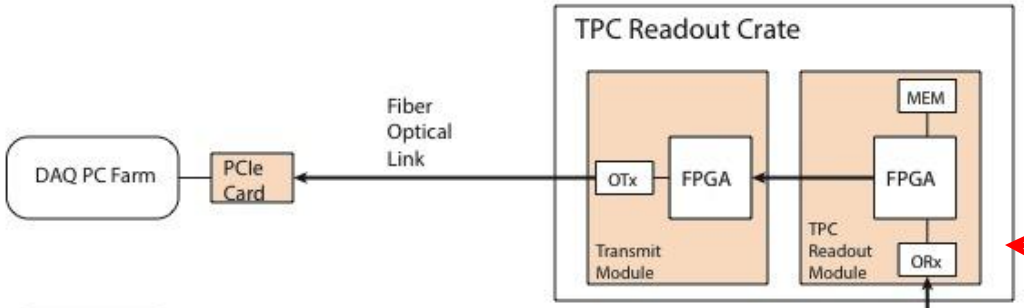
a passion for discovery

U.S. DEPARTMENT OF ENERGY | Office of Science

Outline

- SBND System Overview
- SBND Warm Interface Electronics
  - Warm Interface Board (WIB)
  - Power & Timing Card (PTC)
  - Power & Timing Backplane (PTB)
  - Magic Blue Box (MBB)
    - Used for Timing and Control Fan-out
- Nevis Integration Test
- Summary

SBND TPC Electronics

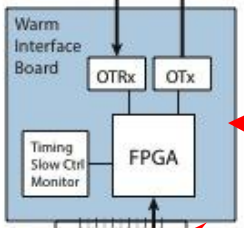


TPC Readout Electronics

Back End Electronics

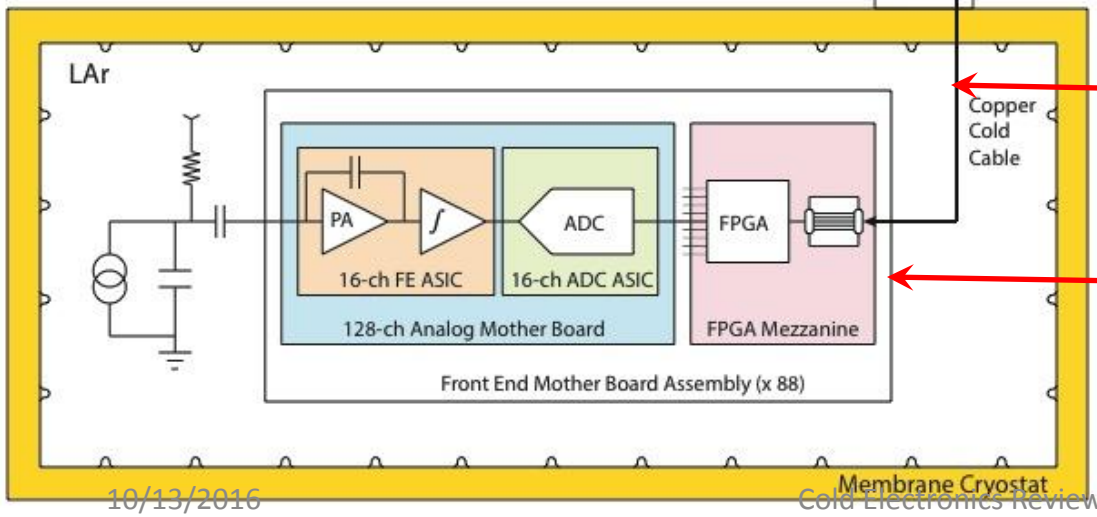
Front End Electronics

- ***Front End Electronics System***
  - ***704 FE ASICs/704 ADC ASICs/88 Cold FPGAs***
  - ***88 Front End Mother Board assemblies***
  - ***4 sets of cold cable bundles, 4 sets of signal feed-throughs***
  - ***~22 warm interface boards***



Warm Interface Electronics

Signal Feed-through



Cold Cable

Cold Electronics

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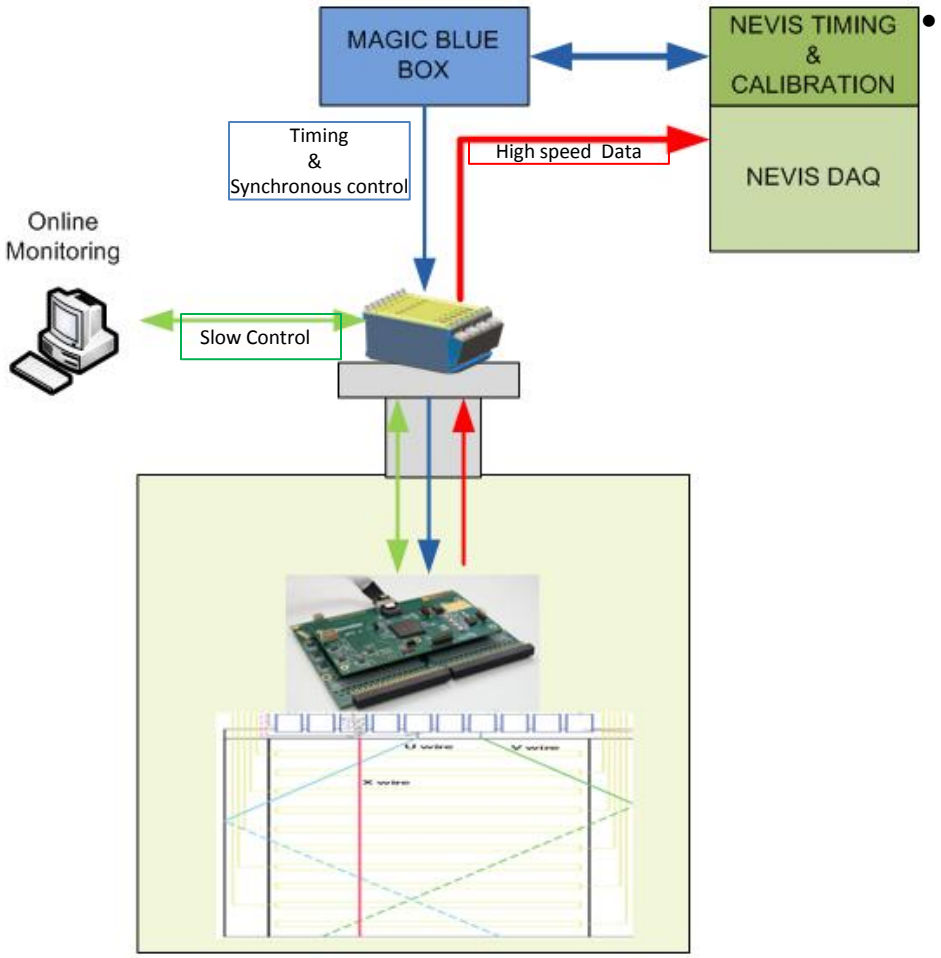
SBND Communication and Control Paths

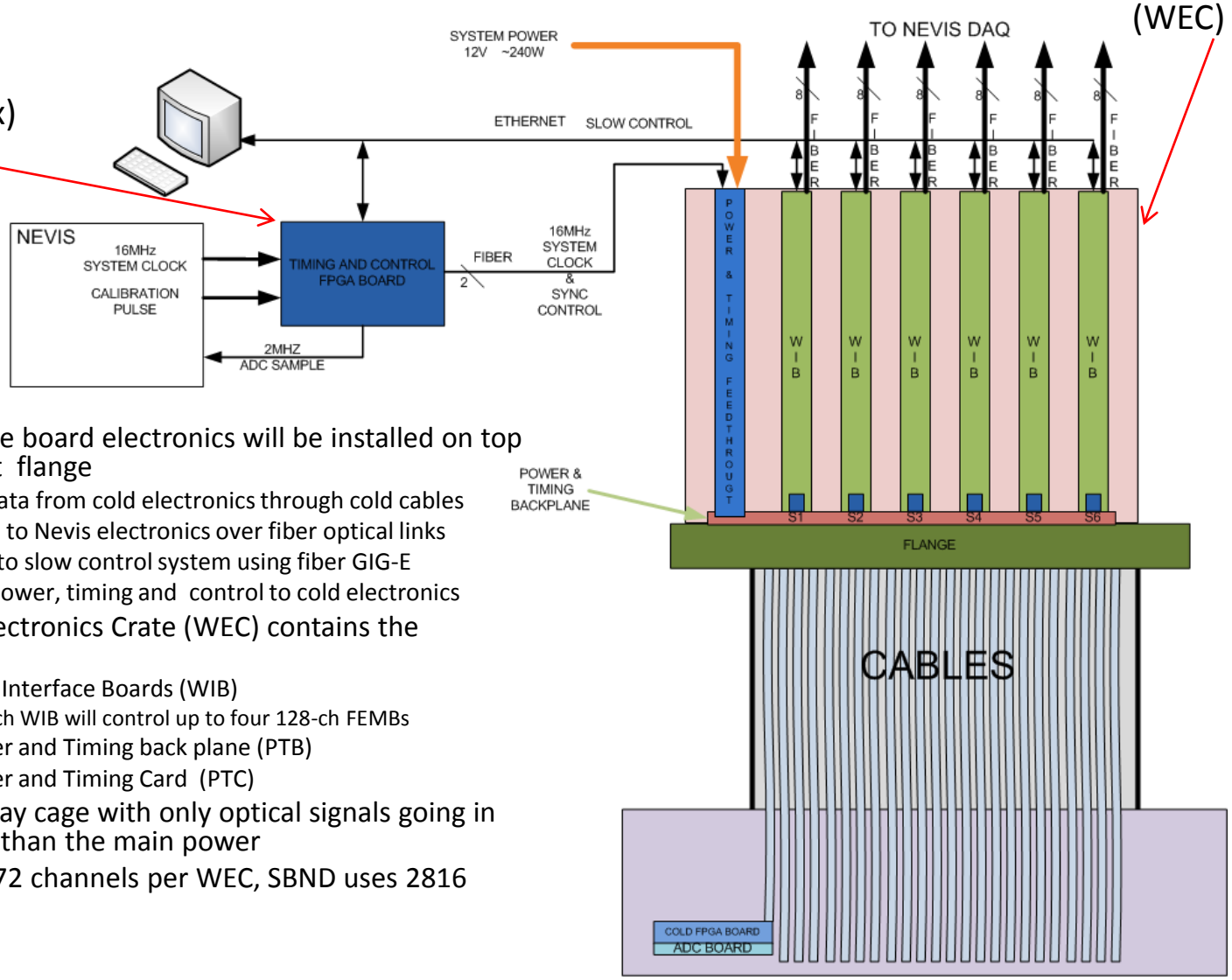


- SBND uses three paths for communication and control
  - High speed Data
    - Unidirectional data sent from FEMB->WIB->(Nevis DAQ)
      - ADC Data
  - Slow control
    - GigE Link WIB <-> Online monitoring system
    - I2c Link FEMB <-> WIB
    - Used to control and monitor all system electronics
      - Program ASIC SPIs
      - Monitor Board voltages & currents
      - System debugging (real time ASIC DATA)
      - FEMB & WIB register control
  - Timing & Synchronous Control
    - A unidirectional path from Nevis DAQ -> MBB-> WIB -> FEMB
      - System clock fan-out
      - ADC sampling clock
      - Synchronous commands such as calibration pulse and time stamp reset

SBND Warm Interface Electronics

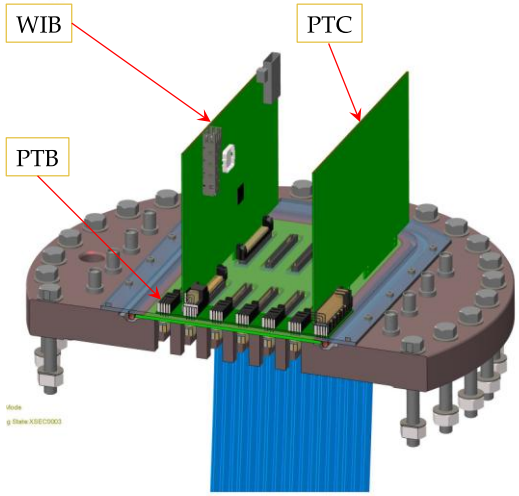
Warm Electronics Crate (WEC)

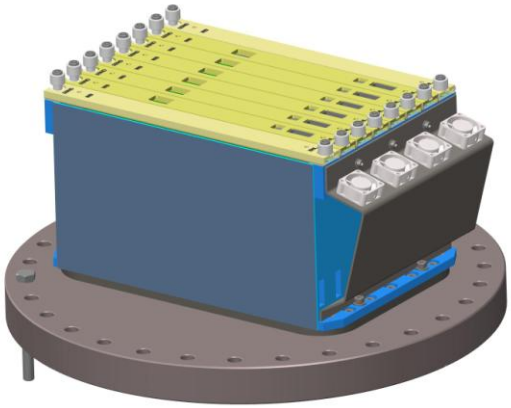
MBB (Magic Blue Box)



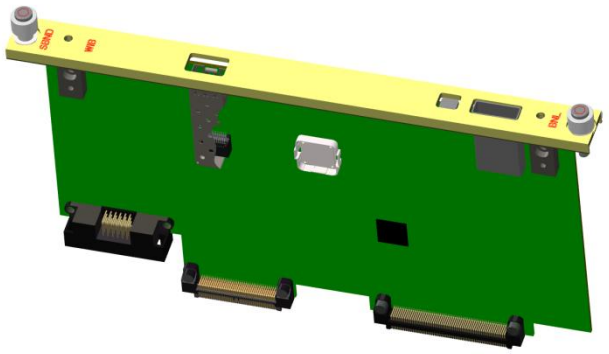
- Warm interface board electronics will be installed on top of the cryostat flange
  - Receive data from cold electronics through cold cables
  - Send data to Nevis electronics over fiber optical links
  - Interface to slow control system using fiber GIG-E
  - Manage power, timing and control to cold electronics
- Each Warm Electronics Crate (WEC) contains the following
  - Six Warm Interface Boards (WIB)
    - Each WIB will control up to four 128-ch FEMBs
  - One Power and Timing back plane (PTB)
  - One Power and Timing Card (PTC)
- WEC is a faraday cage with only optical signals going in and out other than the main power
- Total up to 3072 channels per WEC, SBND uses 2816 channels

SBND Warm Electronic Components

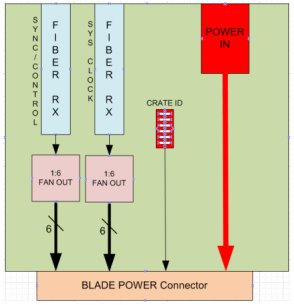




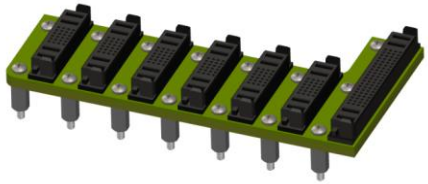
WEC



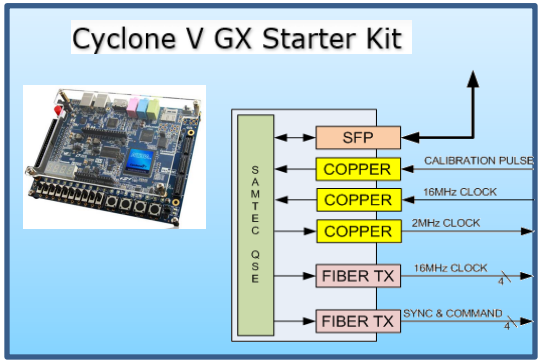
WIB



PTC

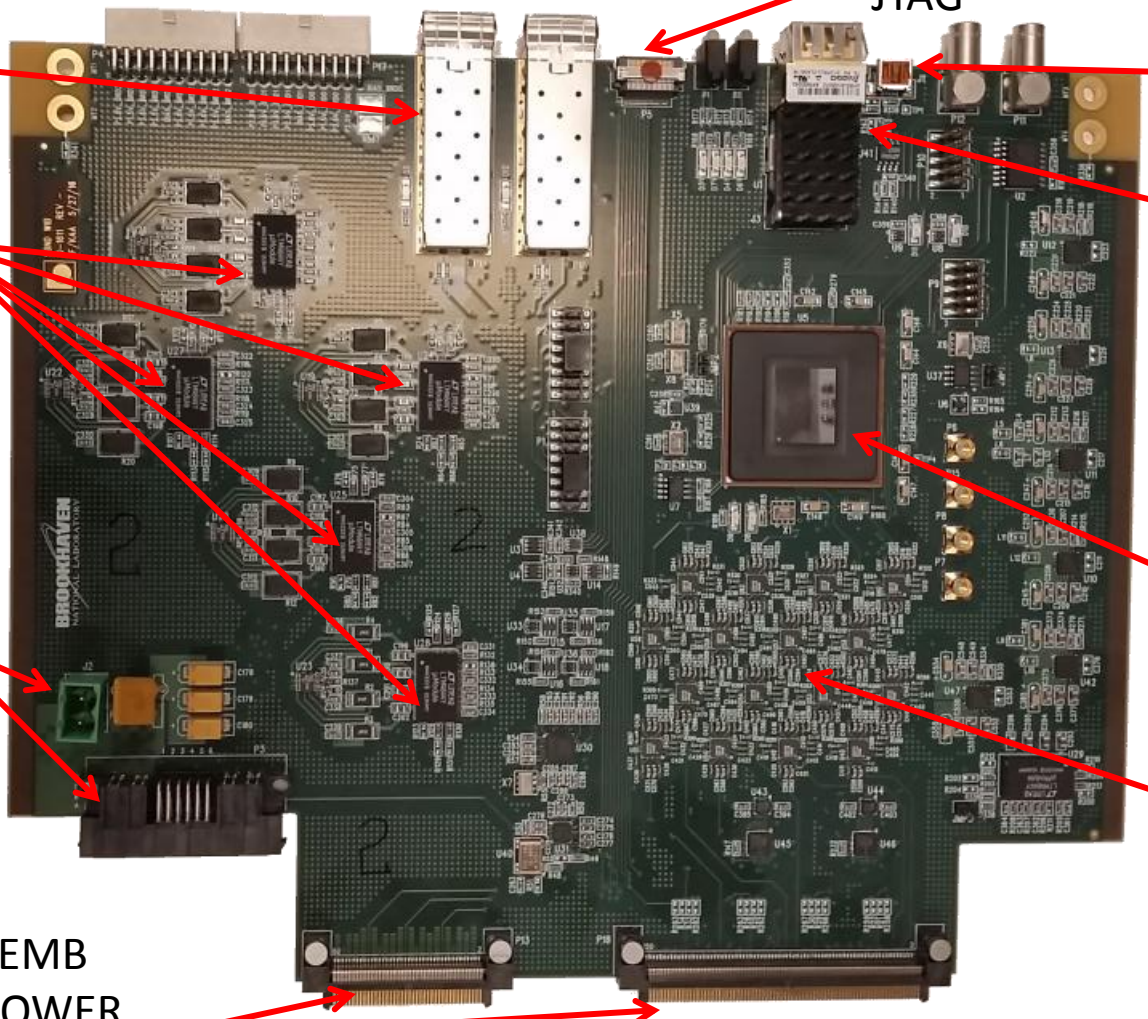


PTB

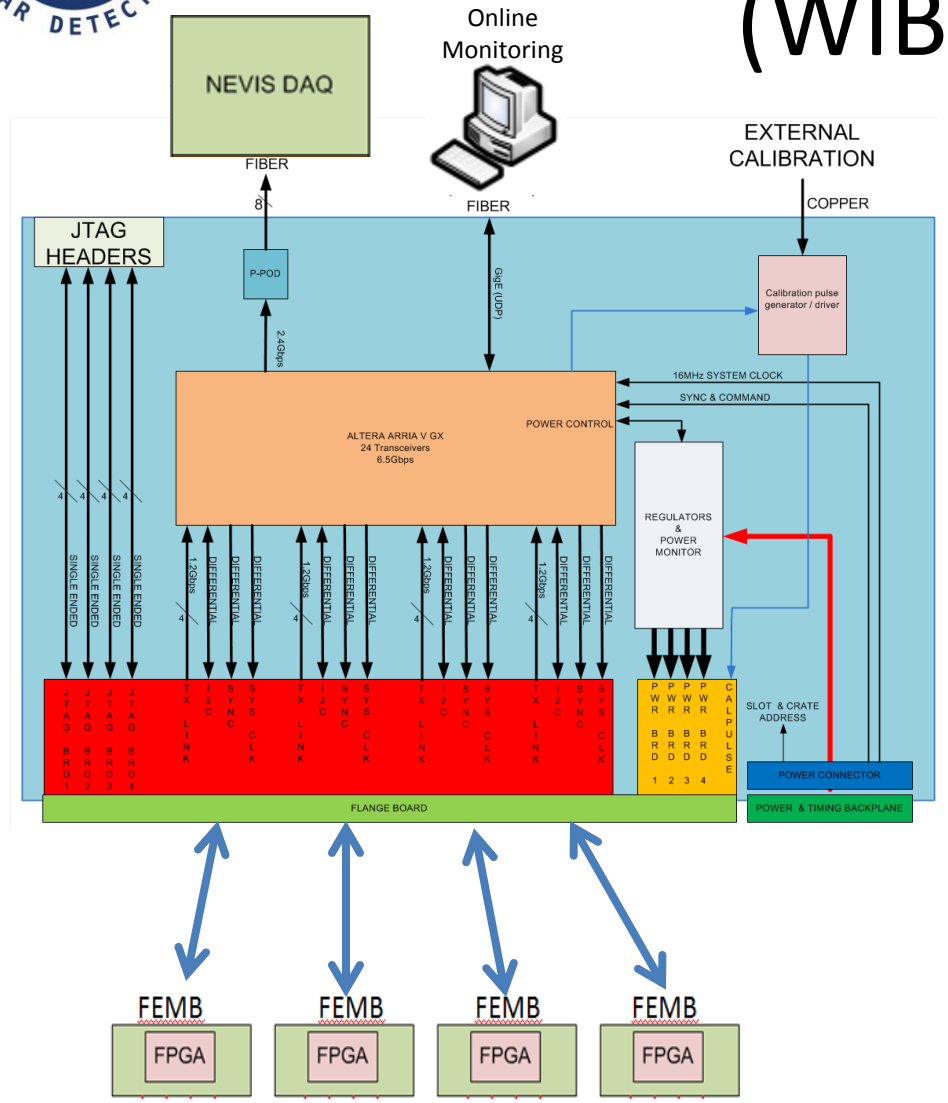


MBB

SBND WIB

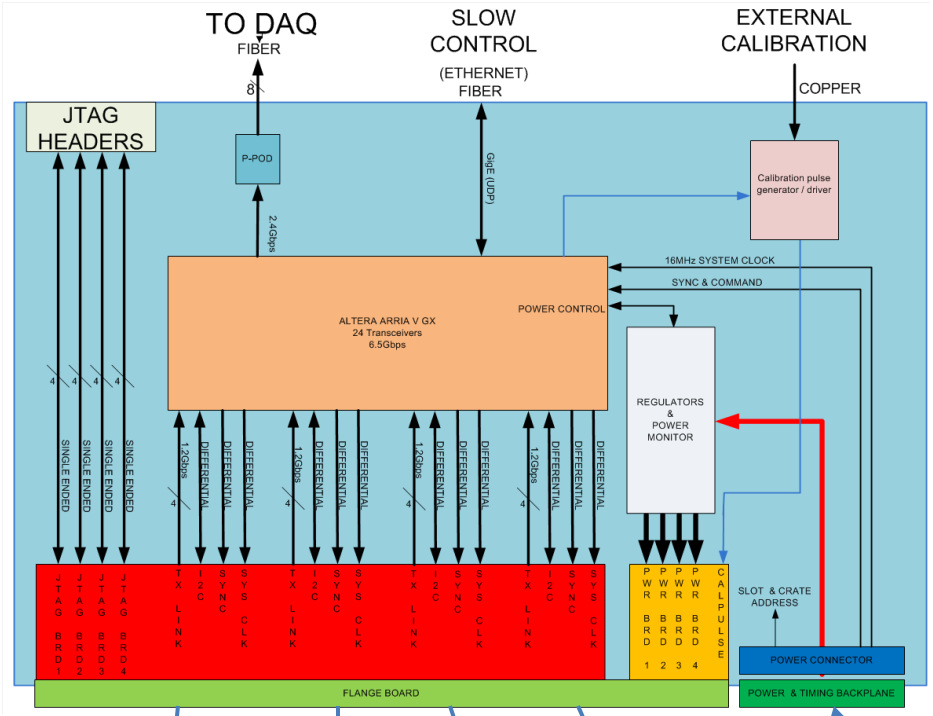

FEMB
JTAG
SFP
GigE
EXT
Calibration
FEMB
Quad
DC/DC
P-POD
12V
Input
Arria v
FPGA
Cable
Equalizers
FEMB
POWER
& DATA

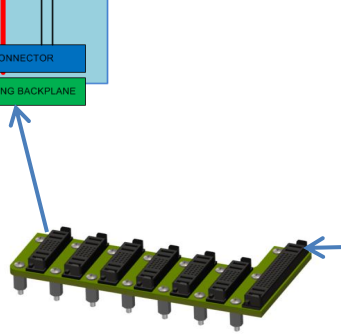
Warm Interface Electronics (WIB)

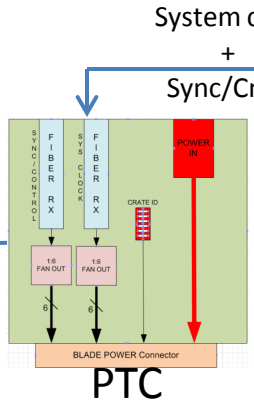


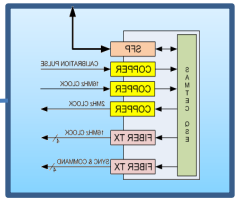
- Interfaces to 4 FEMBs, signals for each FEMB include
  - Four 1.28Gbps receiver links
  - I^2C link (Differential LVDS)
  - 16MHz system clock (Differential LVDS)
  - SYNC/CONTROL (Differential LVDS)
  - FPGA JTAG signals (single ended)
- Sends eight 2.125Gbps links to the Nevis DAQ electronics
- Communicates to online monitoring through a fiber Gigabit Ethernet link using UDP
  - IP address is generated by slot and crate address
- Each FEMB has can be controlled independently over Ethernet

Warm Interface Electronics (WIB)



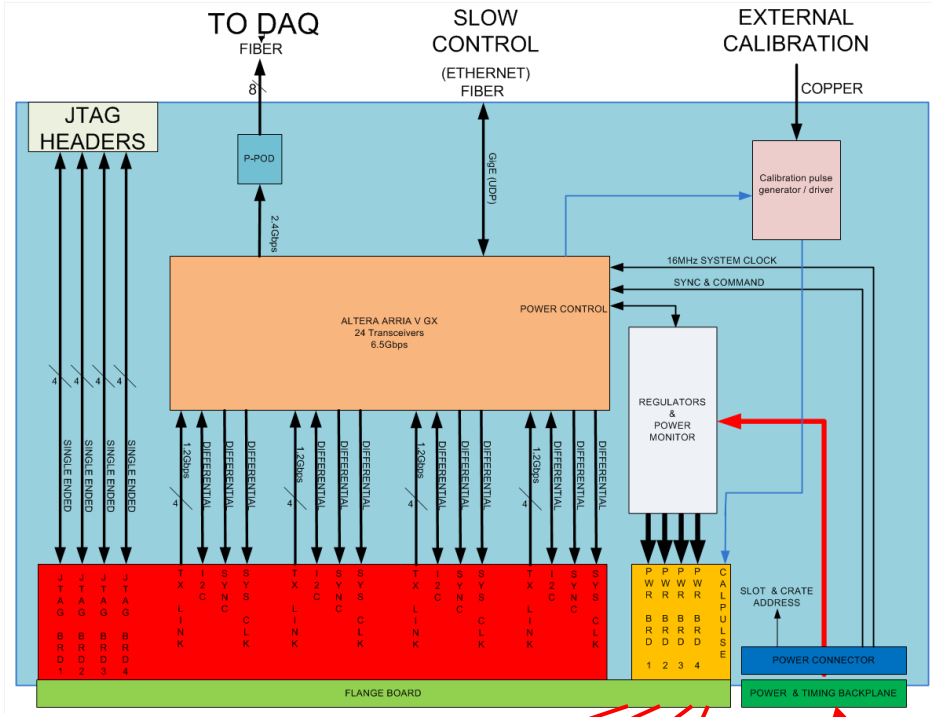


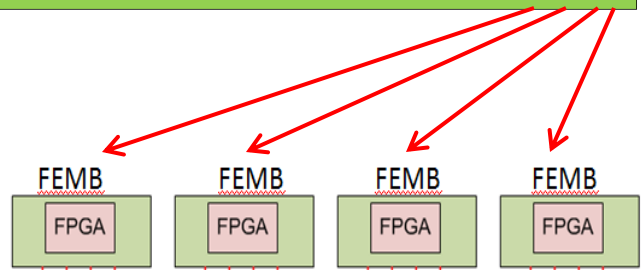


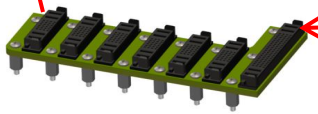


- Receive the system system clock + Sync/Cntrl from Magic Blue Box (MBB) system which will be distributed to the FEBs
  - The WIB can generate the system clock and sync/control internally for system testing
- Built in calibration pulse generator which can be triggered by the Sync/Cntrl link from the (MBB) or from online monitoring
  - External calibration can be accomplished by an input on the front panel of the WIB
  - **Calibration pulse distribution is for risk mitigation only**

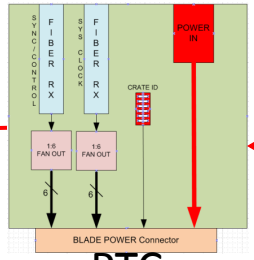
Warm Interface Electronics (WIB)





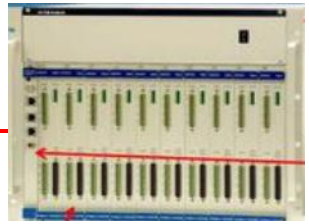


PTB



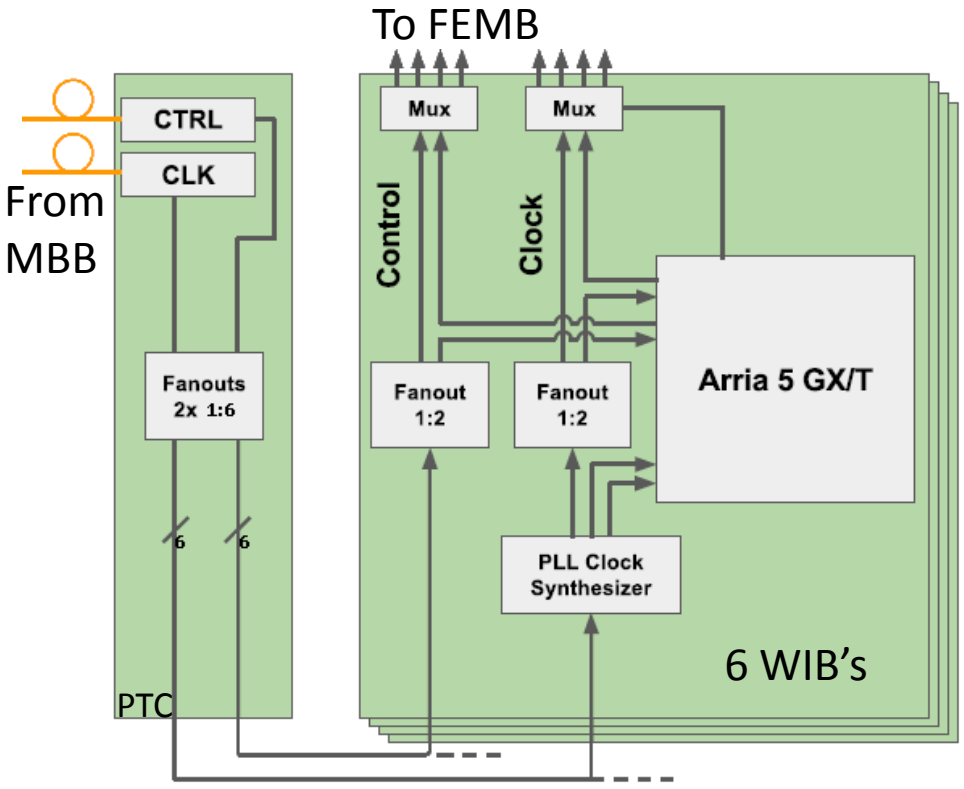
PTC

Wiener MPOD



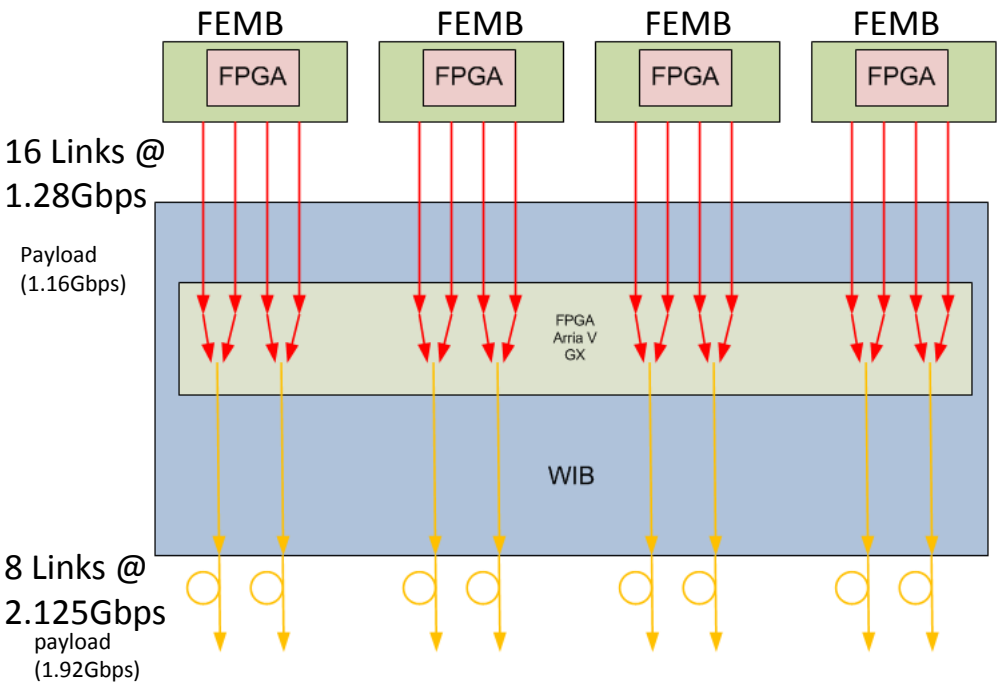
- Power is delivered through Power Timing backplane (PTB)
  - There are 5 DC/DC converters for each FEMB for a total of 20 per WIB
    - Each FEMB requires 1.5V, 2.5V 2.8V, 3.6V and 5V
  - Each DC/DC converter has voltage and current monitoring and can deliver up to 4A
  - Each DC/DC converter can be individually enabled or disabled through slow control
- Alternate power path available from front panel connector

SBND Warm Electronics Timing & Control



- Nevis -> MBB -> PTC->WIB
  - 16MHz system clock
  - Sync/Cntrl
- On WIB
  - System clock go through PLL synthesizer and generates 100MHz clock which is fanned out to the FEMB's and FPGA
  - Sync/Cntrol fanned out to FEMB's
  - Clock & Sync/Cntrl source selectable FPGA or external

SBND Data Path



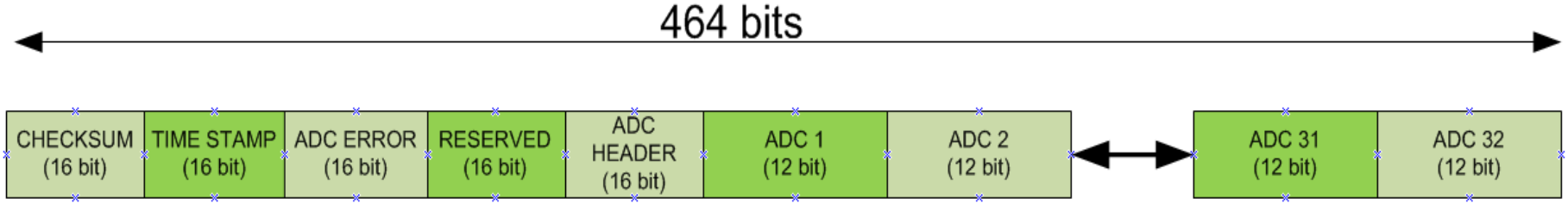
- FEMB
  - Four 1.28Gbps links
  - Payload per link 1.16Gbps
- WIB
  - Strip header from FEMB payload and multiplex 2 links into 1
  - Output link 2.125Gpbs
  - Payload per link 1.92Gbps

High Speed Signal Details

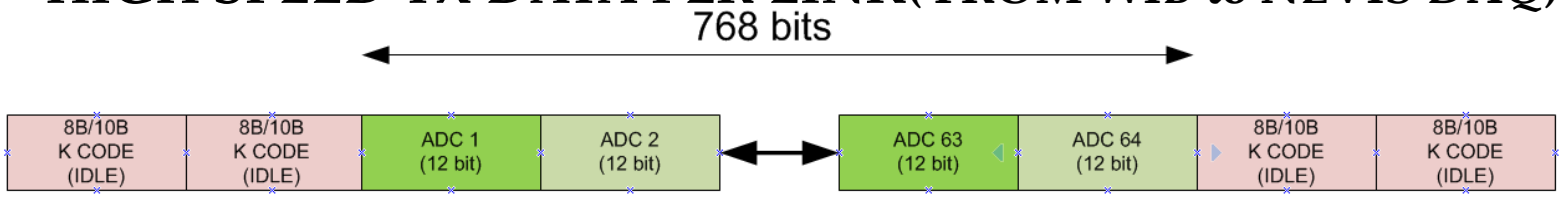
HIGH SPEED WIB RX DATA (FROM COLD FPGA TO WIB)

(16bit (Checksum) + (16bit (Timestamp) + 16bit (ADC ERROR) + 16bit (Reserved) + 16bit (ADC Header) + (12bit(ADC) * 32 (Channels)) * 2MHz * 1.25 (8B/10B encoding) = 1.16Gbps

Link Speed = 1.28Gbps



HIGH SPEED TX DATA PER LINK(FROM WIB to NEVIS DAQ)



(12bit(ADC) * 64 (Channels)) * 2MHz * 1.25 (8B/10B encoding) = 1.92Gbps

Link Speed = 2.125Gbps

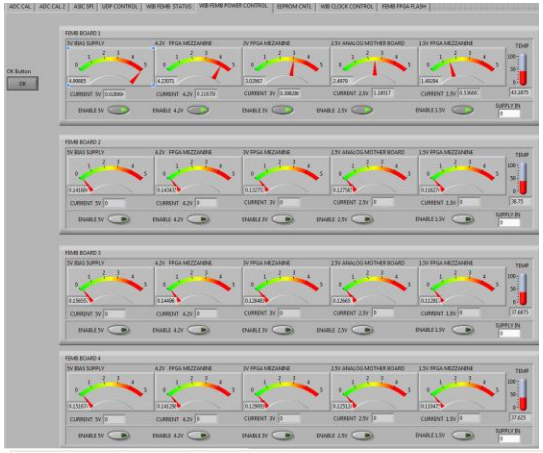
TOTAL DATA RATE

WIB = 8(Links) * 1.92Gbps = **15.36Gbps** WEC = 6(WIBs) * 15.36Gbps = **92.16Gbps**

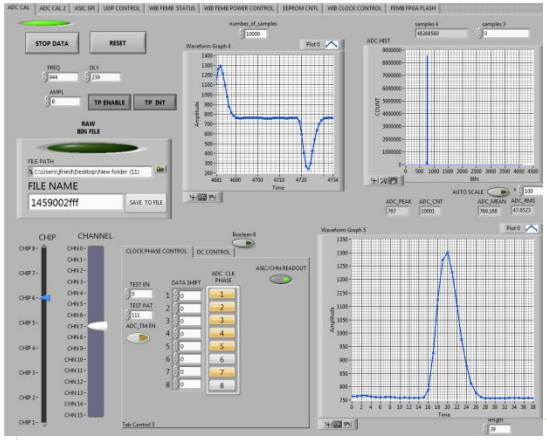
Warm Interface Board (WIB)

Online Monitoring / Debugging Features

- Monitor and control FEMB voltages and currents
  - Can set alert triggers to be sent to online monitoring
- Can monitor FEMB ASIC data sent over high speed link
  - Can set alert triggers to be sent to online monitoring (Such as ADC thersholds)
- Read and write FEMB registers
  - WIB works as a UDP to I2C translator
- Program and verify FEMB FPGA flash memory
- Store default settings on on-board flash device
- Can select to use on-board or system clock
- Can generate internal or external calibration pulse
- Peek at high speed data link in real time over slow control
  - Can monitor one ASICs worth of data (16 channels)
- Can generate high speed test data sent to DAQ
  - PRBS test pattern
  - Counter
  - Channel , Crate , Slot address encoded to aid in mapping
- **Utilize all engineering development tools used at BNL**
  - Can plug a laptop containing BNL tools into the Ethernet switch or directly into a WIB
  - Can be used simultaneously with DAQ system
  - Will simplify debugging of entire system



Power Monitor & Control

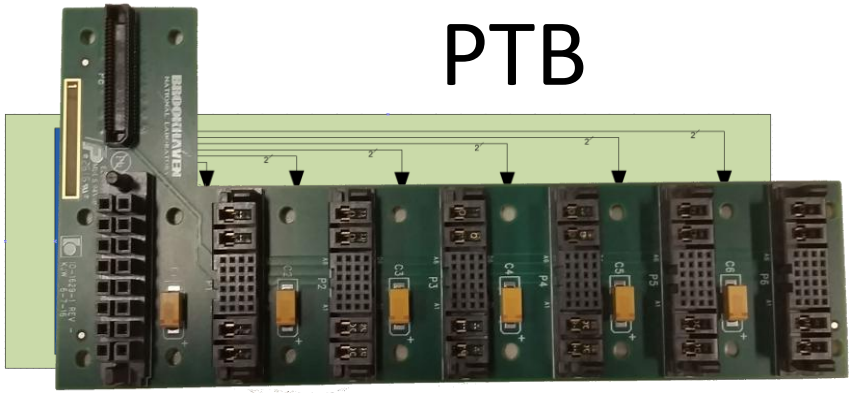


Real-time channel data

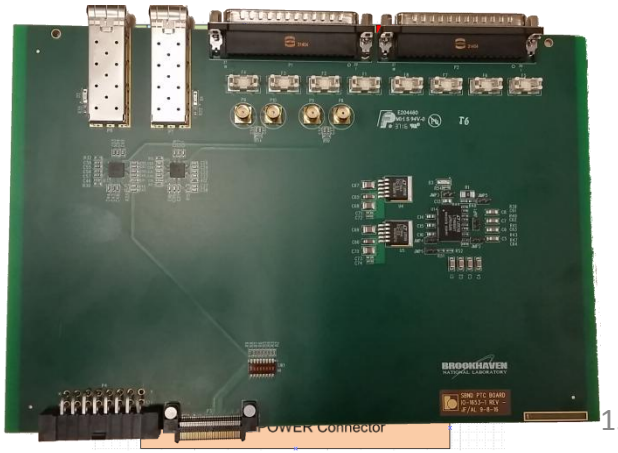
Power & Timing Backplane (PTB)
Power & Timing Card (PTC)

- PTB distributes system clock and Sync/Cntrl signals to each WIB
  - Each signal is a point to point connection and is individually terminated on the WIB
- PTB each slot has a unique slot address
  - Used to generate GIG-E IP address on WIB
- PTC dip switch allows for selection of crate address which is bused to each WIB
- PTC two fiber optic receivers used for 16MHz system clock and Sync/Cntrl signals from MBB
  - The PTC fansout the received signals through a 1:6 clock driver delivering point to point signals to each WIB

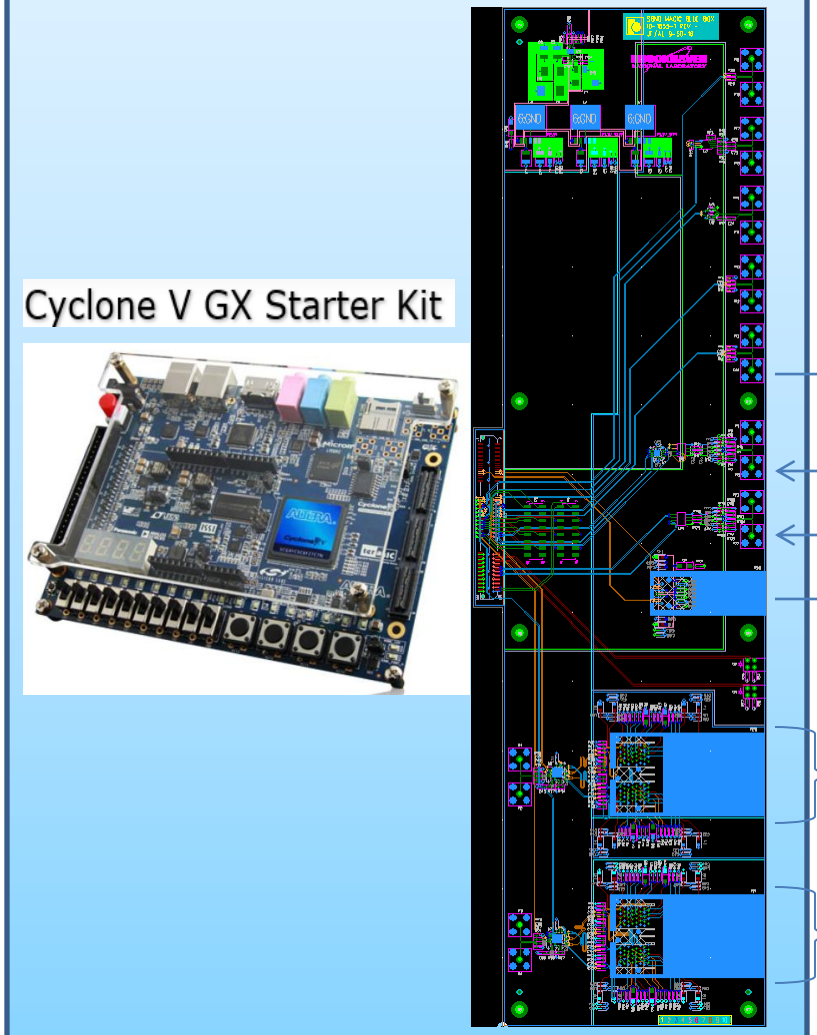
PTB



PTC



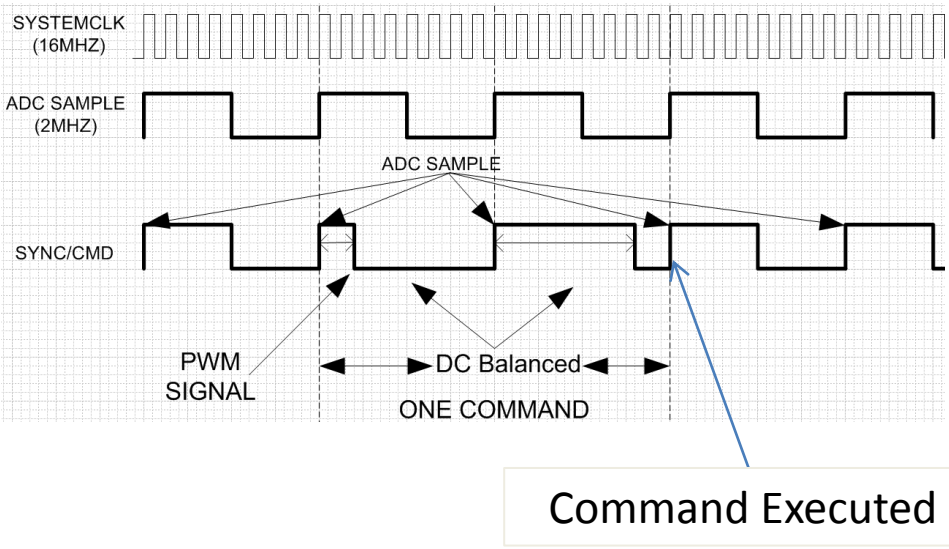
Magic Blue Box (MBB)



- MBB Electronics
  - MBB Design utilizes an Altera Cyclone V evaluation board
    - Simplified MBB design
  - Connections to the Nevis DAQ
    - 16MHz system clock from Nevis DAQ (copper)
    - 2MHz ADC sampling clock goes to Nevis DAQ (copper)
    - Calibration signal from Nevis DAQ synced to the 2MHz clock (copper)
    - 5 Spare copper input signals
    - 5 Spare copper output signals
  - Connections to the Warm Electronics Crate (WEC)
    - Four 16MHz system clocks one to each WEC (fiber)
    - Four Sync/Cntrl signals one to each WEC (fiber)
  - Slow control
    - One SFP module GIG-E which goes to online monitoring

Magic Blue Box (MBB)

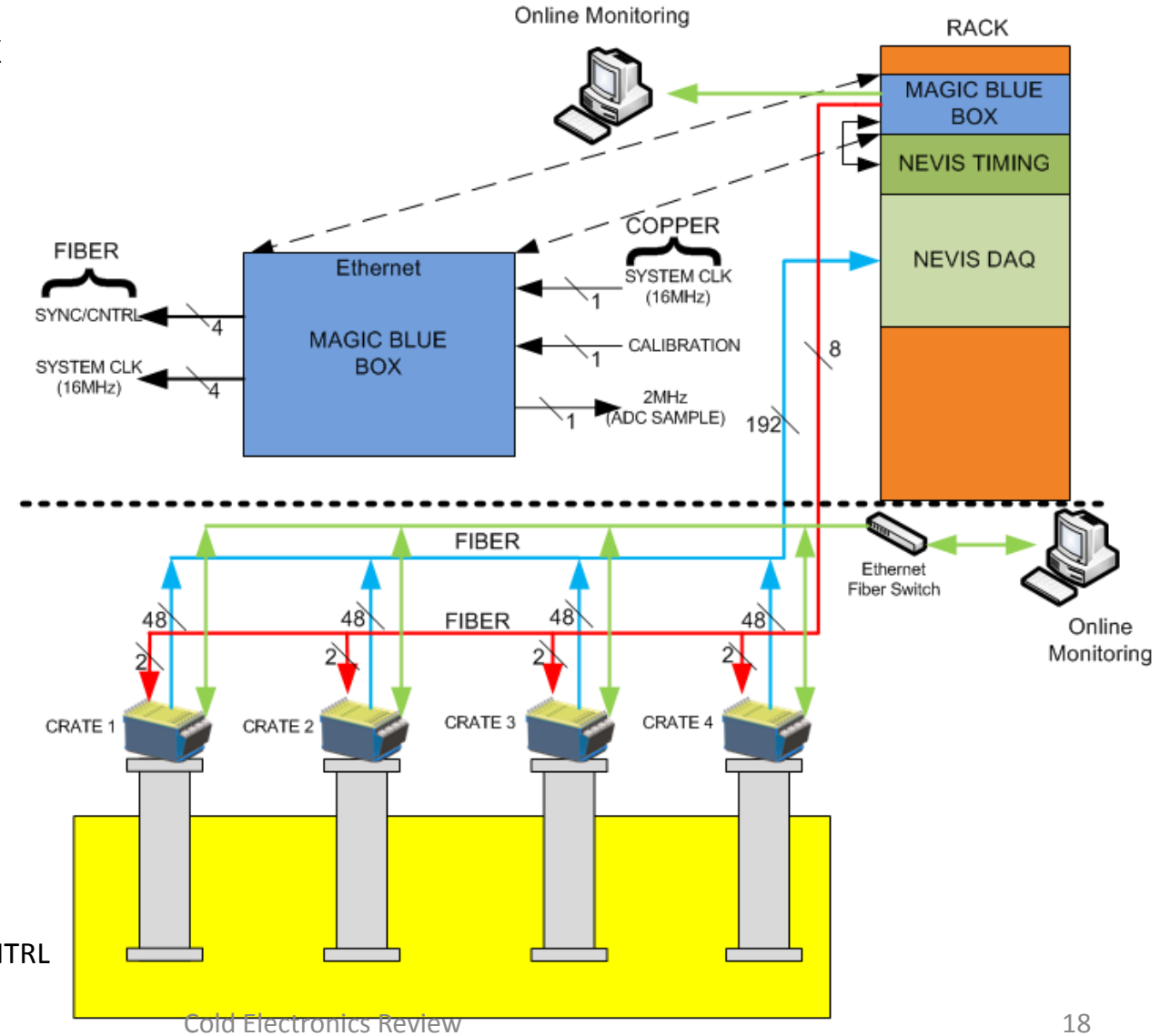
- MBB Features
  - Gigabit Ethernet communication to DAQ for SBND system control
  - Distributes 16MHz system clock to each WEC
  - Generates 2MHz ADC sampling clock from 16MHz system clock
    - Sent to NEVIS DAQ
  - Sends Sync/Cntrl signal to each WEC
    - 2MHz Clock
    - DC balanced pulse width modulated signal to encode synchronous commands
    - can encode up to seven synchronous commands



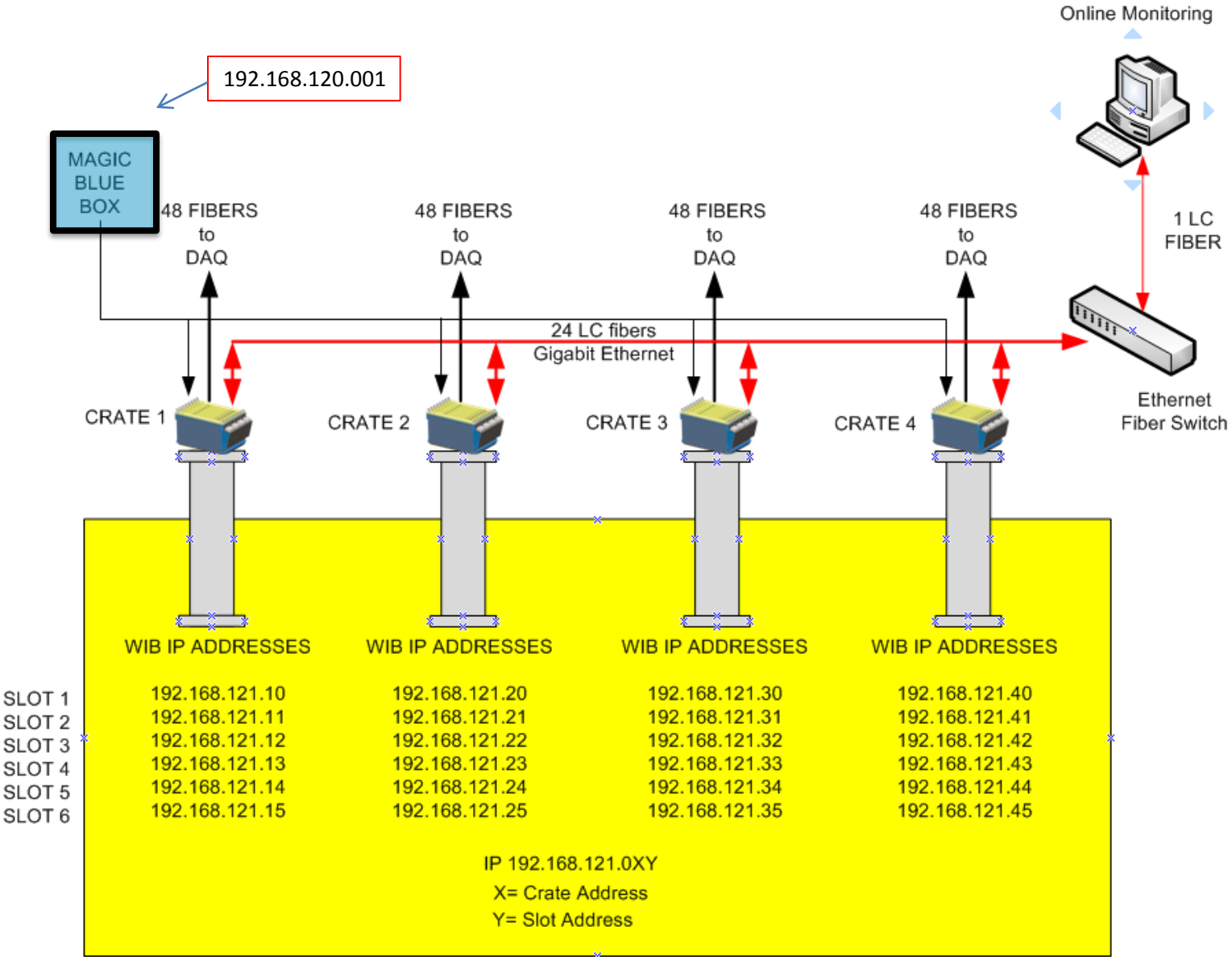
- **System synchronous commands**
  - Calibration pulse
  - Time stamp reset
  - System rest
  - System enable/disable
  - -----TBD-----

SBND TPC Data , Clock & Calibration Signals

- DAQ
  - WIB -> Nevis DAQ RACK
    - 192 Fibers
- System Clock
  - Nevis timing to MBB
    - Copper
  - MBB (DAQ RACK) -> PTC
    - Four Fibers
- Sync/Cntrl
  - MBB (DAQ RACK) -> PTC
    - Four fibers
- Ethernet
  - To online monitoring
  - Six per WEC 24 total
    - WIB <-> switch
    - Fiber
  - One MBB
    - Fiber or copper
- Calibration
  - Nevis timing to MBB
    - Copper
  - MBB (DAQ RACK) -> PTC
    - Encoded on SYNC/CNTRL



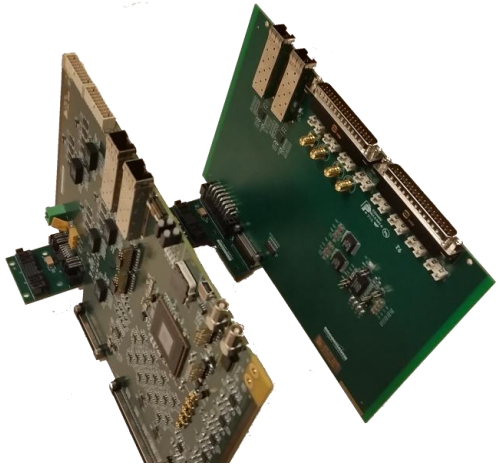
SBND WIB Address Map

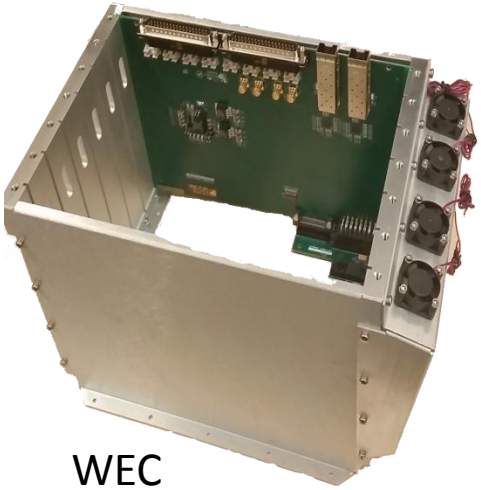


ETHERNET PACKET FORMATION (UDP)

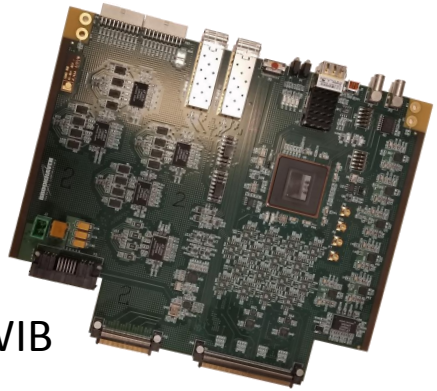
- DEVICE IP 192.168.1XX.0YY (192.168.121.1) = FEMB
  - XX = Crate ID
  - YY = WIB Slot ID
- DEVICE MAC: AABBCCDDXXYY (AABBCCDDEE00) = FEMB
  - XX = Crate ID
  - YY = PTB Slot ID
- SYSTEM KEY = 0xDEADBEEF
- **WIB ETHERNET PORTS**
  - 32000 write port -- Used to write registers
  - 32001 read request port -- Used to read registers
  - 32002 response port -- Used in respond to a read request
  - 32003 high speed data port -- Used to receive alert & high speed data
- **FEMB COMUNNICATION Z = FEMB 1-4**
  - 32Z00 write port -- Used to write registers
  - 32Z01 read request port -- Used to read registers
  - 32Z02 response port -- Used in respond to a read request

SBND Warm Electronic Components

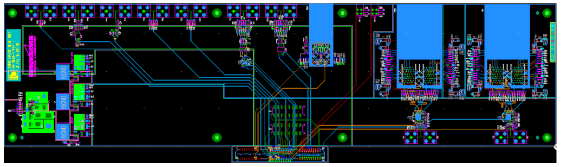




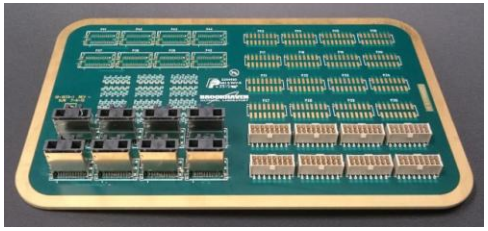
WEC



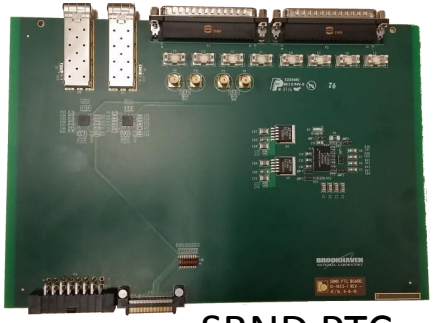
WIB



MBB



SBND FLANGE (prototype)



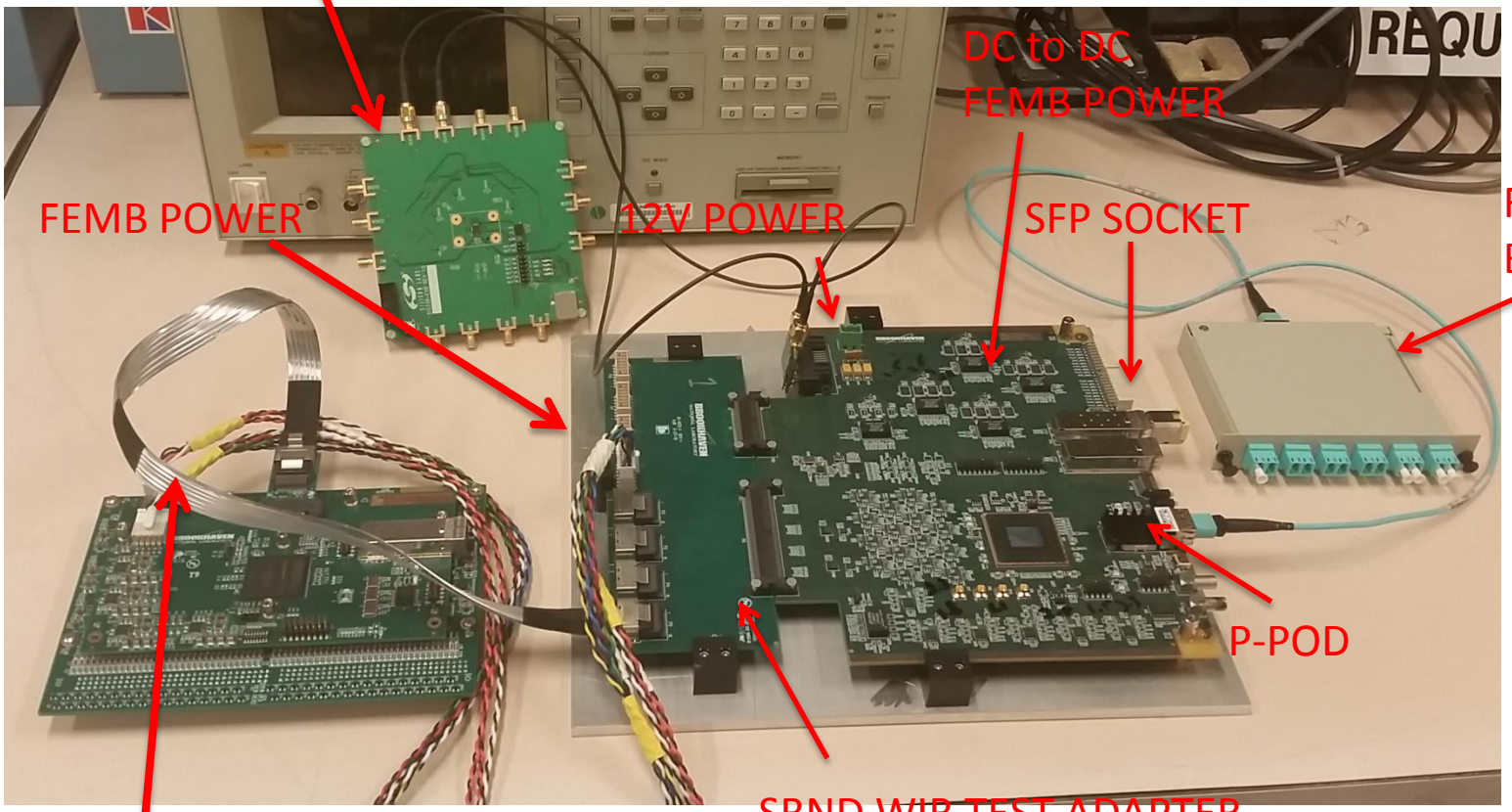
SBND PTC

PTB

BNL-Nevis Integration Test

- BNL & Nevis had an integration test at Nevis Labs on September 22
  - Goal
    - Test optical link between BNL's Warm Interface Board (WIB) and Nevis's Front End Module (FEM).

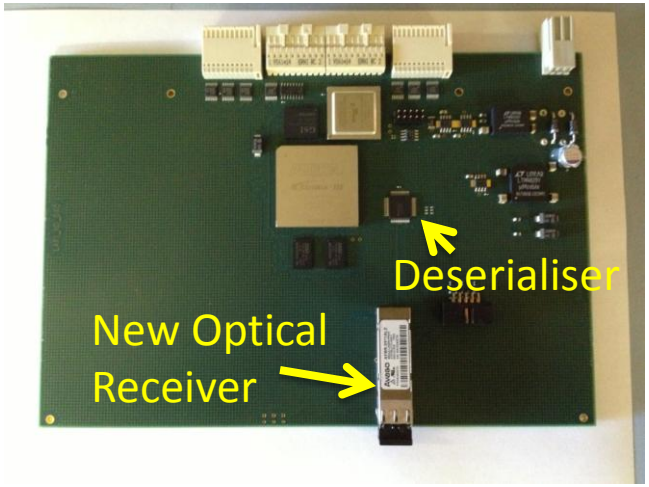
BNL-Nevis Integration Test
BNL Hardware



BNL-Nevis Integration Test Nevis Hardware

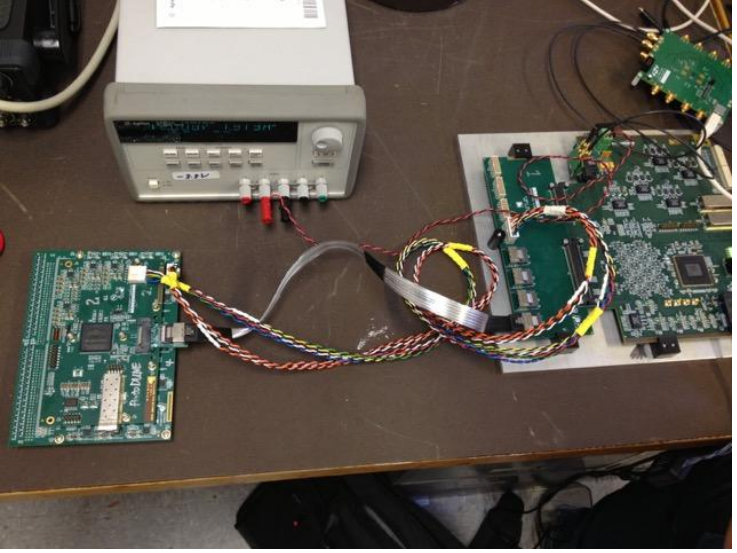
XMIT transmitter module.

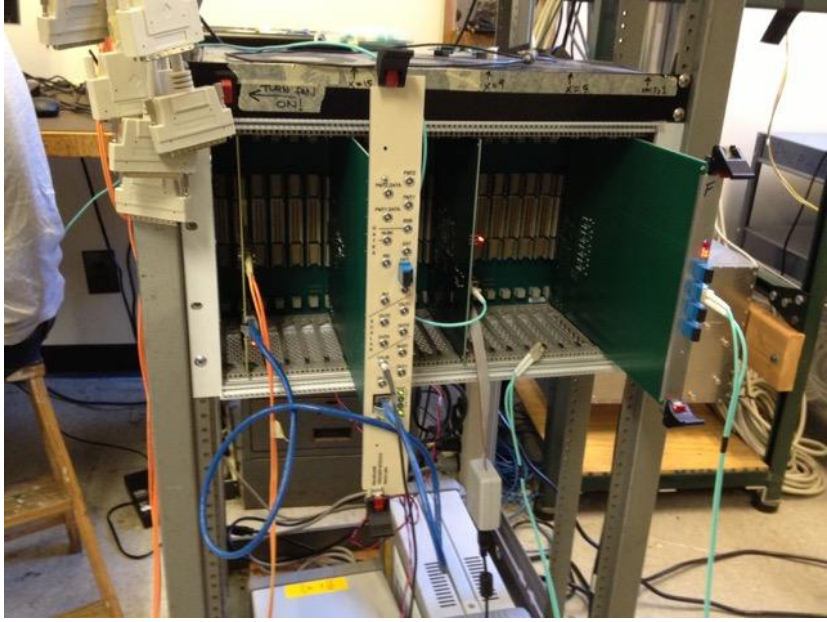
Front End Module



Crate Controller.

Setup





FEMB ASIC's

WIB

Optical

Copper

BNL

Magic Blue Box (MBB) not available. Used SiLabs SI5338 eval board to emulate MBB + PTC. Fed (16 MHz) directly to WIB

Clock

Nevis

Crate

Controller

Trigger

FEM

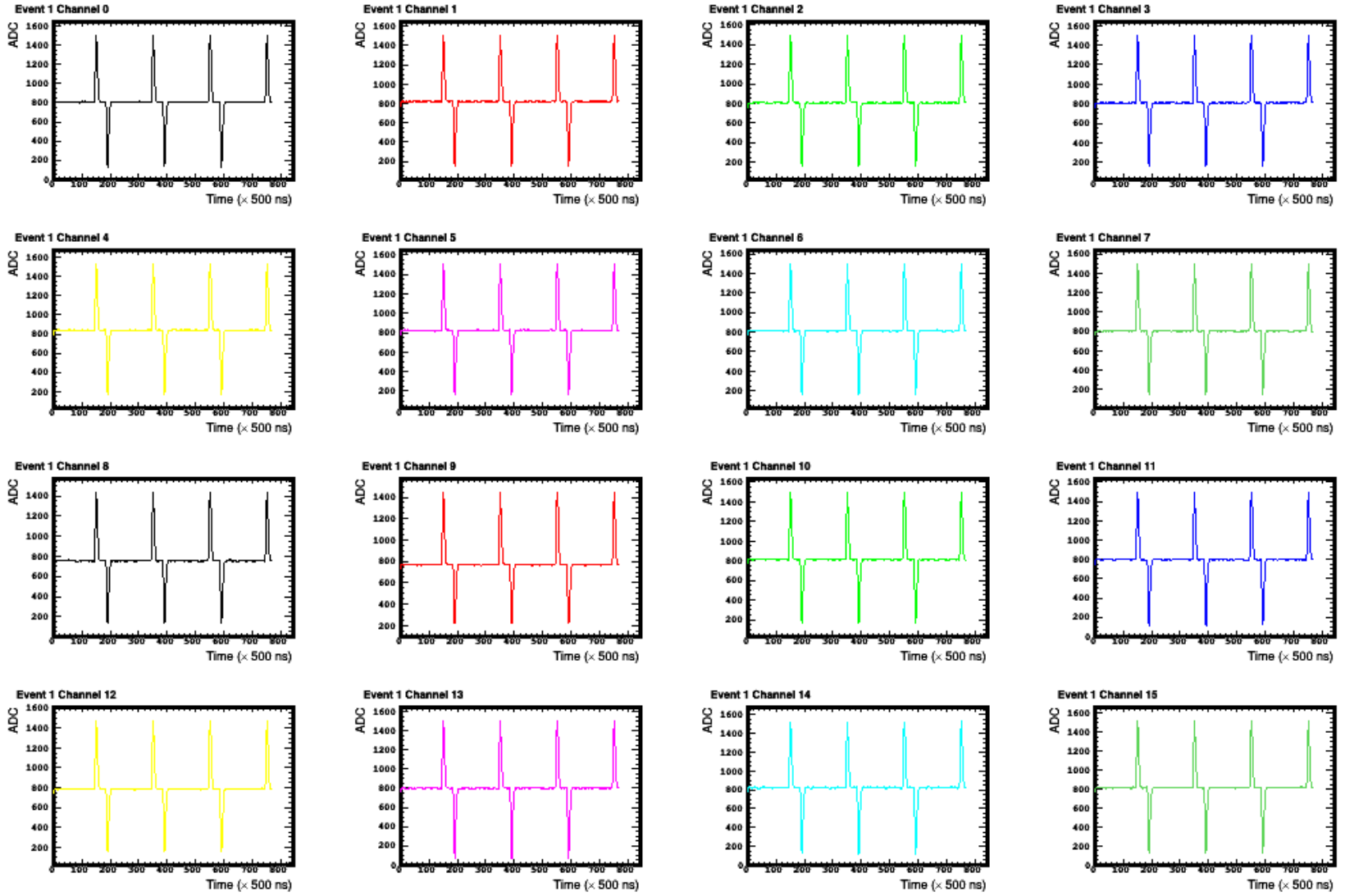
Slow readout through controller (no XMIT used)

PCIe card

DAQ PC

Trigger sent only to controller: Asynchronous readout of WIB

Calibration pulse generated in BNL's ASIC chip 1 (16 channels) read out by Nevis FEM



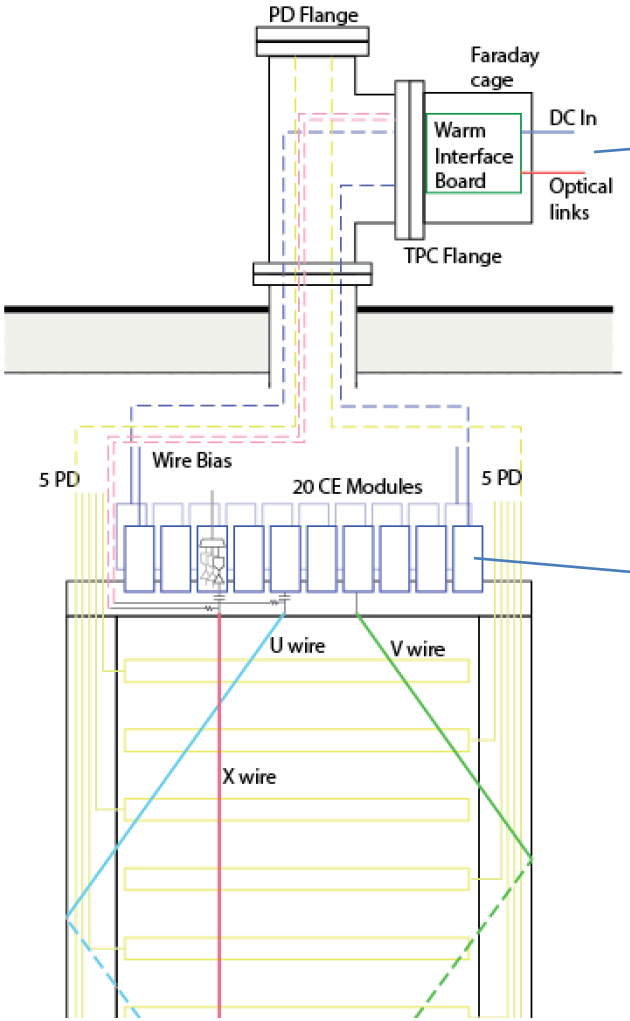
Success!

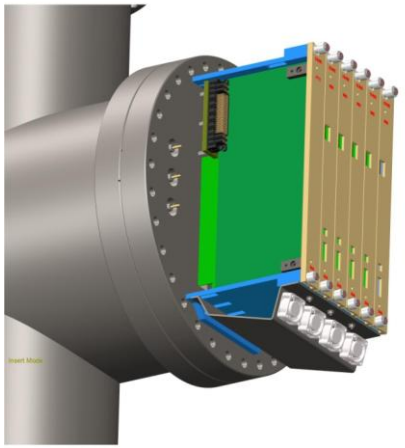
Summary

- The development of SBND warm electronics is making good progress
  - WIB Prototype testing is underway
  - MBB is out for fabrication
  - SBND & ProtoDUNE Flange is out for fabrication
- BNL<->Nevis Integration test
  - September integration test completed successfully but without MBB & PTC
  - November integration test planed to include MBB & PTC

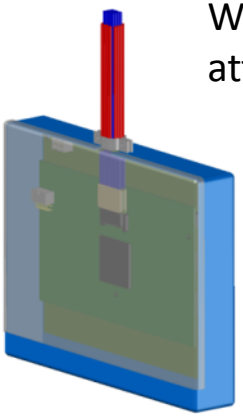
BACK UP

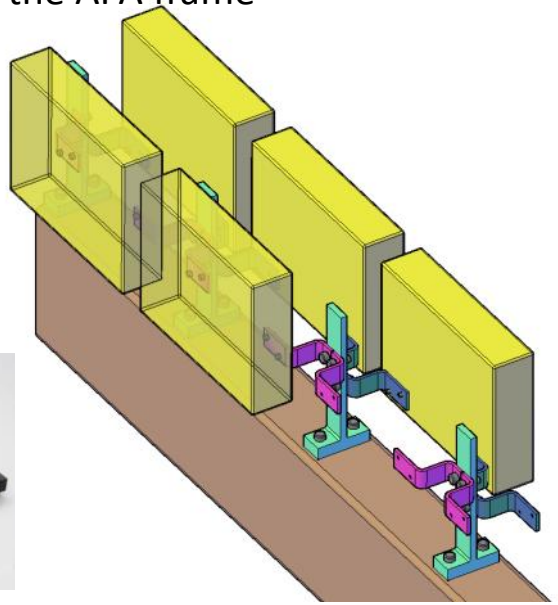
APA with Integrated Warm Electronics





Warm electronics module and its attachment to the APA frame

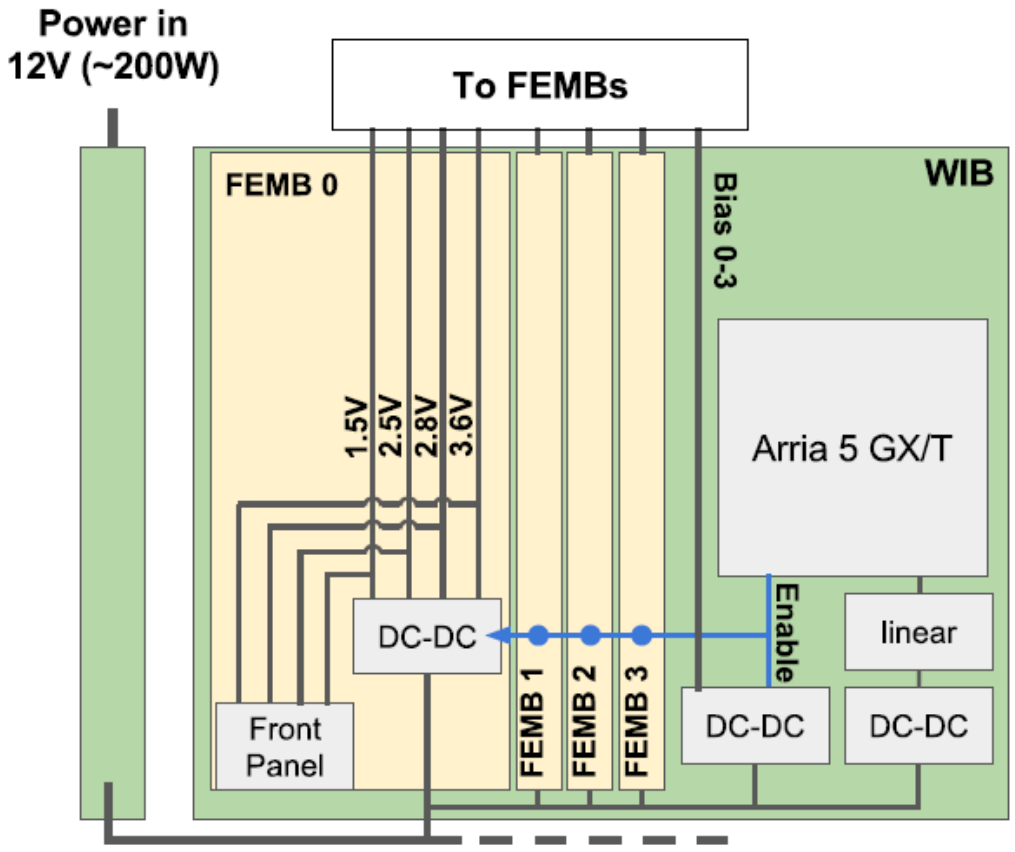




SBND WIB MODIFICATIONS/FIXES

- Replace poly fuse “F1” with 5A fuse holder “0031.7701.11”
- Replace 5V FEMB bias “U28” DC to DC with lower power solution
- Add cable drivers / receiver to lemos on front panel
- Use TPS3847 voltage monitor for WIB local DC to DC ”U29” to fix startup issues
- Add I2C level shifter “TCA9406” to ALL LT2991 power monitors “U19-U23”
- Front panel power inputs should go through sense resistors for power monitoring
- Remove AC coupling from U31 “C272-C277”
- Modifiy ERF8 connector “P18” to allow for unidirectional LVDS
  - JTAG signals rearranged to allow for an extra differential pair
- Add 12V power input at front panel (if there is room)
- Replace SI5338 PLL “U31” with SI5345 PLL
  - Fix clock termination “R53” wrong side of AC coupling
- Added voltage monitoring feature for WIB local power
  - Two LT2991 added
- Add mounting holes. (for bench testing)

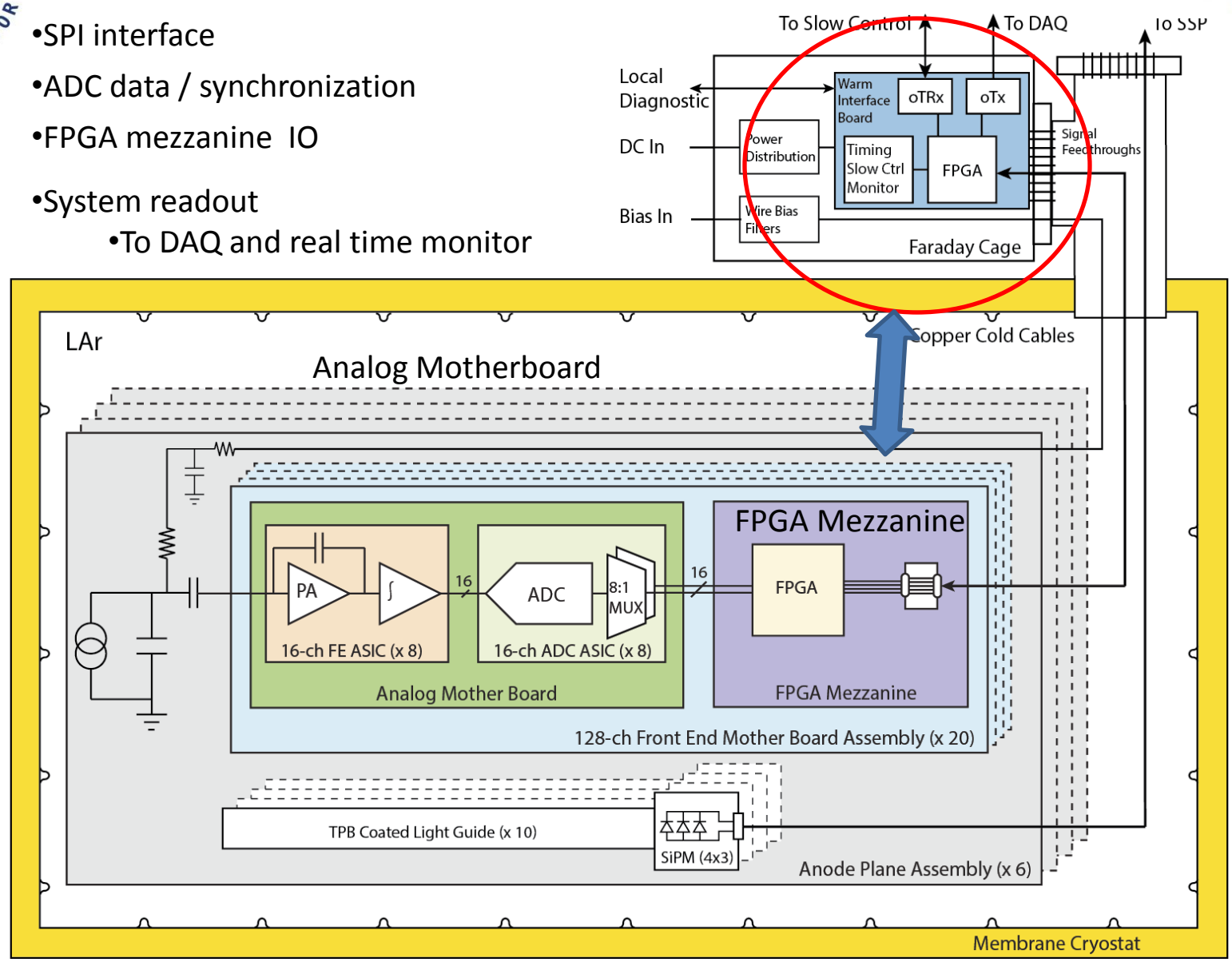
WIB Power



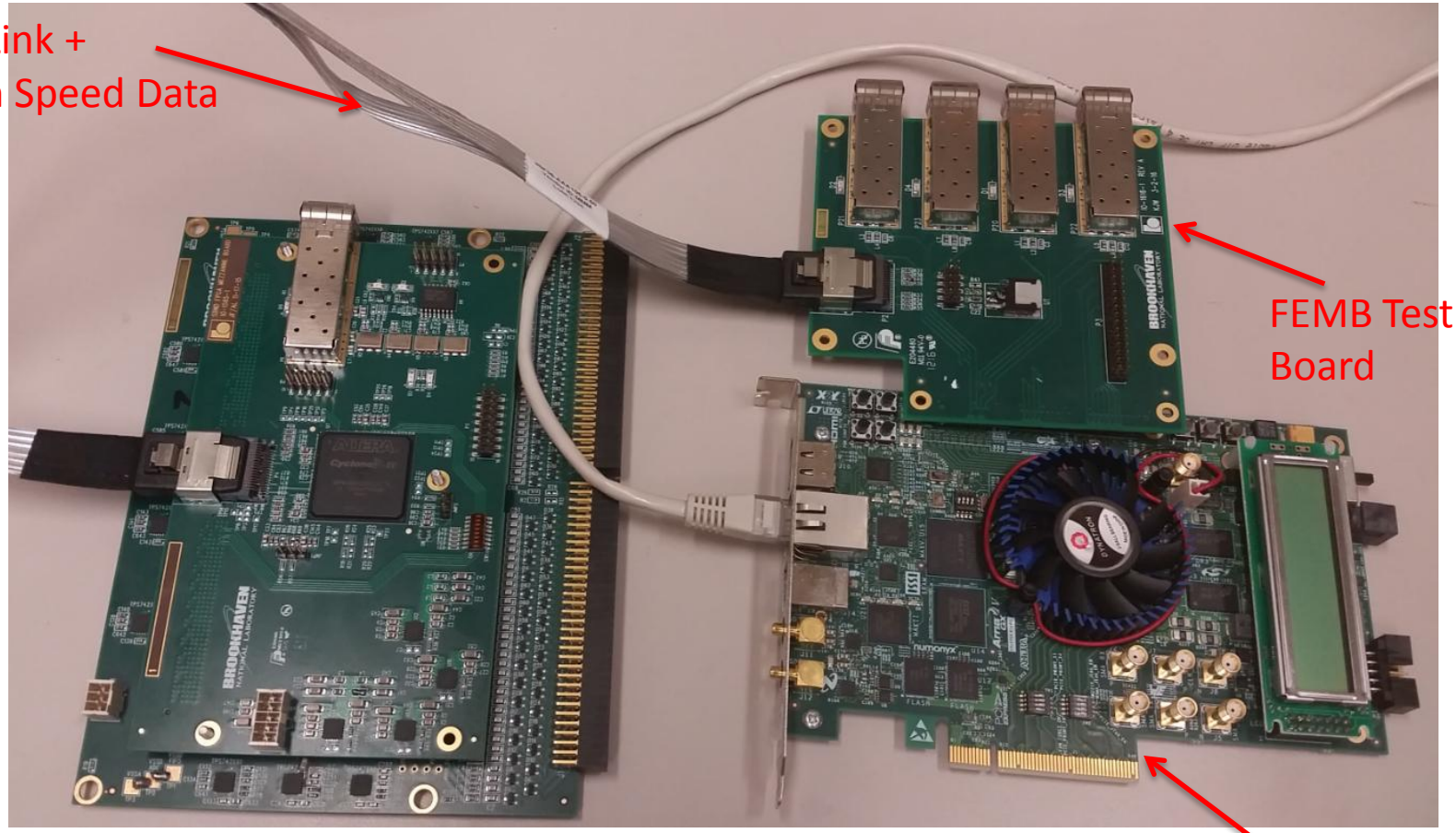
- Power for cold:
  - Each FEMB requires 1.5V, 2.5V, 2.8V, 3.6V and bias
  - Primary power path:
    - External 12V distributed through PTC, backplane
    - Each WIB uses LTM4644 quad DC/DC converters to generate required voltages
  - Alternate power path:
    - Front panel connector receives regulated cold power directly

old Electronics Communicati

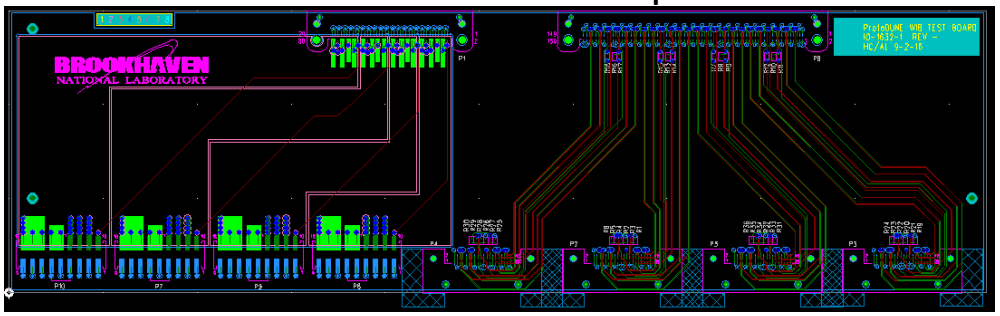
- SPI interface
- ADC data / synchronization
- FPGA mezzanine IO
- System readout
  - To DAQ and real time monitor



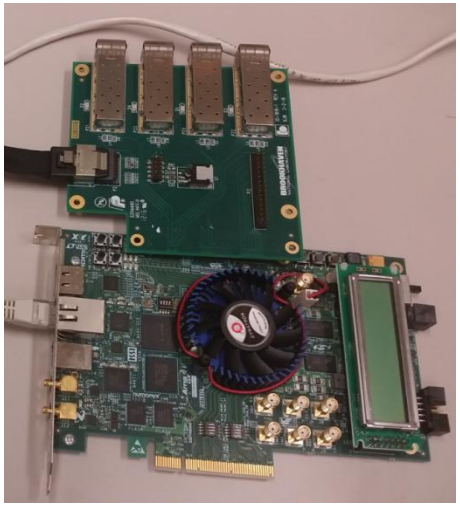
WIB Emulator + FEMB



ProtoDUNE WIB Adapter



SBND WIB Emulator



ProtoDUNE WIB Emulator