BNL Test Stands for Cold Electronics Development

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Outline

- Introduction
- Test stands for SBND and ProtoDUNE-SP
  - FEMB TEST STAND
  - FE ASIC TEST STAND
  - FE ADC TEST STAND
  - INTEGRATION TEST STAND
- Summary

Introduction

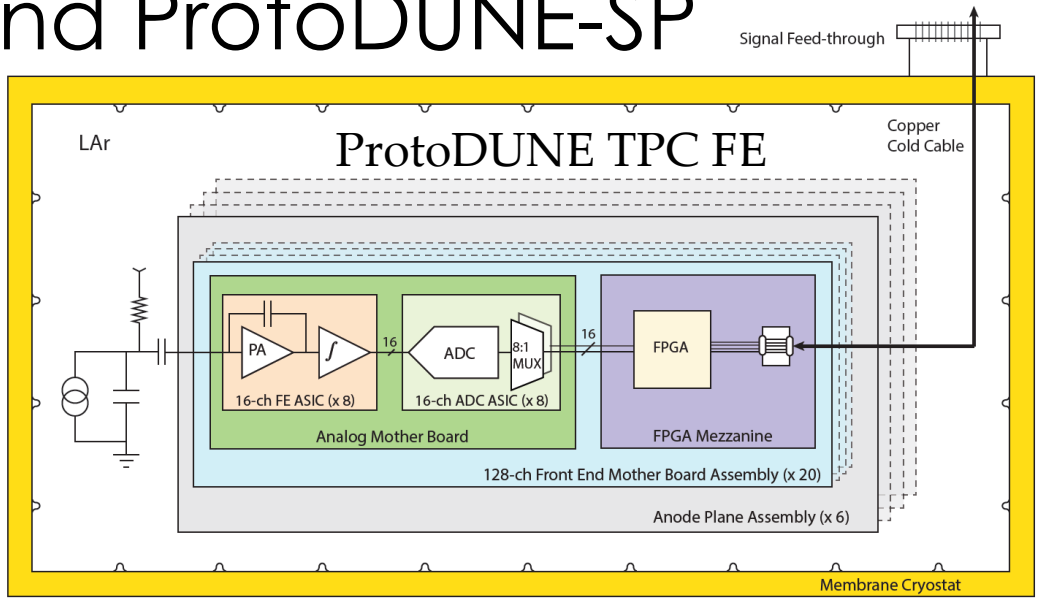
- Cold electronics is an ***enabling*** technology for noble liquid detectors for neutrino experiments
  - It decouples the electrode and cryostat design from the readout design, to achieve **better SNR** independent of the fiducial volume
  - Signal multiplexing results in large reduction in the quantity of cables and the number of feed-throughs, eases the scaling up to 10kton detector
- Test stand of cold electronics is crucial to the characterization of electronics performance
  - Development of various test stands are necessary before the final installation of the cold electronics on detector
  - Integration test (as planned at BNL, Fermilab and CERN) and QA/QC test serve as importance steps to ensure the success of experiments

Test Stands for SBND and ProtoDUNE-SP

- FEMB TEST STAND
  - Introduction of FEMB
  - Overview of FEMB test stand
  - Calibration and ENC calculation
  - List of tests done on FEMB test stand
- FE ASIC TEST STAND
- FE ADC TEST STAND
- INTEGRATION TEST STAND

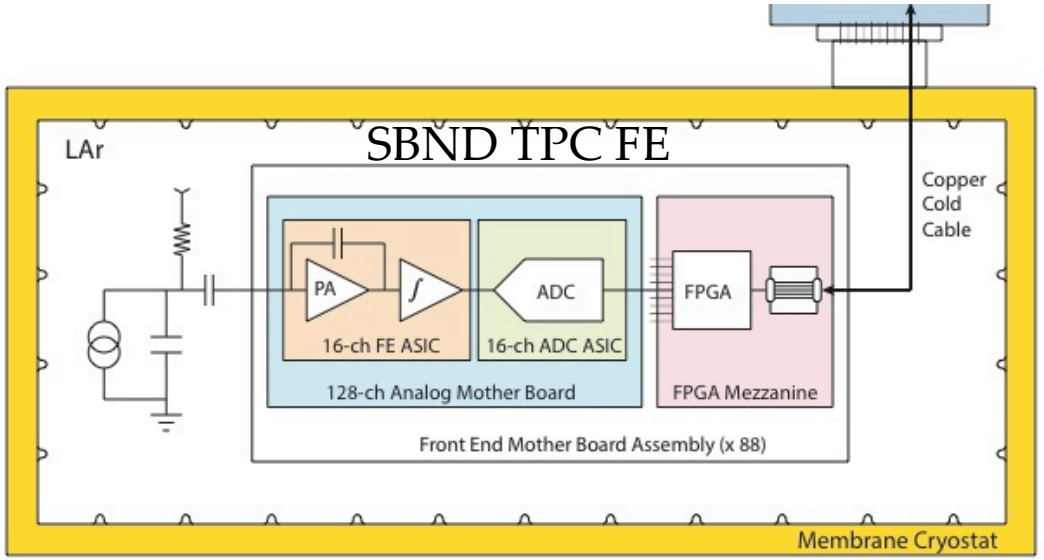
FEMB for SBND and ProtoDUNE-SP

- ProtoDUNE TPC FE
  - 6 APAs
  - 120 FEMBs
  - 128-ch per FEMB
  - Connector: Samtec HSEC8
  - Samtec twinax cable (7m)



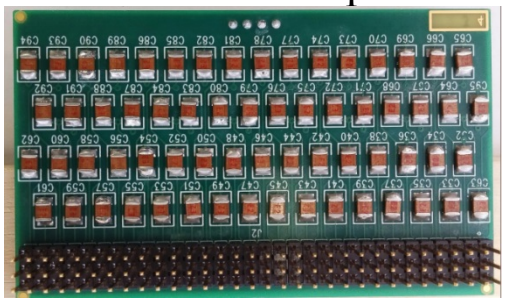
Difference: Connectors and cables to WIB

- SBND TPC FE
  - 4 APAs
  - 88 FEMBs
  - 128-ch per FEMB
  - Connector: Molex 75783-0132
  - 3M miniSAS cable (7m)

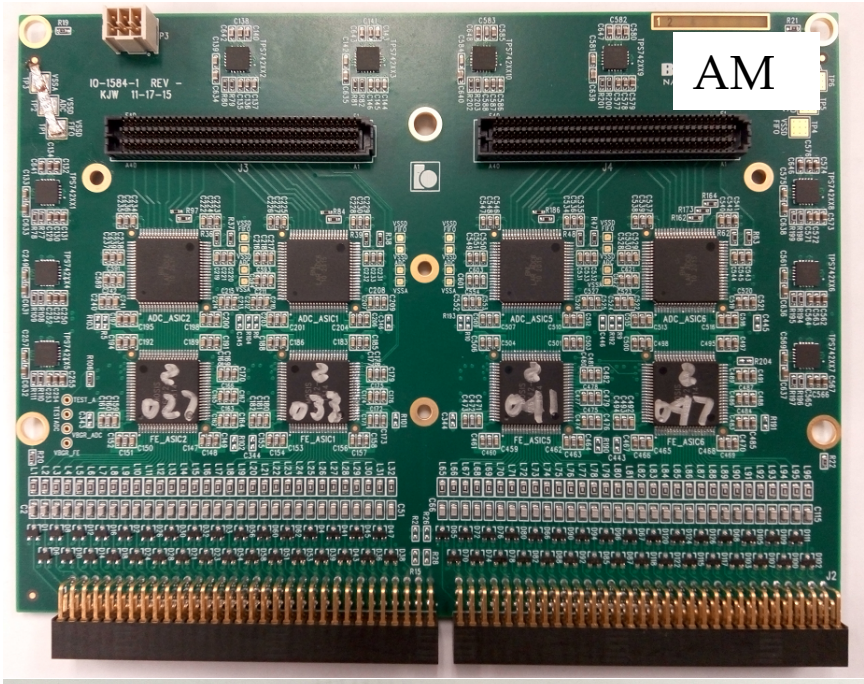


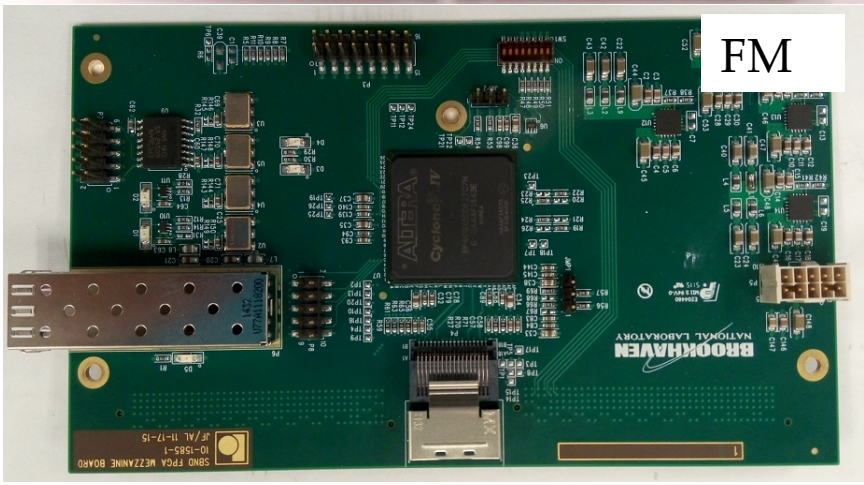
SBND Top FEMB

- SBND FEMB (Top FEMB)
  - AM: Analog Mother Board
    - 8 FE ASICs & 8 V* ADC ASICs
    - 128 FE channels
    - Cold regulators: TI TPS74201
  - FM: FPGA mezzanine
    - FPGA mezzanine is used for multiplexing and readout of digitized detector signals
    - Cyclone IV GX FPGA
    - MiniSAS connector
  - Toy TPC
    - Emulate detector capacitance

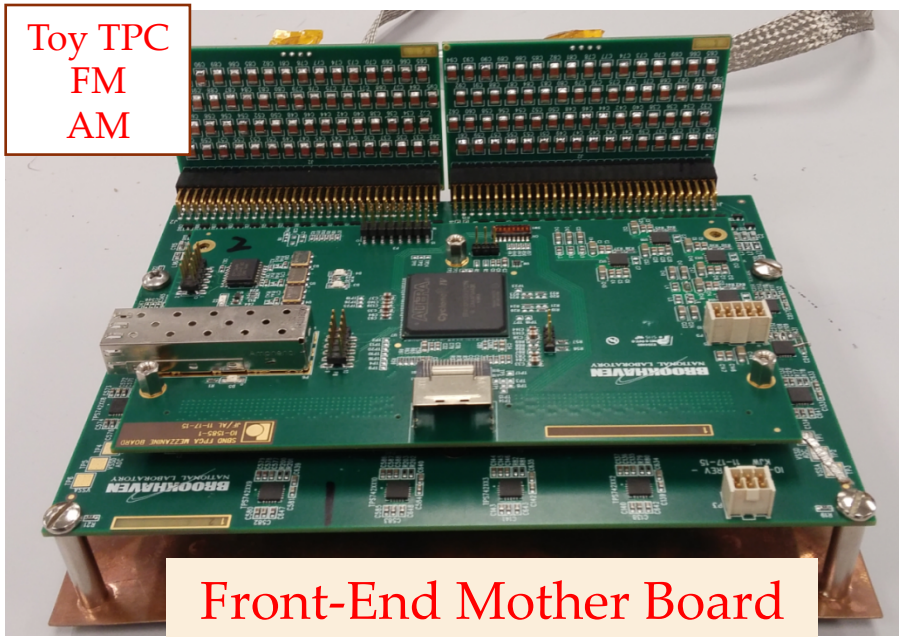


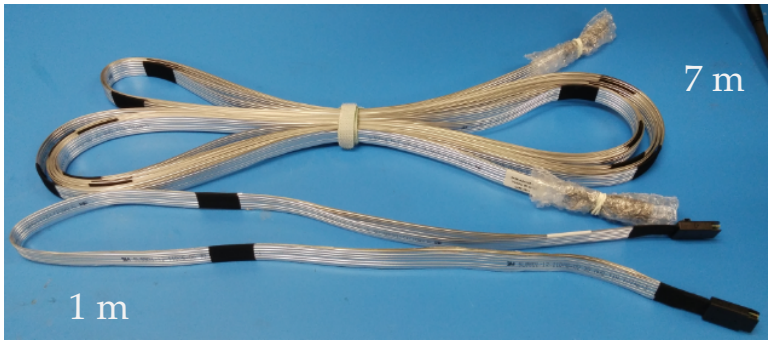
Toy TPC: 150pF





SBND Top FEMB





3M miniSAS cable for SBND

FEMB and Toy TPC form a complete cold electronics assembly

Top FEMB has been used to evaluate the noise performance

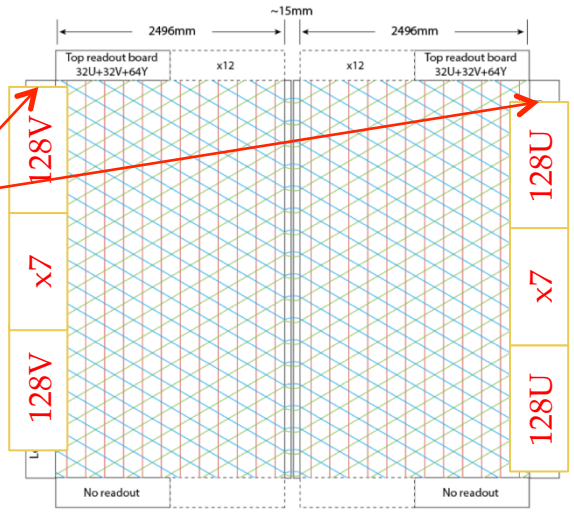
Extensive tests have been carried out to address the low frequency noise of cold voltage regulator

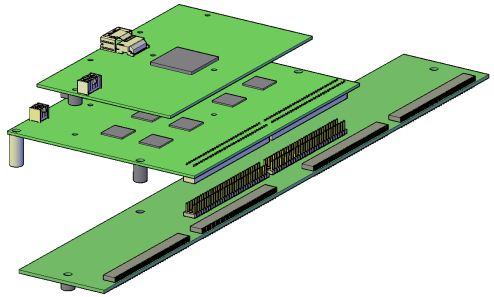
Cold FE ASIC used in TOP FEMB: MB FE ASIC

Cold ADC ASIC used in TOP FEMB: V* ADC ASIC

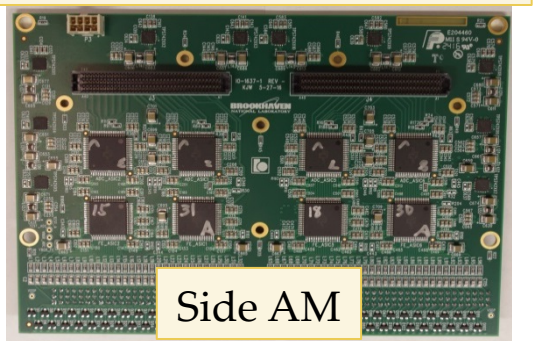
SBND Side FEMB/ProtoDUNE FEMB

- ProtoDUNE FEMB (SBND Side FEMB)
  - Instead of a long side AM, one can build a long side adapter board with a small side AM
    - Same FM design for both top and side FEMB
    - Minimize number of FPGA mezzanines
  - Side FEMB Adapter board
    - Passive board with only mating connectors
  - Side AM
    - Same size of top AM
    - Same design as (Proto)DUNE AM
    - Side AM design has filter on board, it has been assembled with new FE ASICs

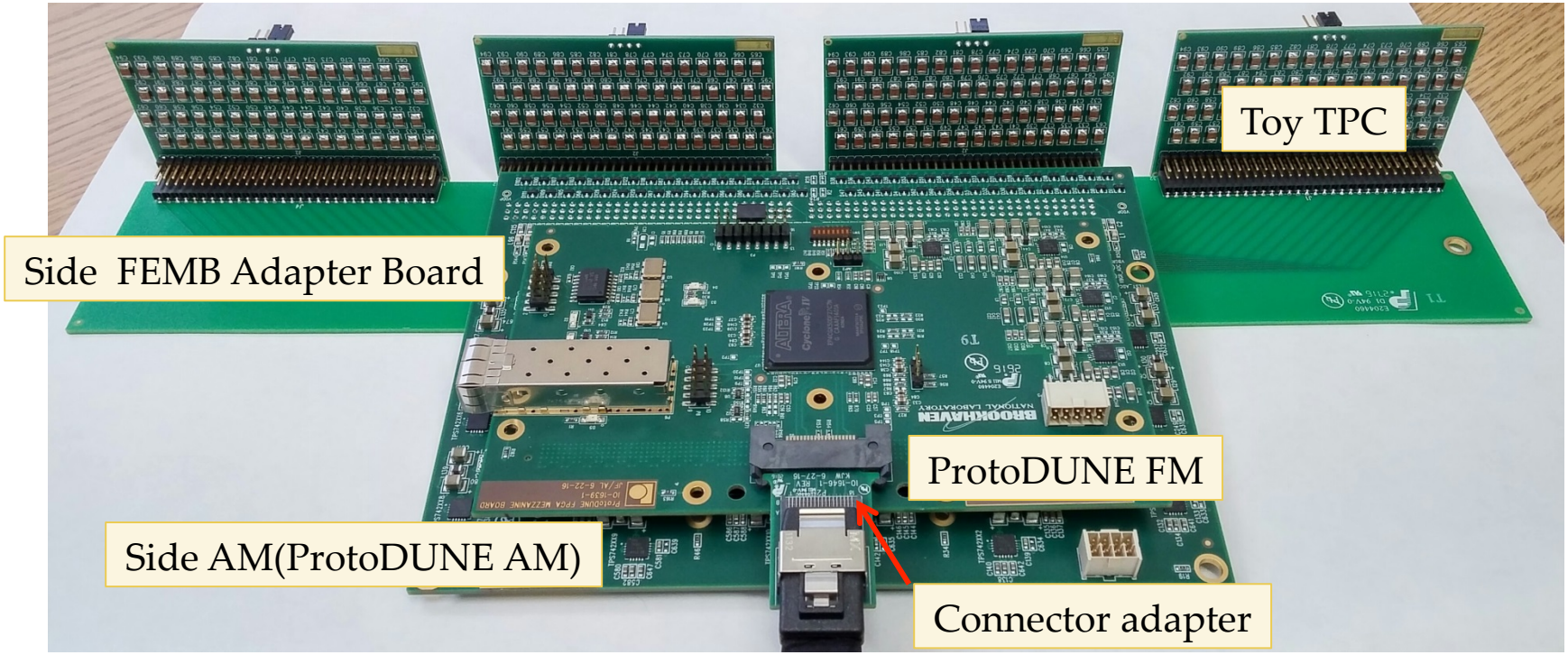




Side FEMB Adapter Board

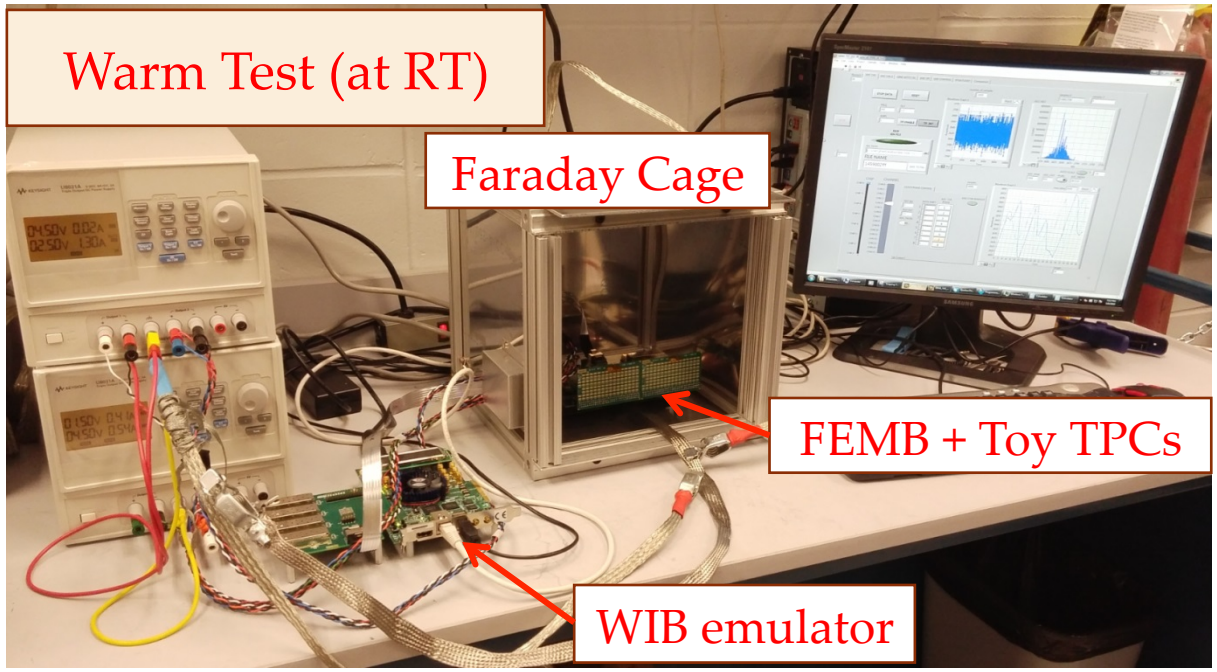


SBND Side FEMB / ProtoDUNE FEMB

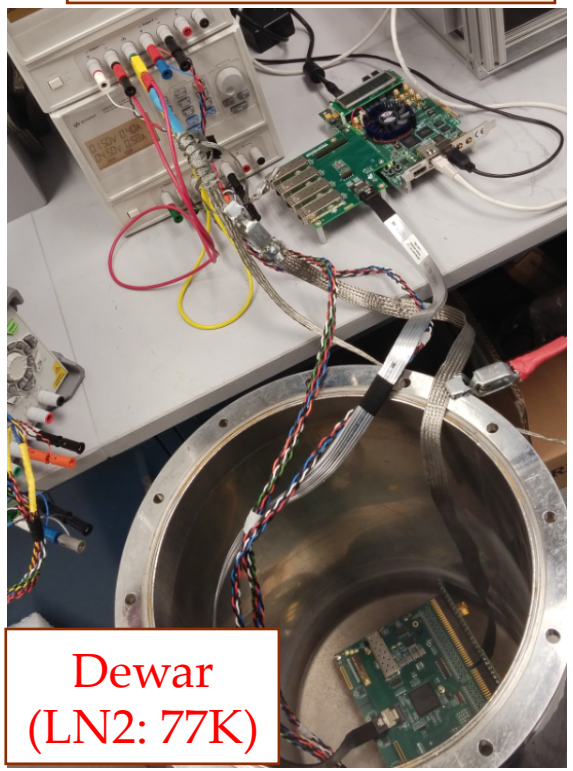


Cold FE ASIC used in TOP FEMB: P1 FE ASIC
Cold ADC ASIC used in TOP FEMB: V*ADC ASIC

FEMB Test Stand



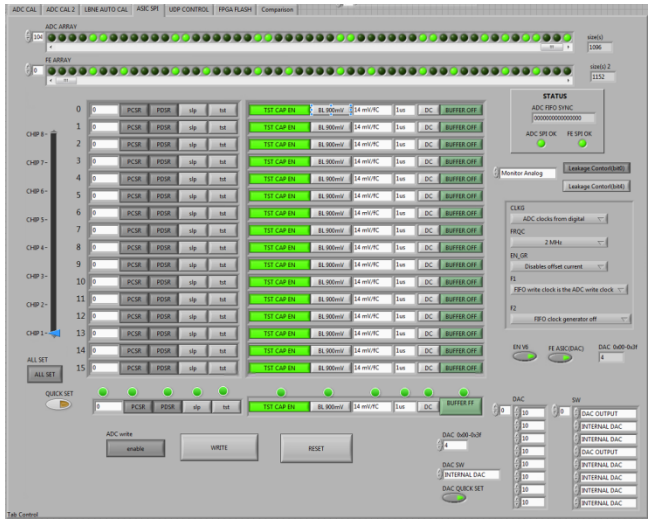
Cold Test (at LN2)



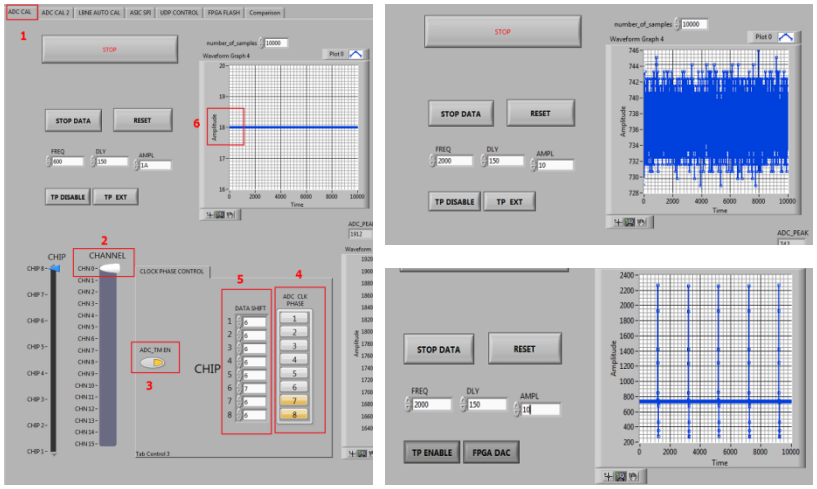
- Characterization of noise performance has been performed on the SBND/ProtoDUNE FEMB
  - Extensive evaluation test of cold voltage regulator filters
  - Careful study of ADC “stuck-bin” effects on ENC measurement

DAQ

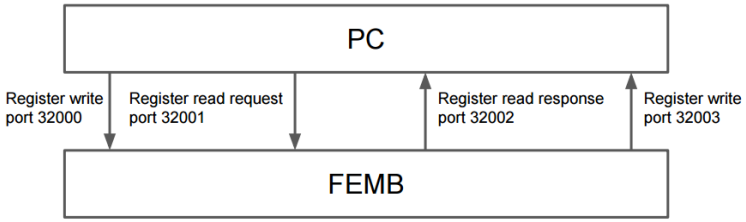
- LabVIEW
  - Live view (GUI), easy to use, especially suitable for debugging
  - Disadvantages: requires many manual operations before data acquisition
- Python scripts
  - Good for getting statistic results
    - Advantages: all tests with different settings can be tested through a script if hardware doesn't need to be changed during the testing
  - Disadvantages: Not as fast as C#



LabVIEW: FE and ADC configuration



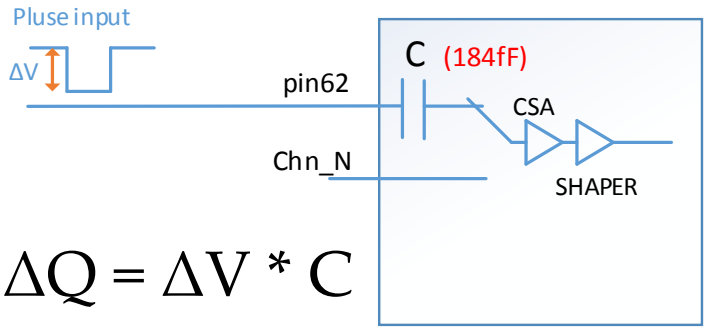
LabVIEW: live view



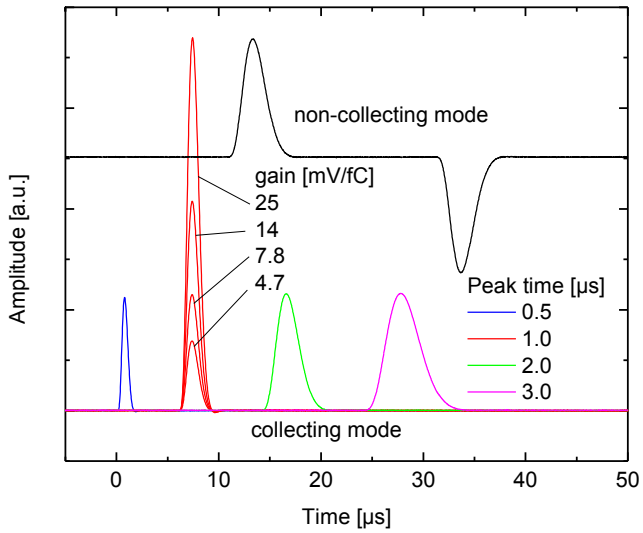
Python scripts

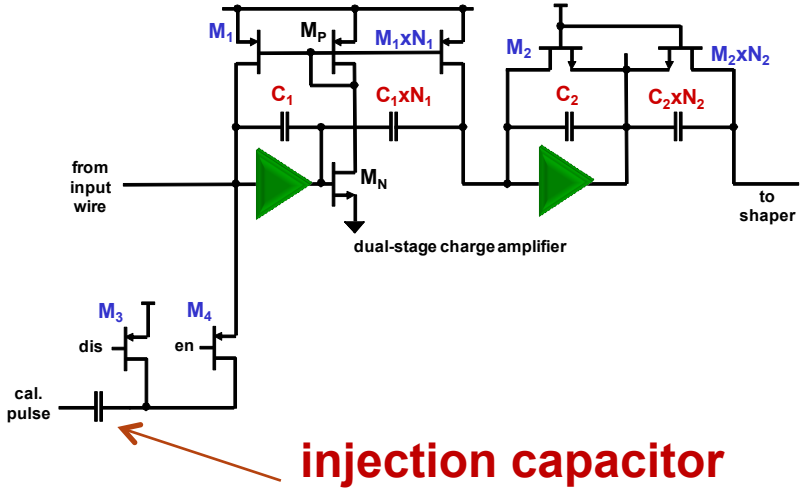
FE-ASIC Calibration and ENC Calculation

- Calibration
  - Step voltages generated by FPGA "DAC"
    - Capacitor is integrated in FE ASIC
  - P1 FE ASIC includes the integrated calibration injection circuit
- ENC calculation
  - 250,000 samples per channel to calculate rms noise



$$\Delta Q = \Delta V * C$$





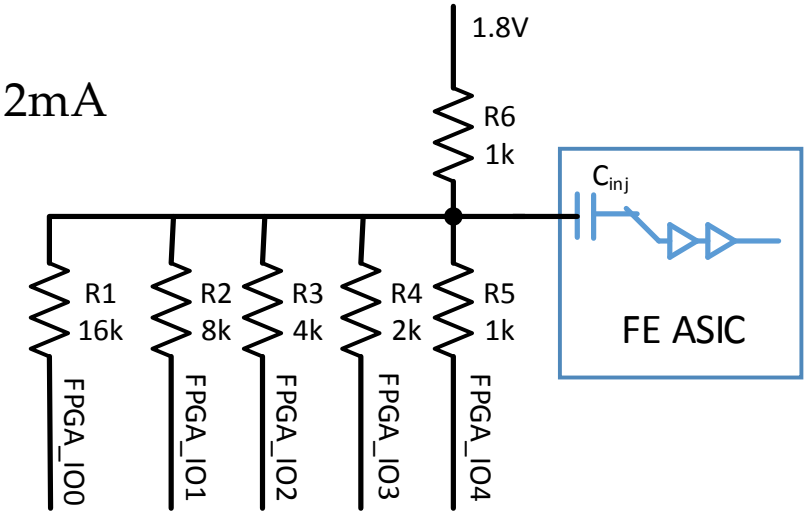
injection capacitor

measured: 184 fF at 300 K

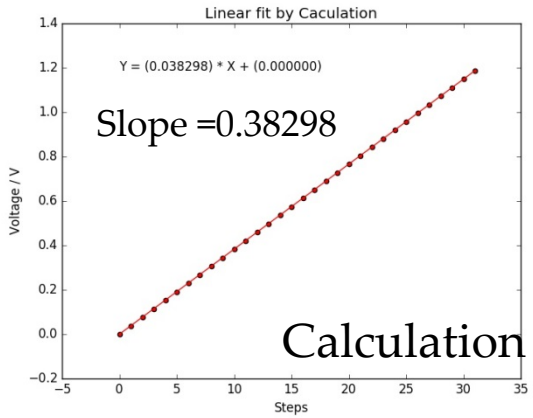
183 fF at 77 K (0.5 %)

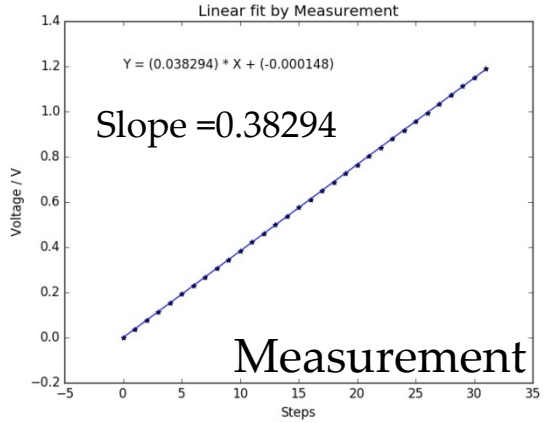
Pulse Generator: FPGA "DAC"

- Schematic
  - FPGA IO source or sink current limit: 2mA
  - Maximize source current: 0.574mA
  - Maximize sink current: 1.187mA
  - R6 = 1kΩ
  - **R1 = 16.02kΩ (1%)**
  - **R2 = 8.06kΩ(1%)**
  - **R3 = 4.02kΩ(1%)**
  - **R4 = 2.00kΩ(1%)**
  - **R5 = 1.00kΩ(1%)**



38.3mV per ΔV. Range up to 30



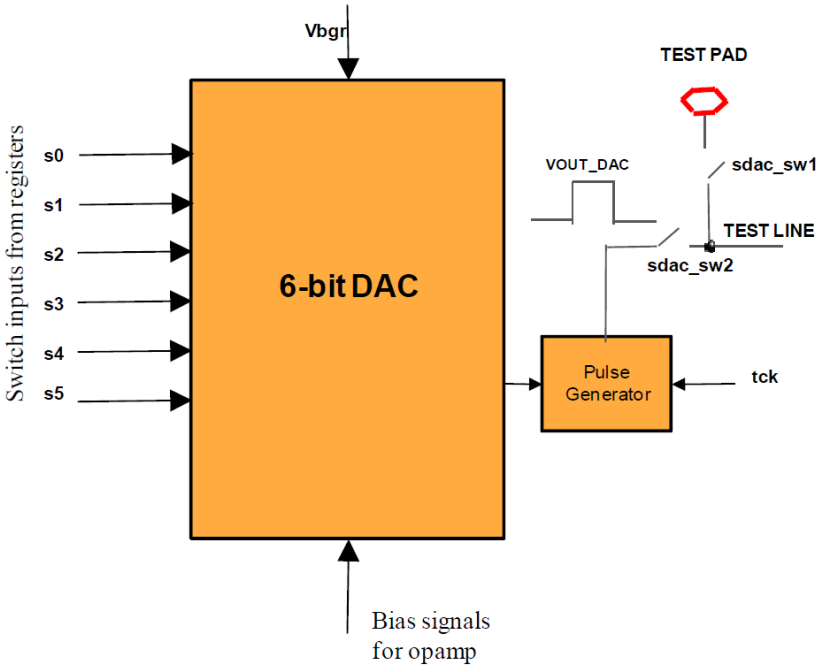


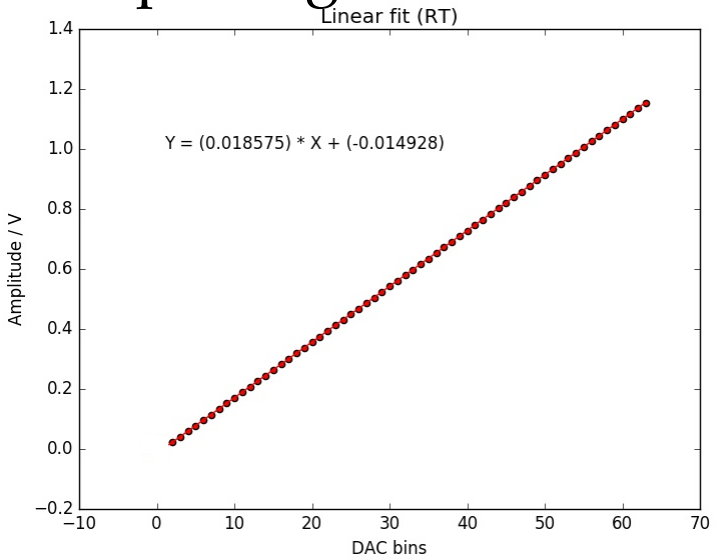
FPGA "DAC" works well at both room and LN2 temperatures

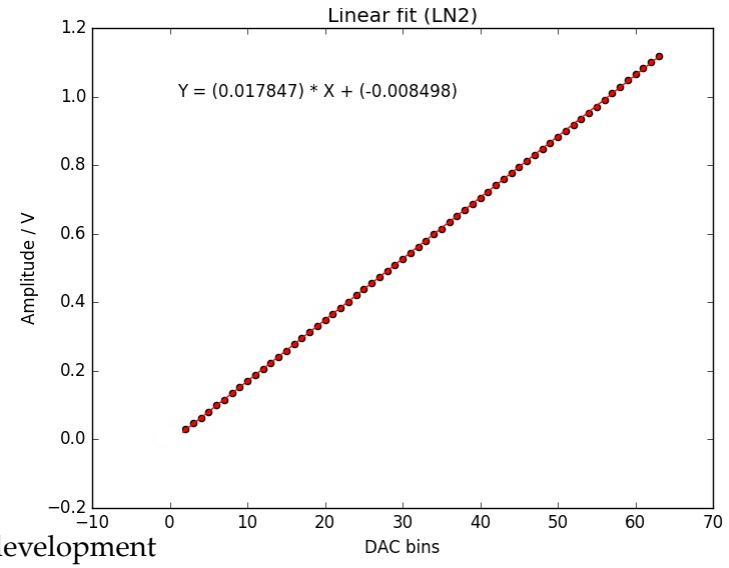
Very good agreement between calculation and measurement

Internal Pulse Generator of P1 FE-ASIC

- P1 FE ASIC integrated 6-bit internal pulse generator







- Output Voltage Range: 0 to 1.18V
- Resolution: 18.75mV
- Power: 1mW
- Temperature Range: 27°C to -200°C
- Settling time: < 130ns
- Linearity: ± 0.12 %

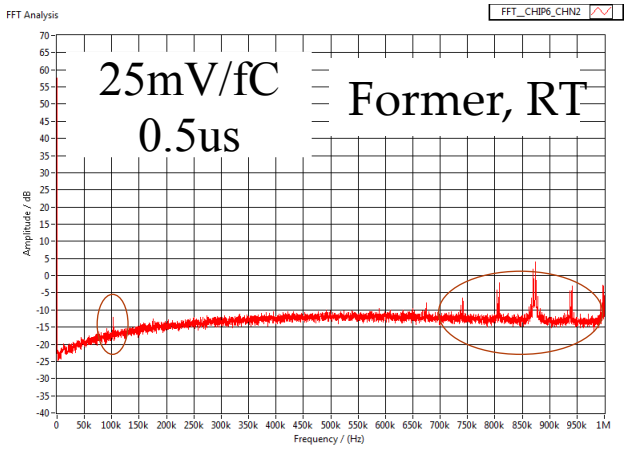
List of Tests Done On FEMB Test Stand

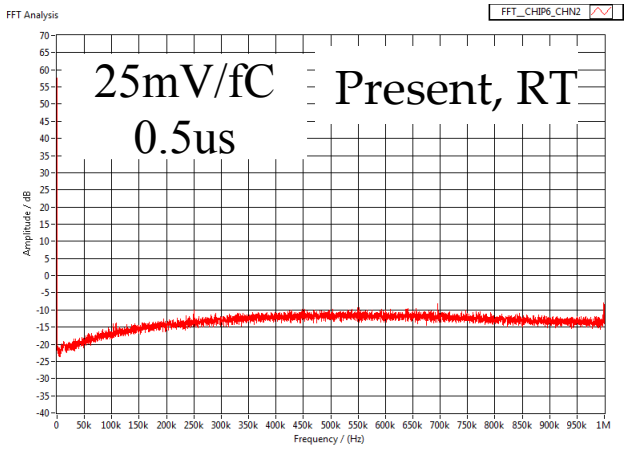
- Noise measurement
  - Shielding and Grounding
  - Study of power supplies
  - Study of regulator
  - Study of filters for regulator outputs
  - Contrast test: scope measurement
- Calibration study
  - Performance of FPGA "DAC" and Internal DAC
  - Calibration with injected pulse generated from FPGA DAC
  - Calibration with injected pulse generated Internal DAC

- Detail test results will be shown in tomorrow talk

Shielding and Grounding

- Good grounding clears high frequency glitches on the FFT spectrum
- A well shielded Faraday cage is made by Ken Sexton
- Reliable grounding cables
- WIB emulator (SBND test board and Altera Arria V evaluation board) is directly connected to the same ground
- All grounding cables are connected to the ground of power supply





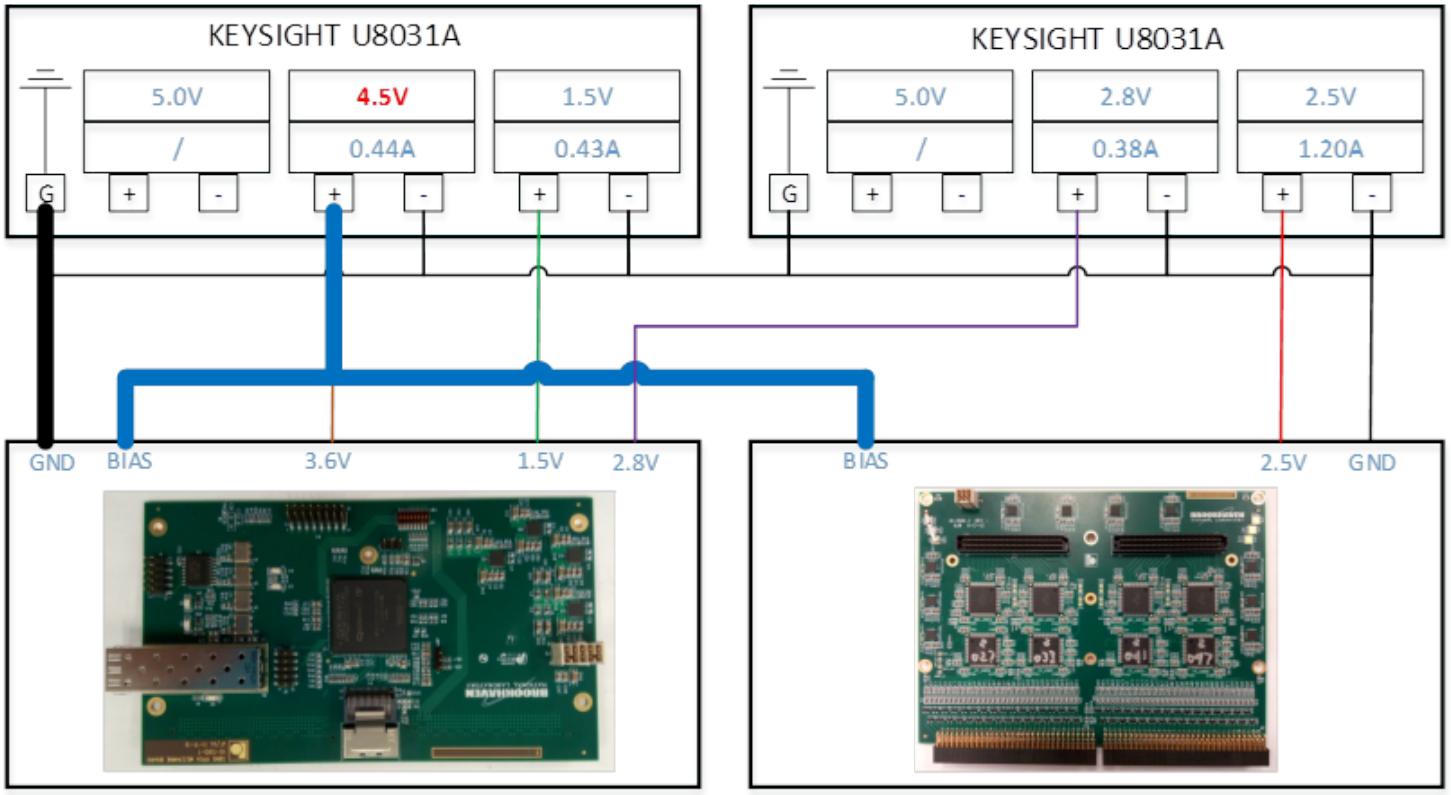
Smooth FFT spectrum, no obvious pick up noise

Study of Power Supplies

- Three power supplies have been studied
  - KEYSIGHT U8031A
  - RIGOL DP832A
  - Batteries

- Test result showed Keysight U8031A is as good as batteries for FEMB
  - Except the 5.0V fixed output

Power Supply Scheme for FEMB



Why abandon 5.0V fixed output of Power supply for regulator bias?

Because 5.0V fixed output noise is 50mVpp but programmable output is 10mVpp. We did find it affects the noise performance.

Low noise power supply is necessary for the noise performance of FEMB.

Study of Regulators

- Comparison between TPS74201 and ADM7151

Regulator	Iout(A)	RMS Noise 10 Hz to 100 kHz (uV rms)	RMS Noise 100 Hz to 100 kHz (uV rms)	PSRR(dB)
ADM7151	0.8	1.6	1	94 @ 100 kHz, 62 @ 1 MHz
TPS74201	1.5A	/	16*Vout (typ) = 28.8	73 @1kHz, 42@300kHz

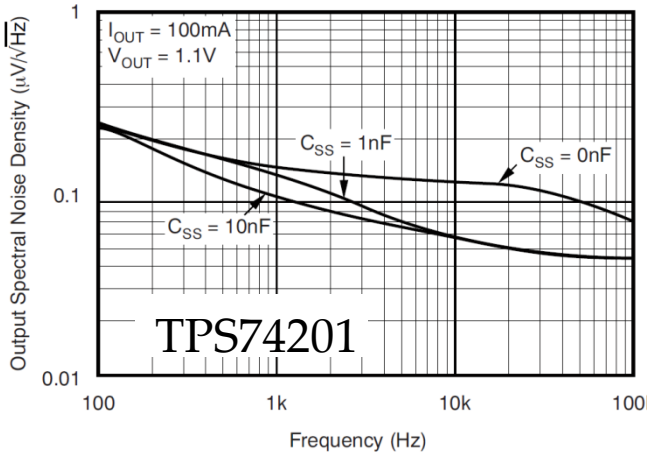


Figure 12. Noise Spectral Density

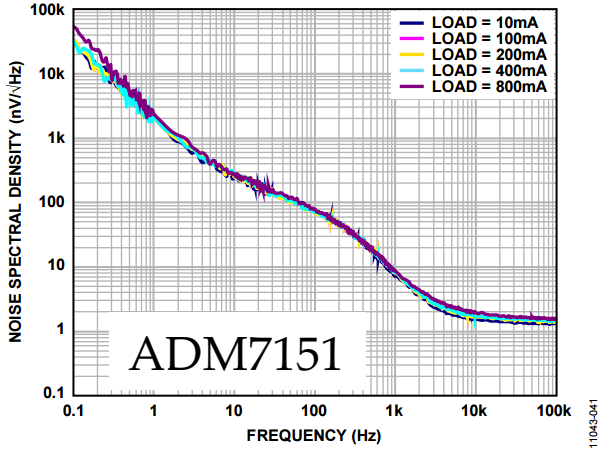
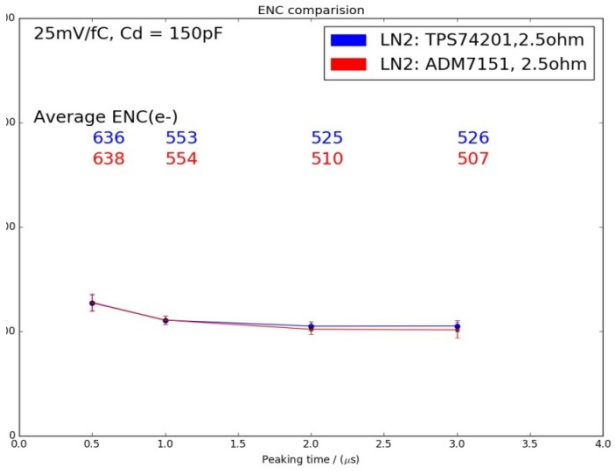


Figure 41. Output Noise Spectral Density at Different Load Currents, 0.1 Hz to 100 kHz



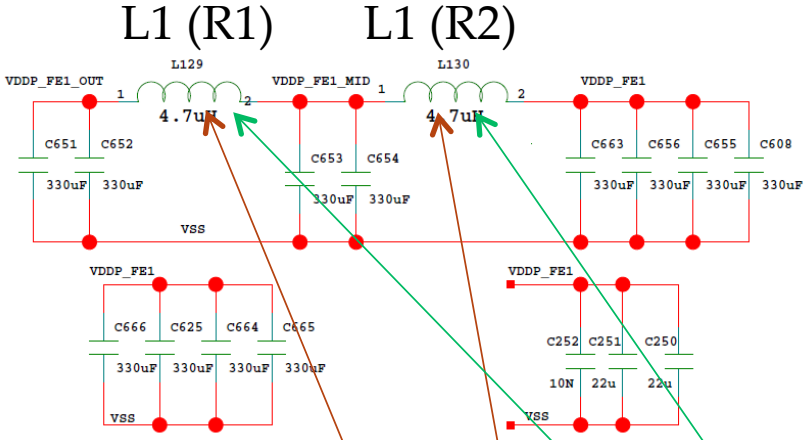
ADM7151 for FEMB gets slightly better noise performance at LN2.

However ADM7151 needs 4.5Vin, not suitable for cold operation

More detailed study for TPS74201 will be shown tomorrow.

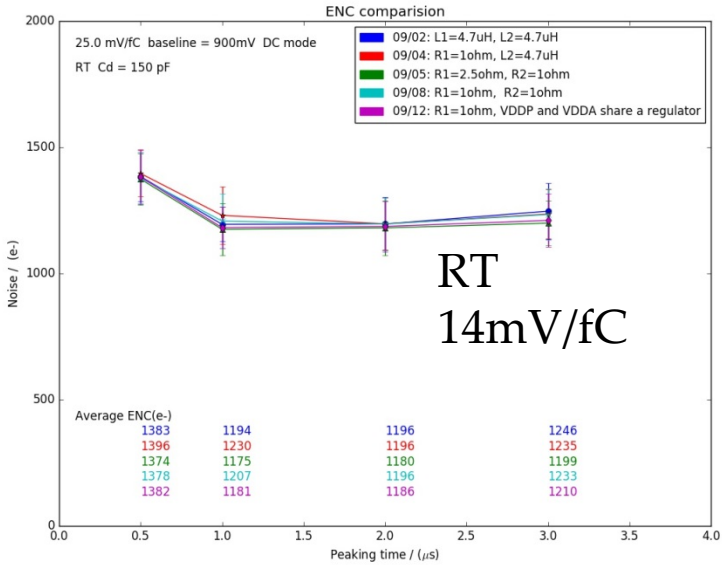
Study of Filter for Regulator Output

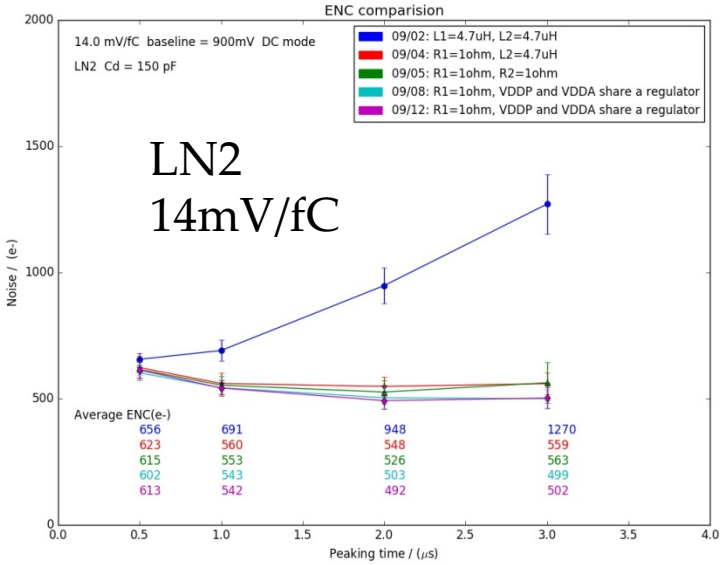
- RC filter vs Chebyshev Filter



	VDDP of FEASIC		VDDA of FE ASIC	
Filter Configuration	L1 (R1)	L2 (R2)	L1 (R1)	L2 (R2)
09/02, Filter1 (Chebyshev)	4.7uH	4.7uH	4.7uH	4.7uH
09/04, Filter2 (R, L)	1 ohm	4.7uH	1 ohm	4.7uH
09/05, Filter3 (R, 0ohm)	2.5ohm	0 ohm	1 ohm	0ohm
0908, Filter4 (R, 0ohm)	1 ohm	0 ohm	1 ohm	0ohm
09/08, Filter54R, 0ohm)	1 ohm	0 ohm	Powered by VDDP	

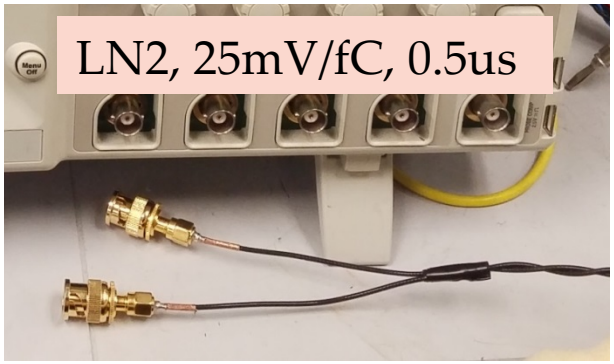
At liquid nitrogen, RC filter is much better than Chebyshev filter, especially in big peak times.

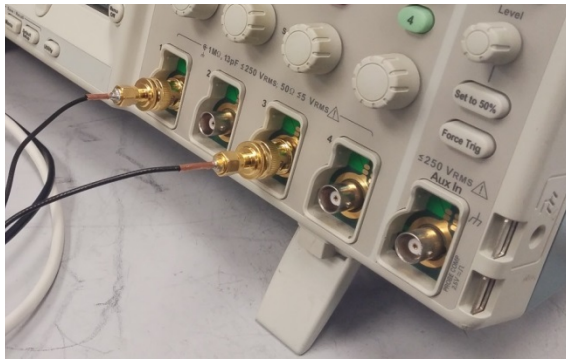


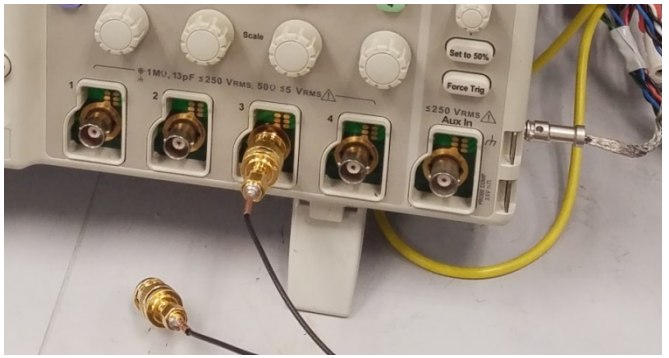


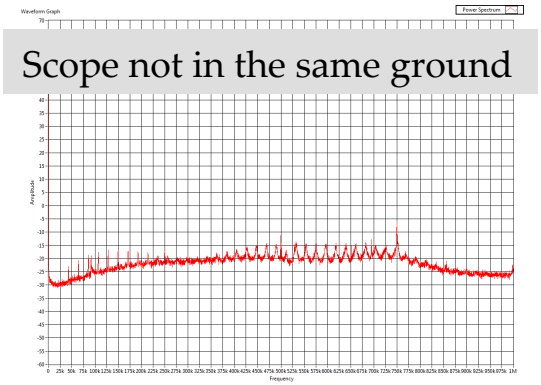
Contrast Test: Scope Measurement

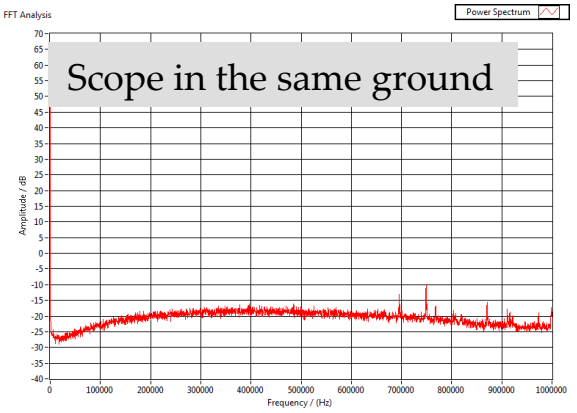
- Chip8, channel14 was observed with scope as well
- Scope was directly connected to the same ground
  - If scope isn't directly connected to the same ground
    - The noise performance becomes worse
    - Many glitches appear in the FFT spectrum



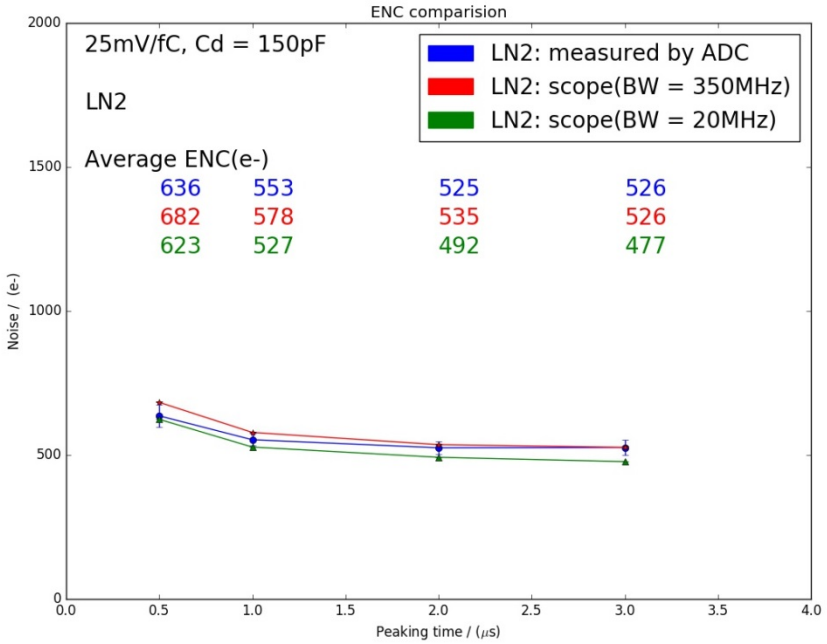








Comparison at LN2

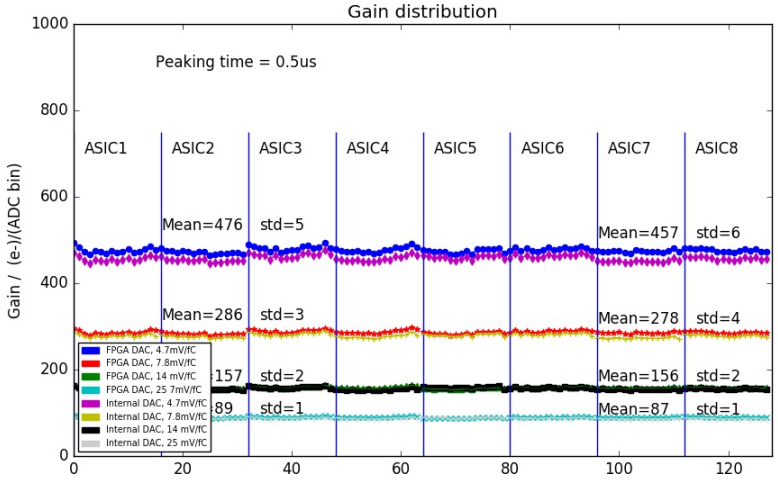


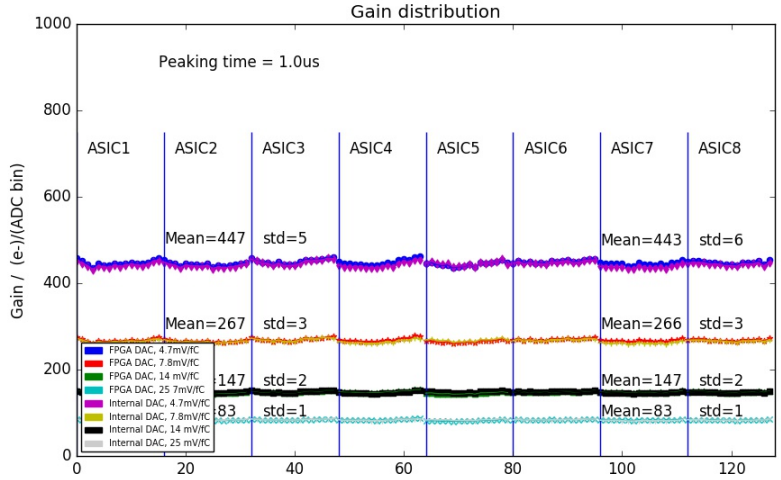
- Blue: average ENC was measured before scope measurement
- Red: ENC of Chip8Chn14 was measured by scope
  - Full bandwidth = 350 MHz
- Green: ENC of Chip8Chn14 was measured by scope
  - Bandwidth = 20 MHz
  - Glitches are filtered by limited BW

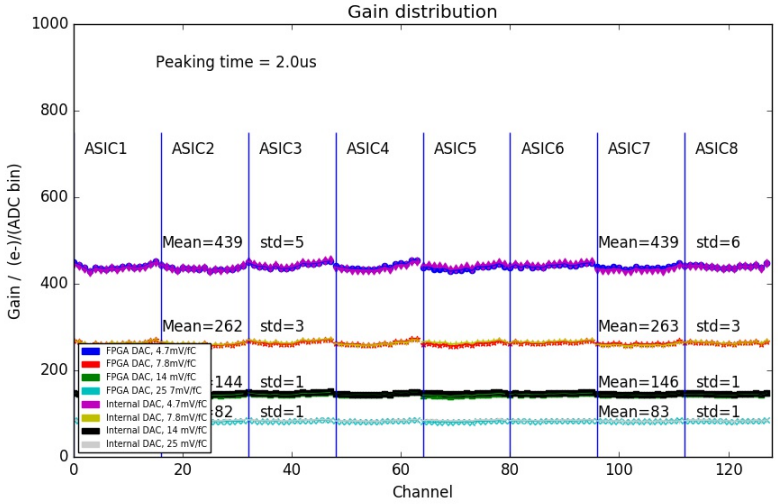
- ENC measured by scope (BW = 20MHz) is comparable with V* ADC measurement
  - ENC measured by scope doesn't include the noise from ADC ASIC
  - ENC measured by ADC includes the noise from ADC ASIC
- Scope measurement with 20MHz is more reasonable
  - Since the glitch is caused by ADC ASIC when sampling operation happens

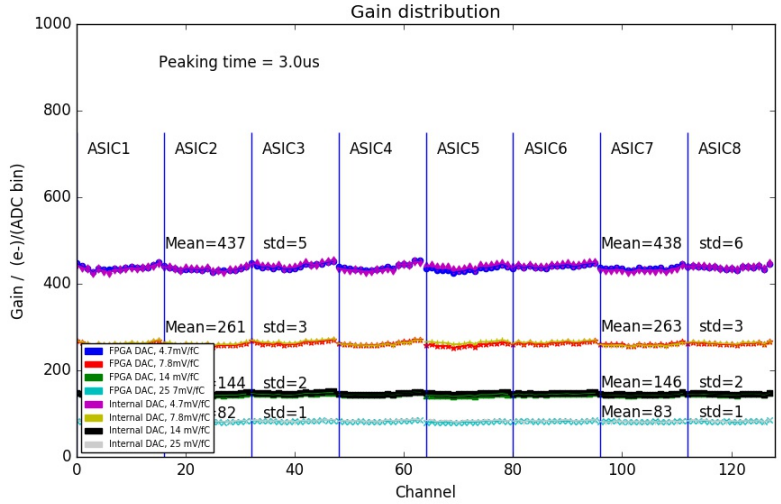
Calibration Study

- Both FPGA-DAC and Internal-DAC are good for calibration





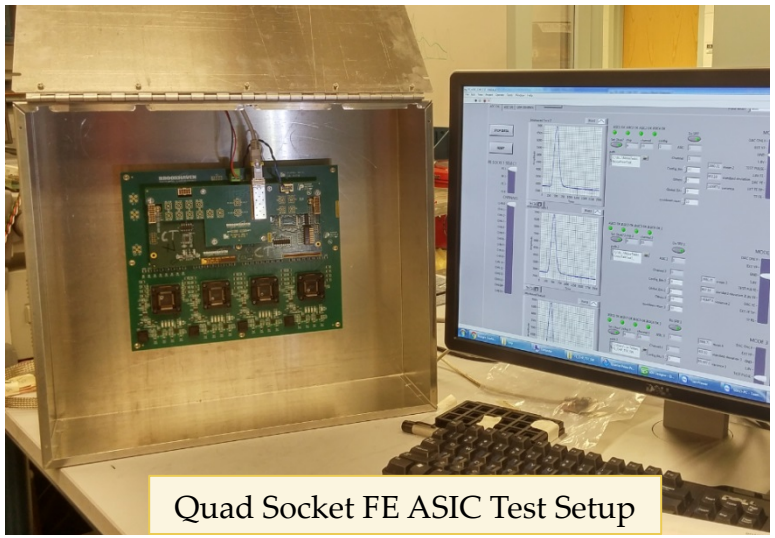




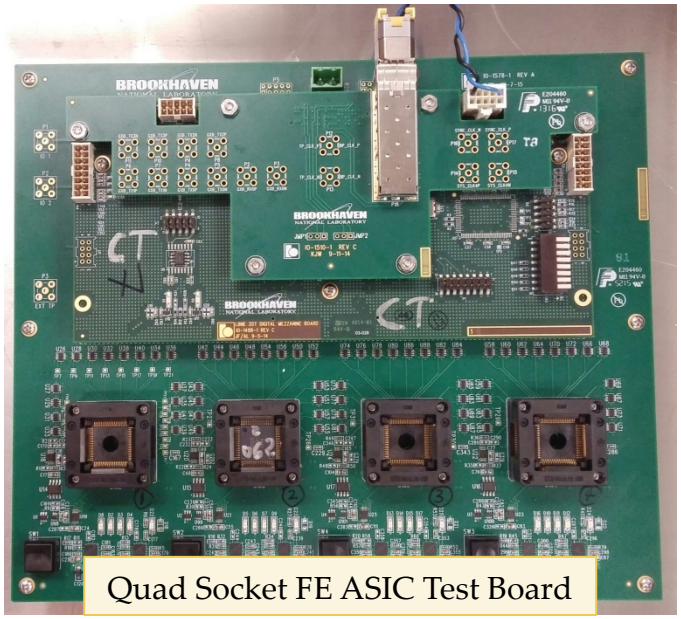
FE ASIC Test Stand

- Warm stand: Quad Socket FE-ASIC test stand
  - Performance test
  - QA/QC test (collaboration with MSU on development)
- Wire-bonding die test stand
  - One die test board
  - Three dies are installed on MB Analog Mother board
  - Evaluation test
- MB six sockets test stand
  - Evaluation test with ASIC packaged by different fabrication companies.

FE ASIC Warm Test Stand



Quad Socket FE ASIC Test Setup



Quad Socket FE ASIC Test Board

- Quad Socket FE ASIC Test Board
  - Readout, DAQ, control and monitoring is through DUNE 35T FPGA mezzanine
  - DAC: TI 16-bit DAC8411 is used to inject test pulse
  - ADC: Linear Tech 14-bit 4.5Msps LTC2314 is used to digitize analog output signal
    - Sampling scope mode for better timing resolution
- The test stand is used to evaluate the P1 FE ASIC
  - Close collaboration with MSU on firmware and software development
- Next step
  - The quad socket test board will be revised to use SBND/DUNE FPGA mezzanine and Enplas clam-shell sockets
  - The new design will accommodate both warm and cold test, with proper shield for low noise measurement

List of Revision of Quad Socket FE ASIC Test Board

- 1. Two versions of Quad Socket FE ASIC Test Board
  - one is for warm test in the RF shielded box
  - the other is for the cold test
- 2. SBND/ProtoDUNE FM is used to replace the 35Ton FM
- 3. Enplas clam-shell socket is adopted
  - Clam shell socket has more reliable operation in cold
- 4. Add 150pF MICA capacitor for each channel of FE ASIC to emulate the detector capacitance
- 5. Except the ADC, the circuit around the FE ASIC is same as SBND/ProtoDUNE Analog Mother
  - Same filters for power supply as FEMB
  - Protection diodes, capacitors and inductors, etc
- 6. Add current sensing capability to each power rails and temperature sensing capability
- 7. Four FE ASIC are unrelated with each other
  - Each FE ASIC has dedicated SPI interface

- The schematics has done, the layout is ongoing

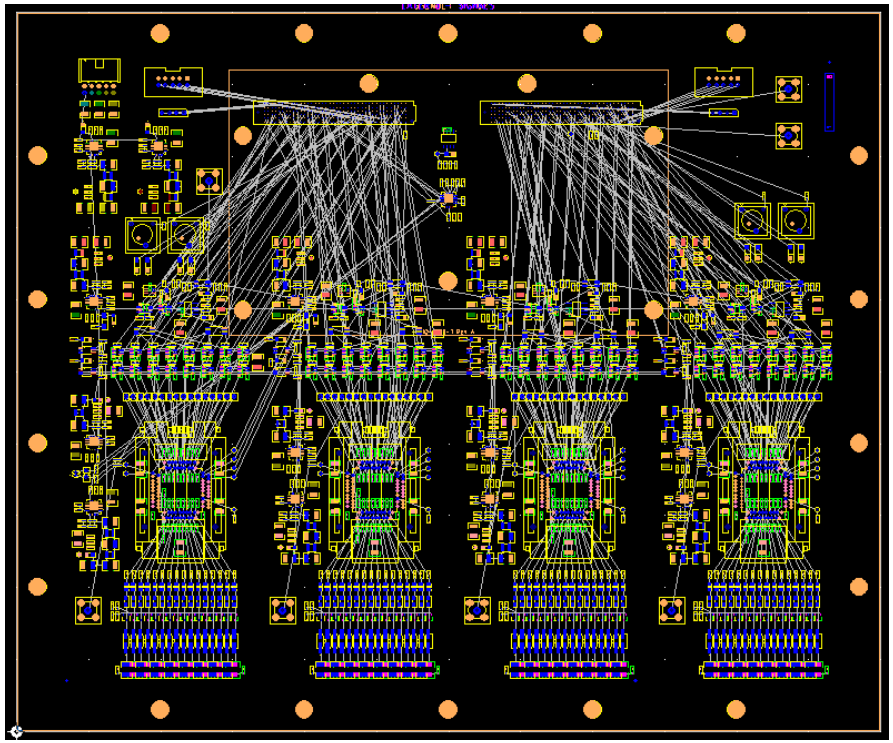
Revision of Quad Socket FE ASIC Test Board

- Layout is ongoing

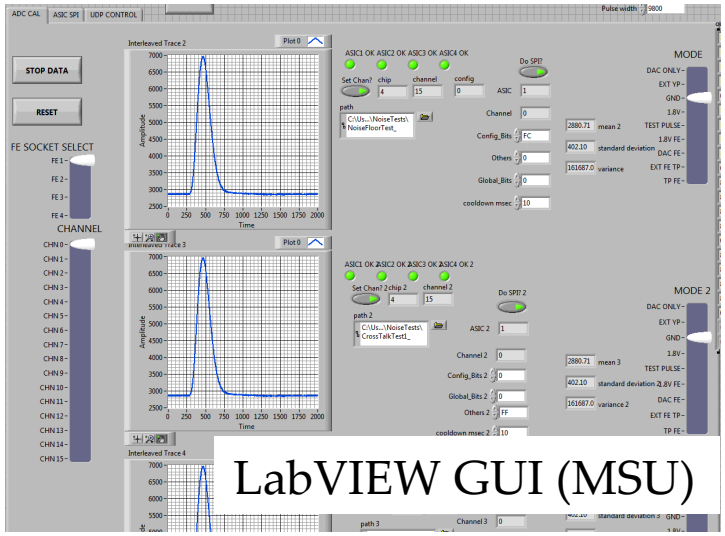
Two versions of Test Board

one is for warm test in the RF shielded box

the other is for the cold test



Layout of test board for warm test

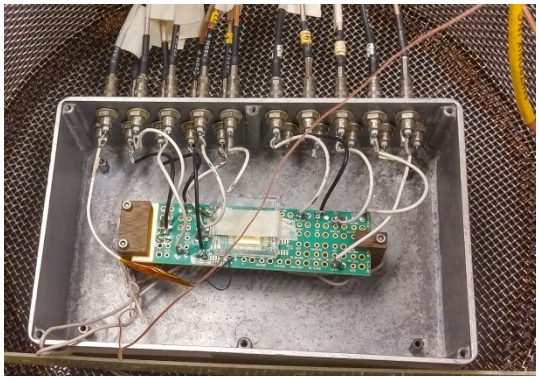


LabVIEW GUI (MSU)

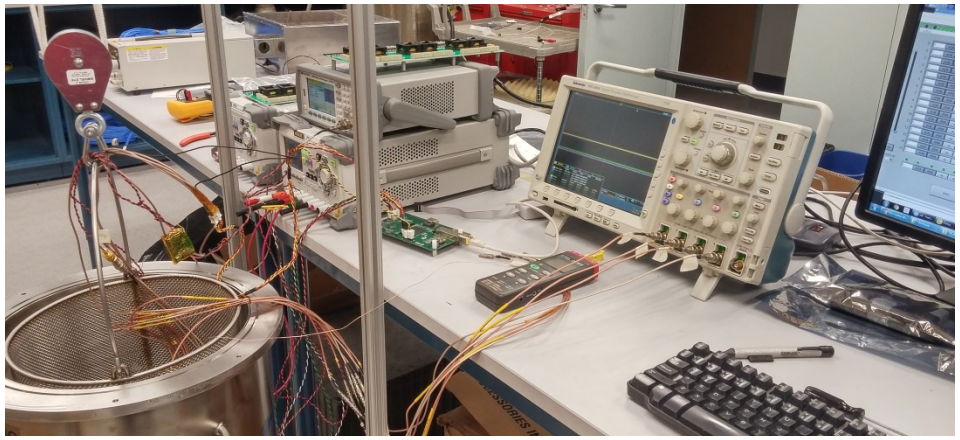
RT shielded box

Wire-bonding Die Cold Test Stand

- Single FE ASIC test board for performance characterization and debug test in LN2
- Wire bonding die has been tested
  - SBND/ProtoDUNE FM for configuration
  - Signal generator for calibration pulse injection
  - Oscilloscope for data acquisition
- List of tests done so far
  - Internal DAC and Pulse Generator Test
  - Peaking Time Test
  - Baseline Test
  - Smart Reset Test
  - Pole-zero cancellation test

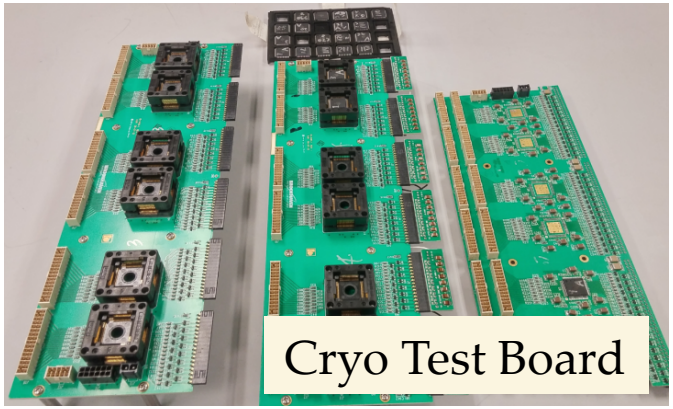


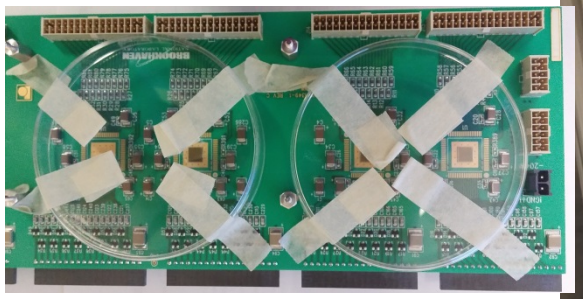
P1 FE ASIC

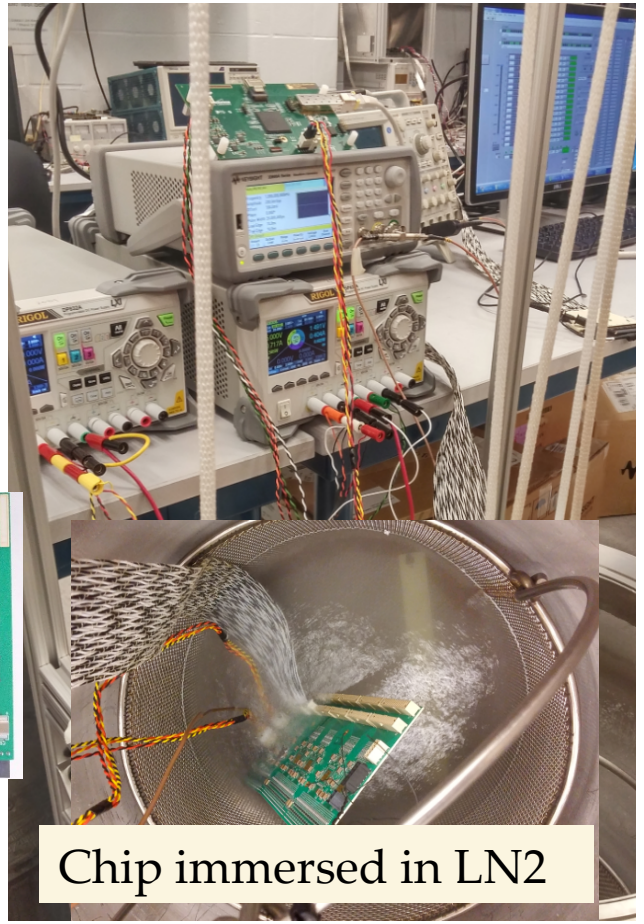


P1 FE Cold Test Setup

- MicroBooNE FE ASIC Cryo Test Board is used
  - SBND/ProtoDUNE FM for configuration
  - Signal generator for calibration pulse injection
  - Oscilloscope for data acquisition
- List of chip tested so far
  - P1 FE ASIC packaged by MOSIS
  - P1 FE ASIC die
  - P1 FE ASIC packaged by Quik-Pak
- Package issue is confirmed

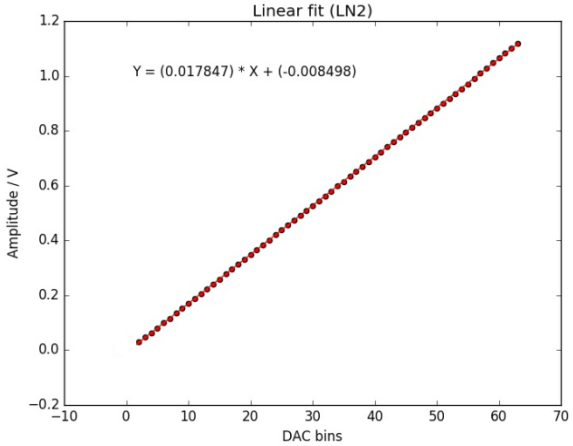

Cryo Test Board

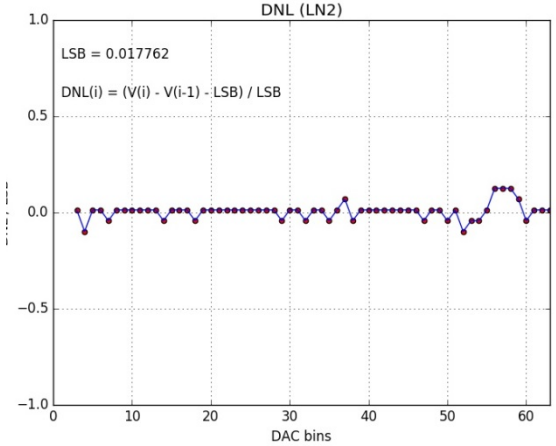

Three wire bonded dies

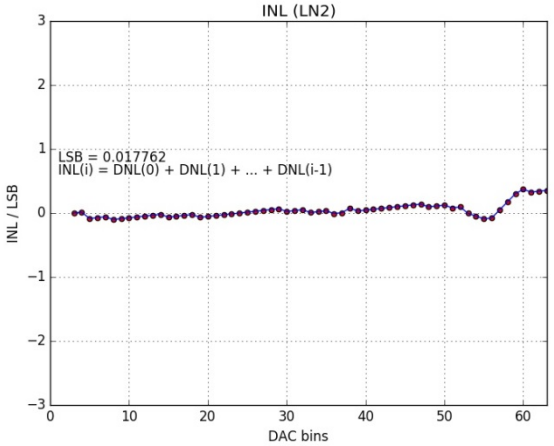

Chip immersed in LN2

Test Summary from SBND FEMB with P1 FE-ASIC

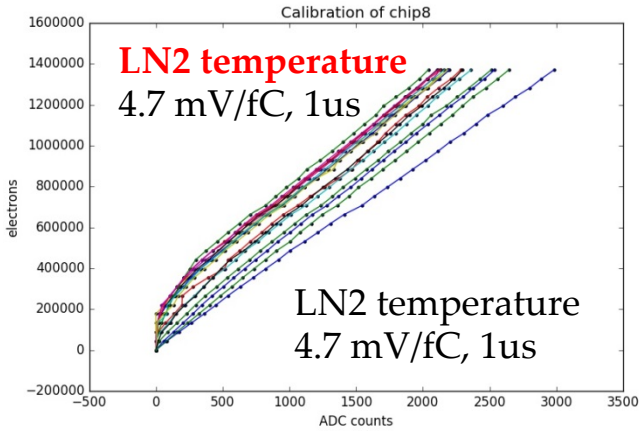
- Performance of internal DAC was studied

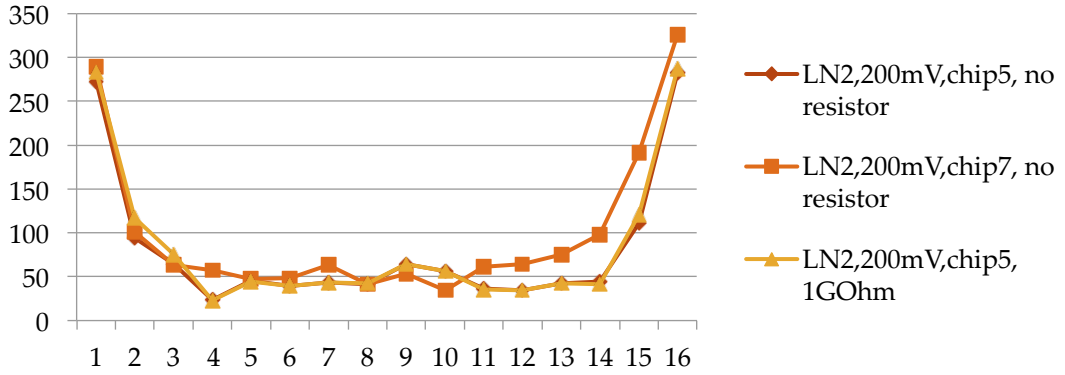






- Located new issue when P1 is set to collection-mode at LN2

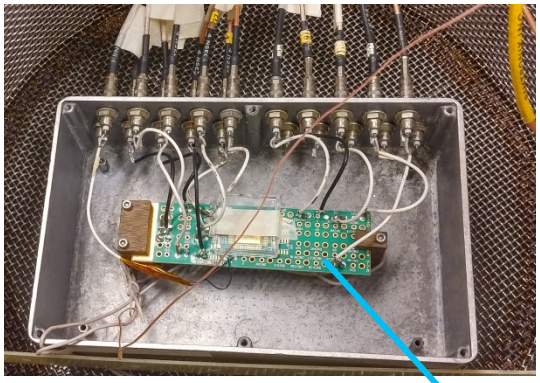




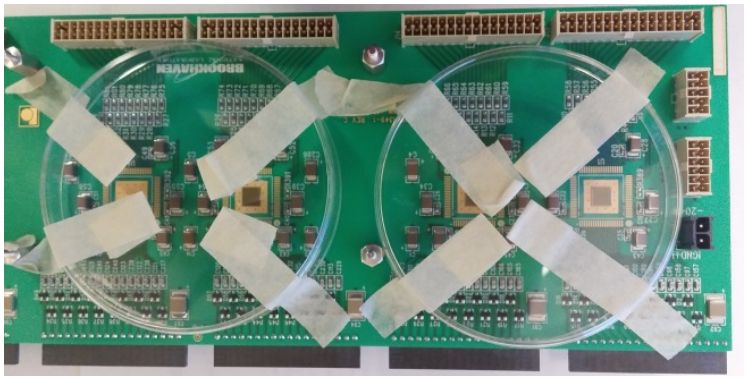
When the baseline is lower than 100mV, the FE channel may fail to amplified the injected pulse properly

Bare Dies Were Studied

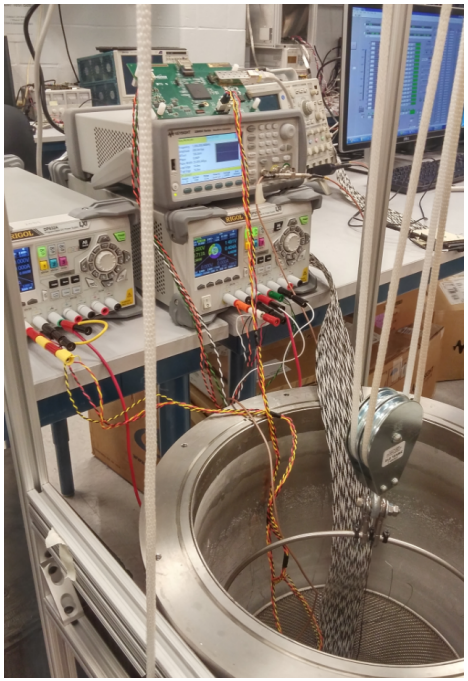
- Wire-bonding die cold test stand



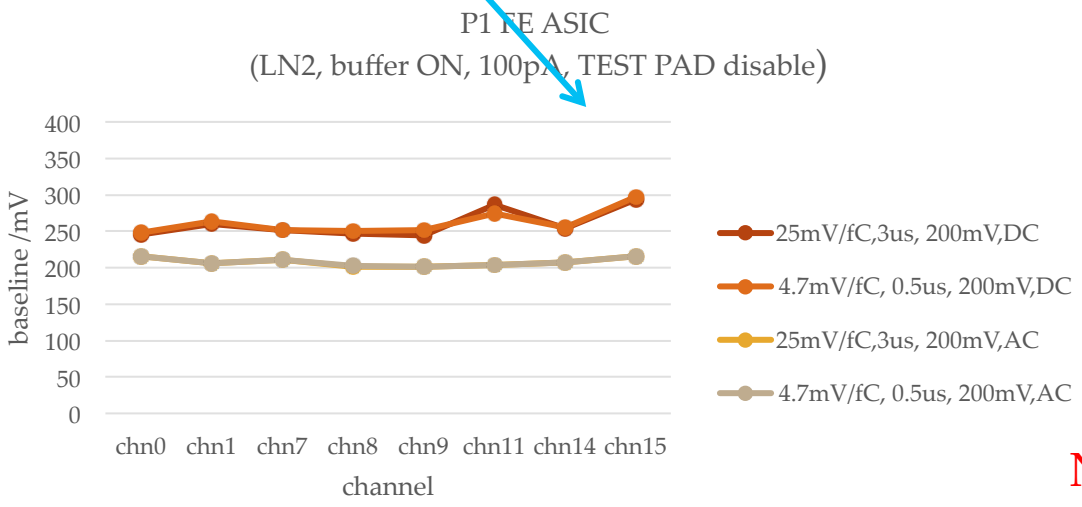
P1 FE ASIC die

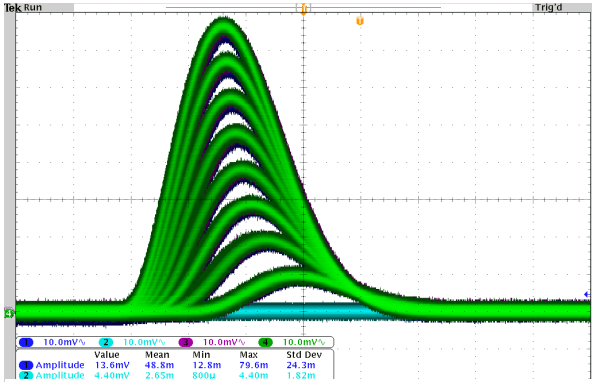


3 P1 dies on MB Cryo Test Board



Test stand



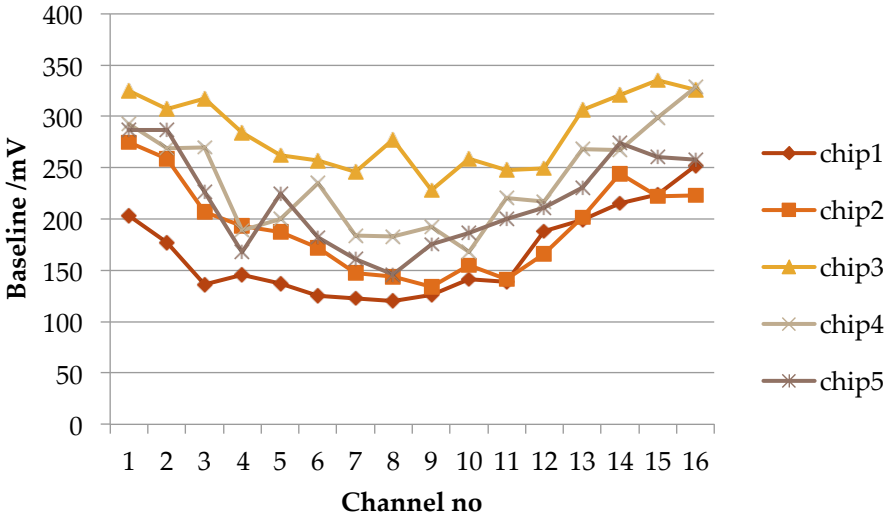


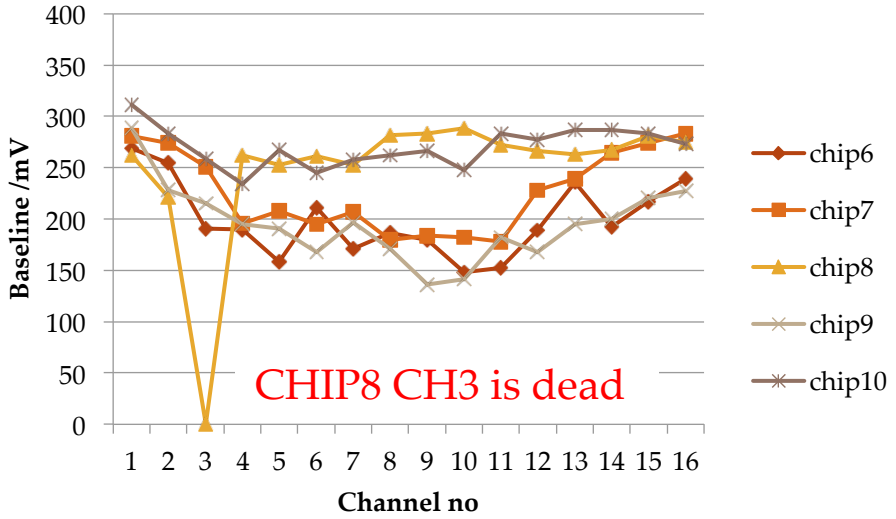
Vpulse = N*10mV, N = 1 ~ 8

No degradation of baseline
Good linearity on all channels

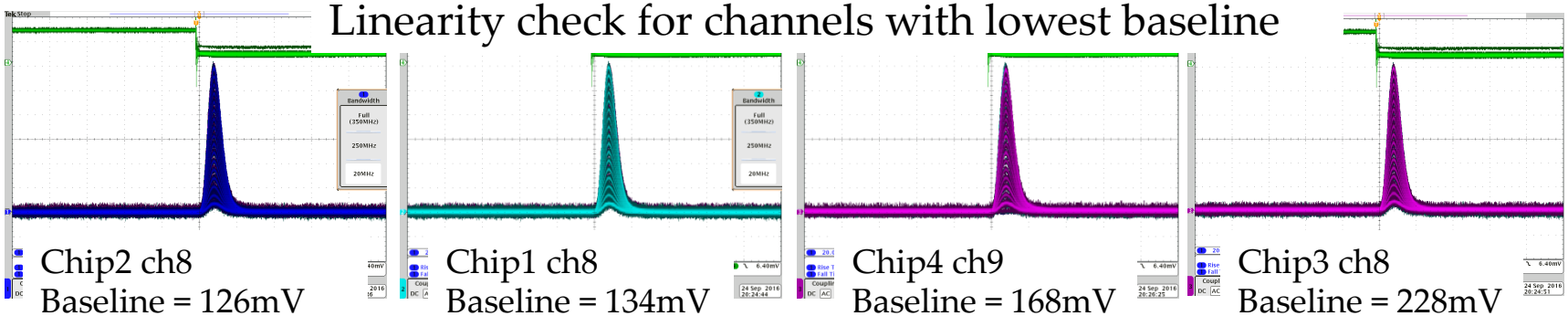
Baseline and linearity check for P1 FE ASIC packaged by Quik-pak

- Test was performed on MB socket cryo test stand





Linearity check for channels with lowest baseline



Chip2 ch8
Baseline = 126mV

Chip1 ch8
Baseline = 134mV

Chip4 ch9
Baseline = 168mV

Chip3 ch8
Baseline = 228mV

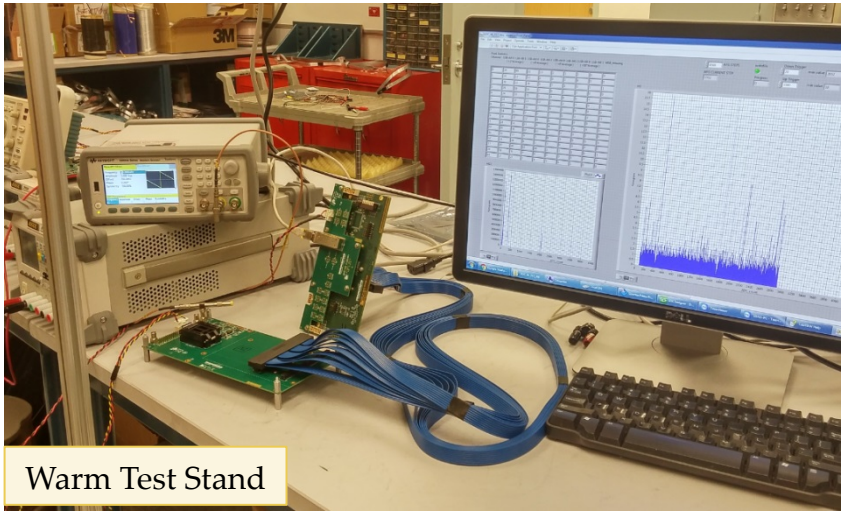
Conclusion: Quik-pak is a qualified packaging house for P1 FE ASIC

ADC ASIC Test Stand

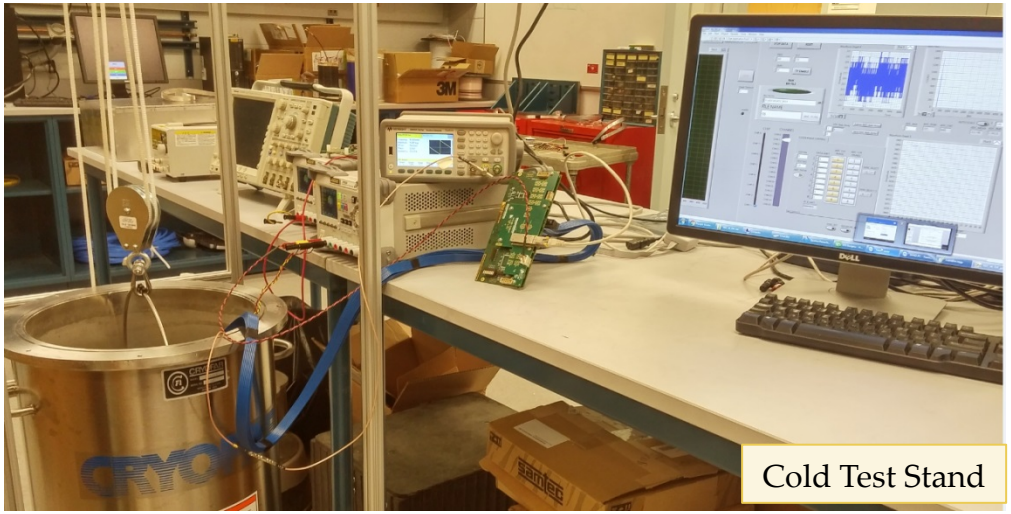
- V* ADC test stand
  - Three different configurations
    - Chip on board
    - Open top socket
    - Clam shell socket with filter
- P1 ADC ASIC test stand
  - One die has been installed on one V* ADC test board
    - Since the P1 ADC ASIC has different configuration interface and pin mapping from V* ADC, modifications on board had been made during the wire bonding process
  - New single socket ADC ASIC test board is ready
    - Revised board is compatible with P1 ADC ASIC and V* ADC ASIC
  - P1 ADC ASIC with package will arrive this week

V* ADC ASIC Test Stand

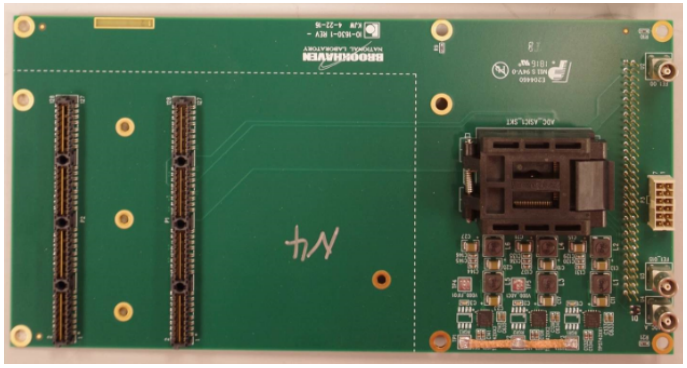
- The test stand has been used to characterize V* ADC ASIC extensively before submission of P1 ADC ASIC in July



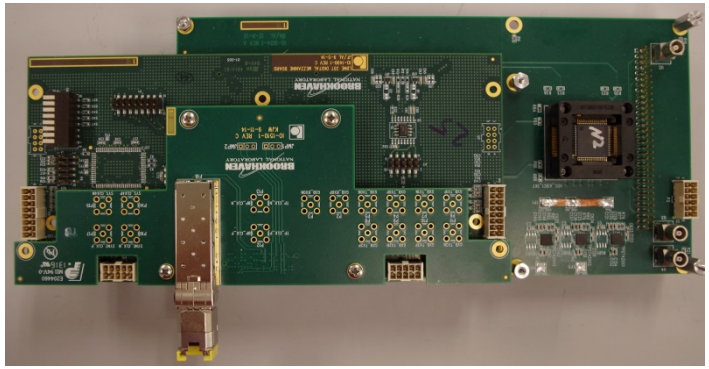
Warm Test Stand



Cold Test Stand



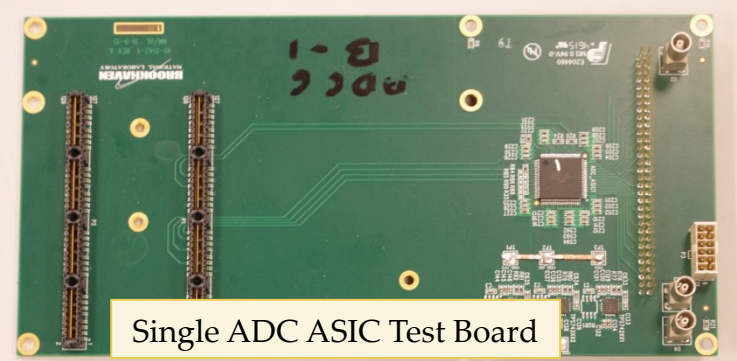
Single Socket ADC ASIC Test Board



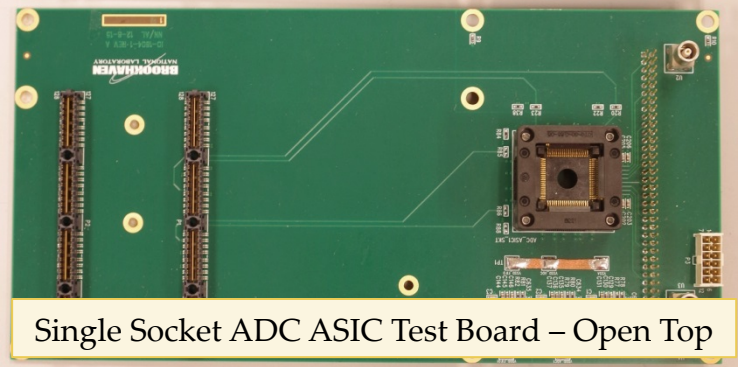
Single Socket ADC ASIC Test Board Assembly

LN2

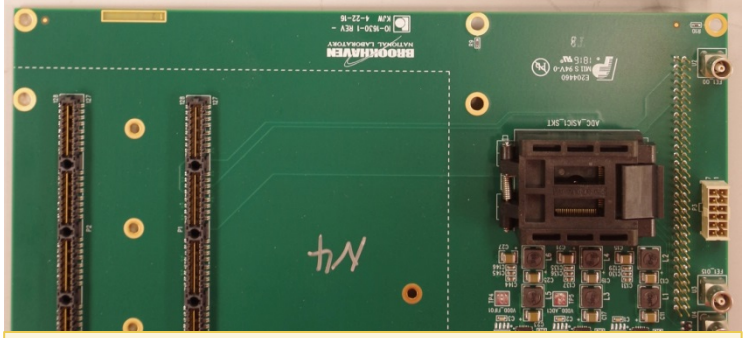
V* ADC ASIC Test Board



Single ADC ASIC Test Board



Single Socket ADC ASIC Test Board – Open Top

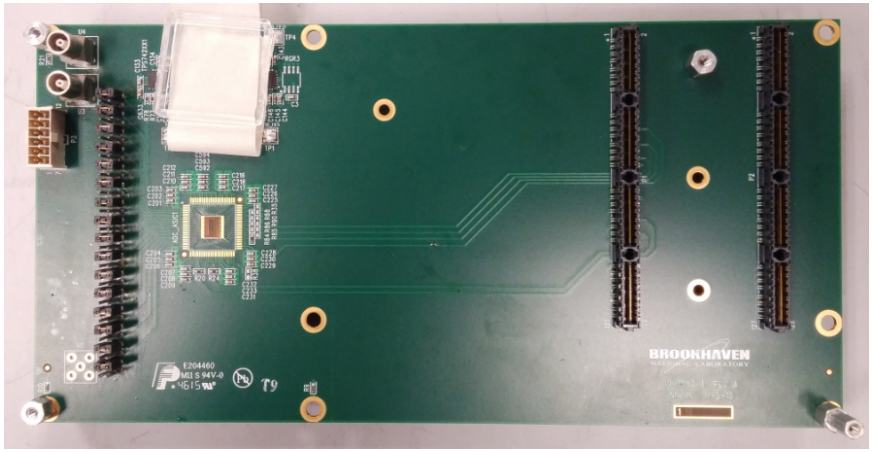


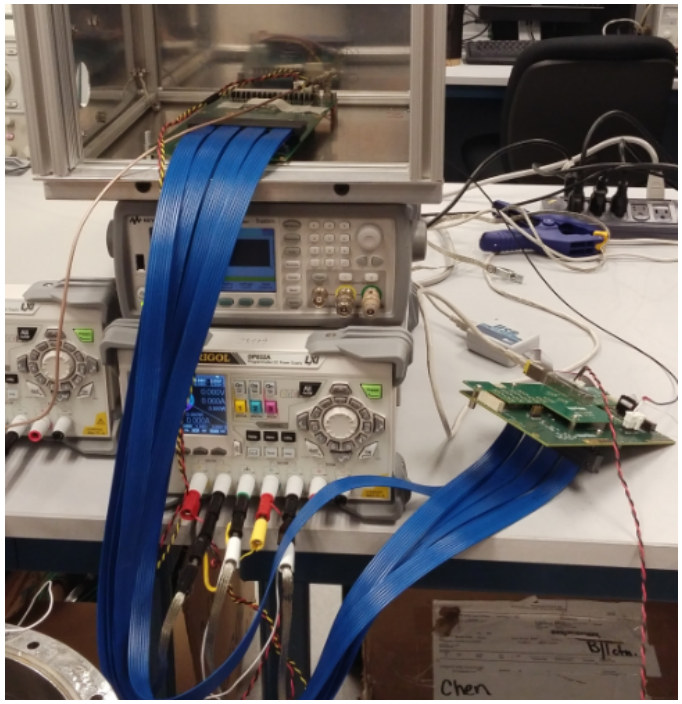
Single Socket ADC ASIC Test Board – Clam Shell

- Single ADC ASIC Test Board
  - Readout, DAQ, control and monitoring is through DUNE 35T FPGA mezzanine
- Three different configurations
  - Chip on board
  - Open top socket
  - Clam shell socket with filter
- Next step
  - Quad socket ADC ASIC test board will be designed for both warm and cold test soon
    - Revised board is compatible with P1 ADC ASIC and V* ADC ASIC

P1 ADC ASIC Die Installed on V* ADC Test Board

- Reuse the test stand for V* ADC test board
- Signal generator (KEYSIGHT 33600A)
  - Two waveforms were used
    - Saw-tooth wave
      - Range is from -0.2V to 1.6V
      - 0.01 Hz
    - DC Source for sweeping each input channel
      - Range : 0.0000 V to 1.60000 V
      - Step = 0.1 mV
- The test is ongoing

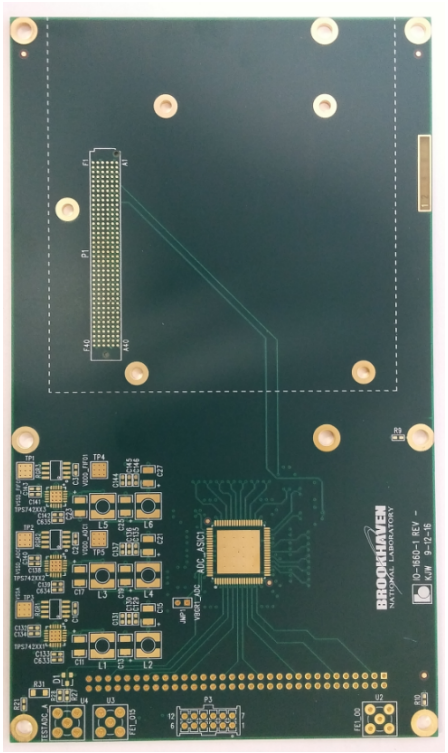




P1 ADC Die Test Stand

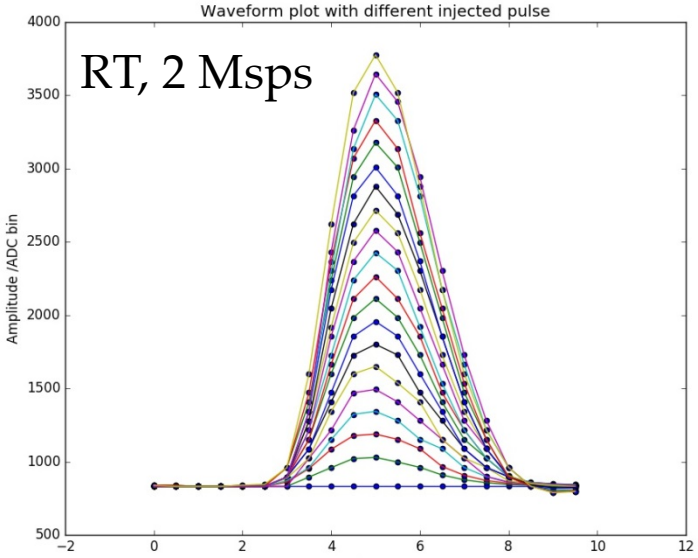
- P1 ADC ASIC with package will arrive soon
- Single P1 ADC ASIC test board with clam-shell socket is ready
- Once the chip arrives, assembly kit for version of chip on board will be delivered to assembly house

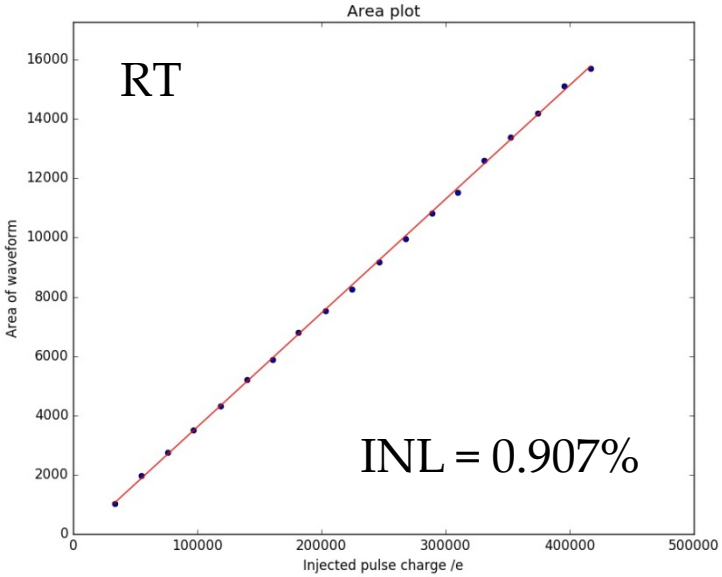
P1 ADC ASIC test board and SBND FM

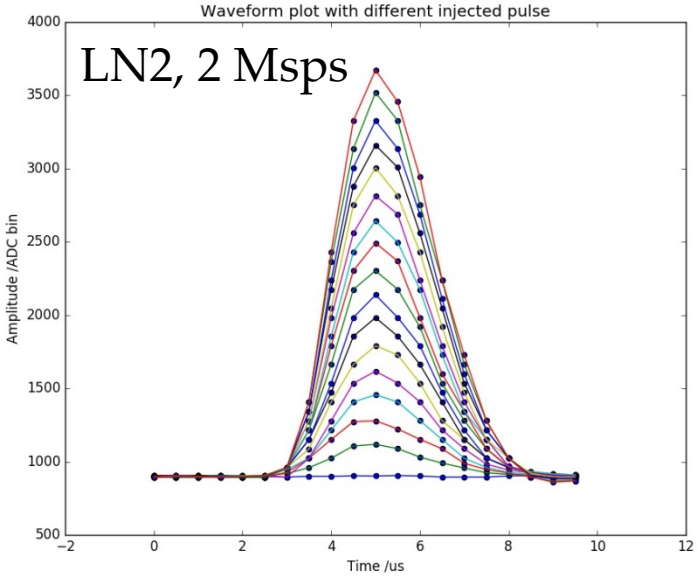


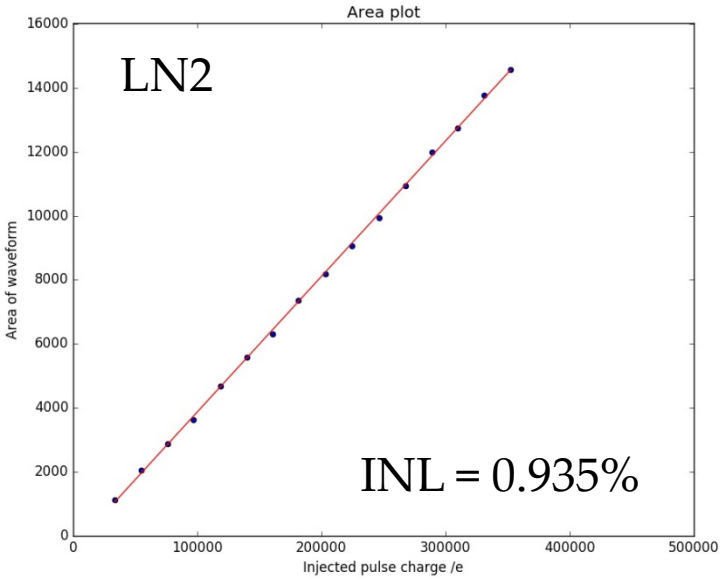
PCB of chip on board
For P1 ADC ASIC

Preliminary Result of P1 ADC die







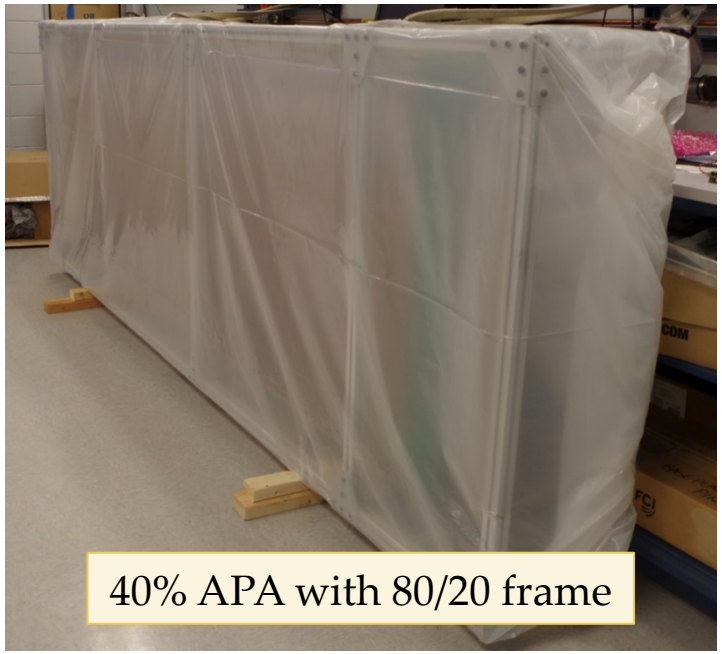


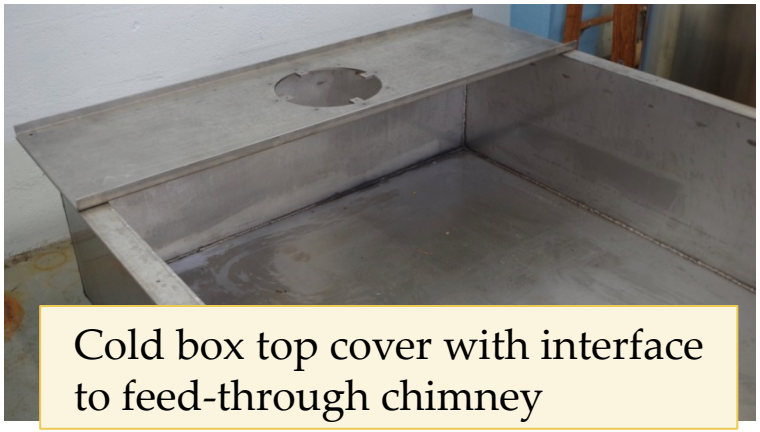
Integration Test Stand

- Integration test stand is an important step to study the detector and readout electronics integration and performance
  - Test stands are being prepared at BNL, Fermilab and CERN with different focus
  - BNL: APA and FEE integration at both RT and LN2
- The TPC APA+Cold Readout+Feed-through+Faraday Cage with Warm Interface and Local Diagnostics should be treated as an integrated whole
  - BNL integration test stand will test the full readout chain from APA to WIB
  - Cold box will house the 40% APA from DUNE prototype, plus cold electronics and cold cable
  - Signal feed-through assembly and warm interface electronics housed in the crate will be installed

Integration Test Stand

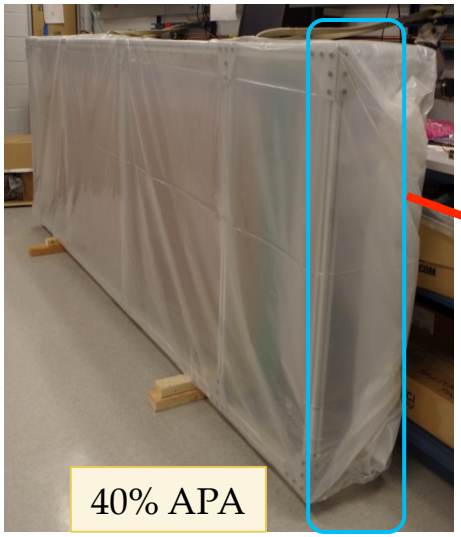

Cold Box

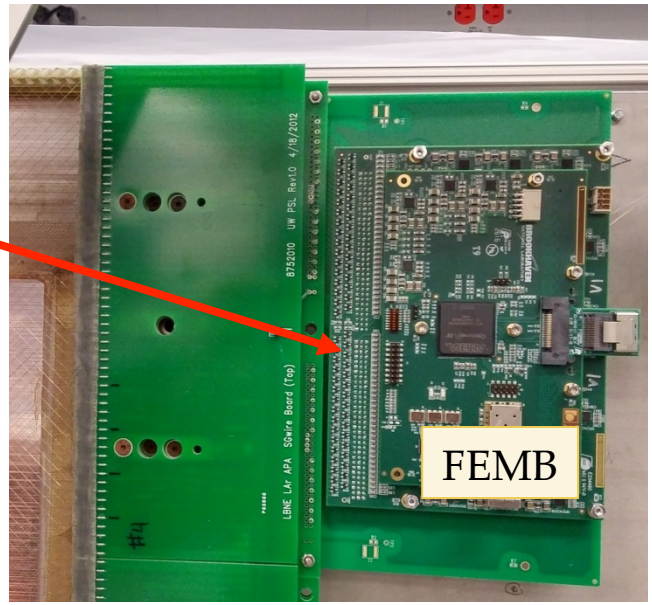

40% APA with 80/20 frame


Cold box top cover with interface to feed-through chimney

- Foam and support installation has been done

Integration Test Stand



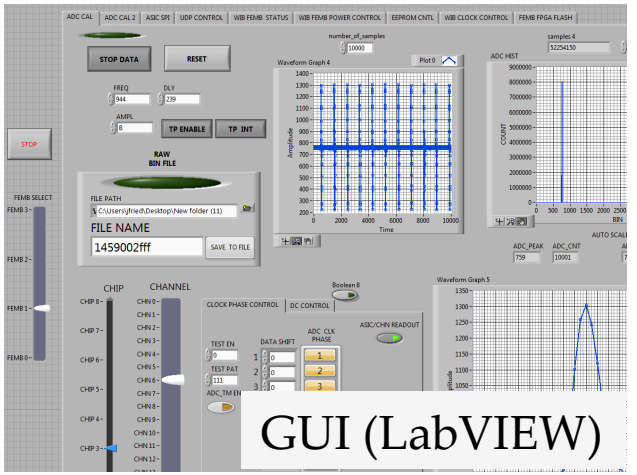


- 8 adapter board had been assembly on the APA
- SBND/ProtoDUNE FEMB will be installed on the adapter board for the integration test

WIB + FEMB is Ready for Integration Test

- Once the flange board arrives, the integration test will start.
  - WIB is able to operate 4 FEMBs now
  - We are working on the python version of DAQ

WIB + FEMB + 7m miniSAS cable + 7m power cables



Summary

- Test stand development and thorough test of cold electronics are important steps to ensure the success of the experiment
- Development of cold electronics test stands are ongoing for both SBND and ProtoDUNE-SP
  - Integration test stand will include active detector as learned from the past experience
  - The experience will be directly applied to the test stand development of the DUNE far detector