Front-End and ADC ASIC Design

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a passion for discovery

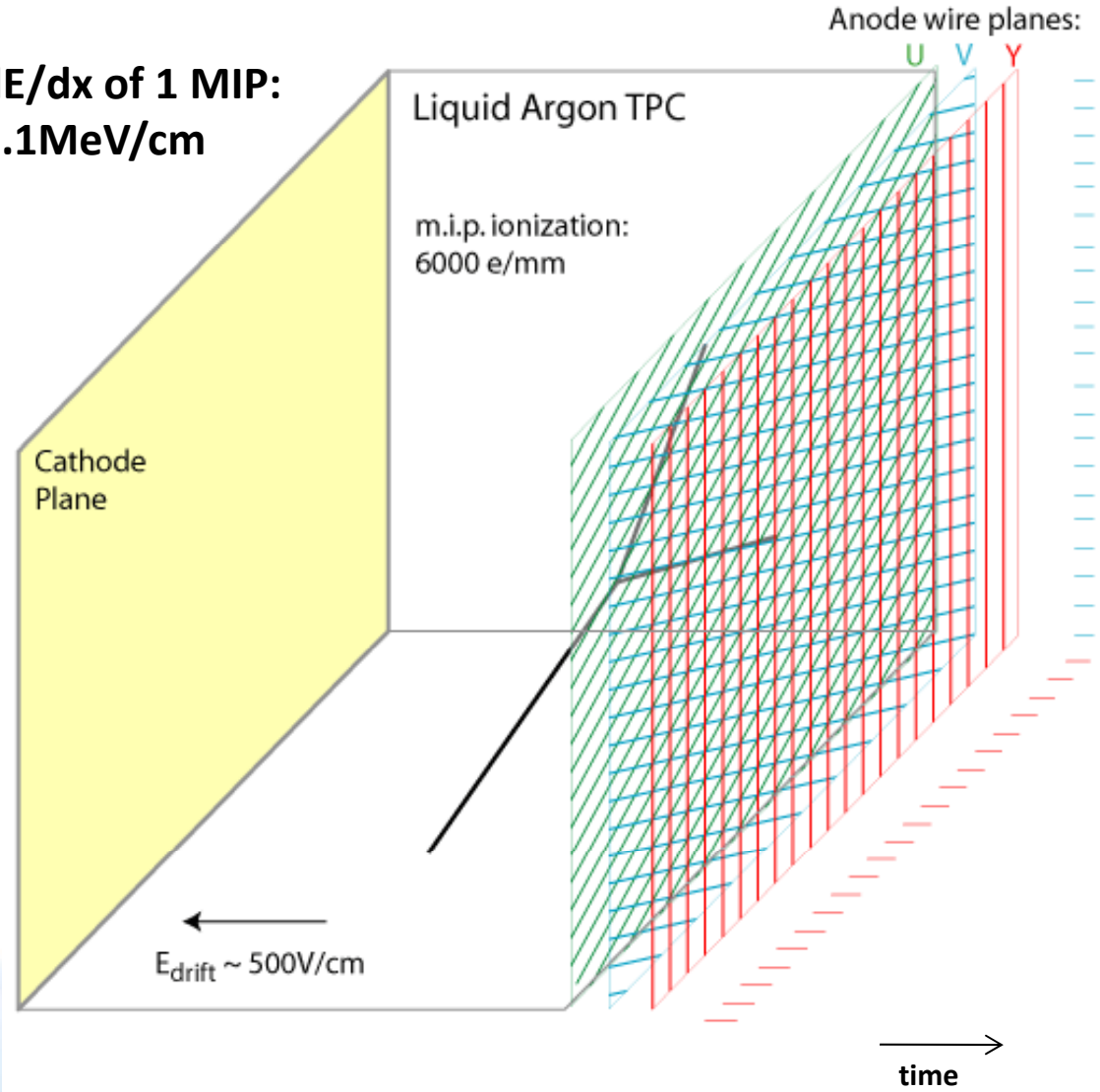
U.S. DEPARTMENT OF ENERGY | Office of Science

Outline

- **Introduction of cold front-end (FE) and ADC ASICs for LAr TPC**
- **CMOS modeling and design for cold electronics**
- **LAr FE ASIC:**
  - Optimizing input MOSFET under power constraint
  - Crosstalk of Adjacent Channels
  - Performance of FE ASIC in MicroBooNE
- **LAr ADC ASIC:**
  - ASIC Feature and operation
  - Current-mode Domino architecture
- **CMOS lifetime study for cold electronics**
  - Basics on hot-carrier effects and lifetime
  - CMOS lifetime in *dc* operation: analog front-end ASICs
  - CMOS lifetime *ac* operation: logic circuits and FPGAs
- **Further R&D for LAr FE and ADC ASICs**

ASIC Specifications from LArTPC:

dE/dx of 1 MIP: 2.1MeV/cm

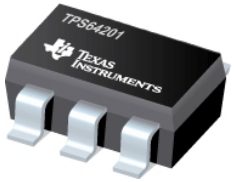


First proposed by C. Rubbia, 1977

- Sense (anode) wires (up to ~ 10m long):
  - ~14-31 kwires/kton
    - up to 200 pF/wire
    - collecting (Y)
    - non-collecting (U,V)
- charge sensitivity
  - range ~200 fC
  - ENC < 1,000 e^-

- sample/buffer events
  - ADC 10-12-bit, 1-2 MS/s
- digital multiplexing
  - 128:4
- power constraint
  - ~ 20 mW /wire (FE+ADc+FPGA)
- operation in LAr
  - > 30 years

Cold Electronics



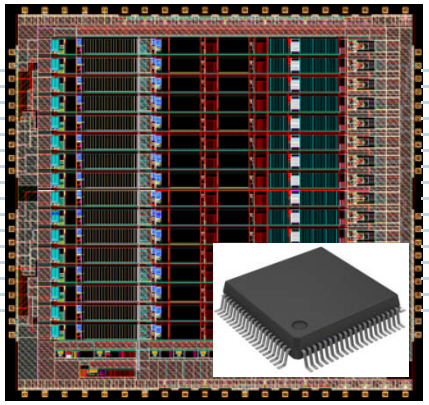
voltage regulation (COTS)
(< 100mV dropout)

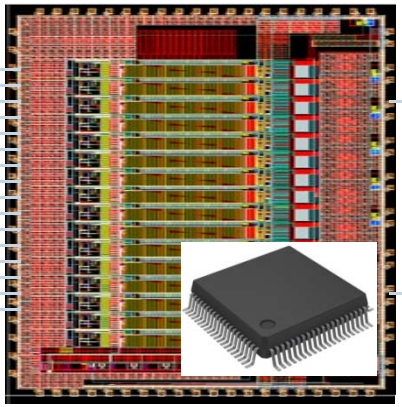
front-end ASIC
~ 5mW/ch.

ADC ASIC
~ 5mW/ch.

FPGA (COTS)
~ 8mW/ch.

sensing wires



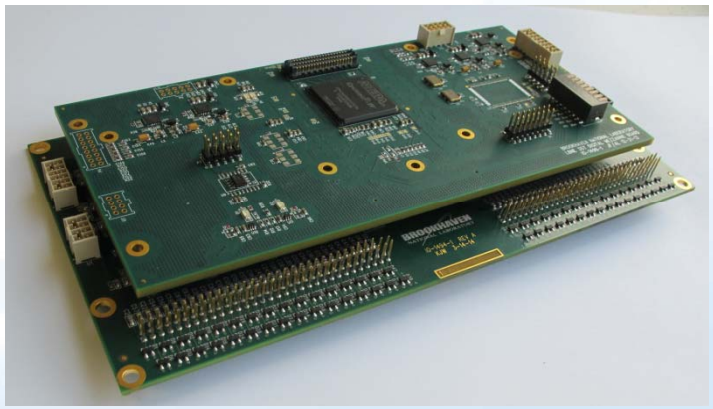


overall 128:4 multiplexing

8 x

1 x

Parallel work
- CMOS lifetime studies



front-end cold module
serving 128 wires
~ 2.4 W

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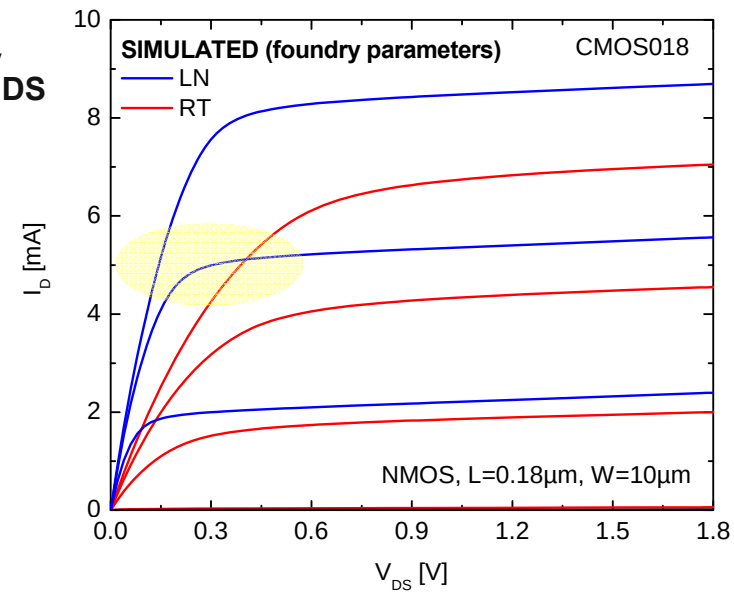
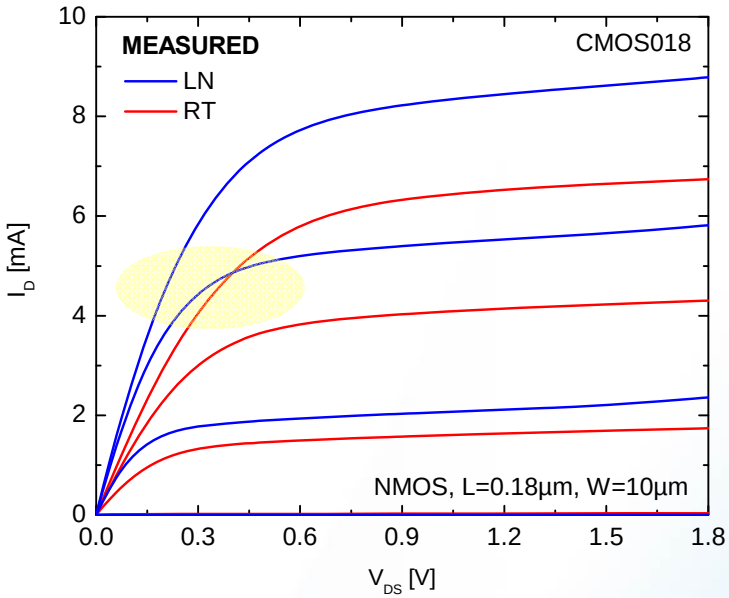
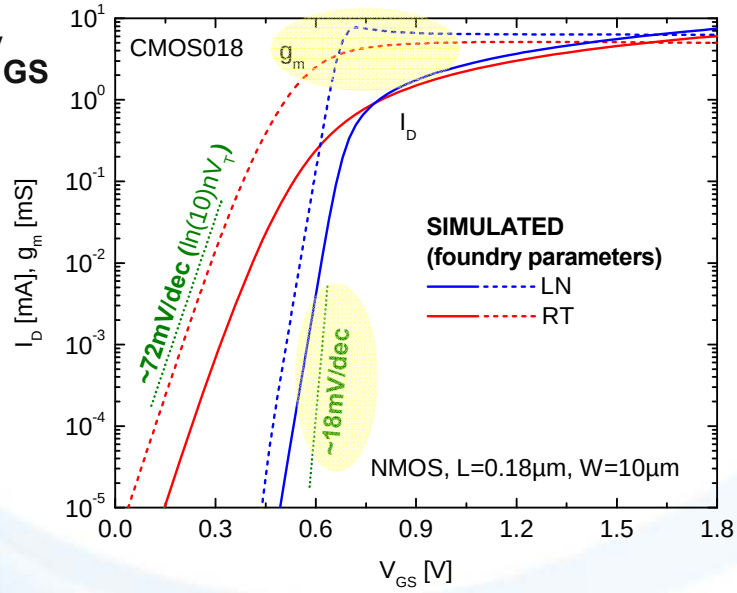
CMOS static characteristics vs. T -- I_D/V_{DS} & I_D/V_{GS}

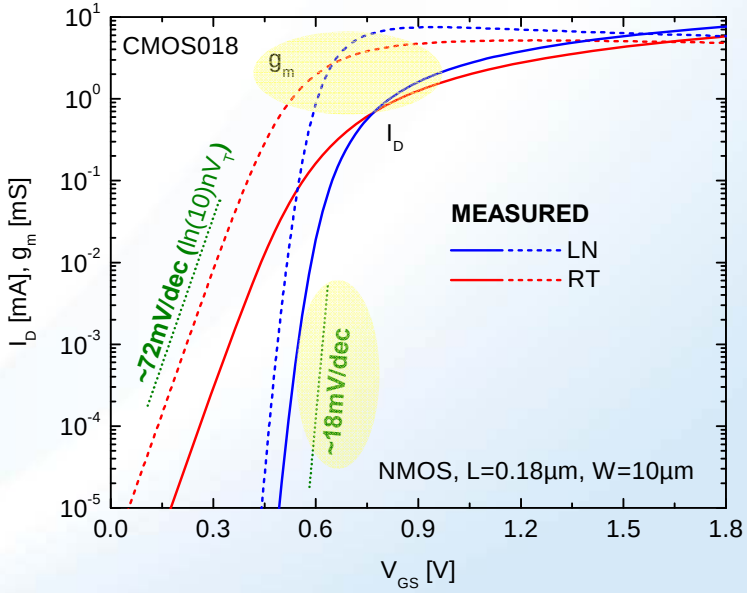
I_D vs V_{DS}





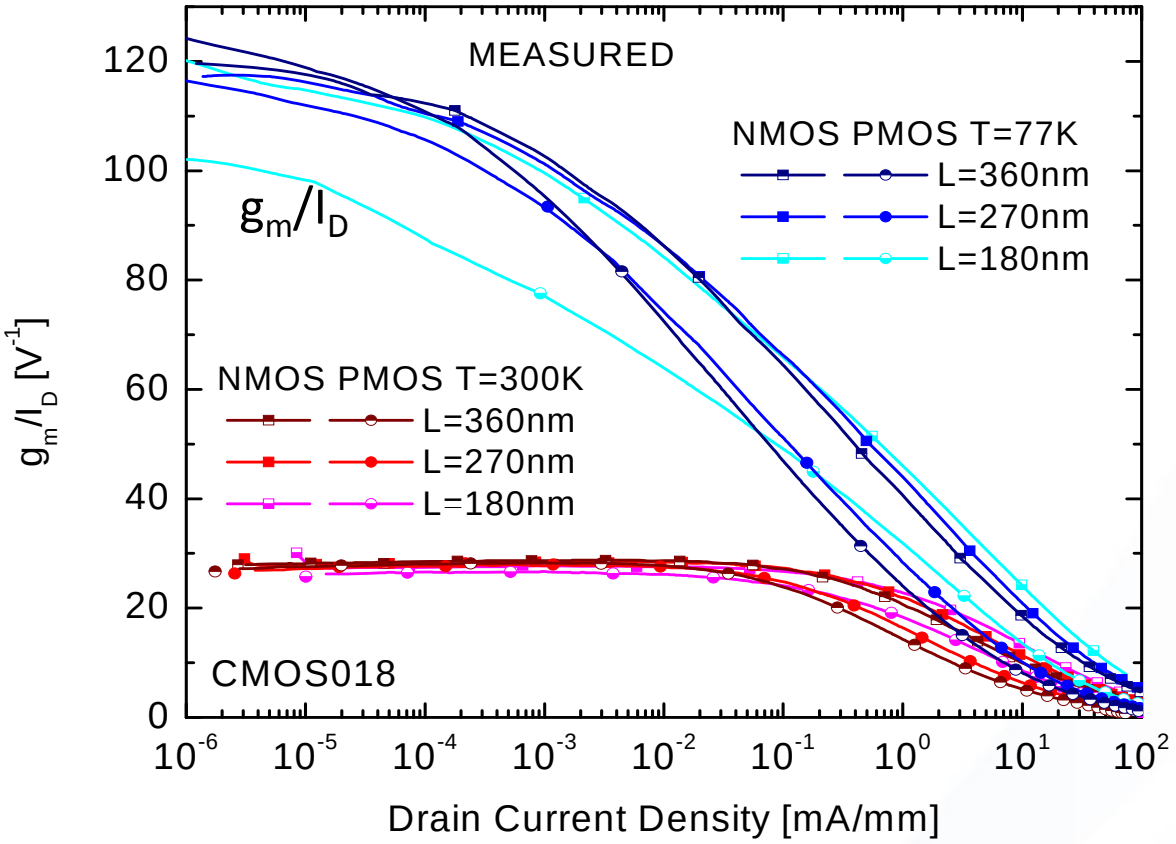
I_D vs V_{GS}





Some differences in saturation voltage, sub-threshold slope, transconductance

CMOS static characteristics vs. T -- g_m/I_D

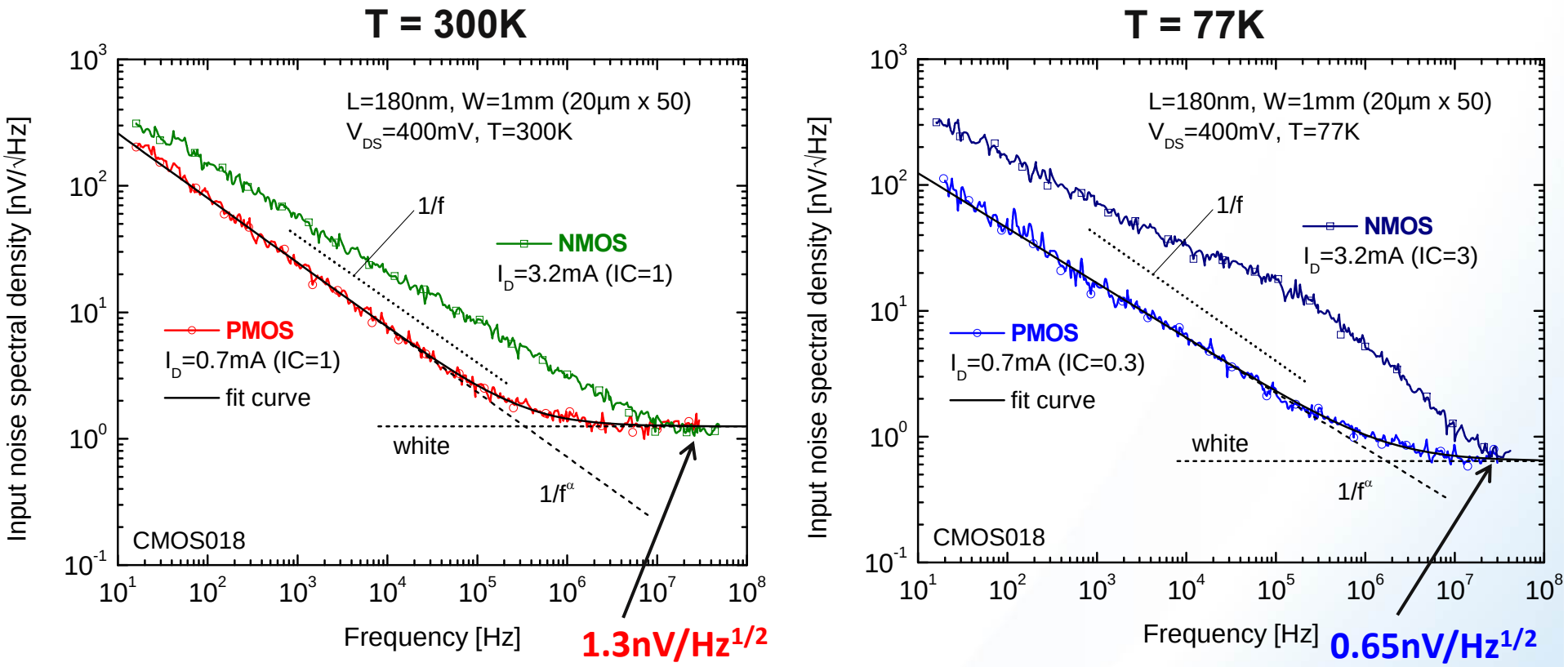


Transconductance/ /drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

At 77-89K, charge carrier ***mobility*** in silicon *increases*, ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher*** ***gain***, ***higher*** ***g_m /I***, ***higher*** ***speed*** and ***lower*** ***noise***.

CMOS Noise Spectral Density *vs.* T



- **White noise at 77K is a factor of 2 lower than at 300K**
- **PMOS**
  - **1/f noise amplitude at 77K is a factor of 2 lower than at 300K**
- **NMOS**
  - **comparable 1/f noise amplitude at 300 K and 77K**
  - **Lorentzian packet at 77K**

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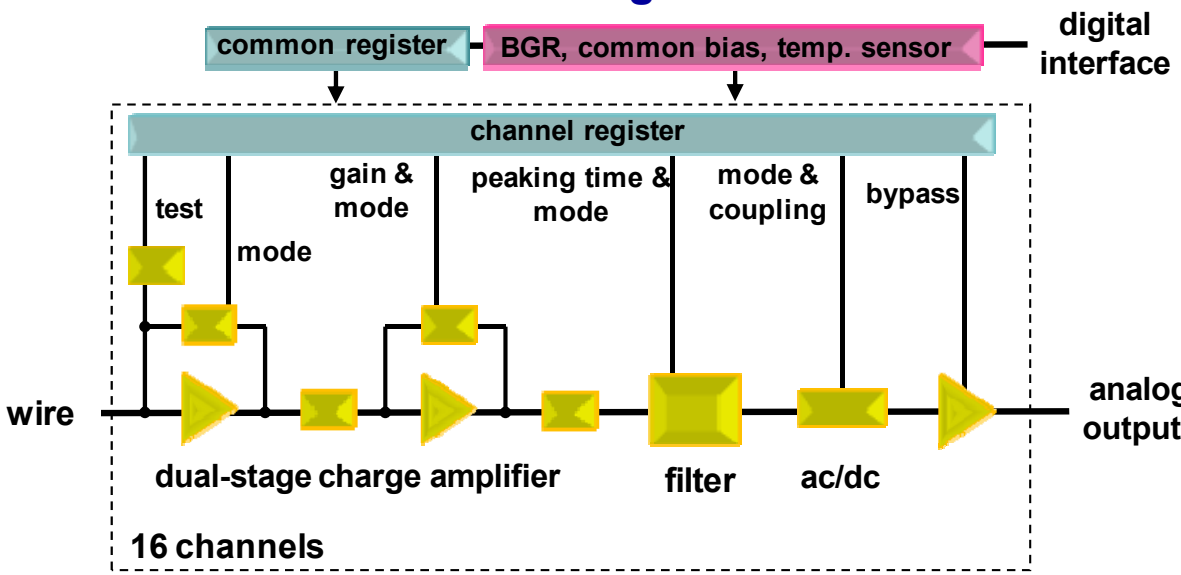
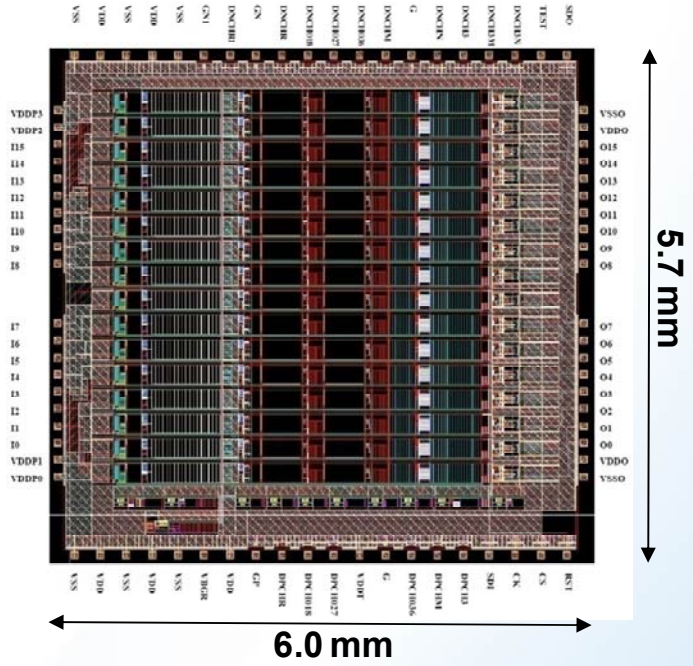
Analog Front-End ASIC

Block Diagram

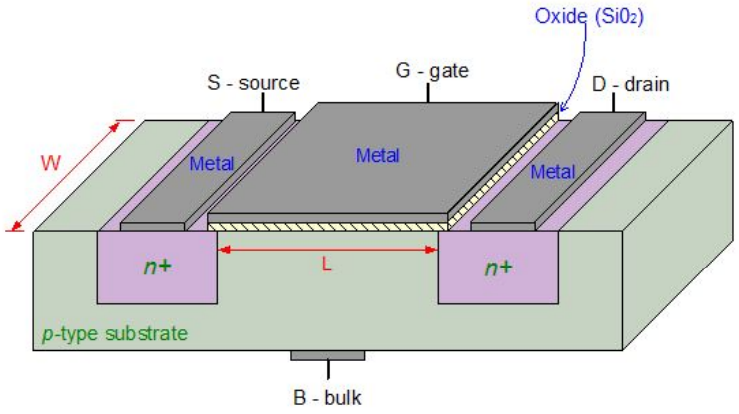




- 16 channels
- charge amplifier, high-order anti-aliasing filter
- programmable gain: 4.7, 7.8, 14, 25 mV/fC
  (charge 55, 100, 180, 300 fC)
  programmable filter
  (peaking time 0.5, 1, 2, 3 μs)
- programmable collection/non-collection mode (baseline 200, 800 mV)
- programmable dc/ac coupling (100μs)

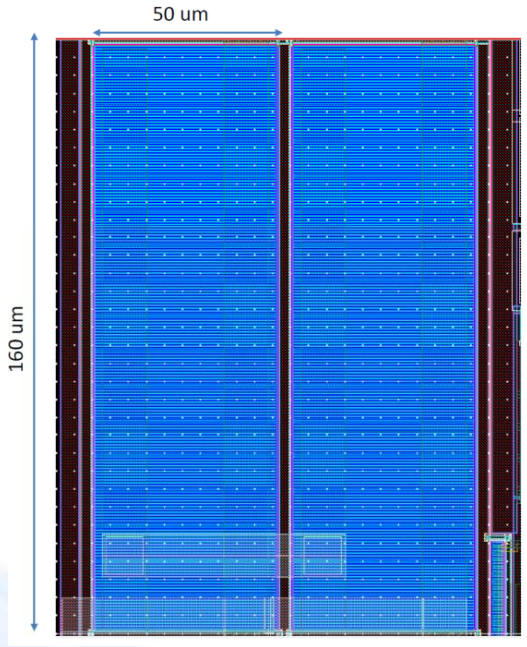
- band-gap referenced biasing
- temperature sensor (~ 3mV/° C)
- 136 registers with digital interface
- 5.5 mW/channel (input MOSFET 3.9 mW)
- single MOSFET test structures
- ~ 15,000 MOSFETs
- designed for room and cryogenic operation
- technology CMOS 0.18 μm, 1.8 V

Charge Sensor-Transistor Capacitance Mismatch under power constraint



$$ENC = \frac{e_n\left(C_d + C_{gs}\right)}{\tau_p^{1/2}} \qquad e_n^2 = 4kT\frac{\gamma}{g_m} \qquad \left[V^2/Hz\right]$$

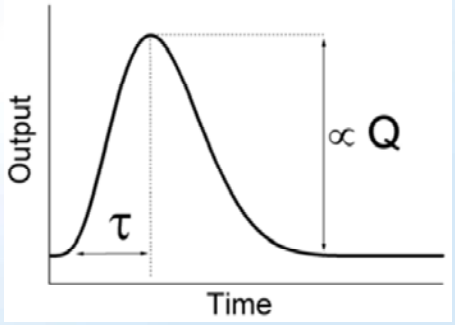
For a very large low noise PMOS transistor W~10mm, L~250nm, W/L~4x10^4, C_{gs}~10pF. Area in 180 nm process: 160µm x 50µm=8,000µm², equivalent to ~ 10^3 small transistors.



The transistor can not match a large (nanofarad) sensor capacitance and we are left with linear dependence of ENC on detector capacitance:

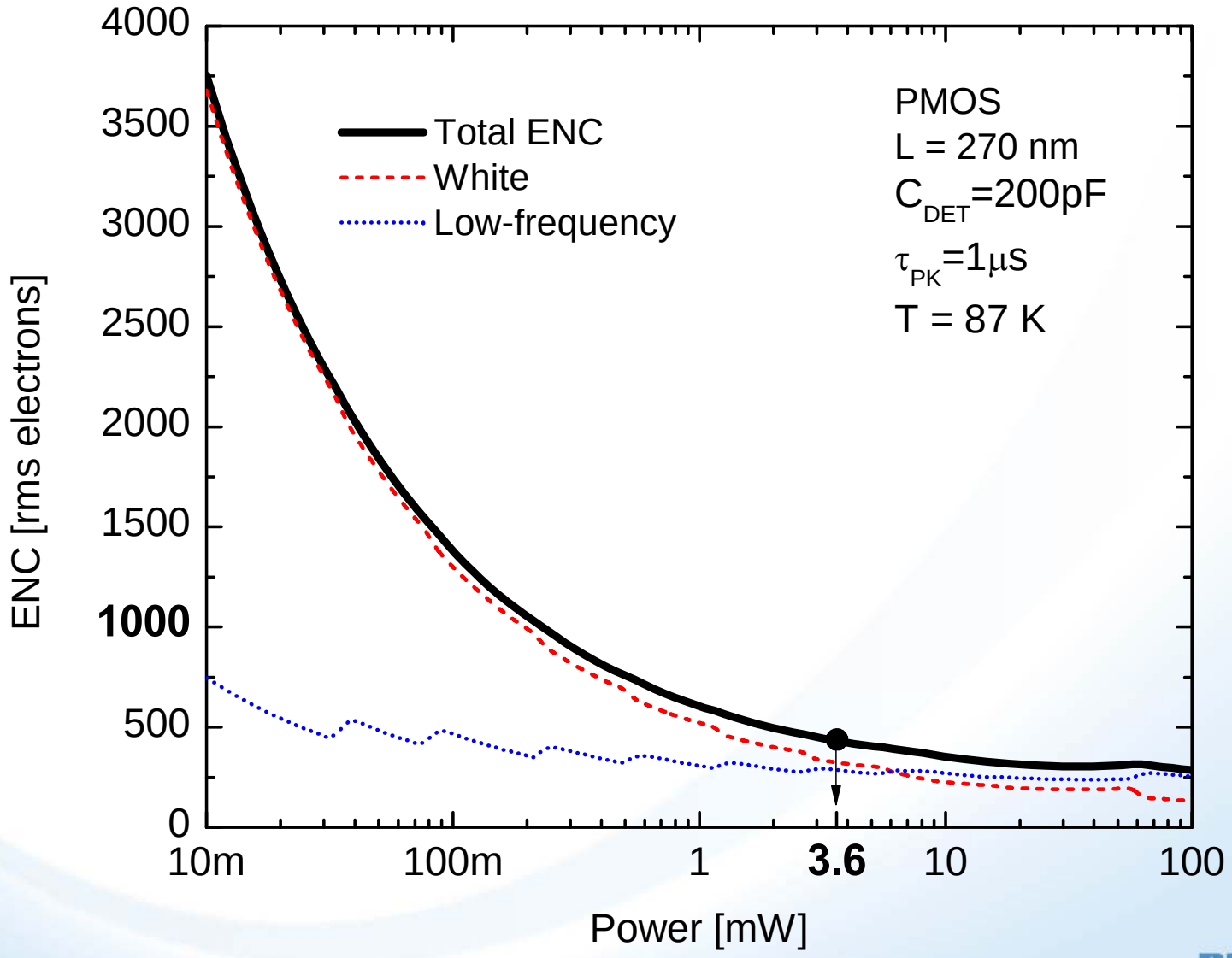
For low power, CMOS in weak inversion: $C_{gs\,opt} \le (1/3)C_{gd}$

$$ENC \approx \frac{e_n C_{\det}}{\tau_p^{1/2}}$$



Layout of Input PMOS in LAr FE ASIC

ENC vs. Power in the Input Cascode



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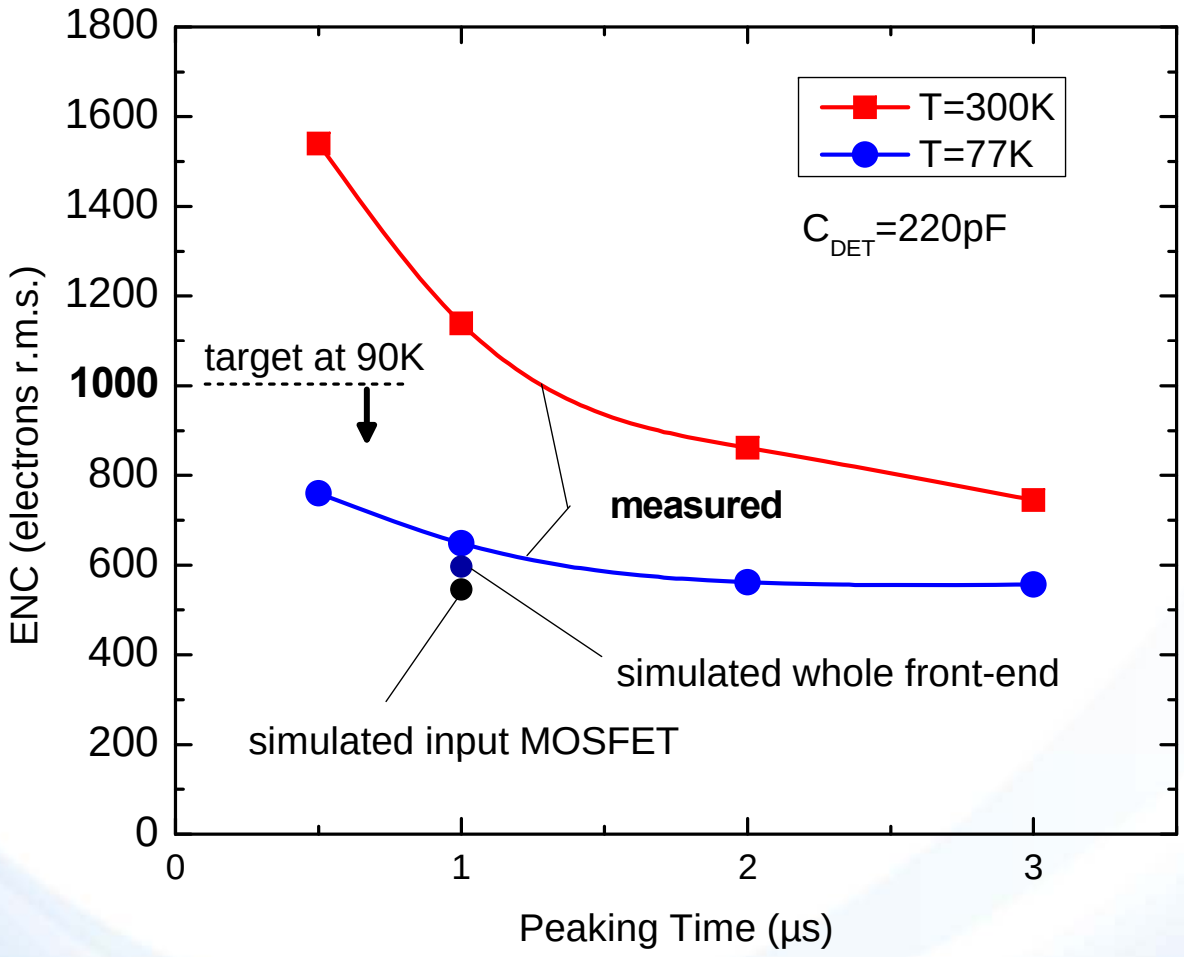
ENC in LArASIC *vs.* peaking time of the anti-aliasing filter at 300K and 90K

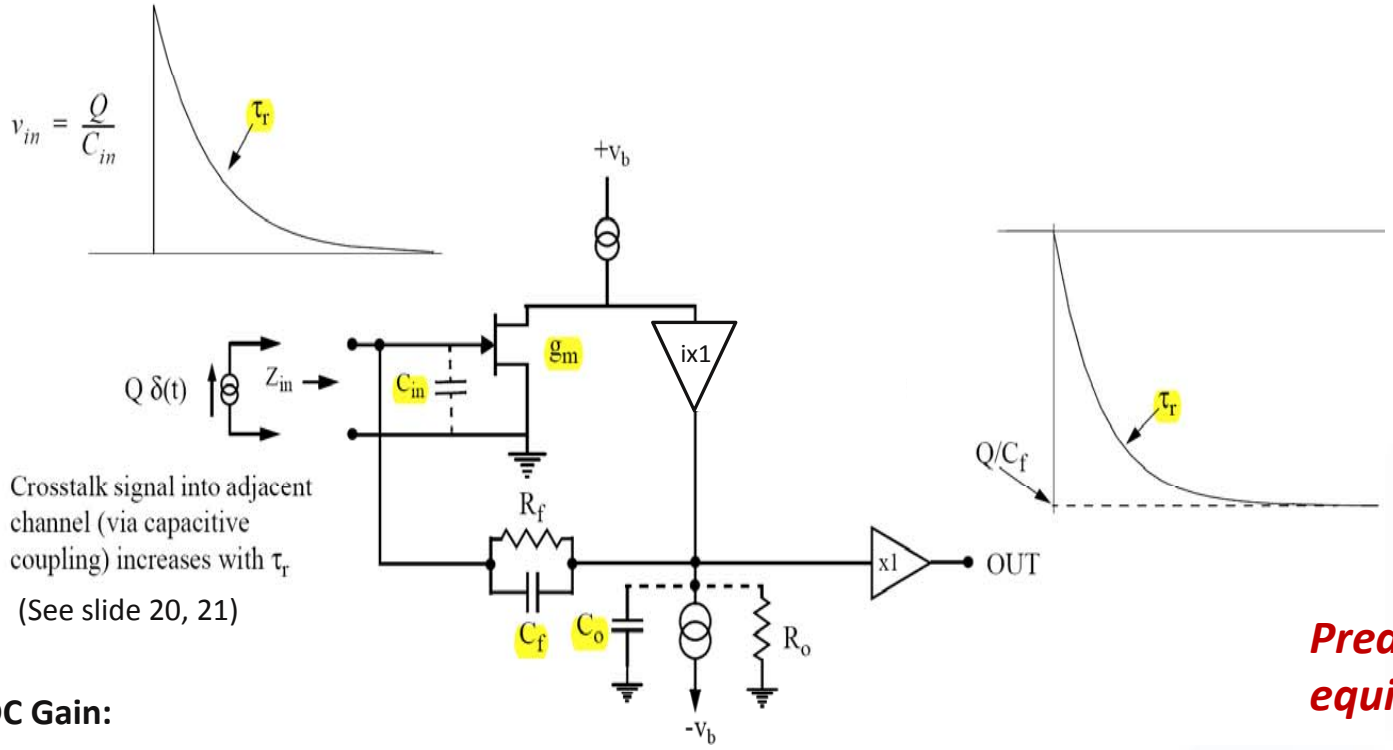


- **White series noise which is dominant at short peaking times *decreases* the most with temperature.**
- **The remaining noise is *dominated by 1/f* noise, which is independent of the peaking time.**

Submersion in Liquid Nitrogen (77K)

Crosstalk Study: Basic Feedback Preamplifier Configuration

Note: feedback function *per se* does not affect ENC (feedback components may add noise)



Crosstalk signal into adjacent channel (via capacitive coupling) increases with τ_r

(See slide 20, 21)

DC Gain:

$$G_o = g_m R_o$$

Gain-Bandwidth:

$$\omega_h = g_m/C_o \quad \Rightarrow$$

Input resistance:

$$R_{in} = \frac{1}{\omega_h C_f} = \frac{C_o}{g_m C_f}$$

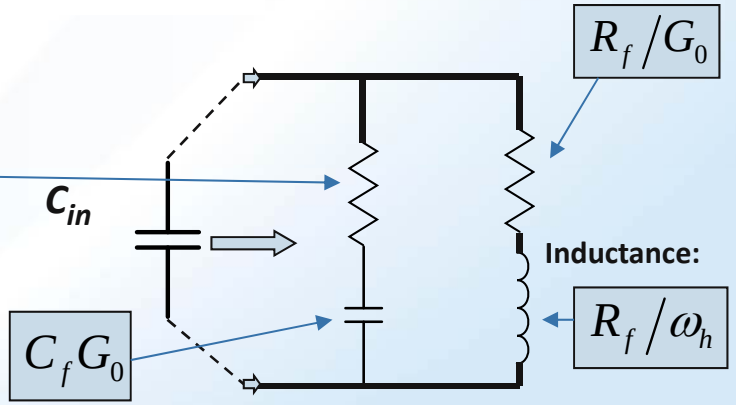
1st pole:

$$\omega_L = \frac{1}{C_o R_o} \quad \Rightarrow$$

Rise time constant:

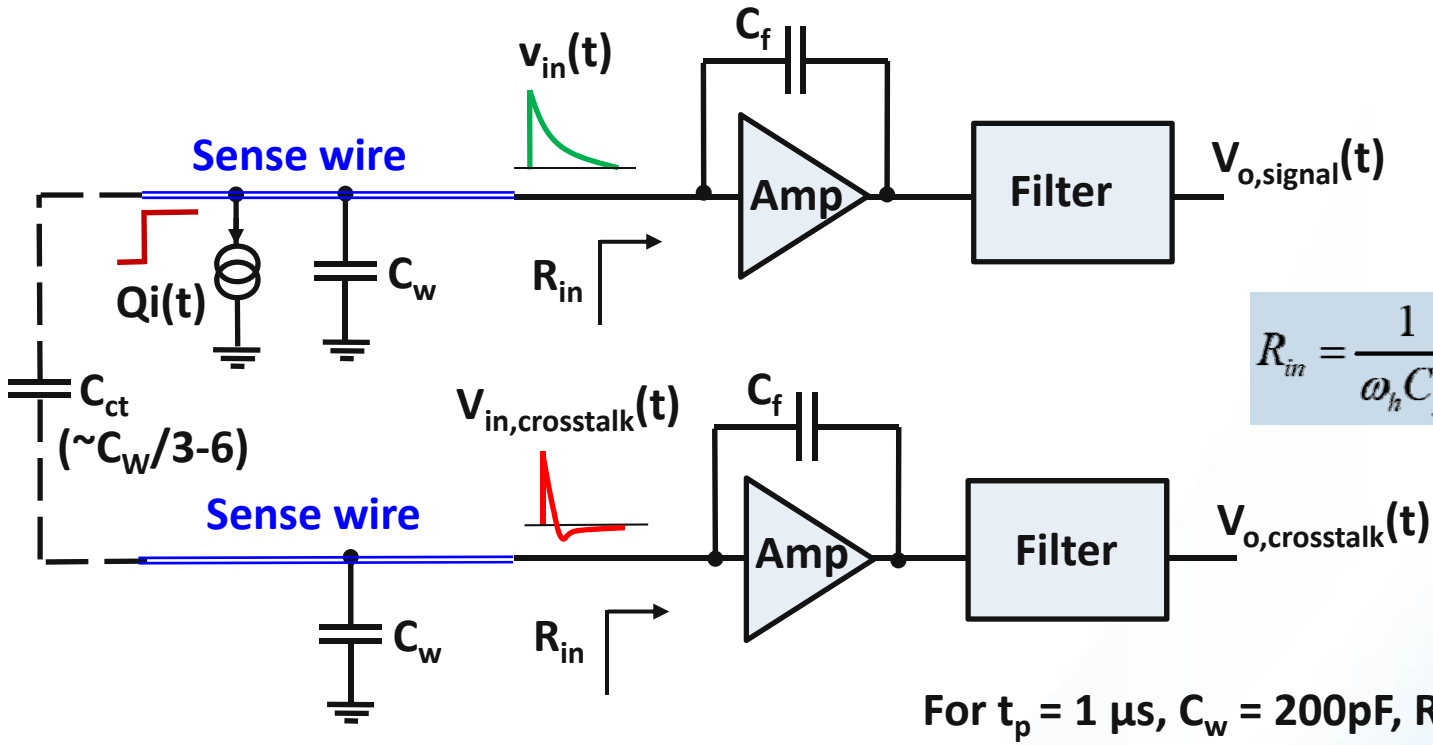
$$\tau_r = C_{in} R_{in} = \frac{C_{in}}{C_f \omega_h} = \frac{1}{g_m} \cdot \frac{C_{in} C_0}{C_f}$$

Preamp input equivalent circuit



A periodic response for $R_f \geq 2 \frac{1}{\omega_h C_f} \cdot \frac{C_{in}}{C_f}$

Crosstalk of Two Adjacent Channels in LAr TPC



$$R_{in} = \frac{1}{\omega_h C_f} = \frac{C_o}{g_m C_f}$$

For t_p = 1 µs, C_w = 200pF, R_{in} = 50 Ω

$$crosstalk \quad ratio = \frac{crosstalk \quad peak}{signal \quad peak}$$

$$\sim \frac{3}{2}\frac{C_{ct}R_{in}}{t_p}$$

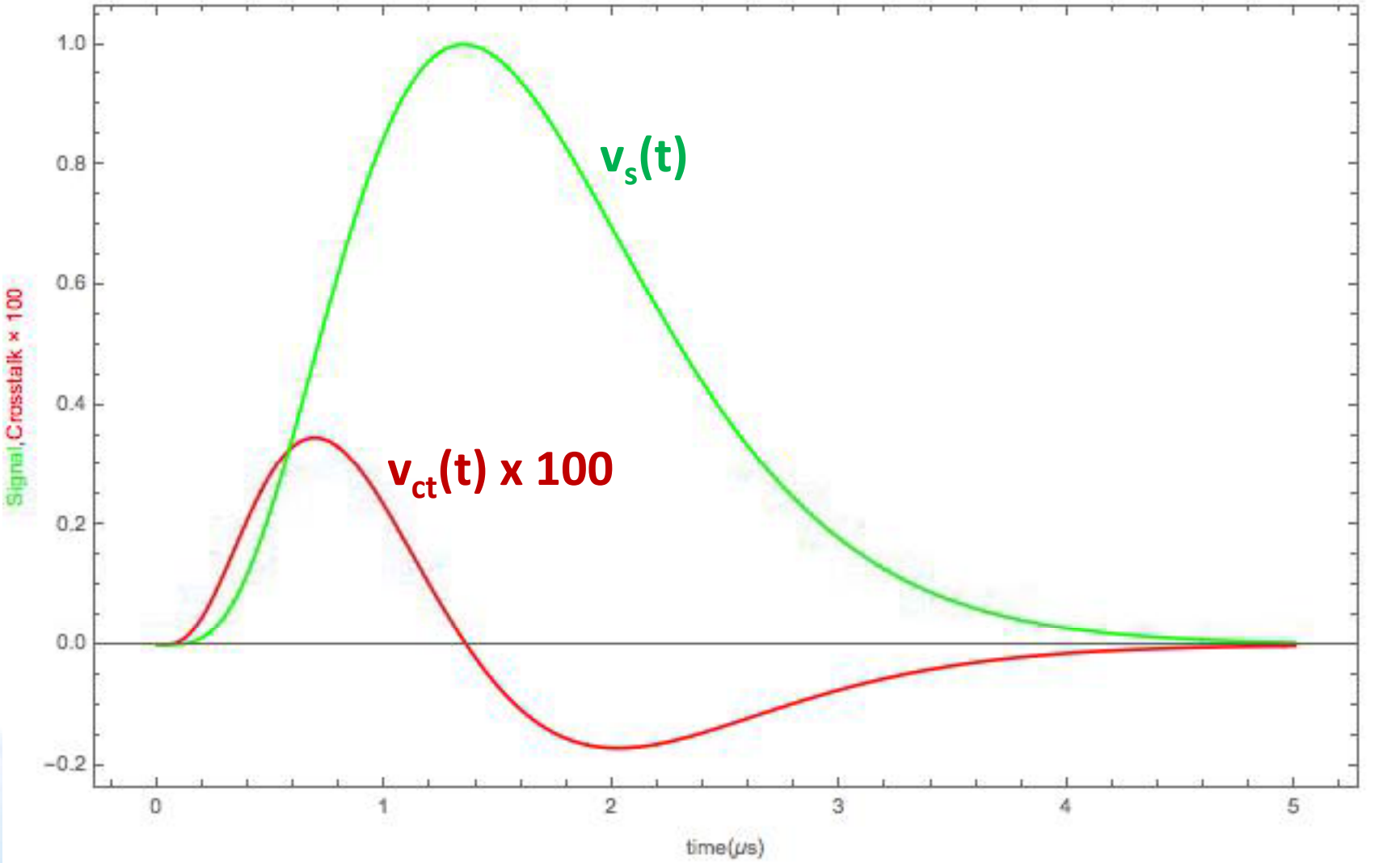
C_{ct}	crosstalk ratio
30 pF	0.225%
40 pF	0.3%
50 pF	0.375%
60 pF	0.45%

Notice that crosstalk decrease with longer peaking time!

FE Output Signal vs. Crosstalk x 100

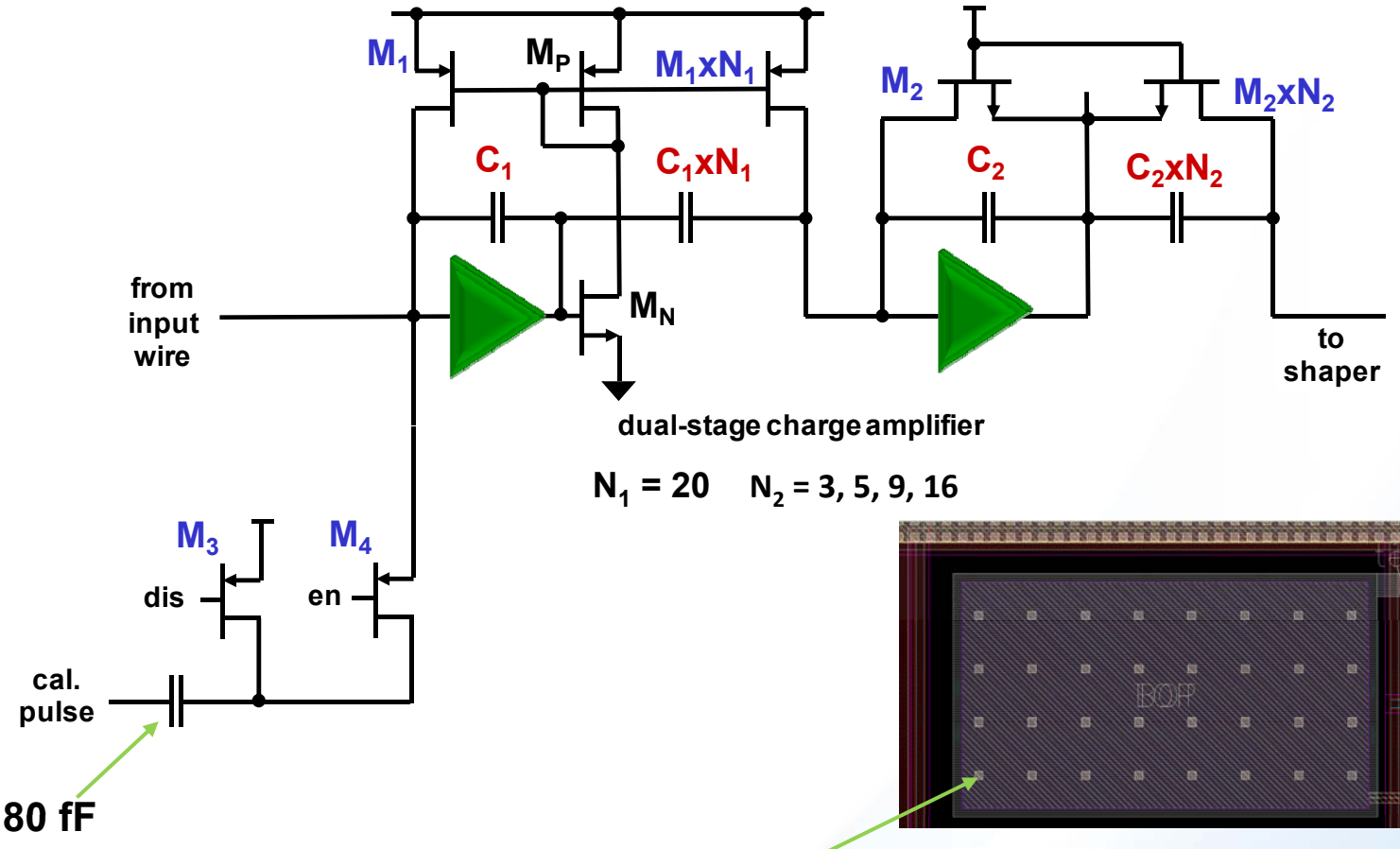
For t_p = 1 µs, C_w = 200 pF, C_{ct} = 50 pF, R_{in} = 50 Ω

$$crosstalk \quad ratio \sim \frac{3}{2}\frac{C_{ct}R_{in}}{t_p}$$



Courtesy of Sergio Rescia

Calibration Scheme



$C_{INJ} \approx 180$ fF

Integrated injection capacitance (10 x 18 μm²)

Measured with high-precision external capacitance

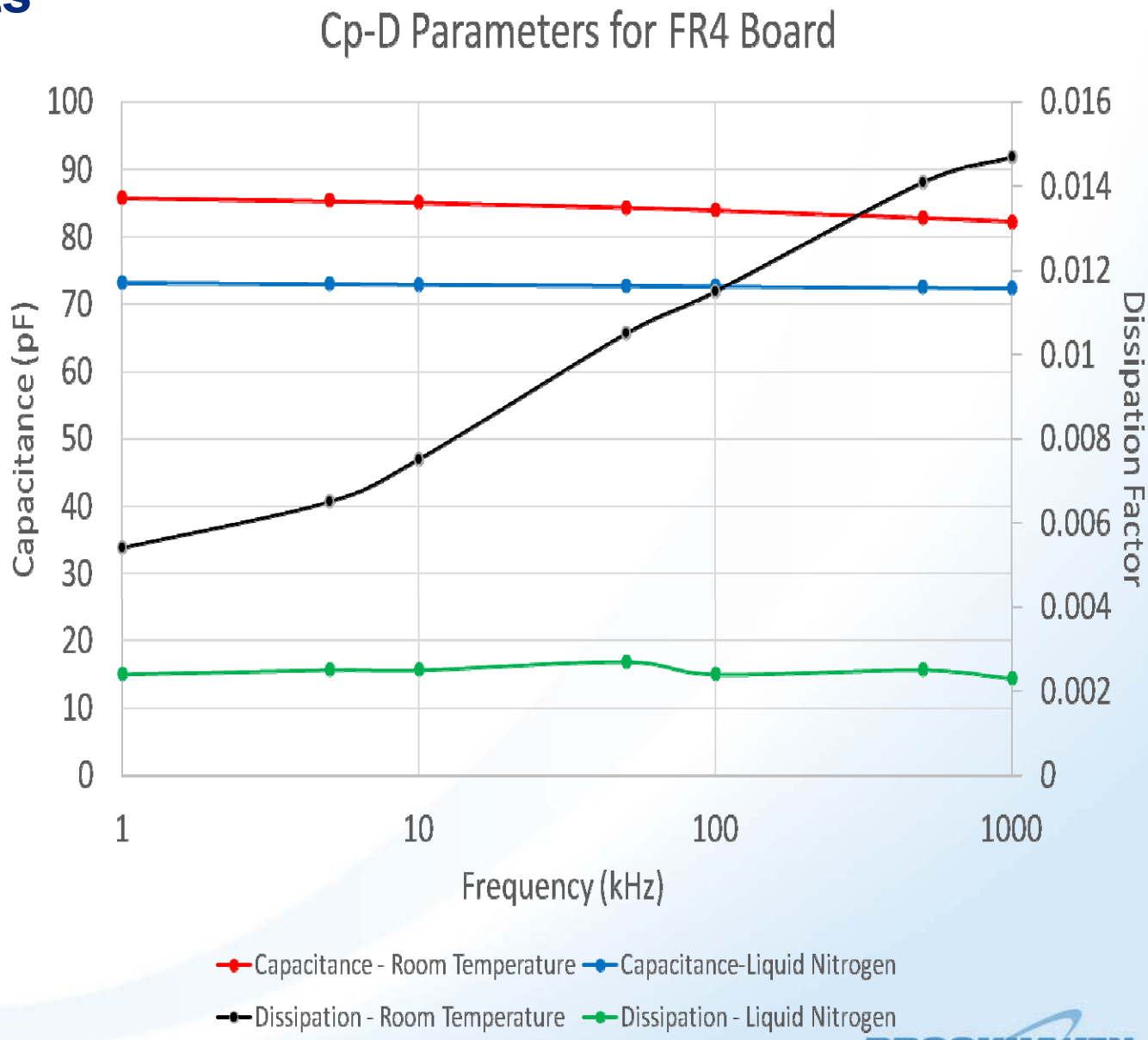
$$C_{INJ} \approx \begin{cases} 184\ fF\ \ at\ \ 300K \\ 183\ fF\ \ at\ \ 77K \end{cases}$$

Integrated pulse generators on ASICs

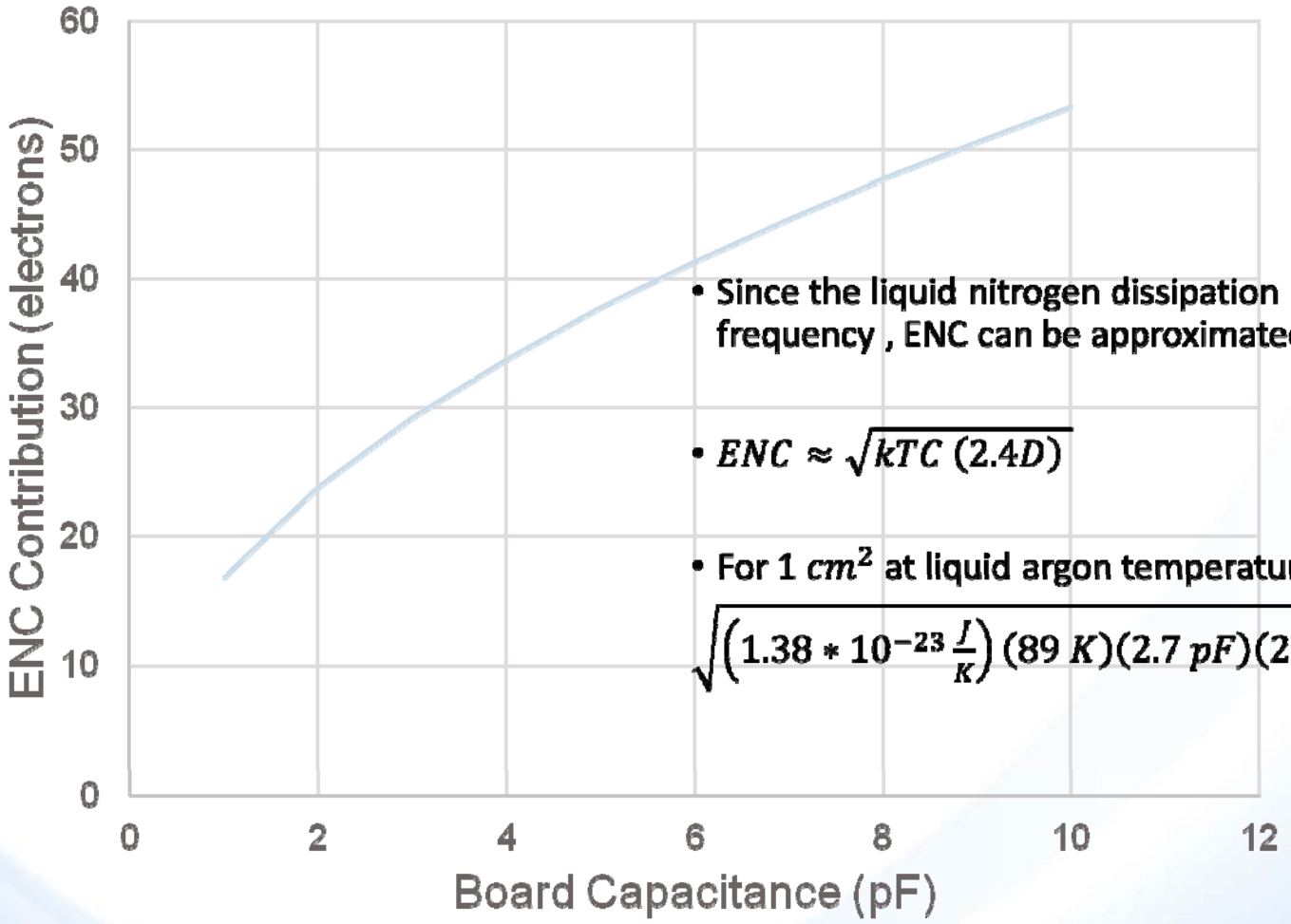
⟹ ***Charge sensitivity calibration of entire TPC during assembly, cooling and operation***

Noise Contribution from Noisy Dielectric of FR4 Board --Testing Results

- Dissipation Factor D remained independent of frequency between 1kHz-1MHz while submerged in liquid nitrogen.



ENC Contribution vs. Board Capacitance at LAr



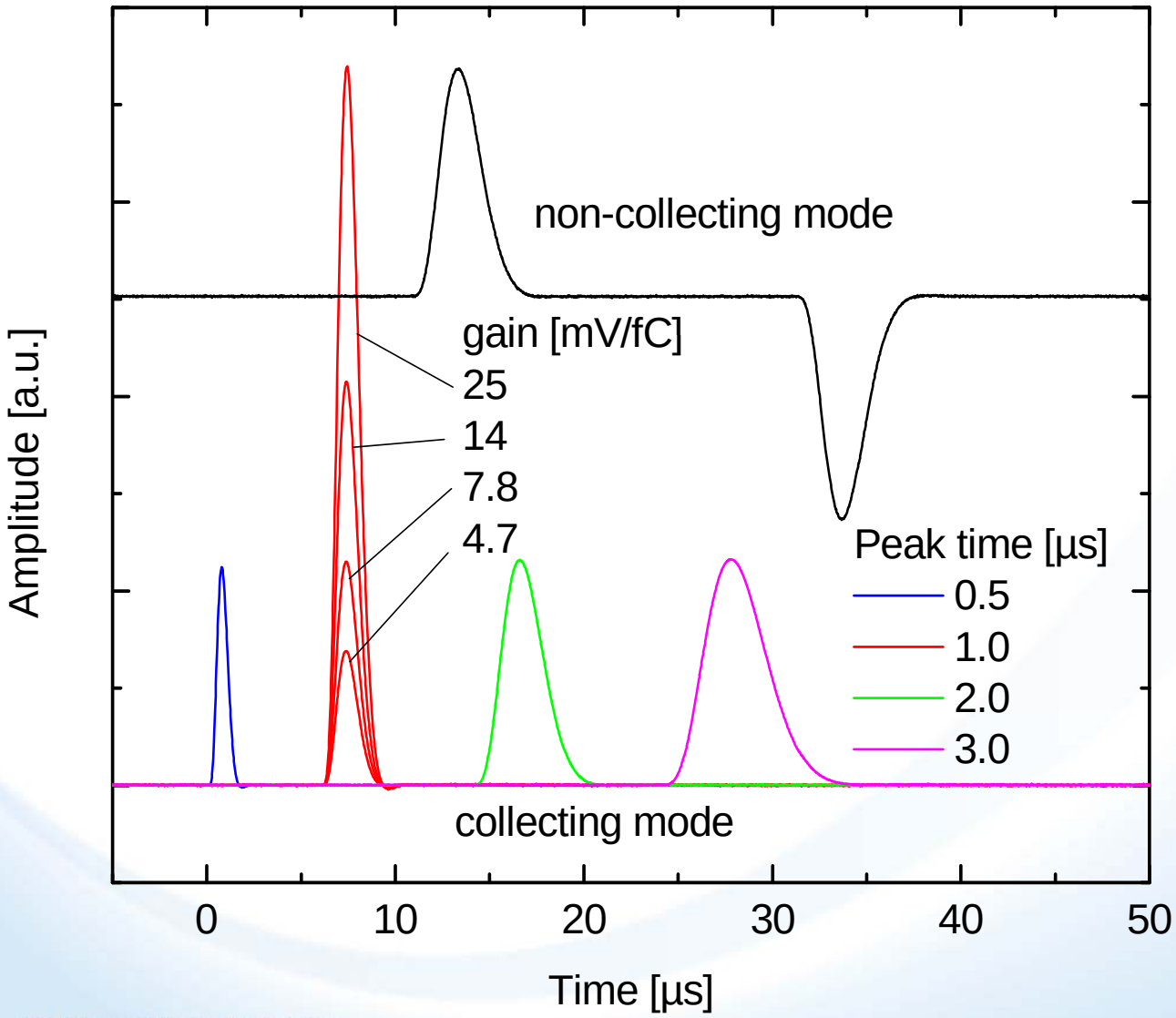
- Since the liquid nitrogen dissipation factor does not depend on frequency , ENC can be approximated by:
- $ENC \approx \sqrt{kTC\ (2.4D)}$
- For 1 cm^2 at liquid argon temperatures:

$$\sqrt{\left(1.38 * 10^{-23}\frac{J}{K}\right)(89\ K)(2.7\ pF)(2.4\ * 0.00247)} = 28 \text{ electrons}$$

On-board trace capacitance from sensing wire to FE ASIC is about 10~20 pF

=> ENC contribution: 60~70 electrons

Signal Measurements: programmable gain, peak time and baseline



Bandgap Reference:

$$V_{BGR} \approx \begin{cases} 1.185\ V & \text{at } 300\ ^{\circ}K \\ 1.164\ V & \text{at } 77\ ^{\circ}K \end{cases}$$

variation ≈ 1.8 %

Temperature Sensor:

$$V_{TMP} \approx \begin{cases} 867.0\ mV & \text{at } 300\ ^{\circ}K \\ 259.3\ mV & \text{at } 77\ ^{\circ}K \end{cases}$$

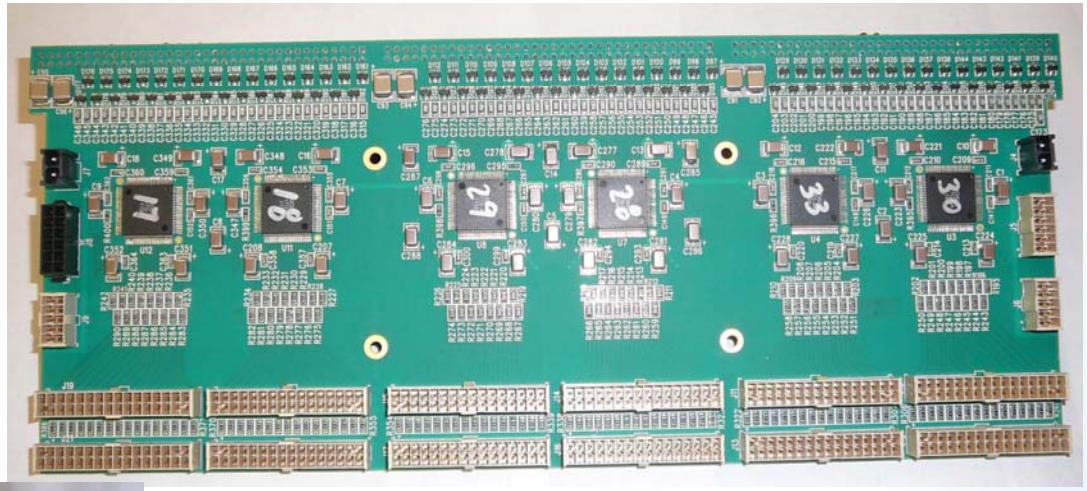
~ 2.86 mV / ° K

Programmable gain, peaking time and baseline

Maximum charge
55, 100, 180, 300 fC

FE ASICs in MicroBooNE

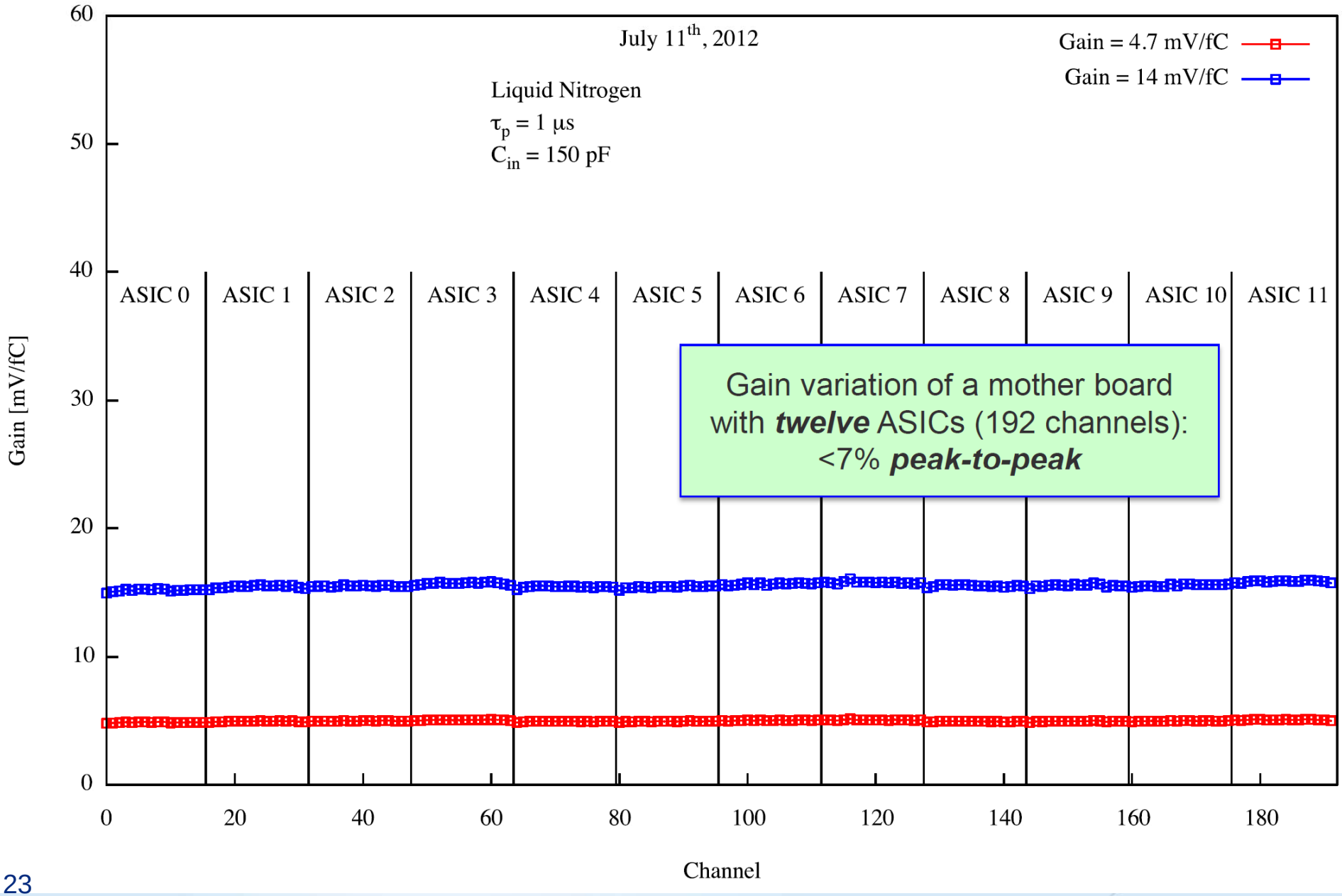
MicroBooNE cold mother board with 12 analog FE ASICs (on top and bottom planes, a total of 192 channels)



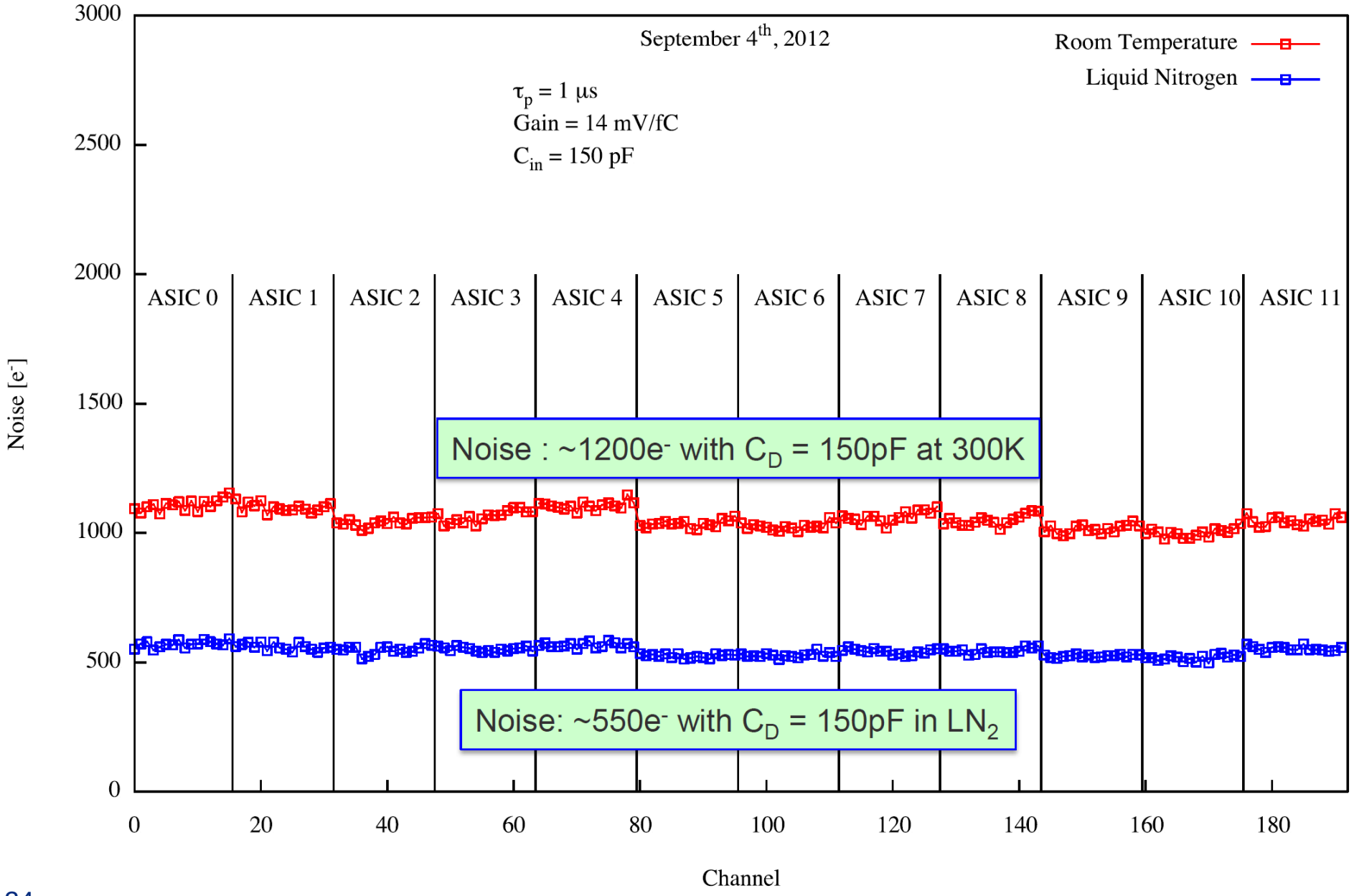
50 cold mother boards (8,256 channels) are installed on MicroBooNE TPC

Courtesy of Hucheng Chen

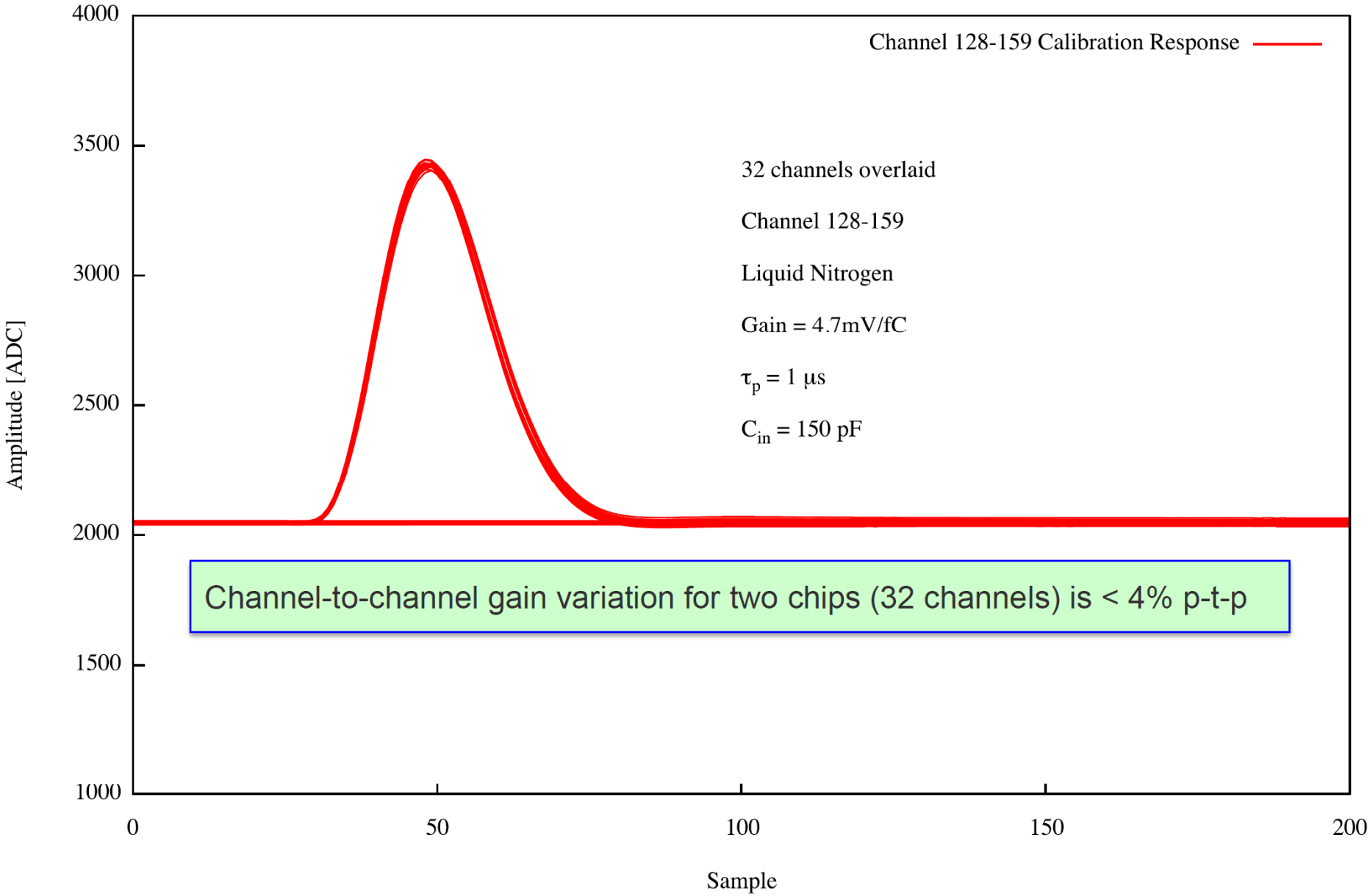
Gain uniformity for 12 ASICs (192 channels)



Noise at 300K and 77K for 12 ASICs (192 channels)



Calibration Response in LN_2



Channel-to-channel gain variation for two chips (32 channels) is < 4% p-t-p

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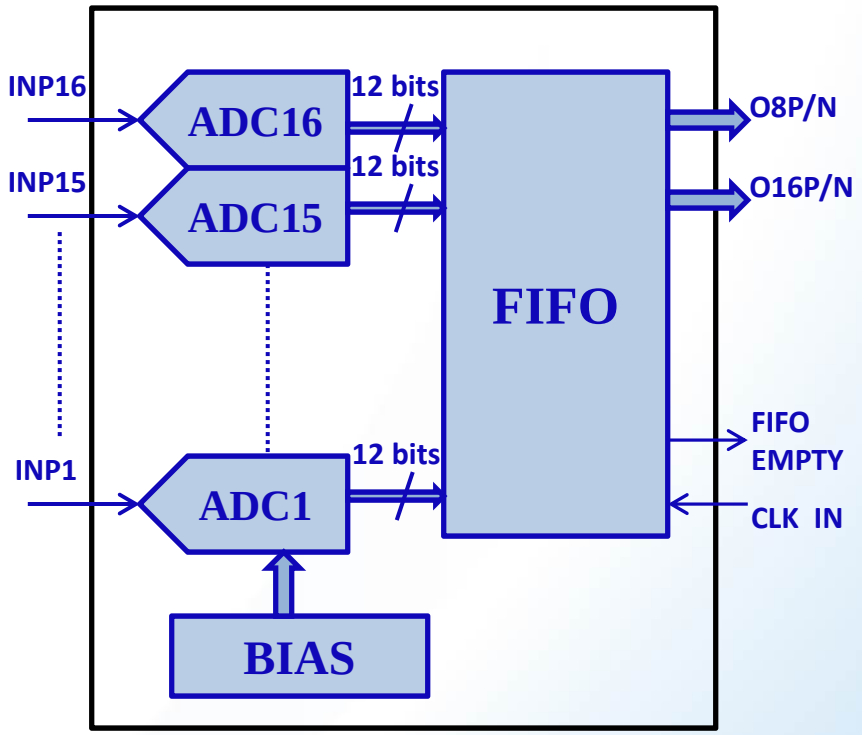
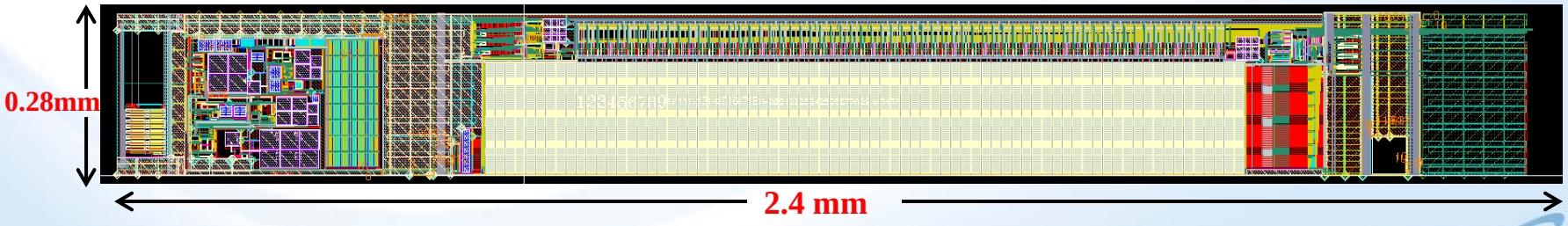
ADC ASIC Features

- Performance parameters :
  - Sampling rate up to 2 MS/s
  - Measured resolution 11.7-bit
  - Low power ADC, ~ 5 mW/ch
  - Input range 0.2 V to 1.6 V
  - Clockless operation, ideal for low noise operation
  - Small area favorable for multi-channel system
- Features
  - Low power mode with < 1us wake-up
  - Adjustable offset
  - Multiple options for internal control signals

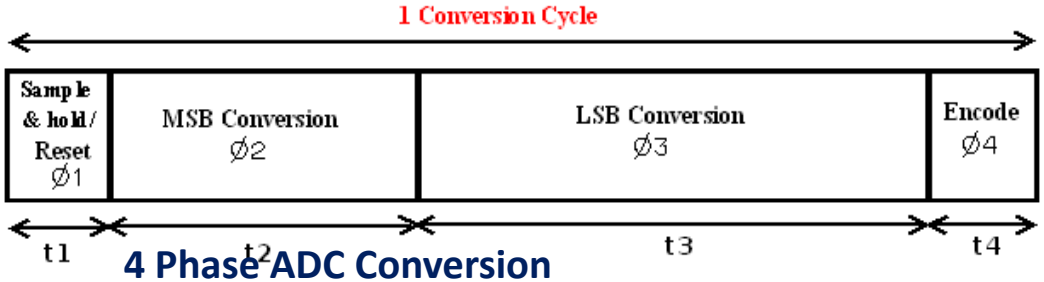


ASIC Simplified Block Diagram



Single ADC Layout

ADC Operation & Functional Block



4 Phase ADC Conversion

•Phases of Operation

- ➢Sampling & Reset: Input sampled and cells reset
- ➢MSB Conversion: MSB bits output
- ➢LSB Conversion: LSB bits output
- ➢Encode: Thermometer code from MSB and LSB converted to binary

•Sample and Hold (S&H) converts input voltage to current

•Blocks of ADC

- ➢LSB, MSB and Encoder

•Multi-phase pattern generator

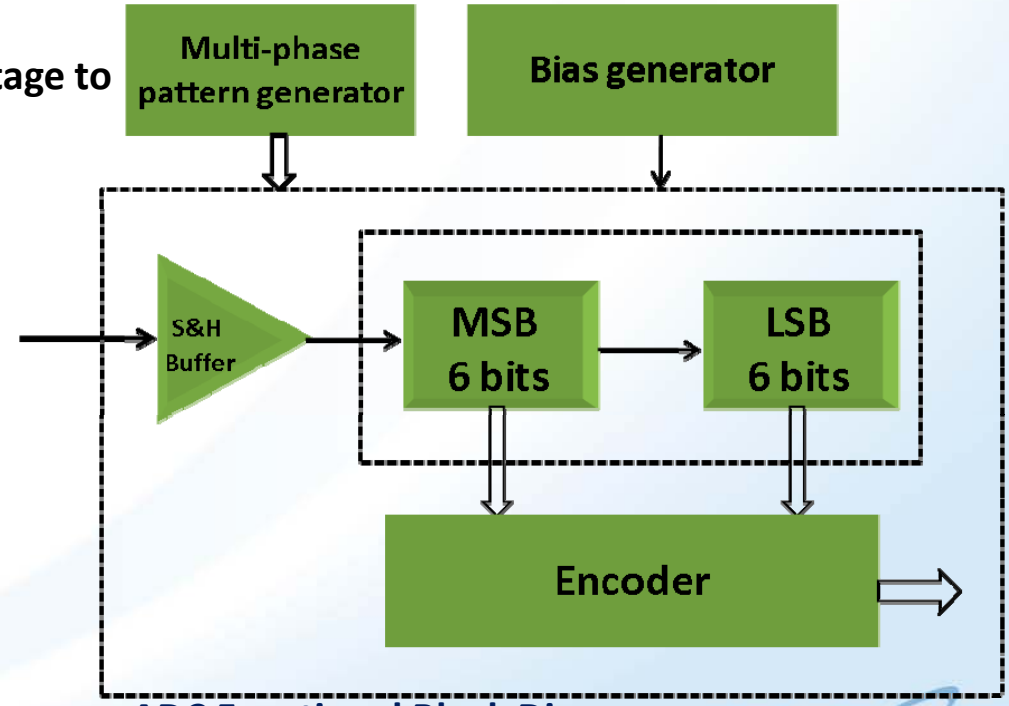
•Bias generator common

•Encoder: Thermometer to Binary.

•MSB: 6 bits →1MSB cell = 64* 1LSB

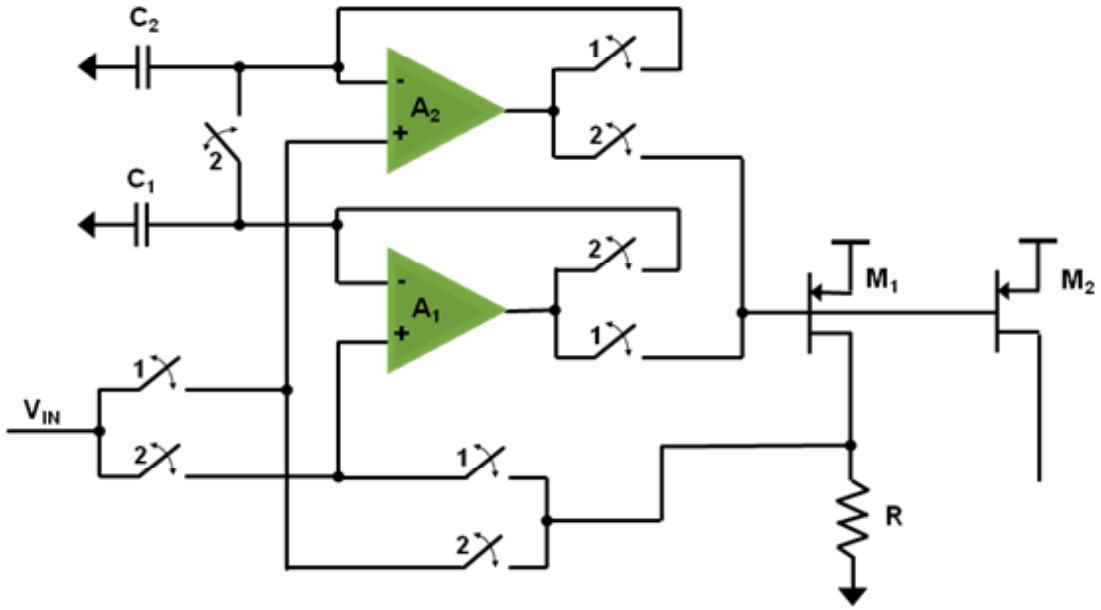
•1LSB cell = 500nA;

•1MSB = 64 LSB cells = 32µA



ADC Functional Block Diagram

ADC Design Modules: S&H Circuit

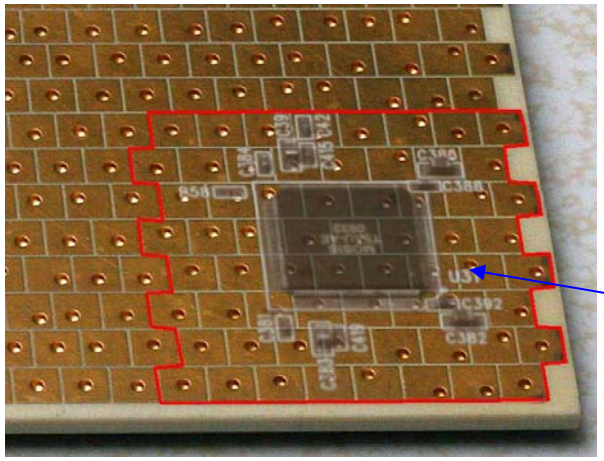


1) All switches 2 closed:
   - A2 charges C2 to VIN
   - A1 transfers C1 (previously charged to VIN-1) to R
2) A1 charges C1 to VIN
   - A2 transfers C2//C1 (pre-charges to VIN) to R
3) M1, M2 current copier multiplier
4) Settling time of S&H 50 ns

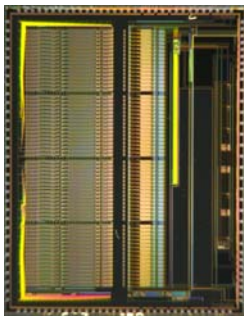
FIFO integrated on chip for data storage

Current-Mode Domino (CMD) Peak-Detect ADC

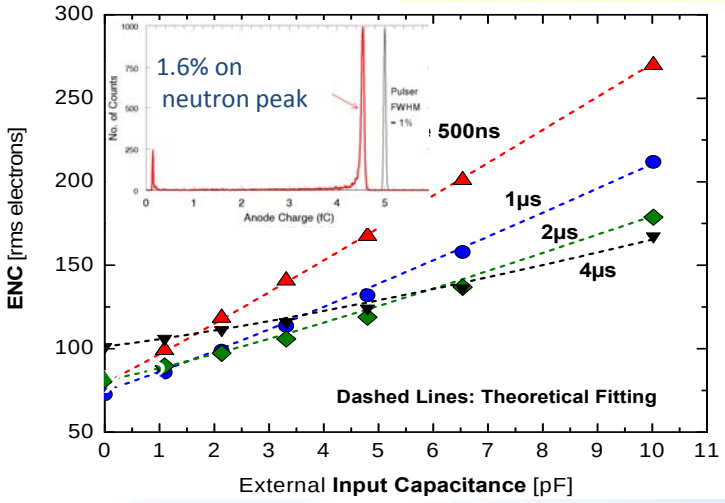
Developed in 2007 for small-angle neutron scattering measurements



- **Low-noise front-end with unity gas-gain**
- **Single-pad induction (small-pixel effect)**
- **Full size: 196 x 196 pad array (10^8 n/s)**
- **Pad 25 mm², 5 pF, rate 5 kHz / pad**



- **64 channels - mixed signal**
- **low-noise charge amp.**
- **current-mode peak detector - 6-bit ADC**
- **18-bit timestamp**
- **110 e^- resol., 1.5 mW/channel**
- **sparse readout and FIFO**
- **ASIC successfully produced in large numbers**



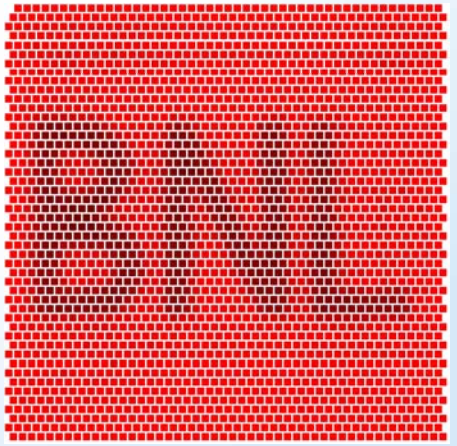


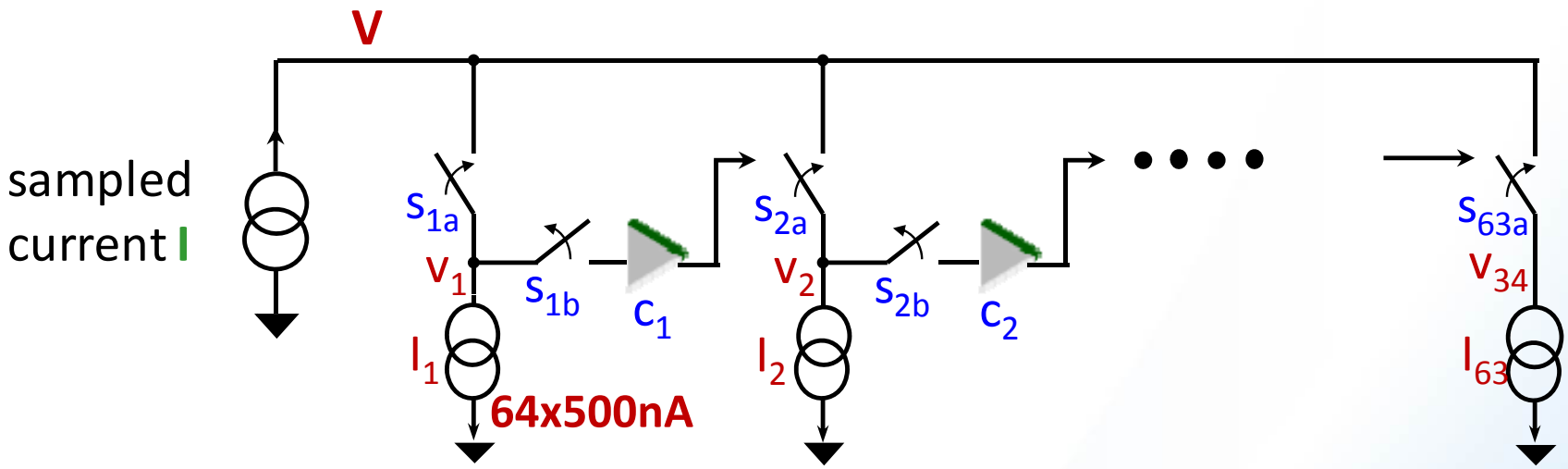
Image from Cd foil, 48x48 pad array

- ***Coded aperture version for Nonproliferation***
- ***Large 1 m² version being developed for ANSTO****

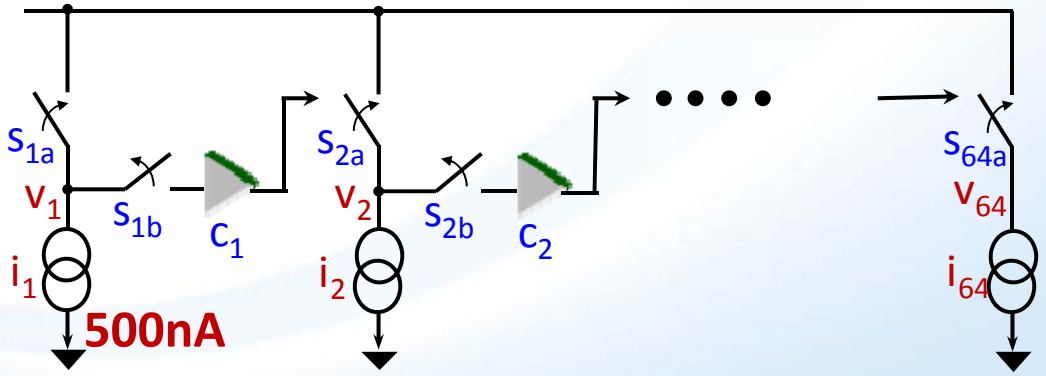
**Australian Nuclear Science and Technology Organization*

Two-Step CMD ADC Architecture for LAr

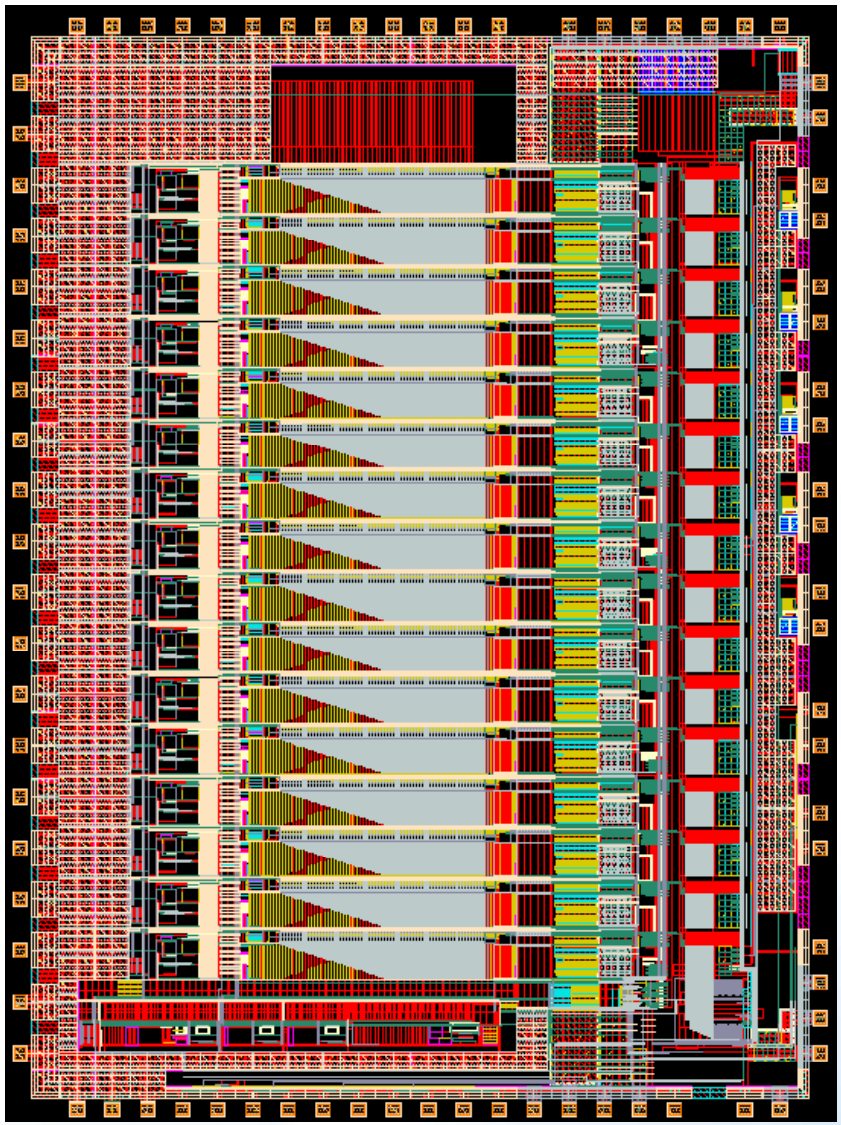
Phase 1: selects n/63 macro-currents I_i (32 µA/cell, 150 ns)



Phase 2: on residual current, selects n/64 micro-currents i_i (500 nA/cell, 250 ns)



LAr ADC Layout



Size ~ 4,500 x 6,100 µm²

Outline

- Introduction of Cold Front-End and ADC ASICs for LAr TPC
- CMOS modeling and design for cold electronics
- LAr FE ASIC:
  - Optimizing input MOSFET under power constraint
  - Crosstalk of Adjacent Channels
  - Performance of FE ASIC in MicroBooNE
- LAr ADC ASIC:
  - ASIC Feature and operation
  - Current-mode Domino architecture
- **CMOS lifetime study for cold electronics**
  - **Basics on hot-carrier effects and lifetime**
  - **CMOS lifetime in *dc* operation: analog front-end ASICs**
  - **CMOS lifetime *ac* operation: logic circuits and FPGAs**

CMOS Lifetime at Cryogenic Temperatures

- **Most failure mechanisms (e.g. electromigration, stress migration, time-dependent dielectric breakdown, and thermal cycling) are strongly temperature dependent [exp(-const./kT)] and become negligible at cryogenic temperature.**

- **The only remaining mechanism that may affect the lifetime of CMOS devices at cryogenic temperature is the degradation (aging) due to *channel hot carrier effects (HCE).***

- **The degradation mainly concerns NMOS devices - PMOS usually exhibits a lifetime much longer than NMOS.**

- ***Lifetime due to HCE aging*: A limit defined by a chosen level of monotonic degradation in e.g., drain current, transconductance, threshold voltage. The device "fails" if a chosen parameter gets out of the specified circuit design range. *This aging mechanism does not result in sudden device failure.***

- **The lifetime due to HCE at both the cryogenic temperature, as well as at room temperature, *is limited by a predictable and a very gradual degradation (aging) mechanism which can be controlled or avoided by device design and operating conditions*. In this study we have been following the basics established in the literature, e.g., Hu et al. (1985), and the practices adopted more recently by Chen&Cressler et al. (2006), as well as by industry.**

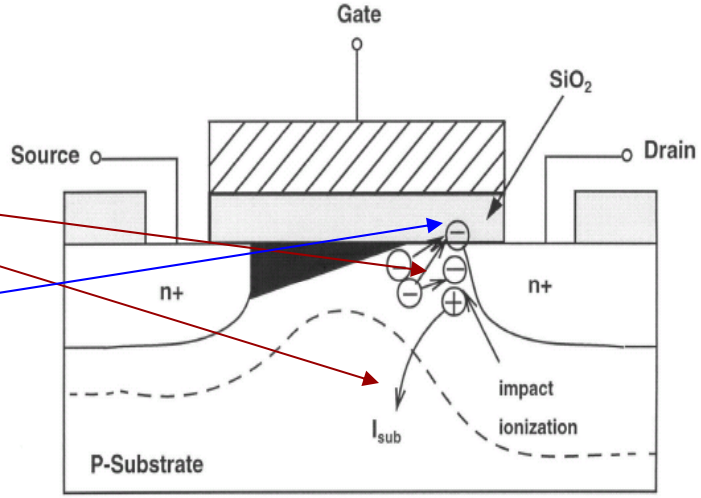
Basics on Hot Carrier Effects (HCE) -1

• Some hot electrons exceed the energy required to create an electron-hole pair, $\varphi_i \cong 1.3eV$ sulting in *impact ionization*. Electrons proceed to the drain. The *holes* drift to the substrate. The ***substrate current***,

$$I_{sub} = C_1 I_{ds} e^{-\varphi_i / q\lambda E_m} \qquad (1)$$

• A very small fraction of hot electrons exceeds the energy required to create an ***interface state*** (e.g., an acceptor-like trap), in the Si-SiO_2 interface, $\varphi_{it} \geq 3.7eV$ electrons (~4.6eV for holes). This causes a change in the transistor characteristics (transconductance, threshold, intrinsic gain). The time required to change any important parameter (the changes in different parameters are correlated) by a specified amount (e.g., gm by -10%) is defined as the ***device lifetime***. It can be calculated as,

$$\tau = C_2 \frac{W}{I_{ds}} e^{\varphi_{it} / q\lambda E_m} \qquad (2)$$



q = electron charge

λ = electron mean free path

***E_m* = electric field** $E_m \propto V_{ds} - V_{dsat}$

I_{ds}= drain-source current

W= channel width

C_1, C_2 - constants

• **I_{sub} is a monitor for all hot-electron effects and it is the best predictor of device lifetime, because all observable hot electron effects (electrical and optical) are driven by a common driving force – the maximum channel electric field E_m , which occurs at the drain end of the channel.**

• **From (1) and (2), the *substrate current is connected to the lifetime* (defined by any arbitrary but consistent criterion) by**

$$\tau I_{ds} \Big/ W \propto \frac{1}{\left(I_{sub}/I_{ds}\right)^{\varphi_{it}/\varphi_i}}$$

$$\varphi_i \simeq 1.3eV; \varphi_{it} \simeq 3.7 - 4.2eV$$

$$\varphi_{it}/\varphi_i \simeq 2.9 - 3.2$$

Basics of Hot Carrier Effects -2

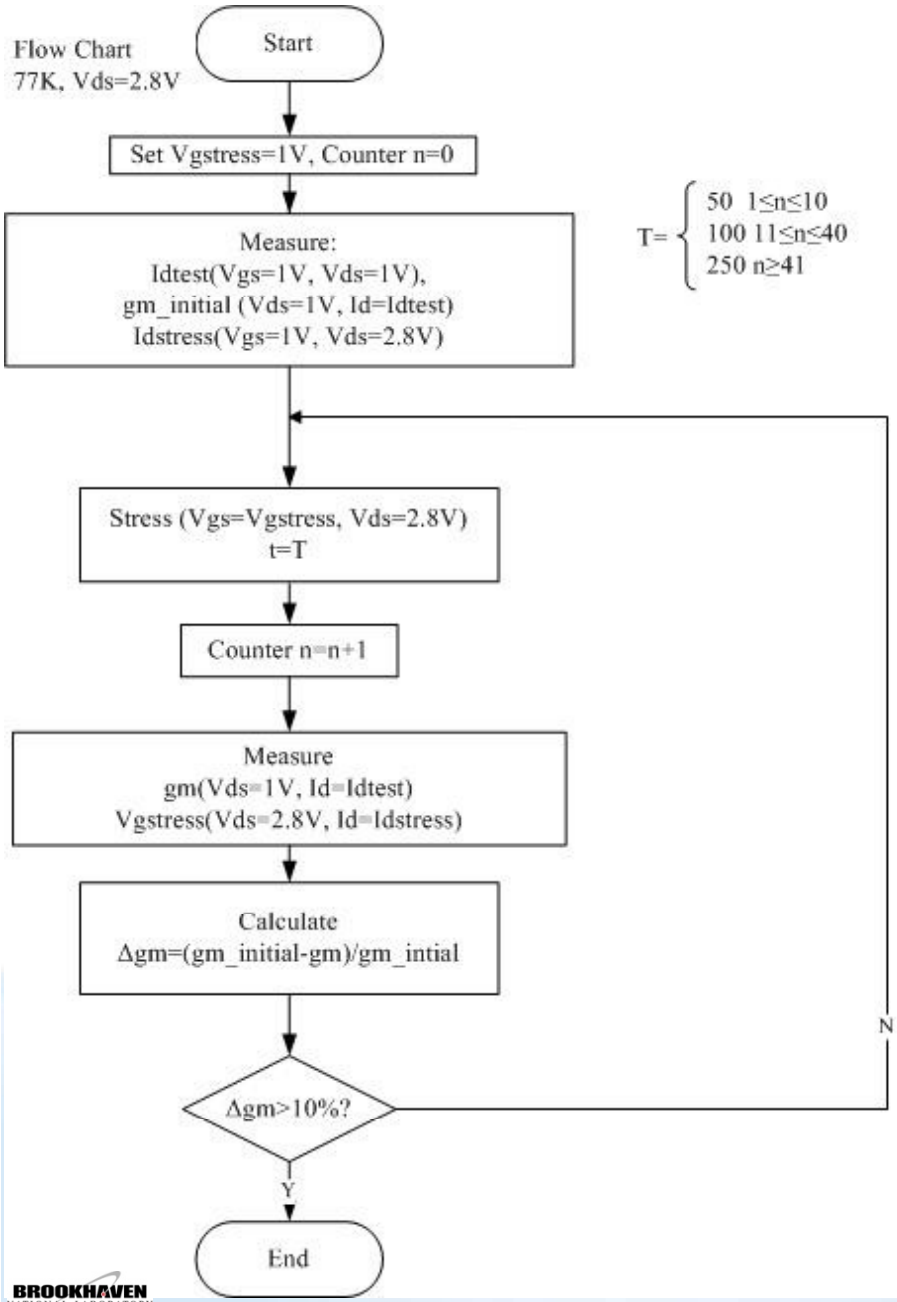
• ***Substrate current*** **is a monitor of** ***impact ionization*** **and of** ***interface states*** **creation**

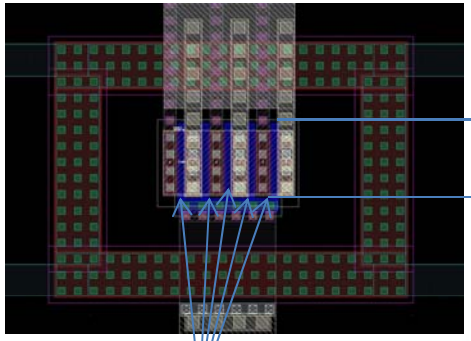
• ***"Degradation"*** **– a decrease in** I_{ds} ***and*** g_m **and increase in** V_{th} **is due to interface state creation**

• **A lower temperature results in a slightly increased** ***mean free path*** λ **increasing the substrate current** I_{sub} **.** ***Degradation of*** V_{th} **,** I_{ds} ***and*** g_m ***is independent of temperature if the product*** $\lambda E_m \approx \lambda V_{ds}$ ***is kept constant.***

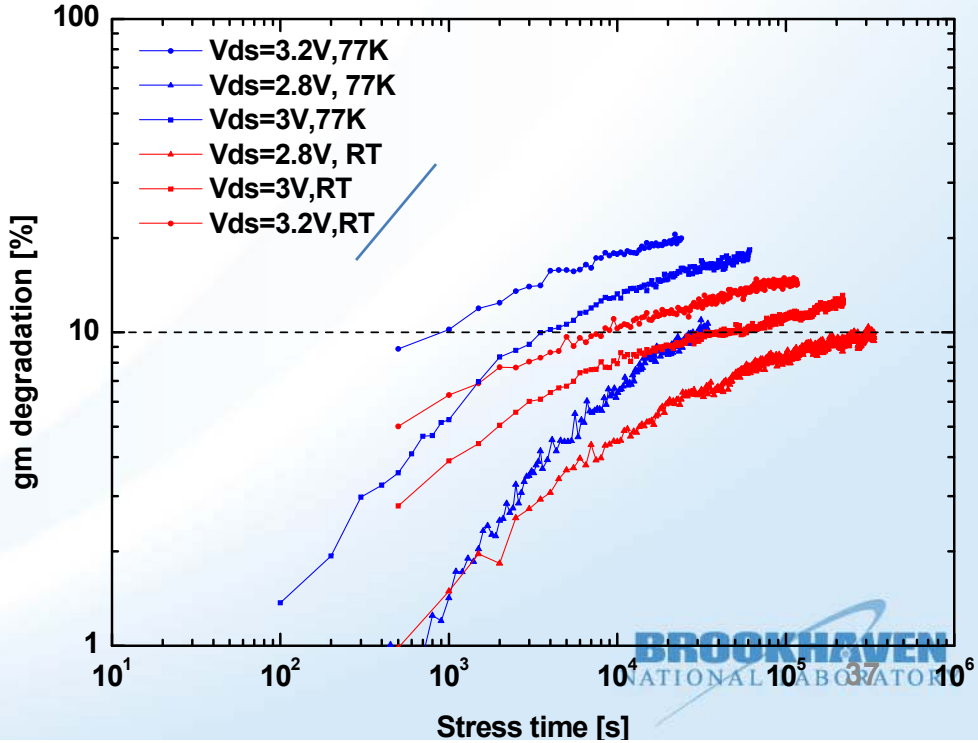
• ***Accelerated lifetime test at any temperature*** **(well-established by foundries): transistor is placed under a** ***severe electric field stress*** **(large** V_{DS}**), to reduce the lifetime due to hot-electron degradation to a practically observable range, by a drain source voltage considerably higher (~80%) than the nominal voltage.**

Stress Test Flow Chart and Layout of test NMOS transistors





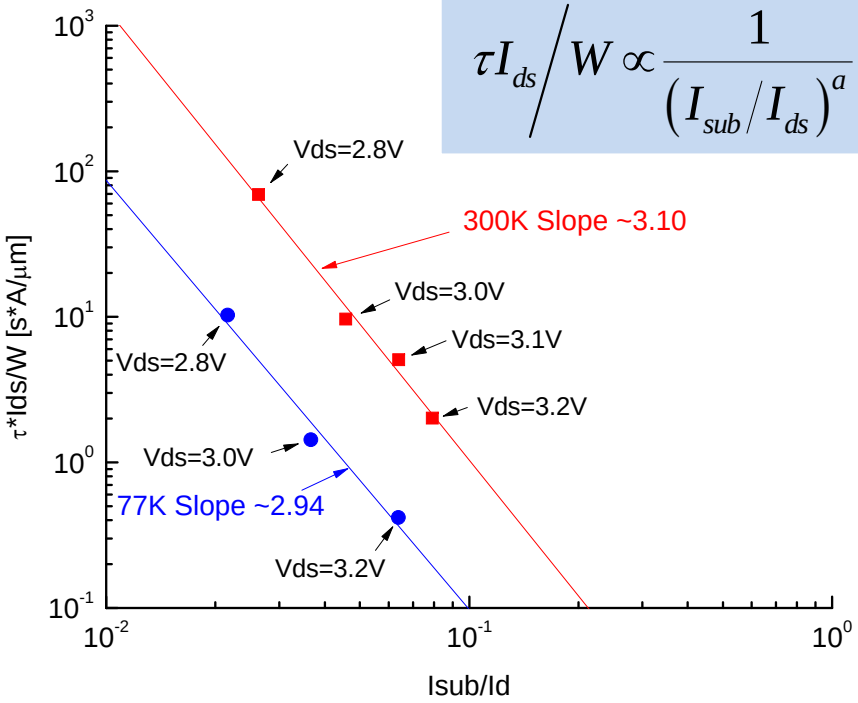
Test transistors, NMOS L=180nm, W=10μm (5 fingers x 2μm), designed to have negligible IR drop and power dissipation <15mW in stress tests to prevent temperature change due to self-heating.



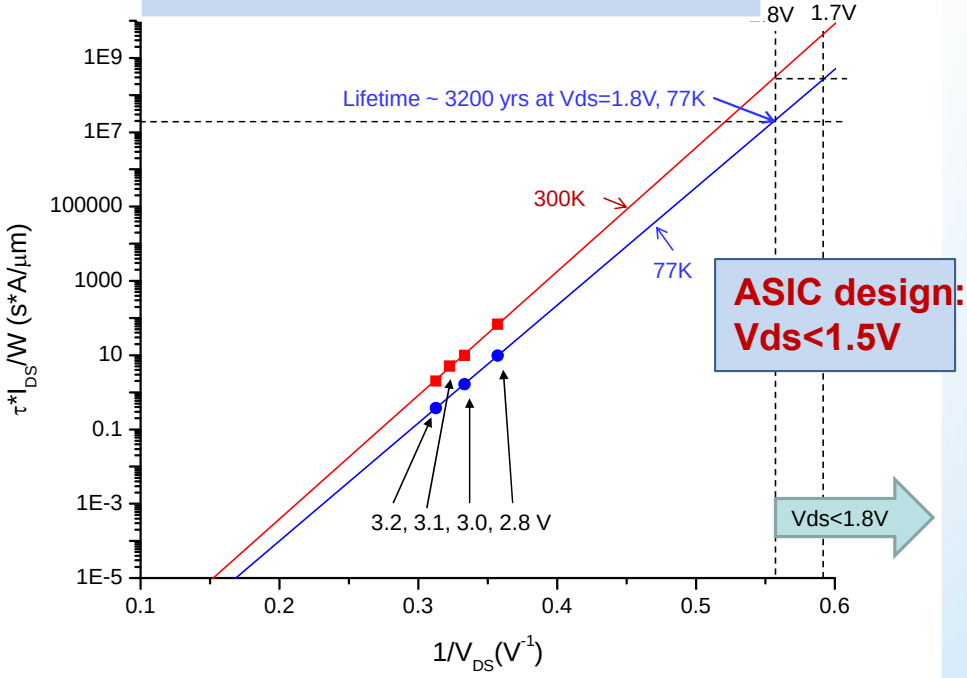
Accelerated Lifetime Measurements (180 nm)

Measurement Type I: "Stress Plot"

$$\tau I_{ds} \Big/ W \propto \frac{1}{\left(I_{sub}/I_{ds}\right)^{a}}$$



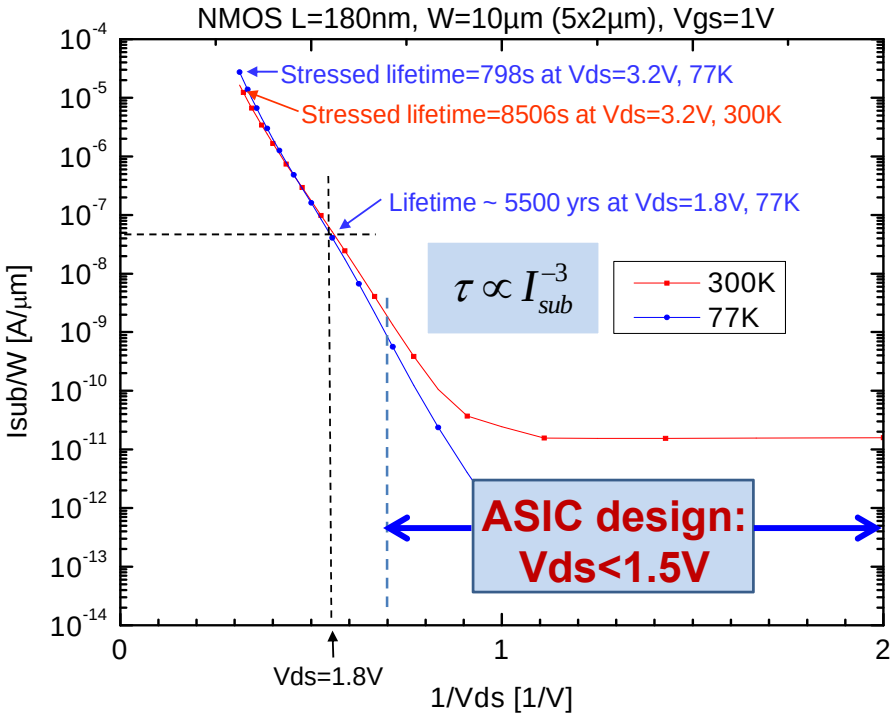
$$\ln\left(\frac{\tau I_{ds}}{W}\right) \propto \frac{\varphi_{it}}{q\lambda E_m} \propto \frac{1}{V_{ds} - V_{dsat}}$$

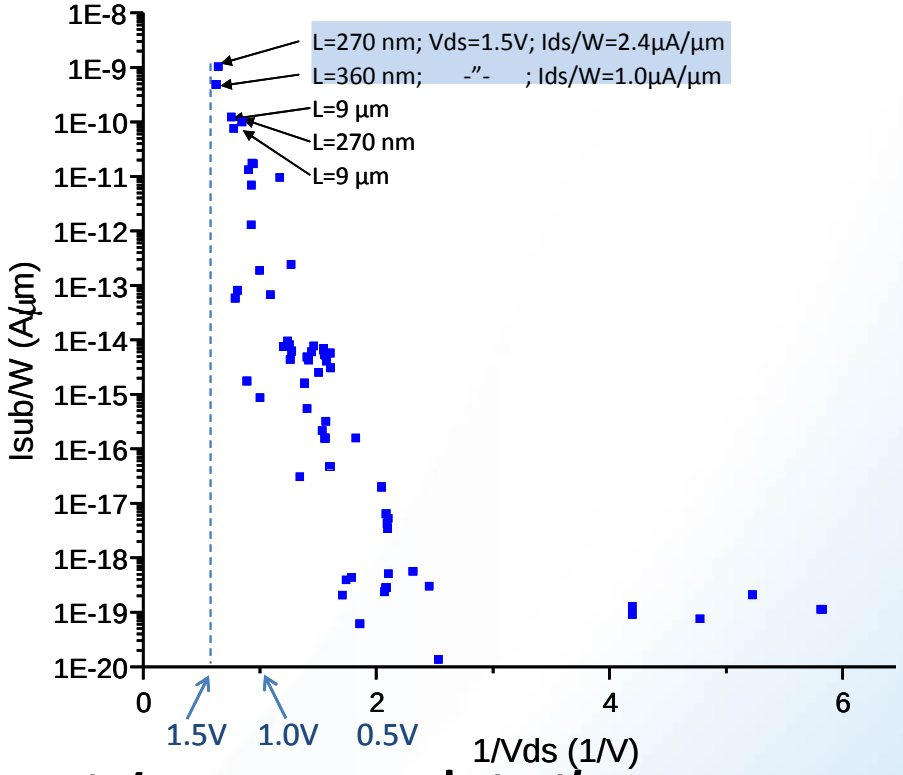


- *If the measured points at both 300K and 77K are close to the characteristic slope for the interface state generation,* $a = \varphi_{it}/\varphi_i \approx 3$ *, it confirms that the degradation follows basic relations for interface state creation. Substrate current must be measured for this stress plot.*

- *The lifetime prediction plot (right) can be derived from the stress plot (left), or from direct measurements of* τ *vs.* V_{ds}*, without measuring the substrate current*

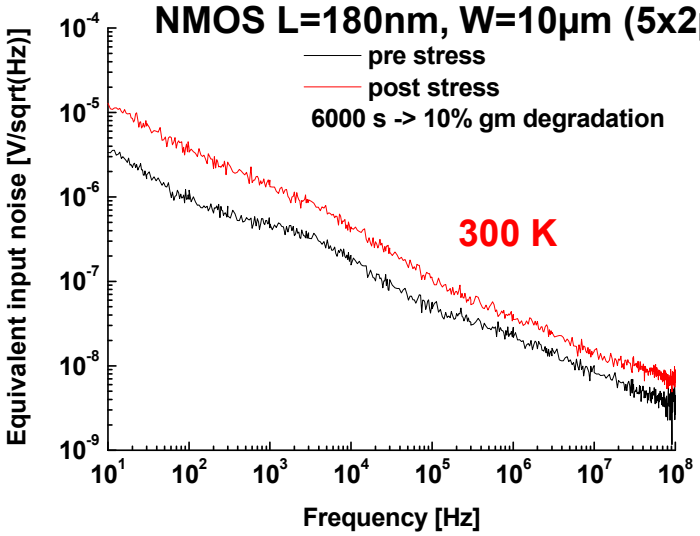
Measurement Type II: Substrate Current Density I_{sub}/W *vs* $1/V_{ds}$

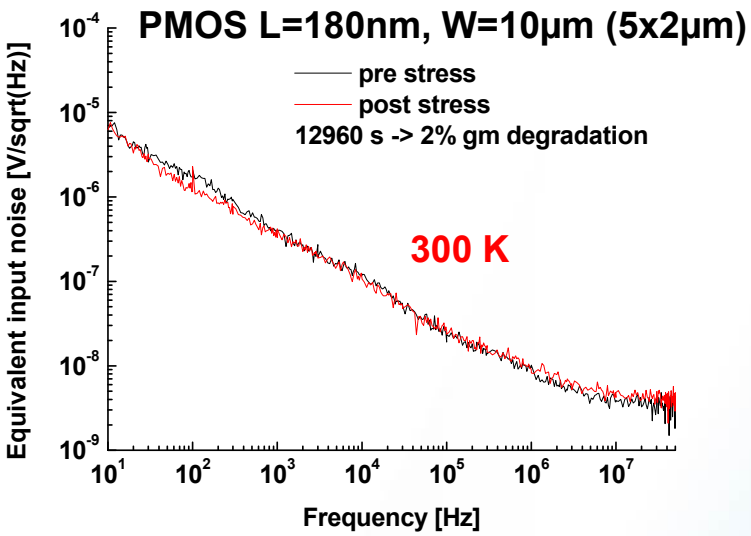


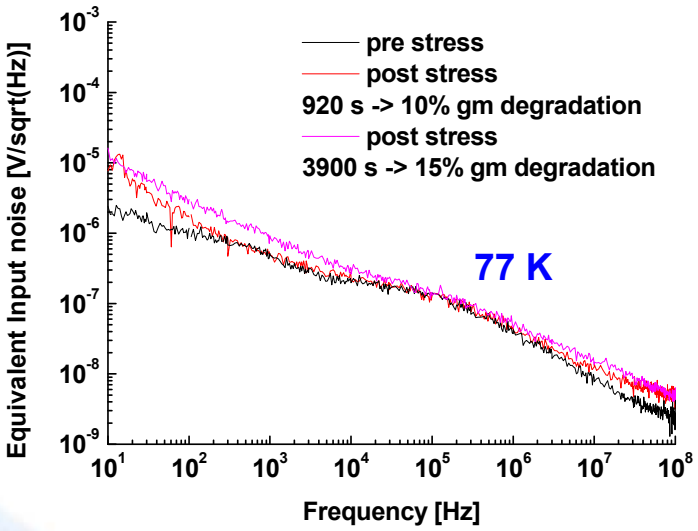


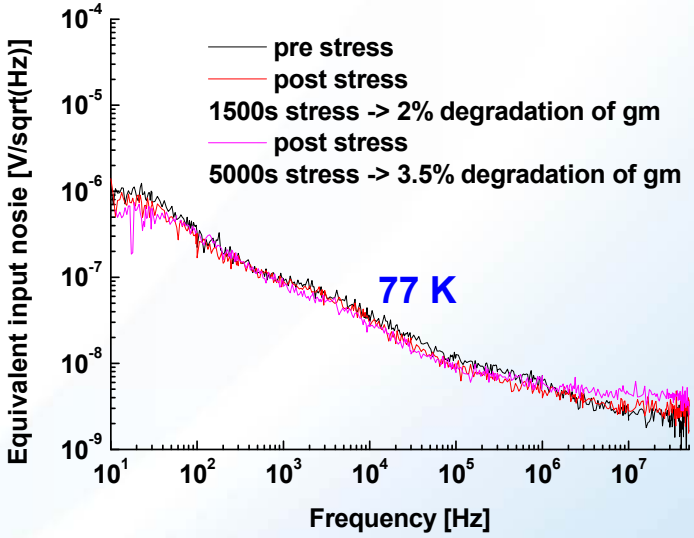
- **One order of magnitude in substrate current I_{sub} corresponds to *three orders* of magnitude in lifetime. At 77 K, V_{ds} = 1.8 V projects a lifetime of ~5500 years.**
- **I_{sub}/W and $1/V_{ds}$ distribution for all transistors in the analog front-end ASIC for LAr TPC (TSMC 180nm, 1.8V node) shows that all transistors are well below nominal voltage of 1.8V and at low I_{sub}; *Reduced* V_{ds} < 1.5 V results in essentially making HCE negligible and a very long extrapolated life time.**

Noise Degradation: Less Degradation in PMOS









- **PMOS: much less degradation than NMOS**
- **PMOS is used in the preamp input and, by design, it is the main noise contributor in the front-end ASIC.**

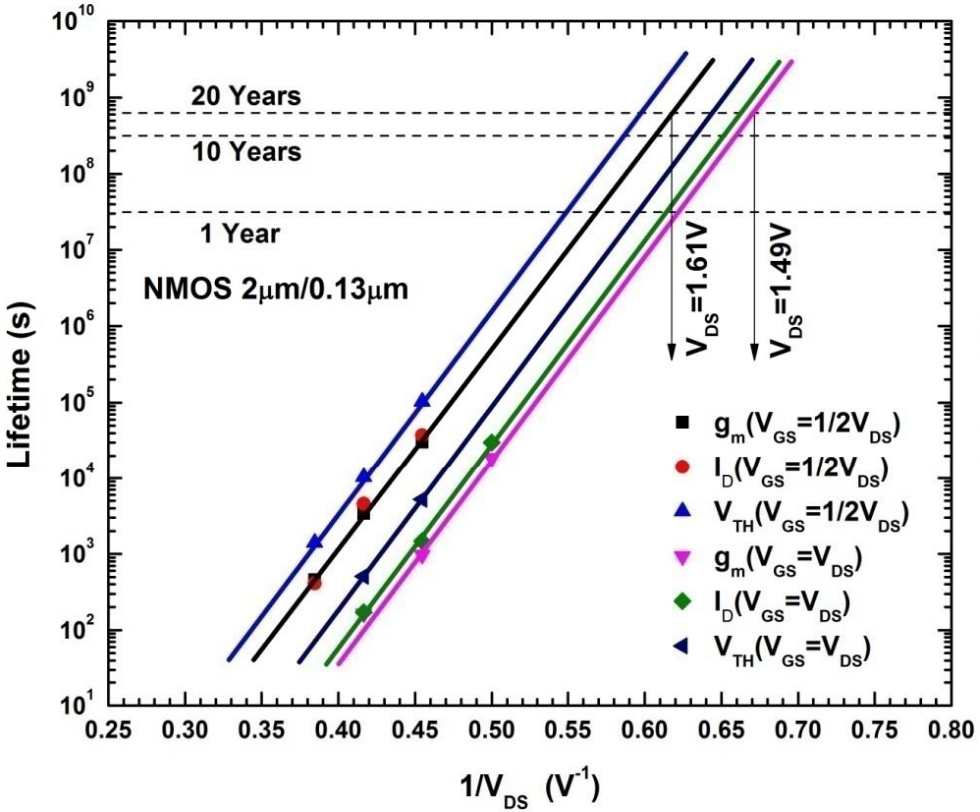
CMOS in *dc* Operation (180nm, 130 nm and 65 nm)

- Reducing V_{ds} at 77K by ~ ***6% makes the lifetime an order of magnitude longer*** in all three technologies → **identical slope *τ vs 1/ V_{ds} at respective nominal V_{ds}***

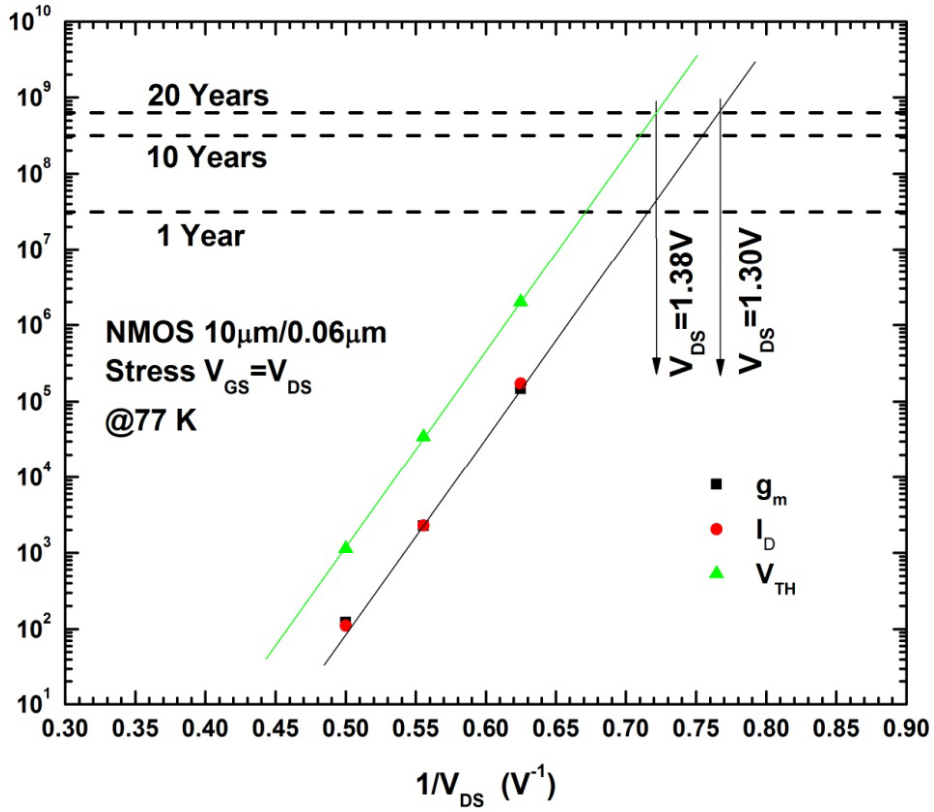
L	65 nm	130 nm	180 nm
ΔVds/Vds: for $\tau_2/\tau_1=10$	~5.3%	~5.7%	~5.5%

(From slide 6)

130 nm



65 nm



(Data for 130nm and 65nm, courtesy of G. Wu_SMU&FNAL)

Why is the dependence of Lifetime on V_{ds} so strong?

The lifetime is given by,

$$\tau = C_2 \frac{1}{\left(I_{ds}/W\right)} e^{\varphi_{it}/\varphi_{he}} \propto \frac{1}{\left(I_{ds}/W\right)} e^{\varphi_{it}/\varphi_{he}}$$

Electrons in the MOS channel reach energies well above thermal both at 300K and at 77K . However the ***mean electron energy,*** $\varphi_{he} = q\lambda E_m \sim 100meV$, at the electric field in the range E_m ≥100kV/cm. At 77K it is slightly higher, $\varphi_{he77K}/\varphi_{he300K} \approx 1.06$

Only a tiny fraction of "hot" electrons reaches the much higher energy $\varphi_{it} \approx 3.7eV$ required to create an ***interface state***. This makes the exponent in the relation for the lifetime very large,

$$\frac{\varphi_{it}}{\varphi_{he}} = \frac{\varphi_{it}}{q\lambda E_m} \sim 40 \pm 4$$

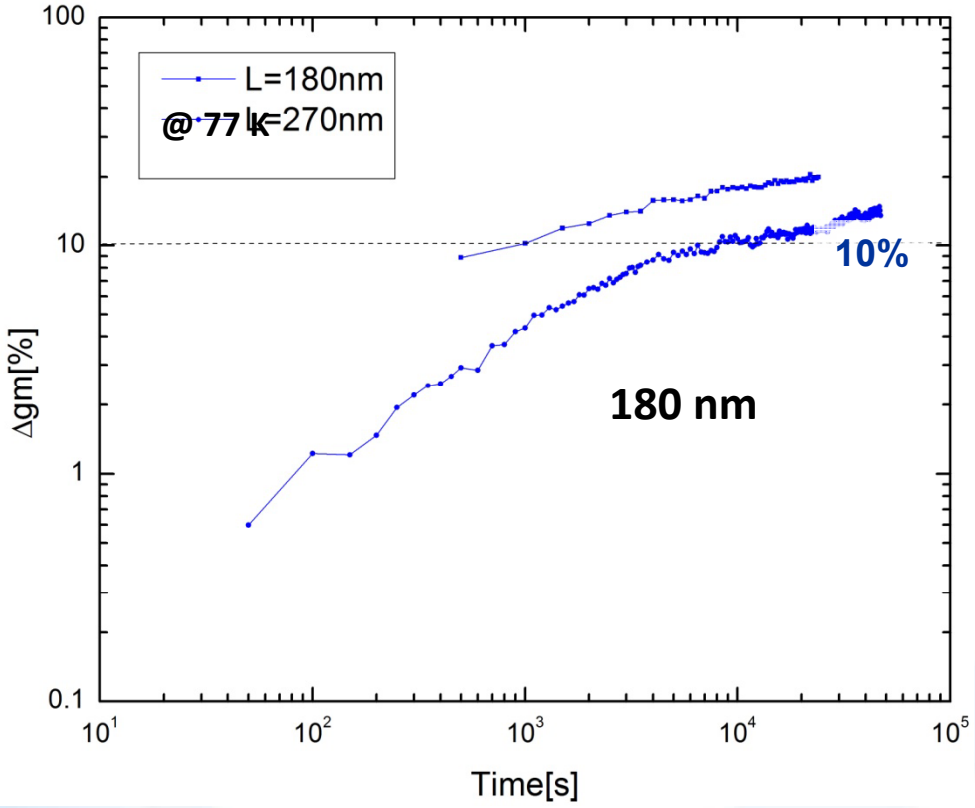
Since $E_m \propto\sim V_{ds}$, the ratio of lifetimes for two slightly different values of V_{ds} is given by,

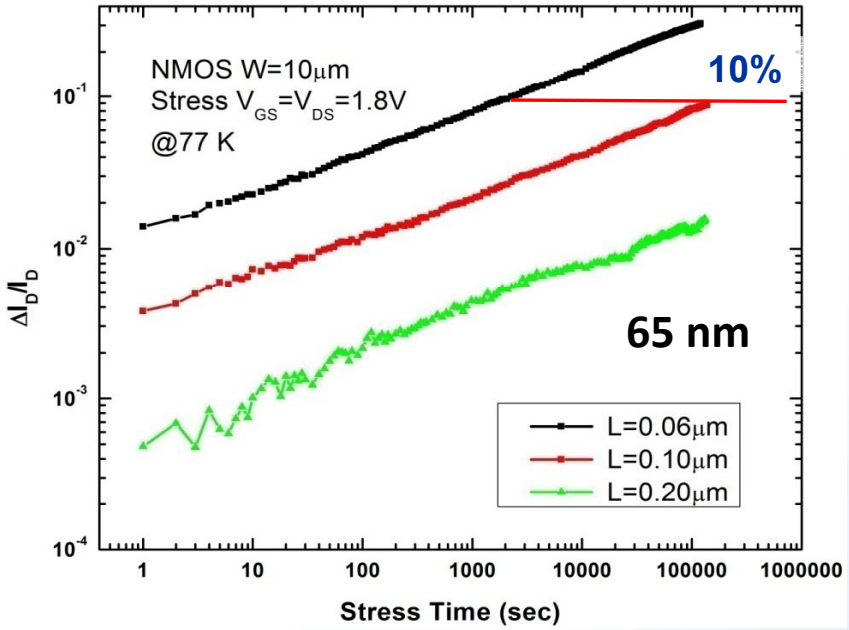
$$\ln \frac{\tau_1}{\tau_2} \approx \frac{\varphi_{it}}{\varphi_{he}} \cdot \left[\frac{V_{ds2}}{V_{ds1}} - 1 \right]$$

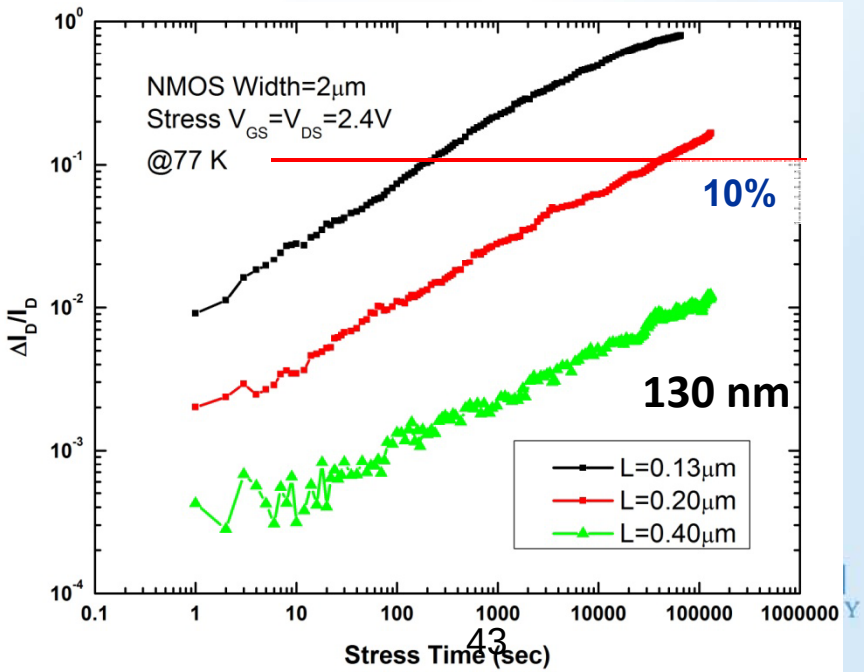
$$for \ \frac{V_{ds2}}{V_{ds1}} = 1.06 \Rightarrow \frac{\tau_1}{\tau_2} \sim 10$$

Much Longer Lifetime with Longer Device

- By increasing device length, the measured lifetime increased by 1-2 orders of magnitude







(Data for 130nm and 65nm, courtesy of G. Wu)

CMOS Lifetime in *AC* Operation: Logic Circuits and FPGAs

• Long established (e.g. Quader&Hu et al.(1994), White&Bernstein (2006)] and adapted by foundries: considering the ***ac*** *stress as a series of short* ***dc*** *stresses, each for* ***effective stress time*** t_{eff} ***during the switching cycle*** $2t_r$, *strung together*.

• **The** ***lifetime of digital circuits (ac operation) is extended by the inverse duty factor*** $1/(f_{ck}\, t_{eff})$ ***compared to dc operation.*** This factor can be quite large at ≤130nm.

• Rough estimation of t_{eff} [Quader&Hu et al. (1994)]:

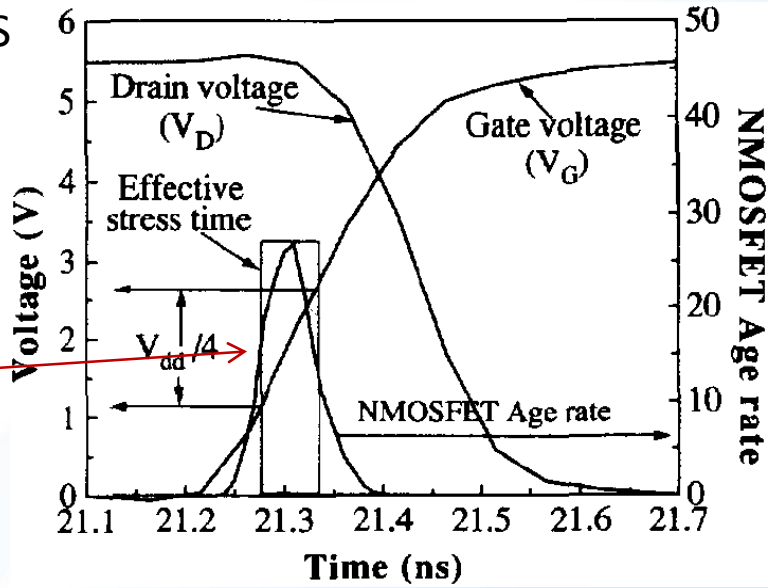
$t_{eff}/t_r \approx 1/4$, t_r = the gate voltage rise time for NMOS

• ***Inverse duty factor at maximum switching frequency*** $f_{ck} \le 1/2t_r$:

$$1/(f_{ck}\, t_{eff}) \approx 8$$

• **Note that the *substrate current* flows only during a small fraction of rise/fall time while V_{ds} is high. More detailed estimation can be found in the design manuals of major foundries.**

Quader&Hu et al. (1994)

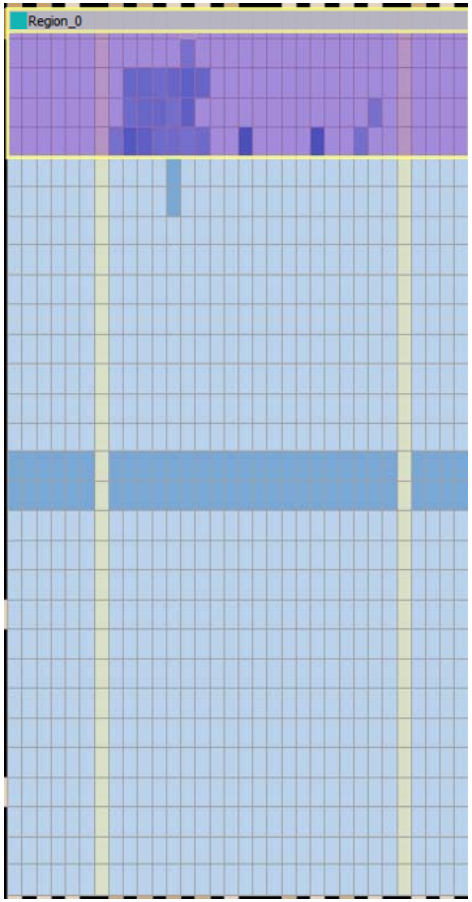


A standard method for evaluating the digital circuit lifetime is to apply accelerated stress test on a Ring Oscillator (RO) and observe the RO frequency degradation under severe stress. Degradation of drain current leads to increased rise (propagation) time and reduced frequency.

FPGA Lifetime Study: Stress methodology

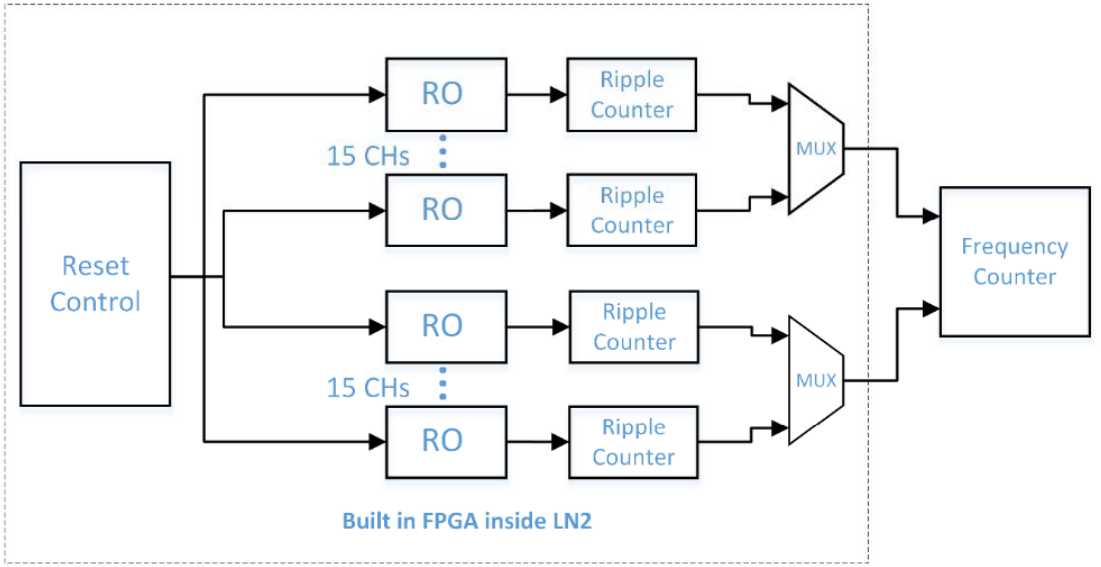
- The stress methodology we adopted follows the standard *Accelerated Lifetime Strategy*. The experiment is composed of two steps performed alternately:
  - Measurement Step: measure frequency of **ring oscillator (RO)** at Vccint=1.2V for 30s.
  - Accelerated Stress Step: accelerate degradation of RO at higher core voltage. Stress device (e.g. Vccint=1.8V) for 3600s.
- In each measurement step, frequency measured from 15s to 30s are averaged for reliable result.
- The degradation criteria is defined as **3% degradation of the frequency** which is widely adopted [J. Zhang and S. S. Chu, 2002].

Experiment Block Diagram and FPGA Floor Plan

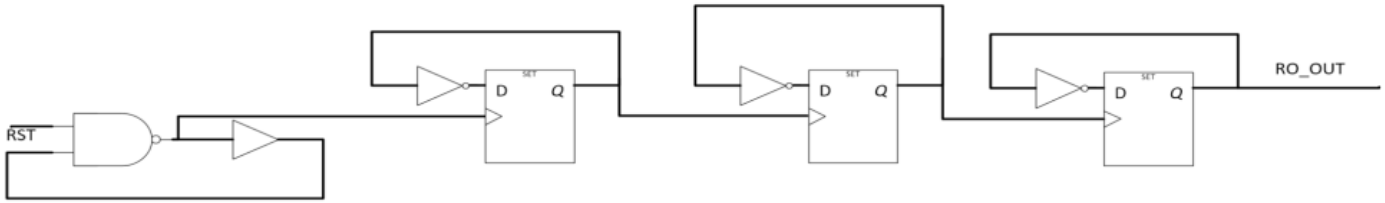


Control Logic (locked down in the area with Logic-Lock)

Experiment Block Diagram

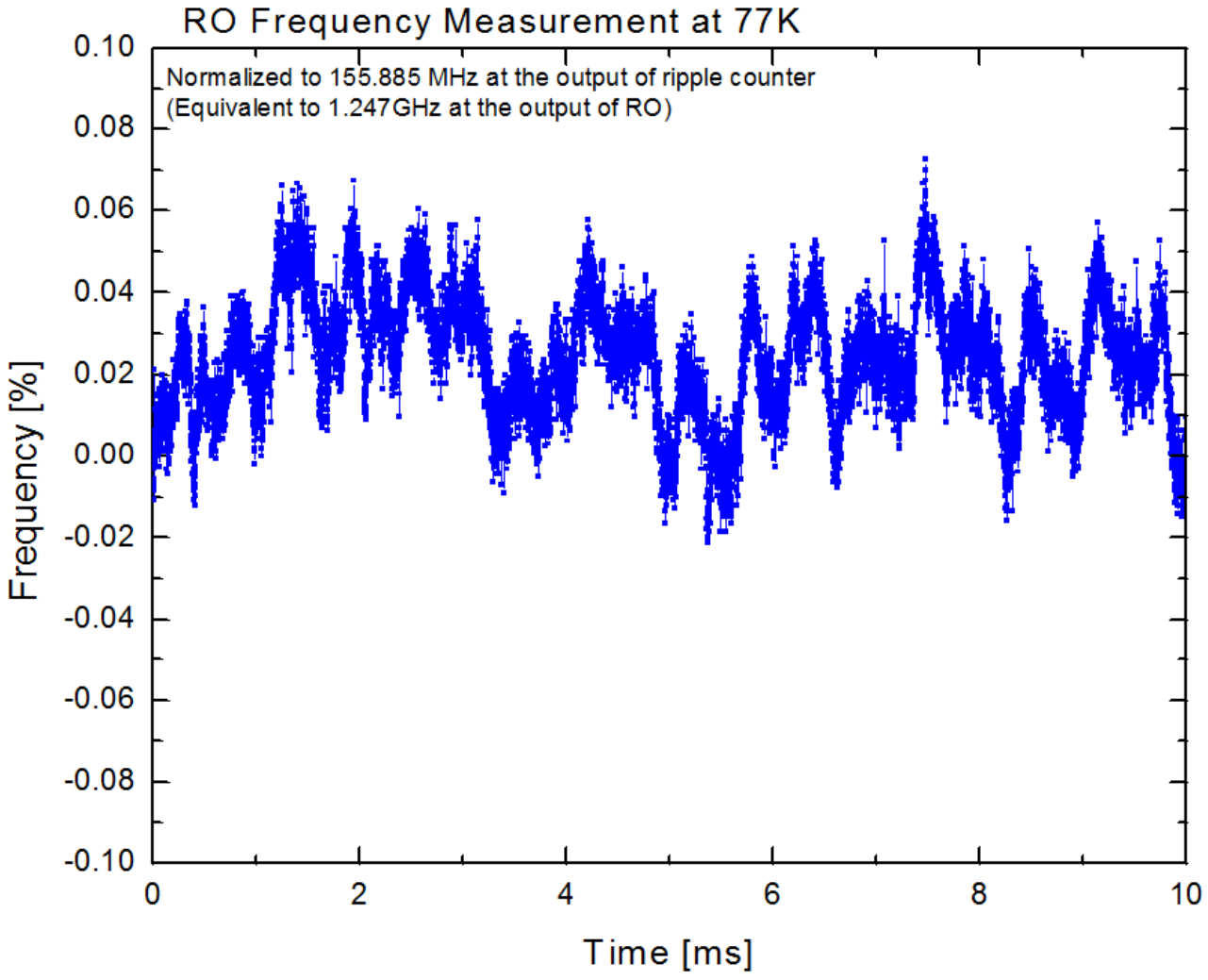


Array of 30 ROs. After the device is stressed under one voltage, another array of ROs will be locked down for stress.



FPGA Floor Plan

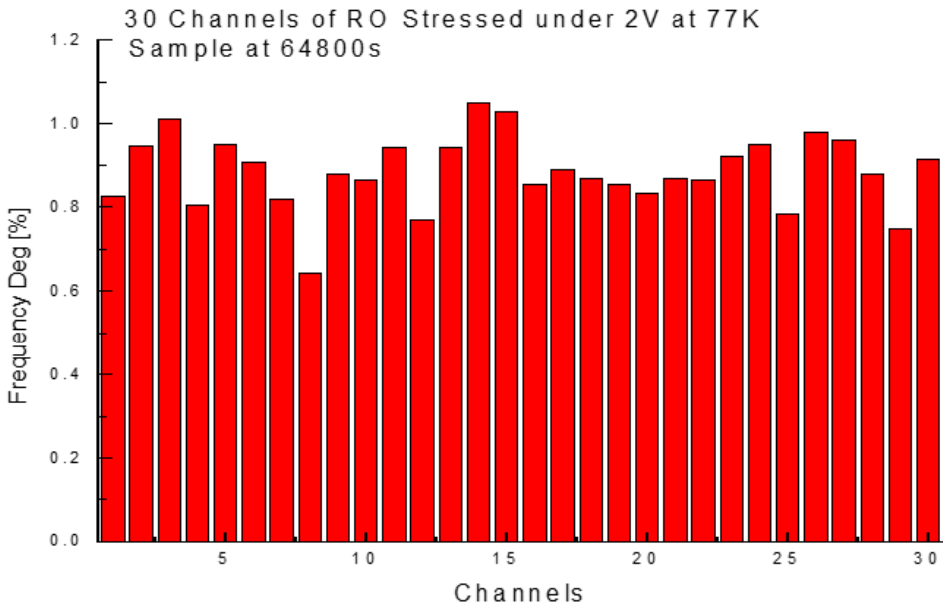
RO Frequency Measurement



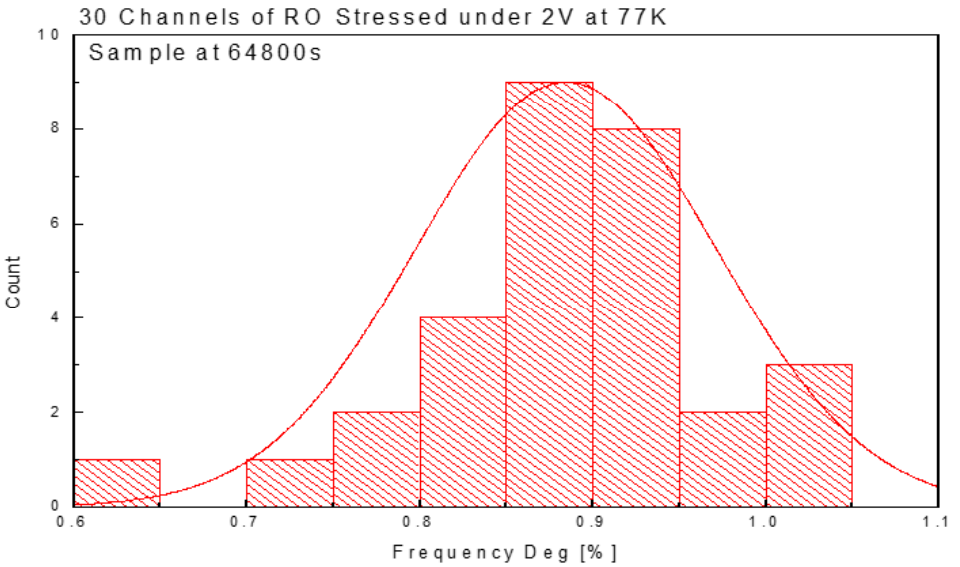
- **Frequency of RO is stable with less than 0.1% variation from peak to peak**

Statistical View of the Degradation of 30 RO Channels

Frequency of 30 RO Channels

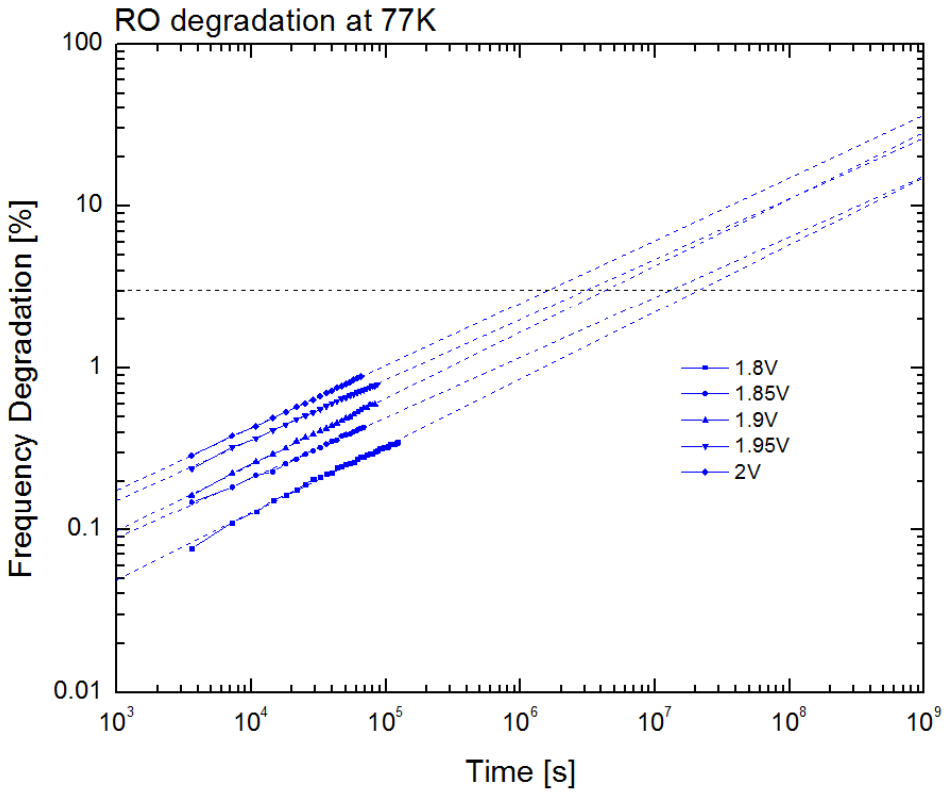


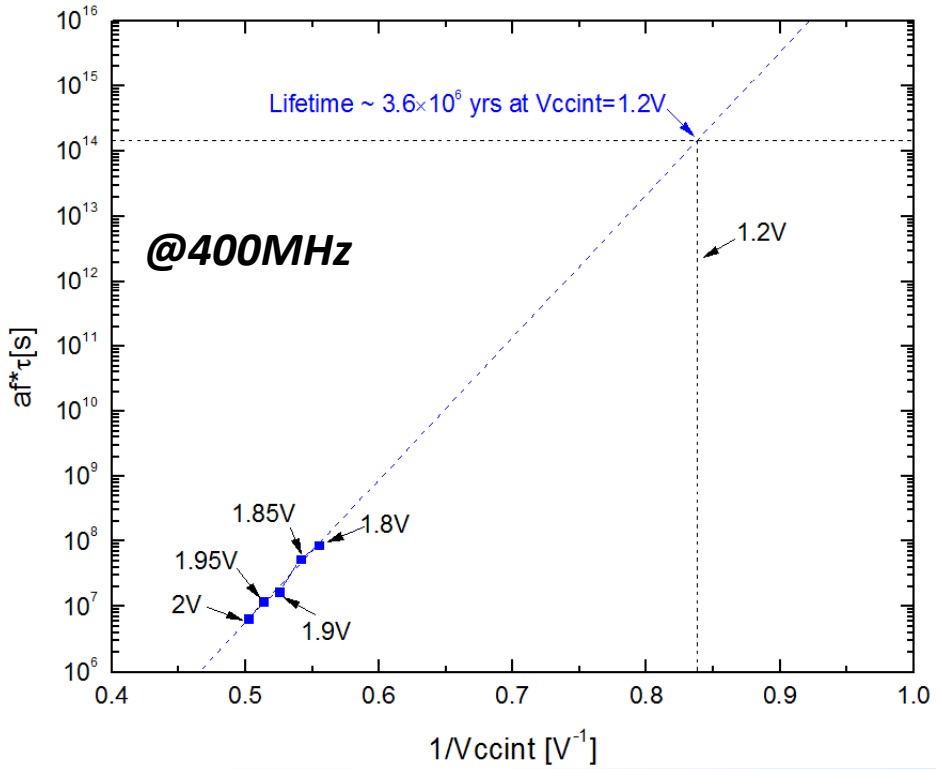
Frequency Histogram of 30 RO Channels.



- **μ=0.88, σ=0.087**
- The mean of 30 RO Channels is used for each stress point to calculate the frequency degradation

Lifetime Projection of FPGA



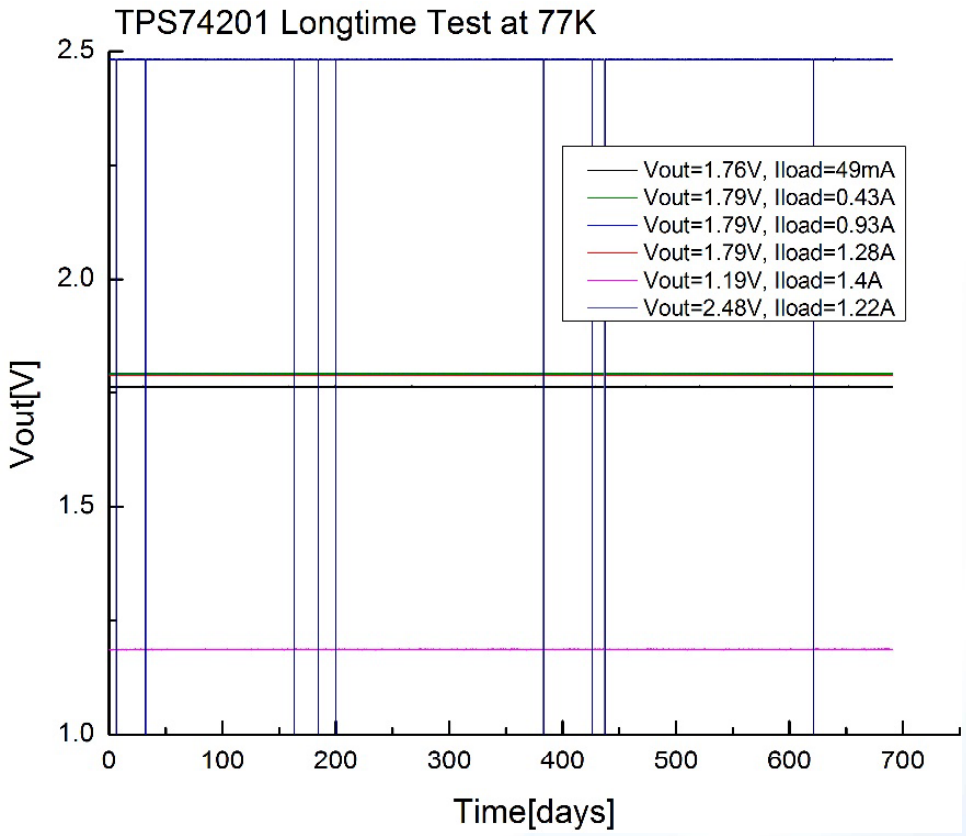


- Traditionally, lifetime is projected by empirical equation $log_{10}\tau \propto 1/V_{ds}$. The target operation frequency is 400MHz while the RO is stress under 1.7GHz. To include the effect of higher stress frequency, frequency acceleration factor α_f is introduced which is defined as $\alpha_f = \frac{f_{stress}}{f_{target}}$. The equation for lifetime projection is modified as:

$$log_{10}\alpha_f\tau \propto 1/V_{ds}$$

- Following the above equation, lifetime of FPGA at 77K is projected to be 3.6×10^6 years for 3% degradation criteria, giving a wide margin over the physical target (>20 years) .

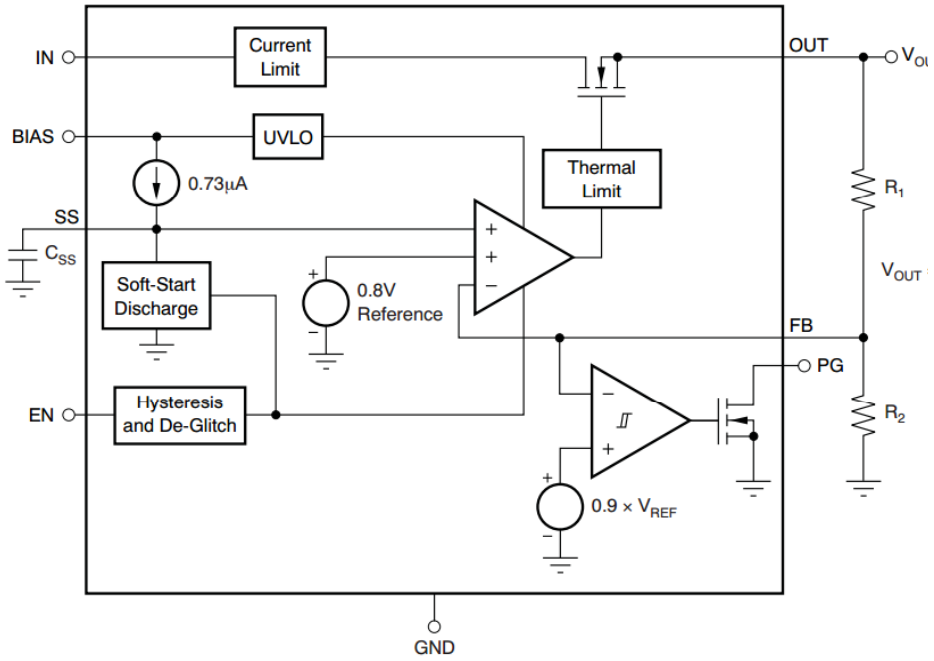
Regulator at 77K-Two Year Continuous Non-stress Test

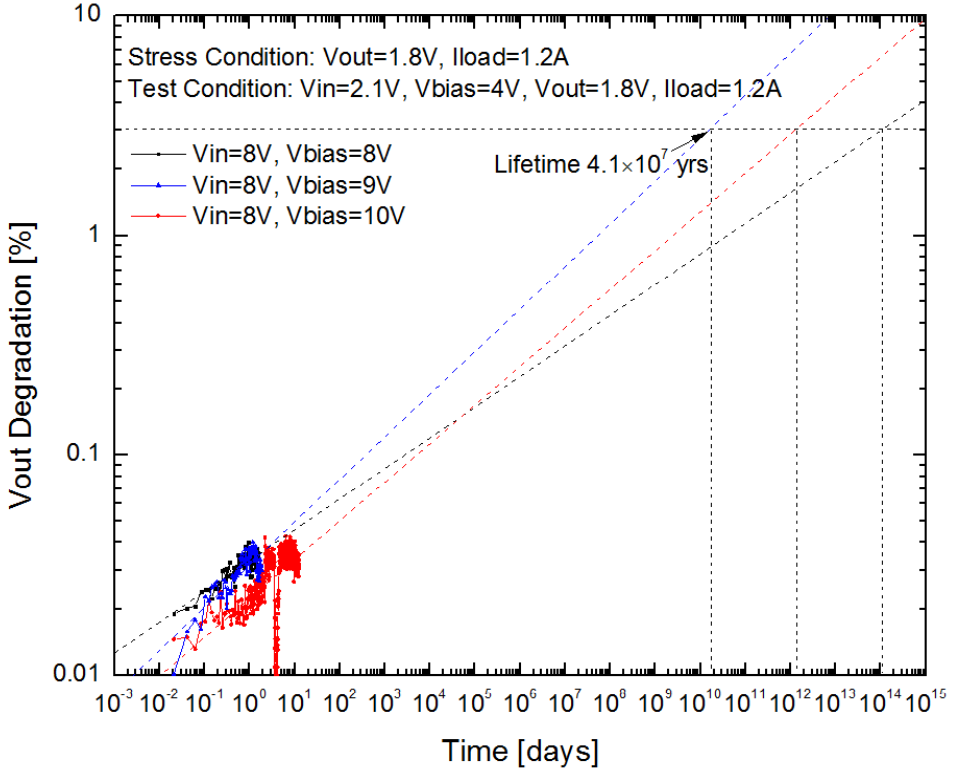


A 2-year continuous non-stress test of six regulators biased at different operating condition has been performed. The output voltage of the regulator is stable over the full range of two years. Voltage drops are due to power glitch (power supply or computer shut down), movement of experiment setup, ect.

Regulator Stress Test

Block diagram of TPS74201





Regulators are stressed under different voltages. For criteria of 3% degradation, the regulator under stress (Vin=Vbias=8V) already exhibits a lifetime of more than 10^7 years. Therefore, the operation of the regulator under normal operation (Vin=2.1V, Vbias=4V) at 77K is not of concern.

Lifetime Risk Analysis and Amelioration

• To alleviate the lifetime risk, custom ASIC should be designed for one or two orders of magnitude longer lifetime than 30 years, by selection of *Vdd* and *L*, essentially to get out of the region of degradation measurable after 30 years.

• The lifetime issue for complex synthesizable logic circuits should be treated separately from the question of how good the transistor/circuit models for low temperature operation might be. The separation of the two issues is easily accomplished by providing a large lifetime margin, so that the circuit and process margins can be treated independently of aging.

• Note that rise/fall times are faster at 77K, even at reduced Vds, than at 300K, and the ASIC data processing speed performance need not suffer due to conservative large lifetime margins.

• The positive lifetime results on the FPGA and voltage regulator suggest, for their use in LAr, the lifetime shouldn't represent a concern. The operation and programmability of FPGAs and voltage regulators has been subject of a separate study.

Further R&D on FE and ADC ASICs

FE ASIC

- Two design issues to be addressed in FE P2 submission:
  - Variation of bias current due to unsupported-wire motion, 1-GOhm resistor is necessary on board to bring channels up
  - Imperfect pole-zero cancellation in cold operation

- Suppression of power supply noise from regulator in cold operation

ADC ASIC

- Stuck code (more severe in cold operation)