An Overview of Cold Electronics Development

HUCHENG CHEN

BROOKHAVEN NATIONAL LABORATORY

OCTOBER 12TH, 2016

BROOKHAVEN NATIONAL LABORATORY

a passion for discovery

U.S. DEPARTMENT OF ENERGY | Office of Science

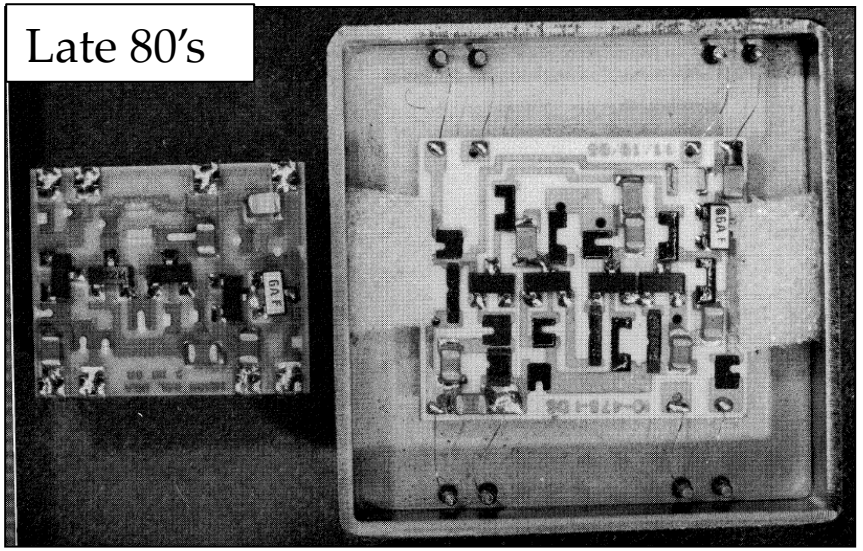
Outline

- Cold Electronics Development
  - A Brief History of Cold Electronics
  - Advantages of Cold Electronics
  - R&D on CMOS Cold Electronics
- Cold Electronics System in LAr TPC Experiments
  - SBND
  - ProtoDUNE-SP
- Summary

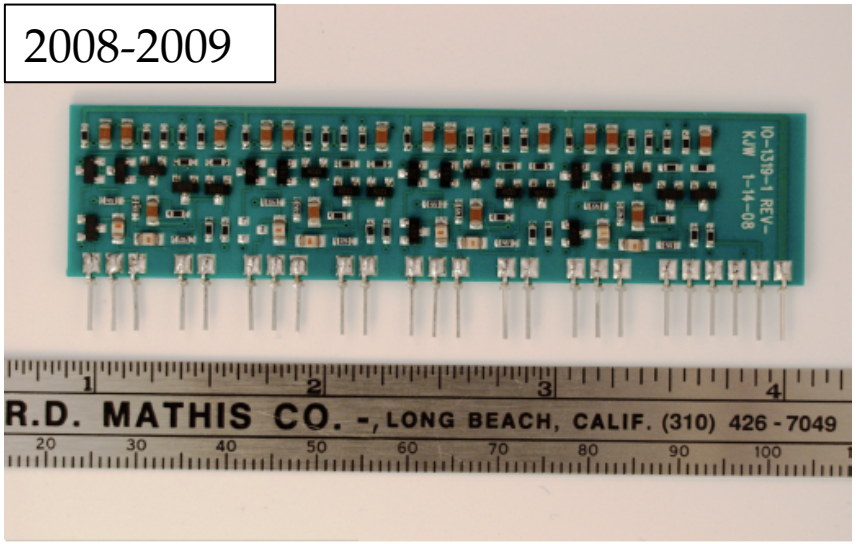
A Brief History of Cold Electronics

- Cryogenics Front-End based on JFET
- Technology mature and available as of today
  - Reliability issues require a careful choice of component and high reliability assembly
  - Ceramic hybrid with co-fired traces and surface mount components properly tested
- Helios-NA34
  - Liquid Argon calorimeter
  - 576 preamplifiers
  - Operation: 4 years, multiple cool-downs
  - Failure: 1 caused by mechanical contact
- Several years of experience
  - ***MicroBooNE front-end design started from JFET as well***

Late 80's

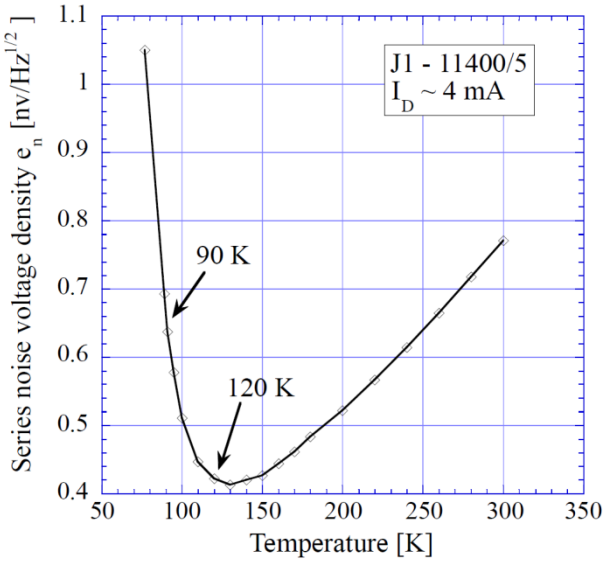


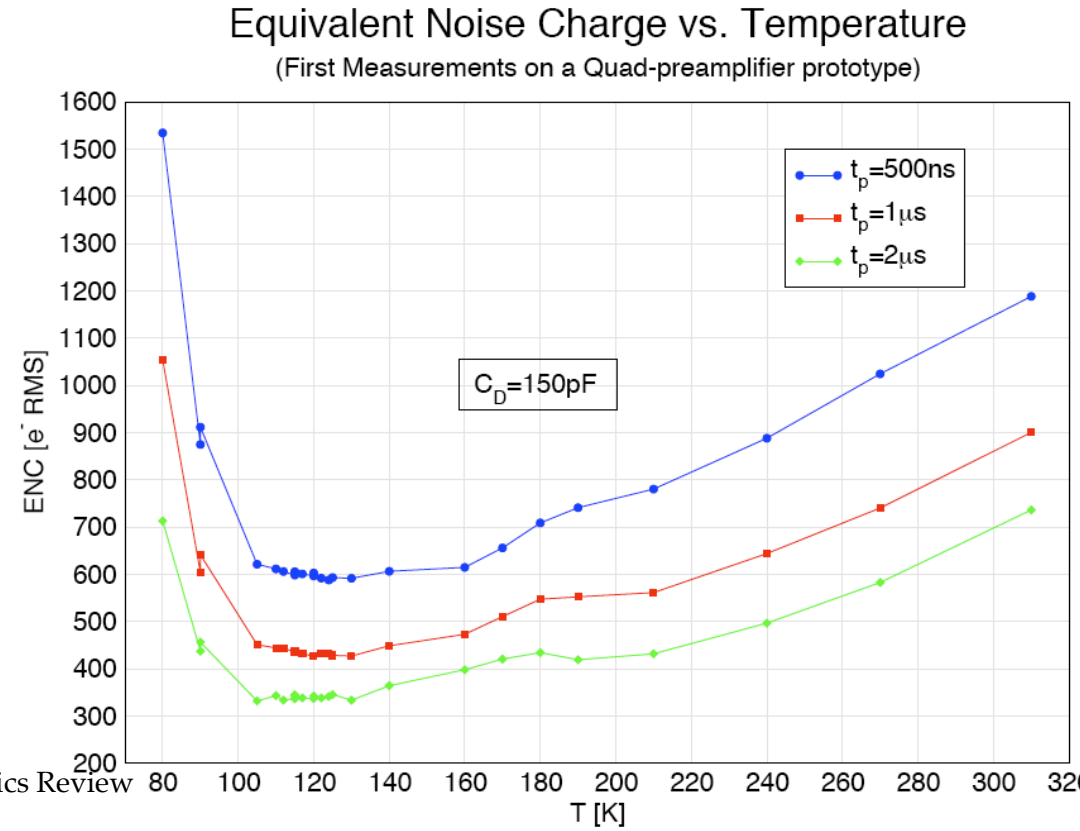
2008-2009



Performance of Cold Electronics (JFET)

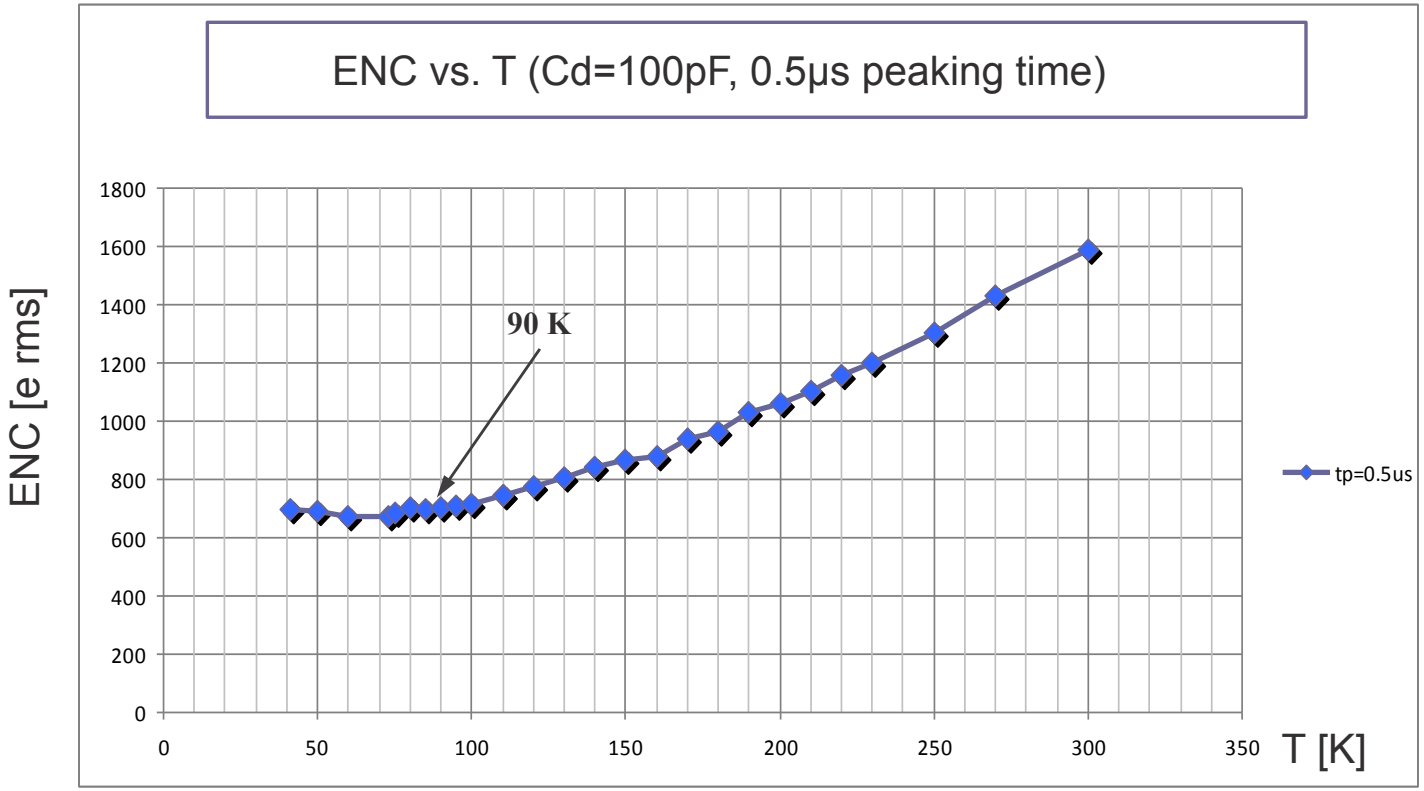
- JFET based preamplifier designed for MicroBooNE
- Bulk mobility and transconductance increase as temperature decreases, carrier freeze out causes ENC increasing when temperature lower than ~100K
  - ***MicroBooNE originally planed to operate JFET in GAr phase to improve the noise performance***





Performance of Cold Electronics (CMOS)

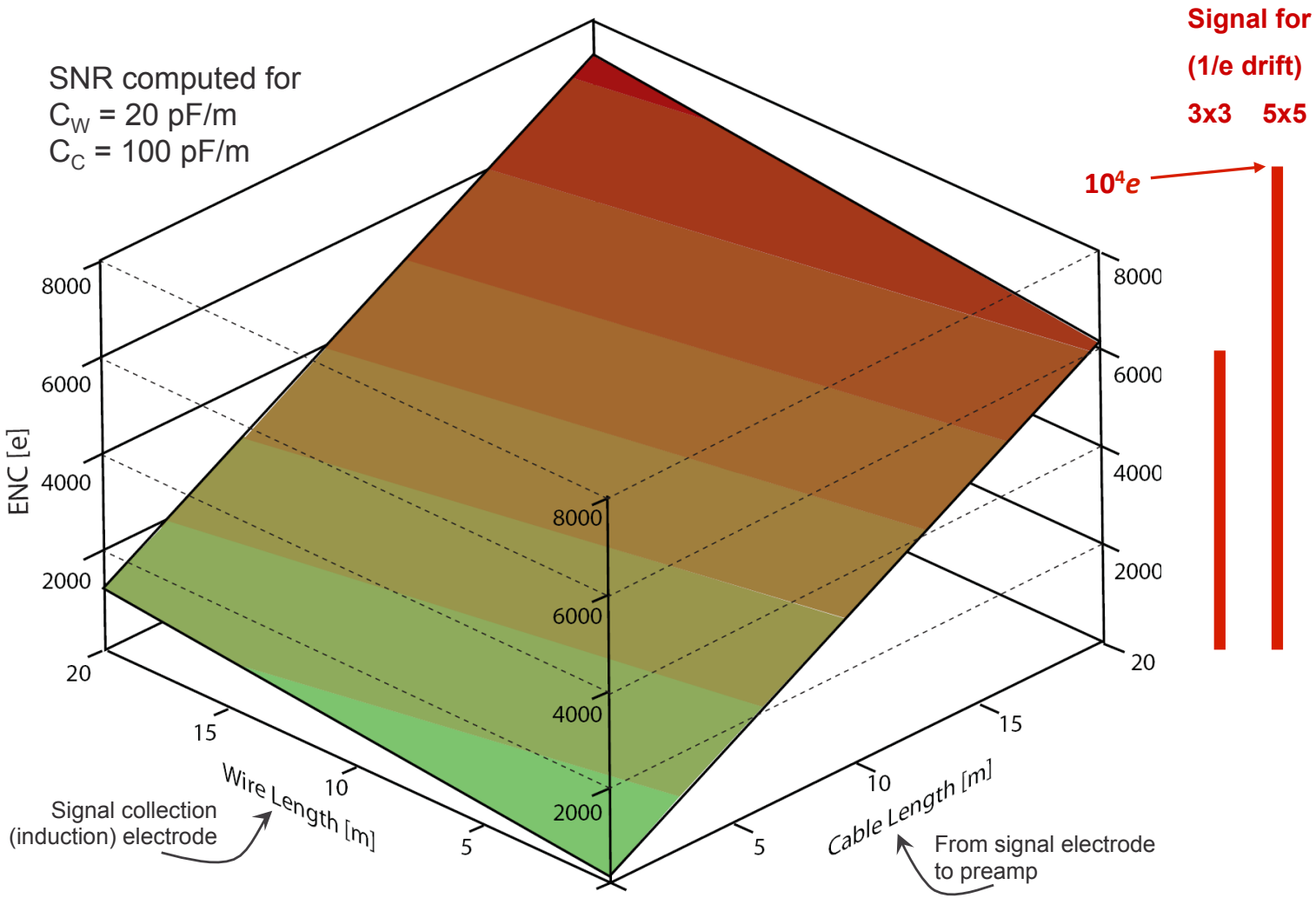
- Test result of existing ASIC in 0.25 *μm (not designed for LAr)*
- CMOS in LAr has less than half the noise as that at room temperature, higher mobility and higher transconductance/current ratio
- ***MicroBooNE has adopted the cryogenic CMOS analog front end ASIC developed for LBNF/DUNE LAr TPC program in 2010***



Motivation of Cold Electronics

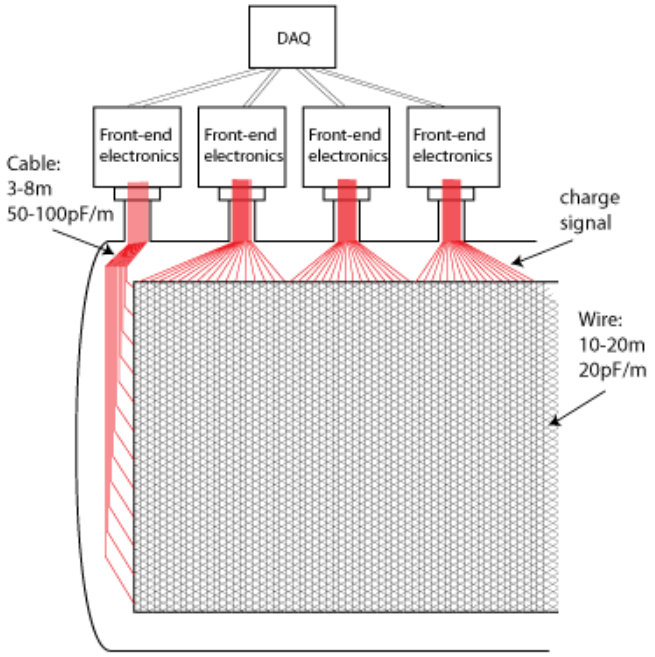
- Cold electronics decouples the electrode and cryostat design from the readout design. With electronics integral with detector electrodes the noise is independent of the fiducial volume (signal cable lengths), and much lower than with warm electronics
  - The amplifier serial input noise, $e^2 \propto C_d^2/g_m$, linearly increases with detector and cable capacitance, C_d, and decreases with input stage transconductance, g_m
- Signal multiplexing results in large reduction in the quantity of cables (less outgassing) and the number of feed-throughs/ cryostat penetrations
- R&D of CMOS cold electronics started in 2008
  - ***The cold electronics development for LAr TPCs was launched, before the final decision for LAr TPC (and not for Water Cherenkov) for LBNF/DUNE had been made***
  - MicroBooNE started with plans for JFET's and, the FE ASIC caught up with MicroBooNE delays

Advantages of Cold Electronics



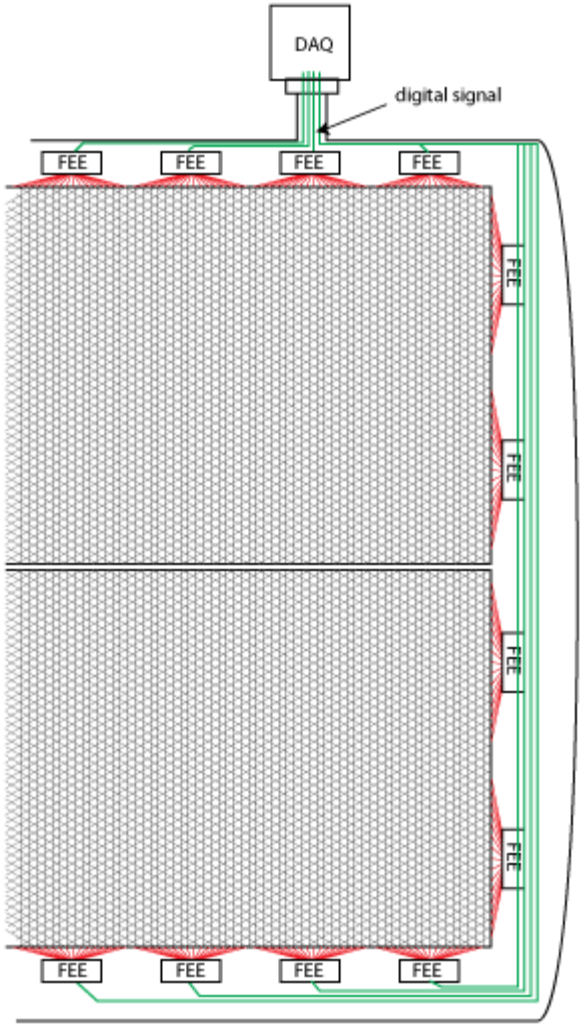
Advantages of Cold Electronics

- A typical readout configuration with warm electronics: long cables connect the sense wires to the FEE, resulting in large electronics noise. To reduce the cable length, one has to implement cold feed-throughs below the liquid level, which increases the cryostat complexity.



Advantages of Cold Electronics

- Having front-end electronics in the cryostat, close to the wire electrodes yields the best SNR
- Highly multiplexed circuits with fewer digital output lines not only greatly reduce the number of cryostat penetrations, but also give the designers of both the TPC and the cryostat the freedom to choose the optimum configurations



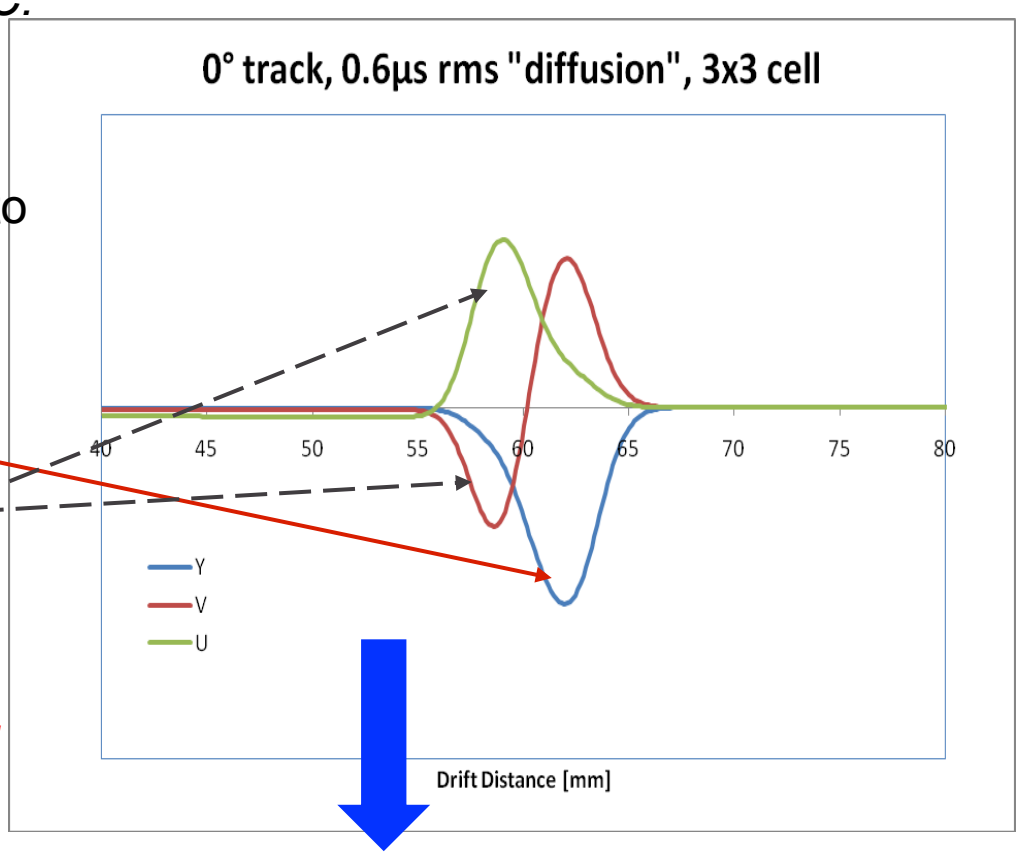
Signals in LArTPC

Charge signal:

- A 3mm MIP track should create *210keV/mm x 3mm /23.6eV/e = 4.3fC.*
- After a 1/3 initial recombination loss: *~2.8fC*
- Assume the drift path to equal the charge life time, reducing the signal to 1/e≈0.368.
- The expected signal for *3mm* wire spacing is then ≈*1fC=6250 e*, … and for *5mm, ≈10^4 e*, for ***the "collection signal"***.
- The induction signals are smaller

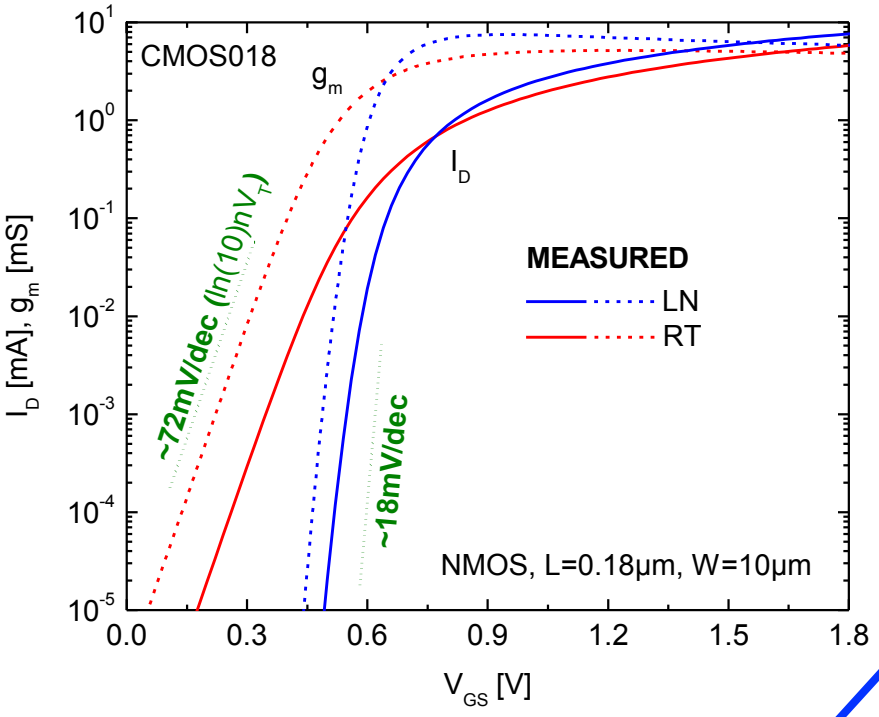
- The ***time scale*** of TPC signals is determined by the ***wire plane spacing*** and ***electron drift velocity***, *(~1.5 mm/μs at 500 V/cm)*.

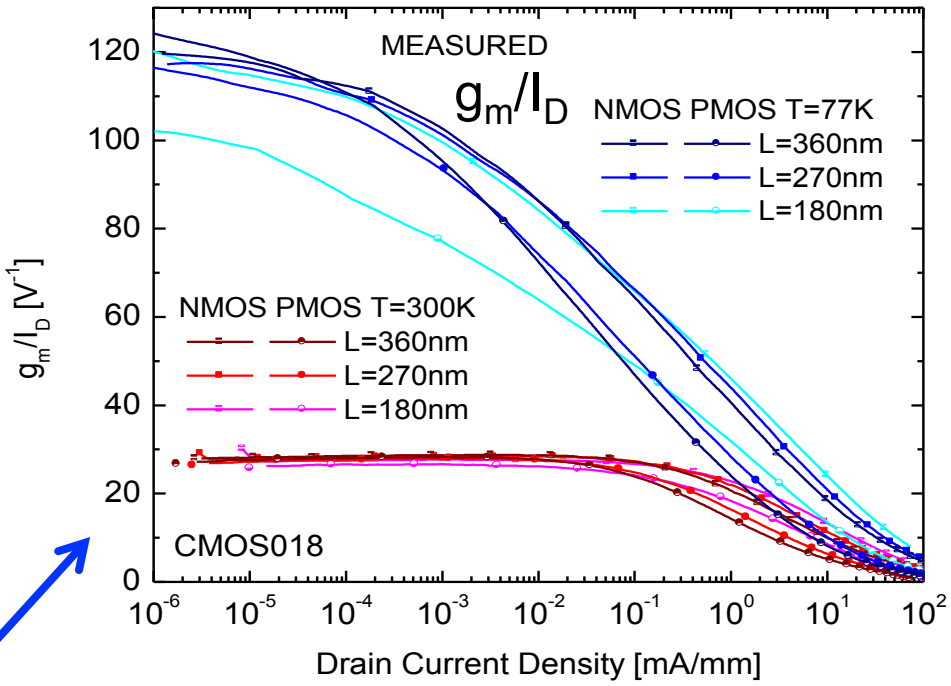
Induced Current Waveforms on 3 Sense Wire Planes:



Sampling rate ***≤ 2 Ms/s***

CMOS Characteristics in LAr



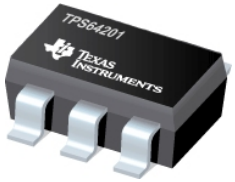


Transconductance/ drain current

$$\frac{g_m}{I_D} \rightarrow \frac{q}{nk_BT} = \begin{cases} \sim 30 \ \ at \ \ T = 300K \\ \sim 116 \ \ at \ \ T = 77K \end{cases}$$

At 77-89K, charge carrier ***mobility*** in silicon *increases* and ***thermal fluctuations*** *decrease* with ***kT/e***, resulting in a ***higher gain, higher*** g_m/I_D, ***higher speed*** and ***lower noise***.

Cold Electronics

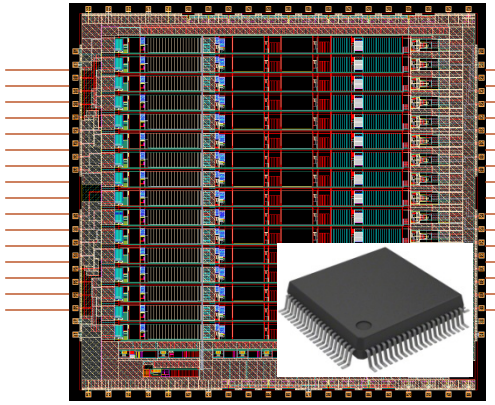


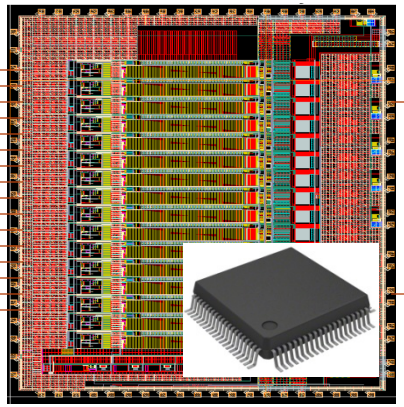
voltage regulation
(COTS)
(< 100mV dropout)

Front end ASIC
~ 5mW/ch.

ADC ASIC
~ 5mW/ch.

FPGA (COTS)
~ 8mW/ch.



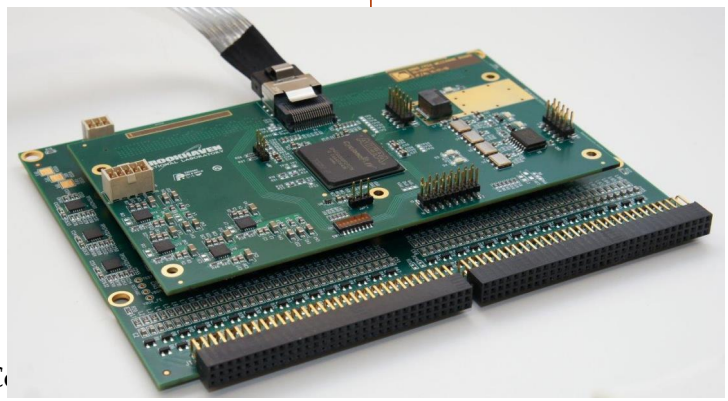


overall 128:4
multiplexing

8 x

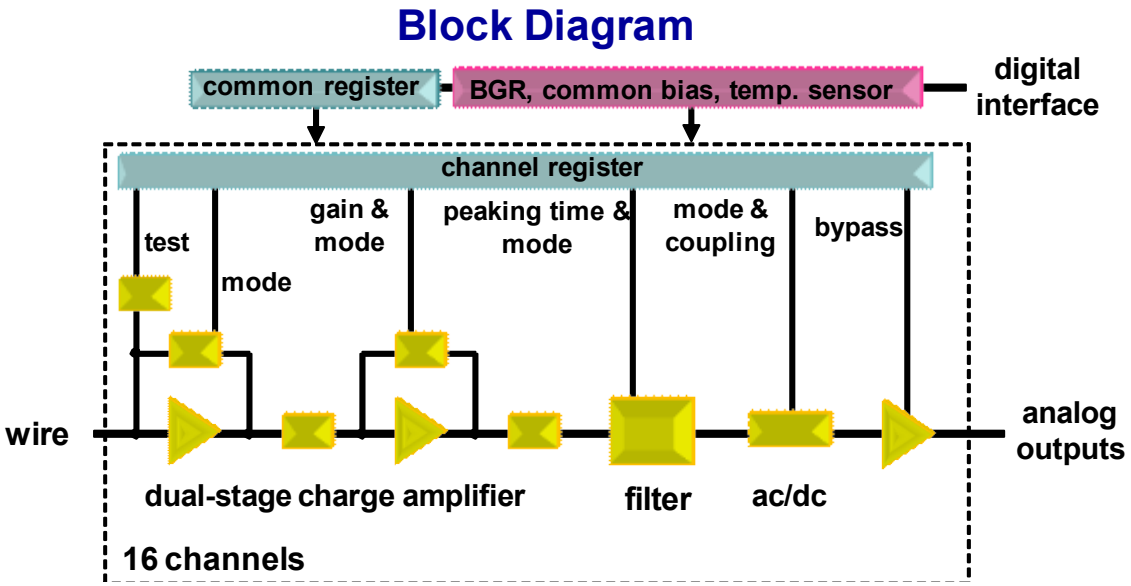
1 x

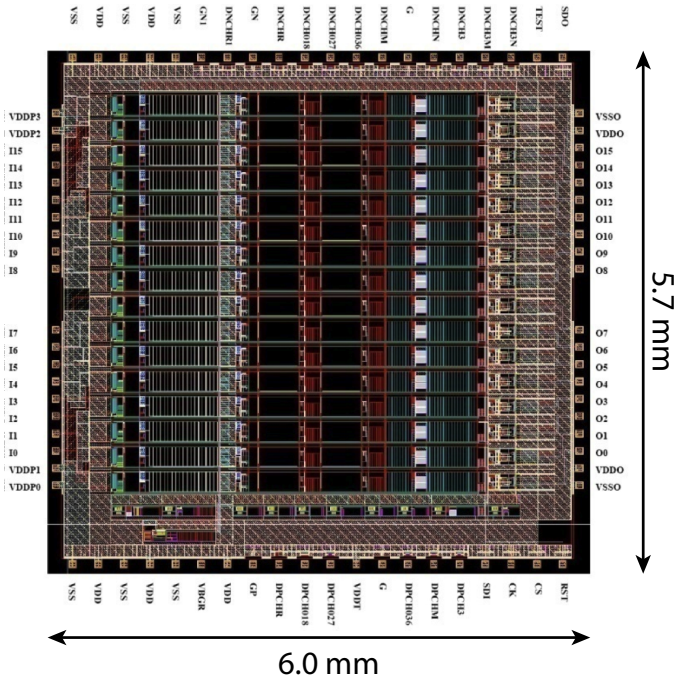
A Complete Front End Readout Chain for SBND and ProtoDUNE-SP TPC



Front end mother board assembly serving 128 wires
~ 2.4 W

Front-End ASIC

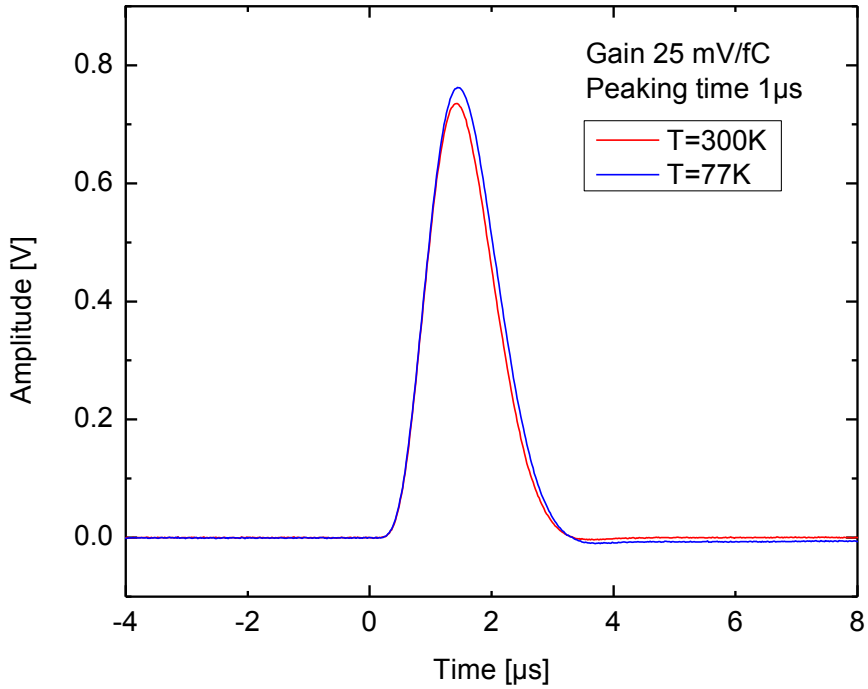




- 16 channels, programmable
- charge amplifier, high-order filter
- adjustable gain: 4.7, 7.8, 14, 25 mV/fC
  (charge 55, 100, 180, 300 fC)
- adjustable filter time constant
  (peaking time 0.5, 1, 2, 3 μs)
- selectable collection/non-collection mode
  (baseline 200, 900 mV)
- selectable dc/ac coupling (100μs)
- ***build in pulse generator with 6-bit DAC***

- rail-to-rail analog signal processing
- band-gap referenced biasing
- temperature sensor (~ 3mV/°C)
- 136 registers with digital interface
- ~ 5.5 mW/channel (input MOSFET 3.9 mW)
- single MOSFET test structures
- ~ 16,000 MOSFETs
- designed for 77K-300K operation
- designed for long lifetime
- tech. CMOS 180 nm, 1.8 V, 6M, MIM, SBRES

FE ASIC - Programmability



Bandgap Reference

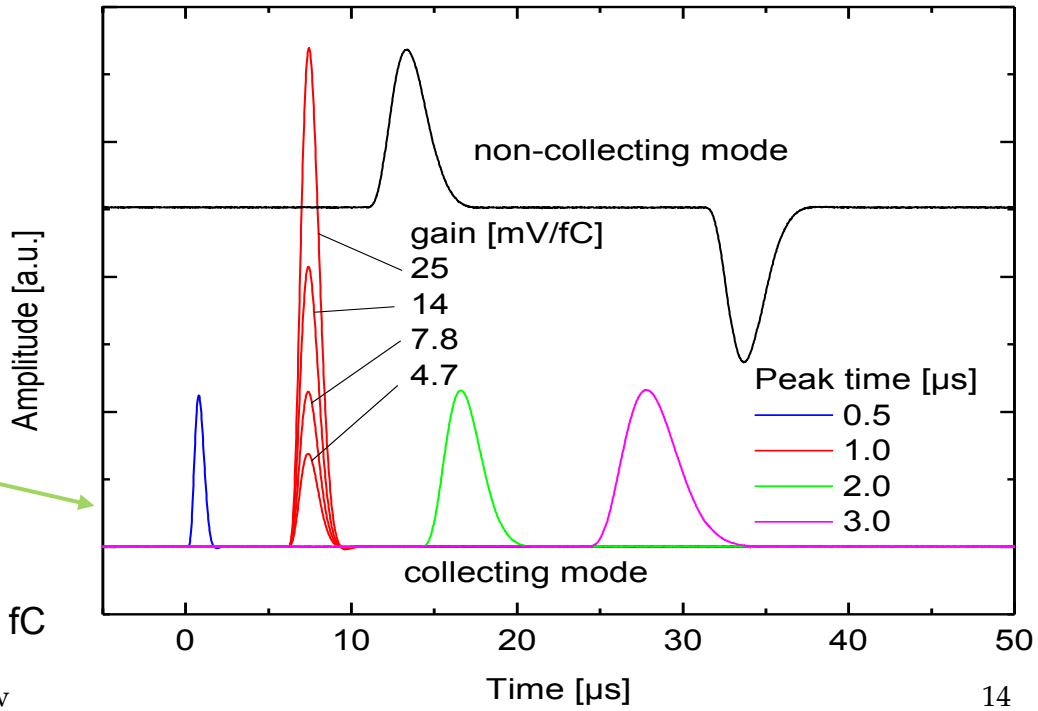
$$V_{BGR} \approx \begin{cases} 1.185\ V \ \text{at}\ 300\ ^{\circ}K \\ 1.164\ V \ \text{at}\ 77\ ^{\circ}K \end{cases}$$

variation ≈ 1.8 %

Temperature Sensor

$$V_{TMP} \approx \begin{cases} 867.0\ mV \ \text{at}\ 300\ ^{\circ}K \\ 259.3\ mV \ \text{at}\ 77\ ^{\circ}K \end{cases}$$

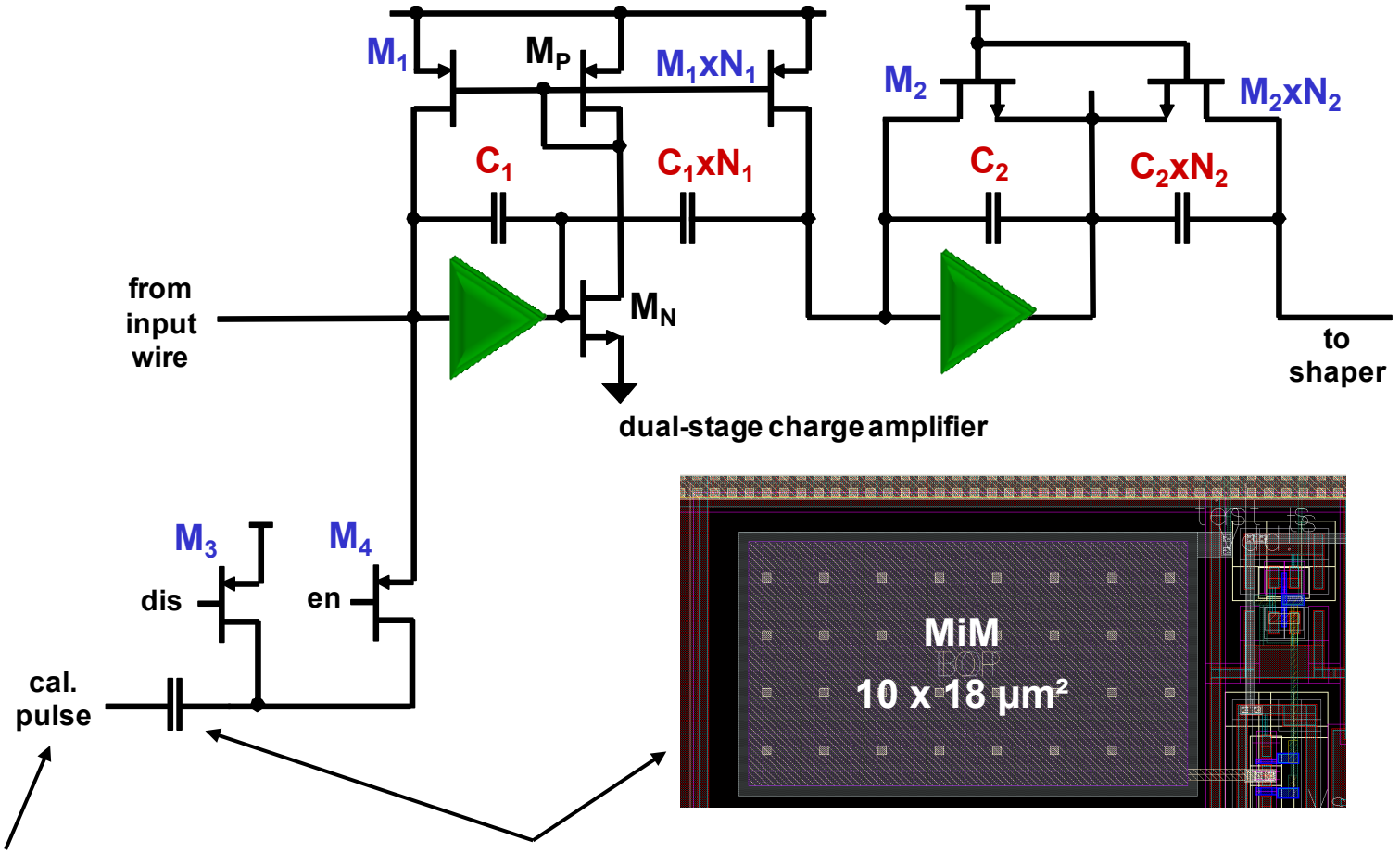
~ 2.86 mV / °K



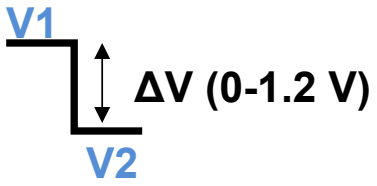
Adjustable gain, peaking time and baseline

maximum charge 55, 100, 180, 300 fC

FE ASIC - Calibration Circuit



external pulse generator



injection capacitor (per-channel enable)

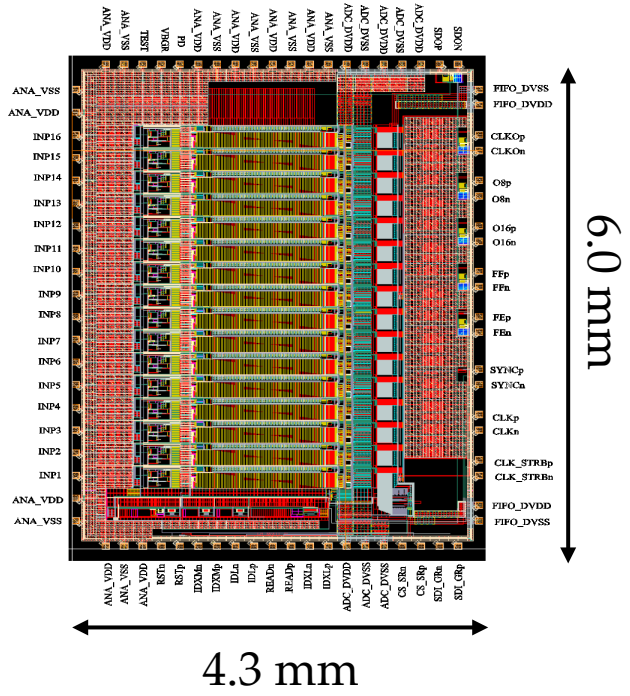
- nominal value: 198 fF
- same-run non-uniformity 0.25 % rms
- run-to-run non-uniformity 2.5 % rms
- measured: 184 fF at 300 K
  183 fF at 77 K (0.5 %)

$$\Delta Q = C_{inj} \cdot \Delta V$$

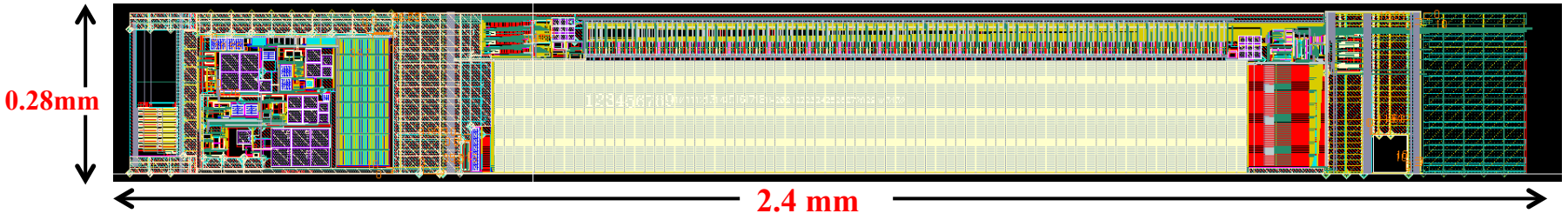
↓

0-230 fC

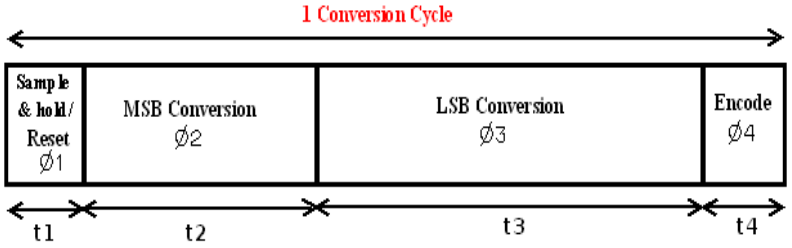
ADC ASIC



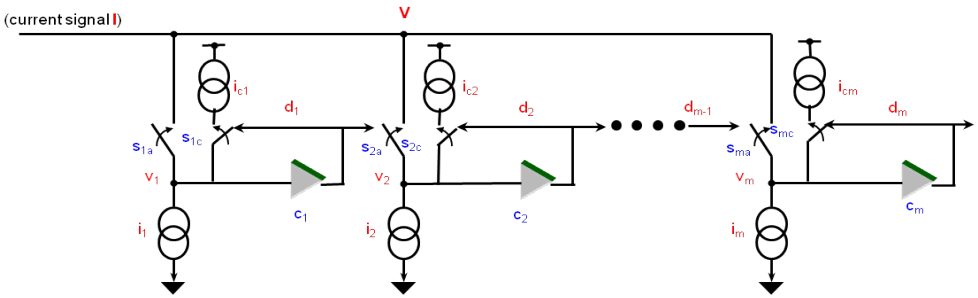
- 16 channels, programmable
- sample/hold
- 12-bit ADC at 2MS/s sampling rate
- current-mode domino architecture
- FIFO 192s bit wide x 32 bits deep
- multiplexer 8:1 or 16:1
- serializer 12:1
- adjustable offsets
- ~4.5 mW/ch.
- power-down modes
- ~ 320,000 MOSFETs
- designed for 77-300Koperation
- designed for long lifetime
- tech. CMOS 180nm, 1.8 V, 6M, MIM, SBRES



ADC Operation & Functions



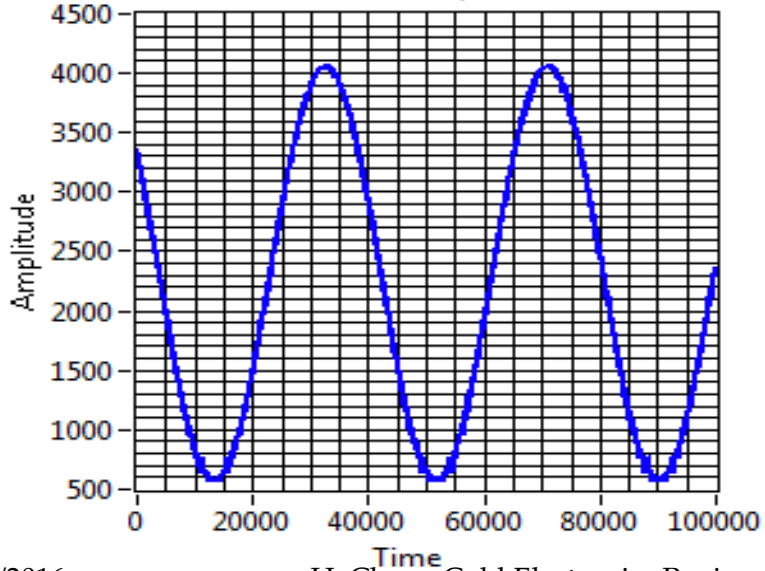
4-phase ADC conversion
- sampling / reset
- MSBs Conversion
- LSBs Conversion
- encoding

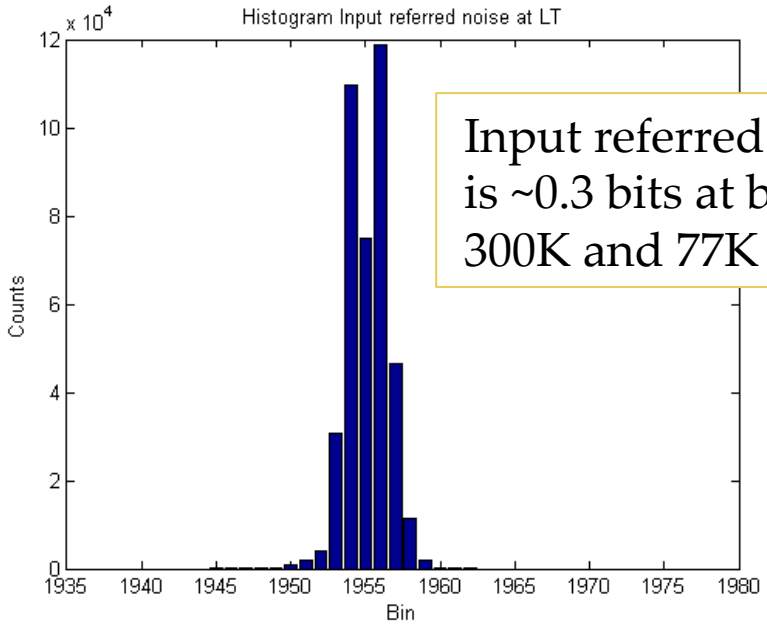


Current-mode domino architecture, 2 steps

MSB: 6 bits → 1 MSB cell = 64 LSB cells
- 1 LSB cell = 500 nA
- 1 MSB cell = 32 uA

Sinusoidal sampled in LN2

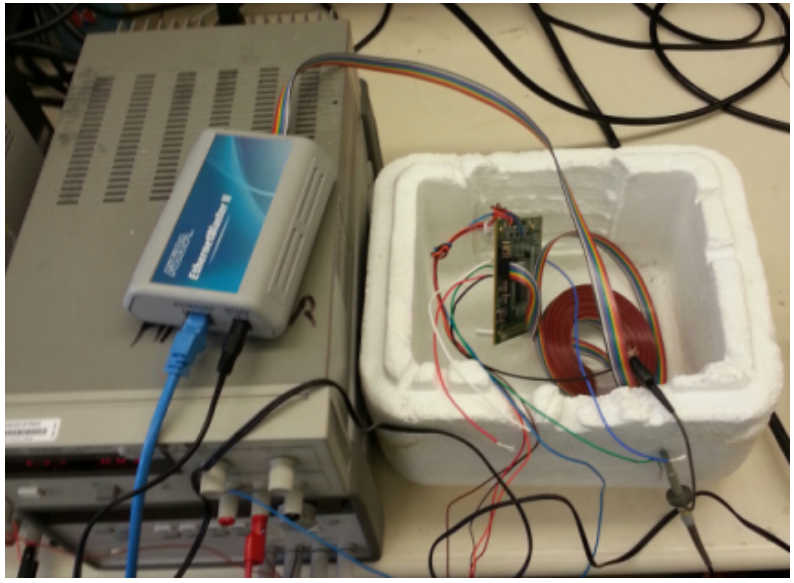




Input referred noise is ~0.3 bits at both 300K and 77K

Cold FPGA

Vendor	Family	Technology	Speed of GTX [Gbps]	# of GTX	Memory [Mbit]	Core Voltage [V]	Status	
ALTERA	Arria GX	90nm	3.125	4 - 12	1.2 - 4.5	1.2	Tested by BNL	✔
ALTERA	Arria II	40nm	6.375	8 - 24	2.9 - 16.4	0.9	Tested by BNL	✗
ALTERA	Stratix II GX	90nm	6.375	4 - 20	1.4 - 6.7	1.2	Tested by SMU	✔
ALTERA	Cyclone IV E	60nm	N/A	N/A	0.3 - 3.9	1.0, 1.2	Tested by BNL	✔
ALTERA	Cyclone IV GX	60nm	3.125	2 - 8	0.5 - 6.5	1.2	Tested by BNL	✔
ALTERA	Cyclone V GX	28nm	3.125	4 - 12	1.2 - 12.2	1.1	Tested by BNL	✗
XILINX	Virtex 5	65nm	6.5	0 - 24	0.9 - 18.6	1.0	Tested by BNL	✗

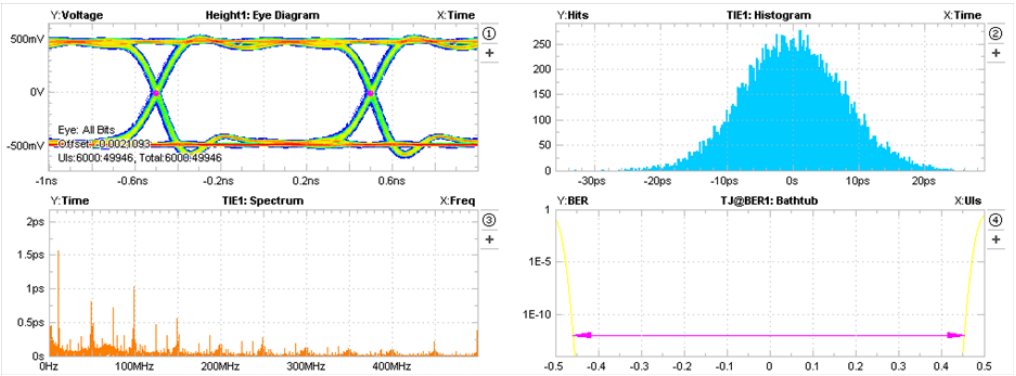


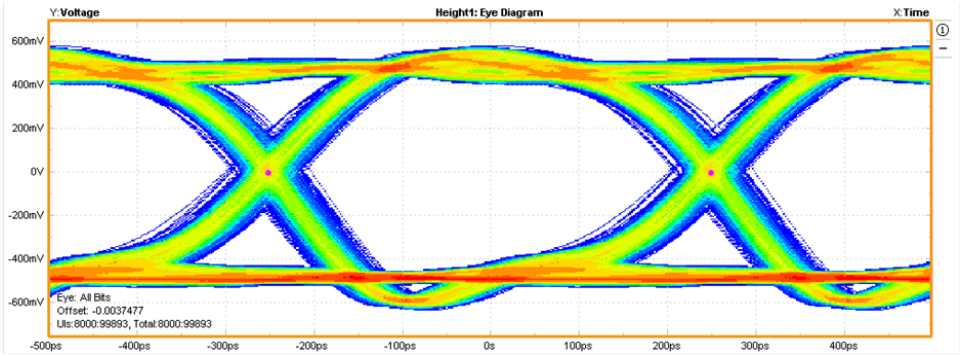
EPCS4	4Mbit	✔
EPCS16	16Mbit	✔
EPCS64	64Mbit	✗
EPCS128	128Mbit	✗
EPCQ16	16Mbit	✔
EPCQ32	32Mbit	✔
EPCQ64	64Mbit	✔
EPCQ128	128Mbit	✔

- FPGA Configuration Methods Tested in LN2
  - JTAG through ~50 feet of single ended cable
  - FPGA flash programming through I2C EPCS/EPCQ

Cold FPGA

Qualified FPGA for Cold Operation





- Test of Cyclone IV GX Transceiver Starter Board in LN_2
  - Transceiver works well at both 1Gbit/s and 2Gbit/s
  - Height
    - 839mV @ 1Gbit/s
    - 823mV @ 2Gbit/s
  - Eye Width
    - 914ps @ 1Gbit/s
    - 357ps @ 2Gbit/s
  - On board SRAM works with BIST
    - 18-Mb SRAM from ISSI IS61VPS102418A-250TQL
    - Cyclone IV GX is running with Nios II processor and utilization of ~80% fabric resources

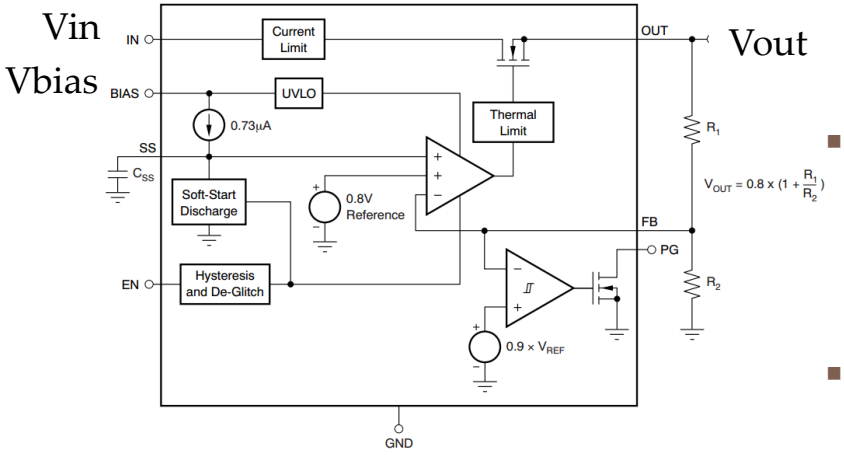
Cold Regulator

Vendor	Part Number	Iout	Vout	Vin	Note
ADI	ADP1708	1A	0.8V to 5.0V	2.5V to 5.5V	
ADI	ADP1741	2A	0.75V to 3V	1.6V to 3.6V	
ADI	ADP124ACPZ-1.8	500mA	1.8V	2.3V to 5.5V	
ADI	ADP130AUJZ-1.8	350mA	1.8V	2.3V to 3.6V	
ADI	ADP170AUJZ-1.8	300mA	1.8V	2.0V to 3.6V	
Globaltech	GS2915L18F	150mA	1.8V	2.3V to 6.0V	
Intersil	ISL9021	250mA	0.9V to 3.3V	1.5V to 5.5V	
Intersil	ISL80113	3A	0.8V to 3.3V	1V to 3.6V	
Linear	LTC3026	1.5A	0.4V to 2.6V	1.14V to 5.5V	
Linear	LTM4616	16A	0.6V to 5V	2.7V to 5.5V	POL Converter
Linear	LTM4619	8A	0.8V to 5V	4.5V to 26.5V	POL Converter
Maxim	MAX8517	1A	0.5V to 3.4V	1.425V to 3.6V	
National	LP38502TJ-ADJ	1.5A	0.6V to 5V	2.7V to 5.5V	
TI	TPS73701	1A	1.2V to 5V	2.2V to 5.5V	
TI	TPS78601	1.5A	1.2V to 5.5V	2.7V to 5.5V	
TI	TPS78618	1.5A	1.8V	2.7V to 5.5V	
TI	TPS78625	1.5A	2.5V	3.0V to 5.5V	
TI	TPS74201	1.5A	0.8V to 3.6V	0.9V to 5.5V	

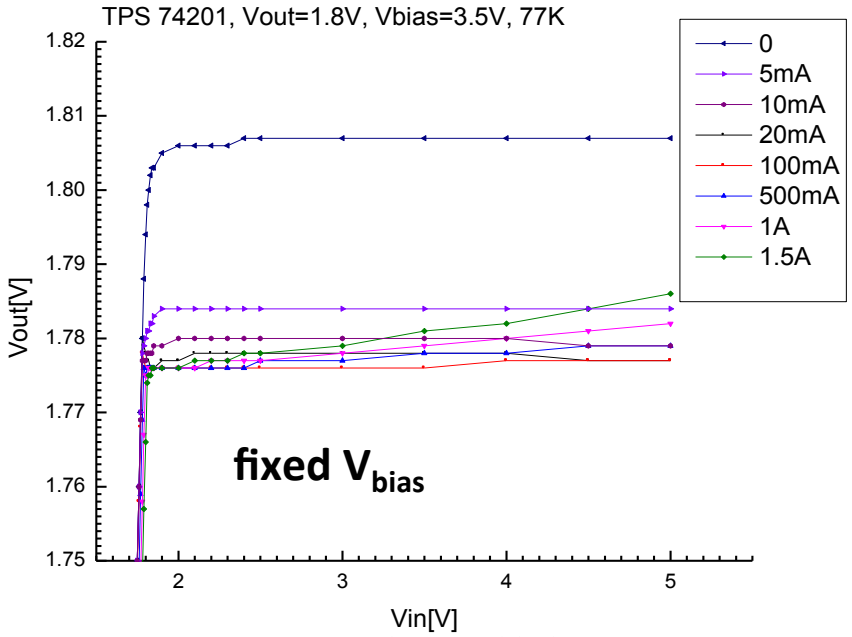
- Cryogenic test of commercial voltage regulators that could be used to power LAr TPC cold electronics
- Stable and low-noise regulation, low dropout (low power) are critical

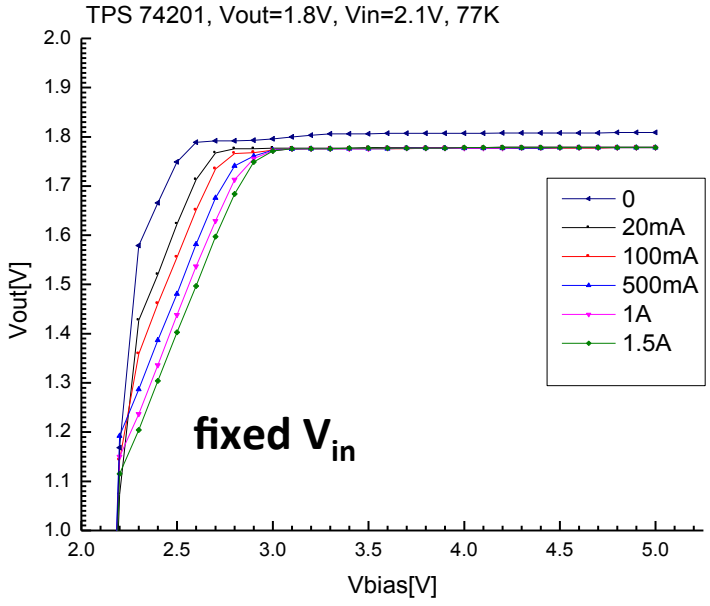
Cold Regulator Qualification

TI TPS74201



- TI TPS742xx voltage regulator family has been identified working well at cryogenic temperature recently
- 1.5A max I_{out}, 0.8V-3.6V adjustable V_{out}, and separate V_{in} makes it an ideal candidate for all of the cold electronics chain
- Low frequency noise will need to be filtered out properly to achieve optimum noise performance of cold electronics

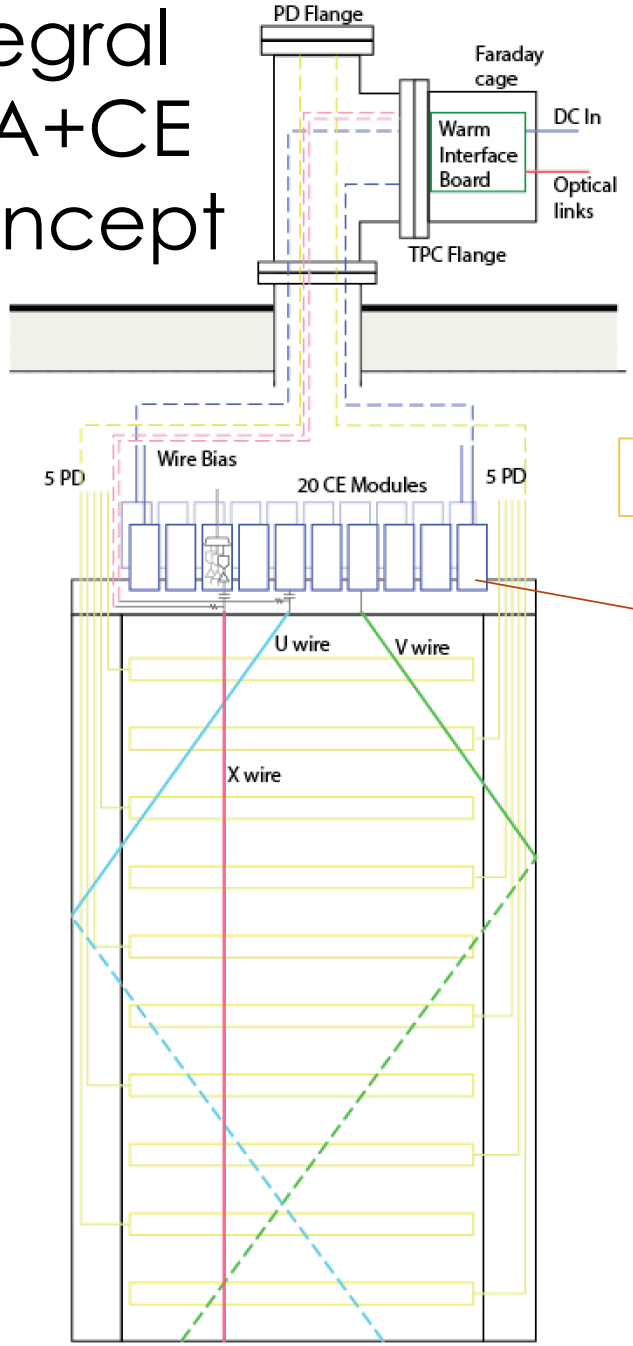


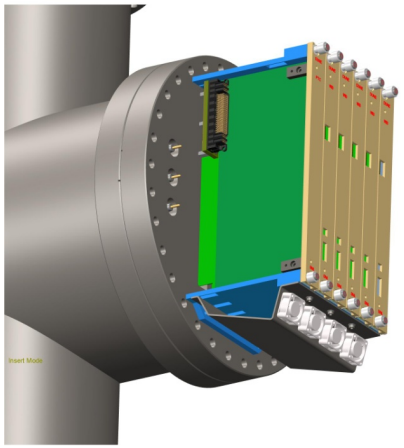


Cold Electronics System in LAr TPC Experiments

- Readout electronics developed for low temperatures (77K-300K) is an ***enabling*** technology for noble liquid detectors for neutrino experiments
  - Front end ASICs are integrated with the TPC electrodes in noble liquid to minimize the capacitance and **noise**
  - On chip **digitization** to convert to digital signals inside detector cryostat
  - **Multiplexing** to high speed serial link, to reduce cable plants, minimize outgassing, make possible the scalability to larger detector volumes
  - **Cold FPGA** to house the flexible algorithms for data processing and data reduction
- Cold electronics is one of three R&D goals ***successfully*** achieved by MicroBooNE experiment
  - Together with non-evacuated single wall cryostat with foam insulation, and 2.5m long drift
- Full cold readout chain with CMOS ASICs and FPGA will be used to instrument the SBND and ProtoDUNE-SP LAr TPC
  - To have a chance at achieving a good performance, **the integral design concept** of APA+CE+Feed-through, plus Warm Interface Electronics with local diagnostic and strict isolation and **grounding rules** will have to be followed

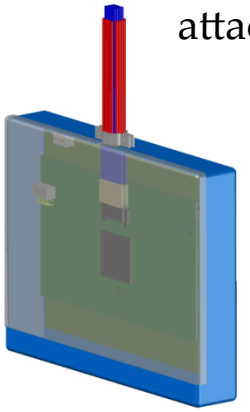
Integral APA+CE Concept

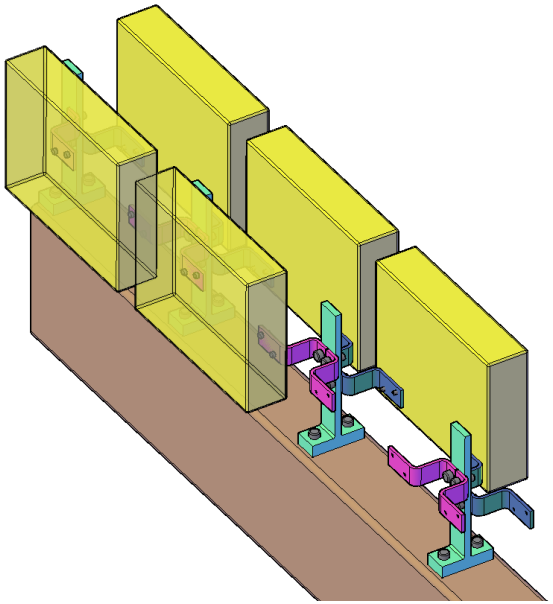




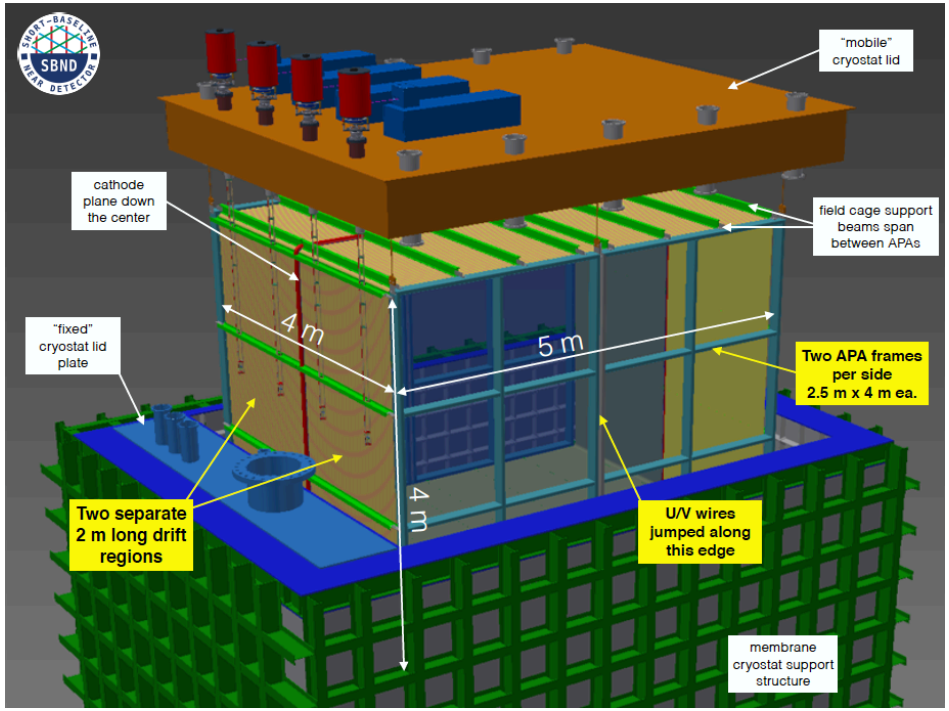
ProtoDUNE-SP

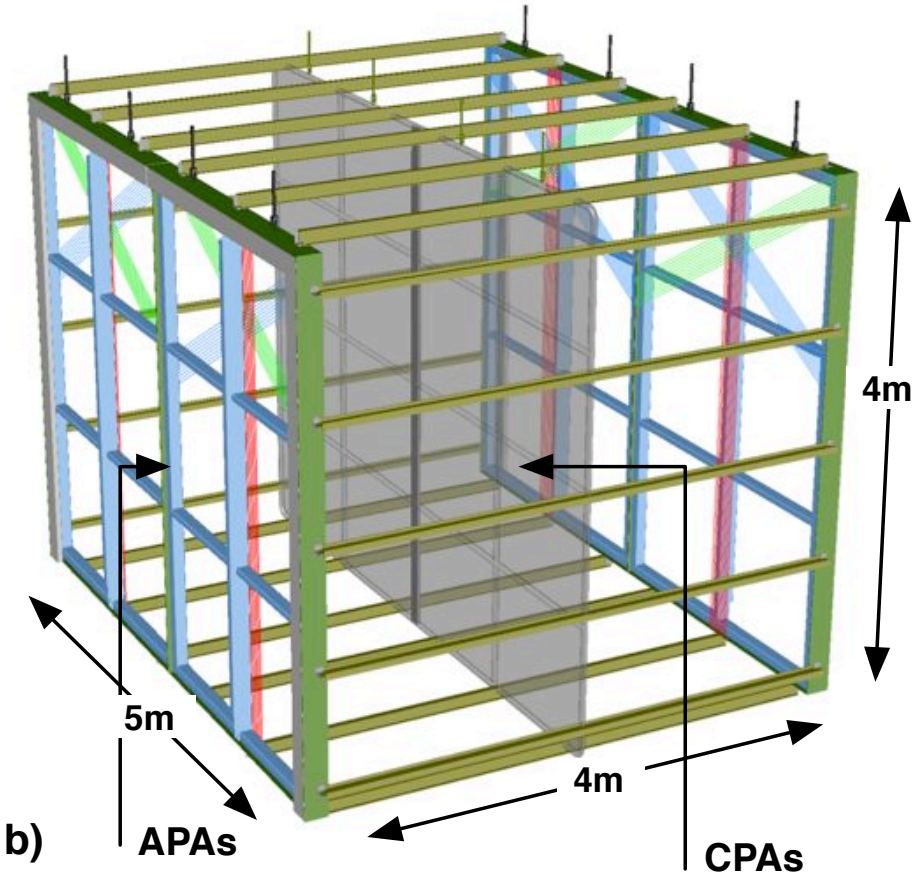
Cold electronics module and its attachment to the APA frame





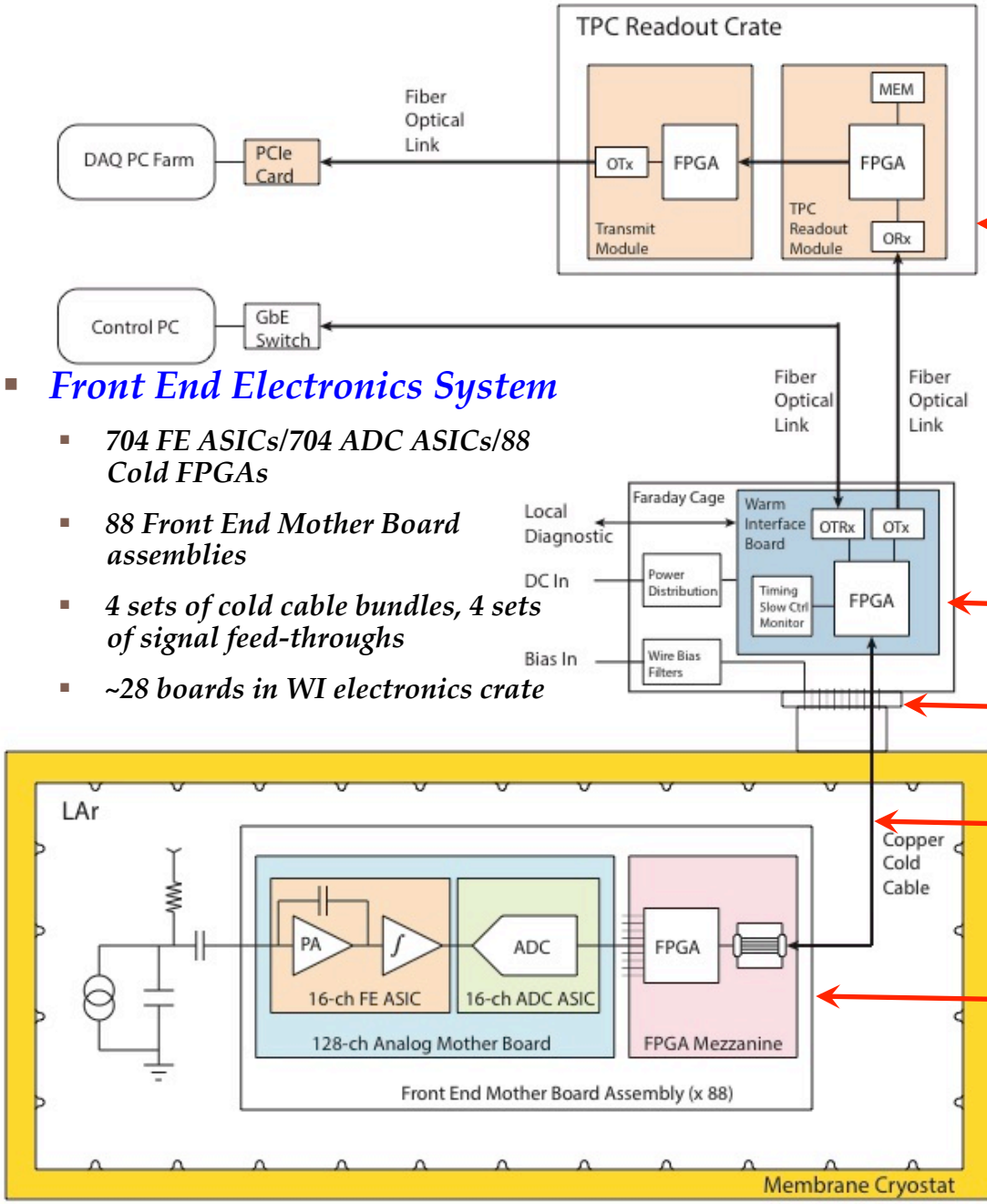
SBND TPC





- SBND TPC: 4 APAs and 2 CPA

SBND TPC Electronics



- ***Front End Electronics System***
  - *704 FE ASICs/704 ADC ASICs/88 Cold FPGAs*
  - *88 Front End Mother Board assemblies*
  - *4 sets of cold cable bundles, 4 sets of signal feed-throughs*
  - *~28 boards in WI electronics crate*

Back End Electronics

Front End Electronics

TPC Readout Electronics

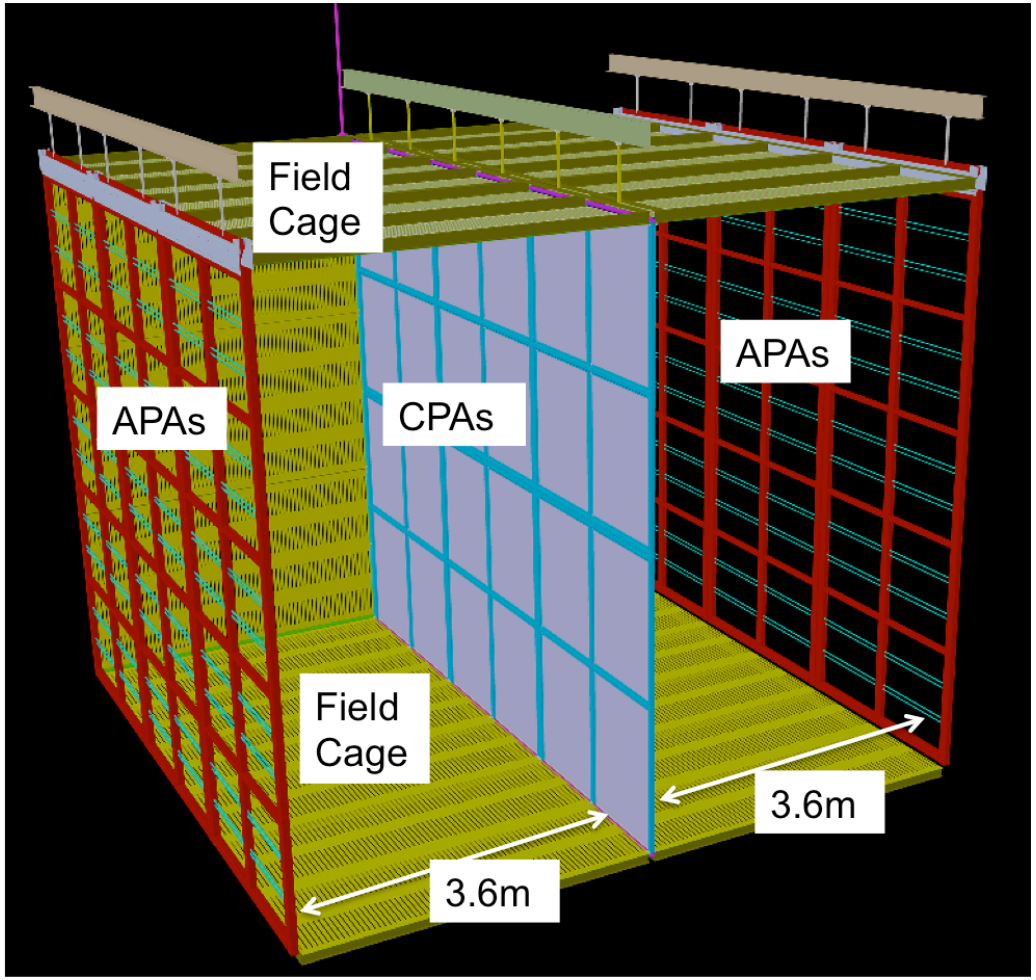
Warm Interface Electronics

Signal Feed-through

Cold Cable

Cold Electronics

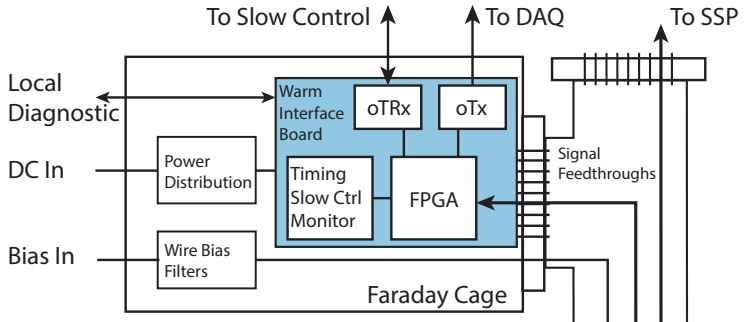
ProtoDUNE-SP

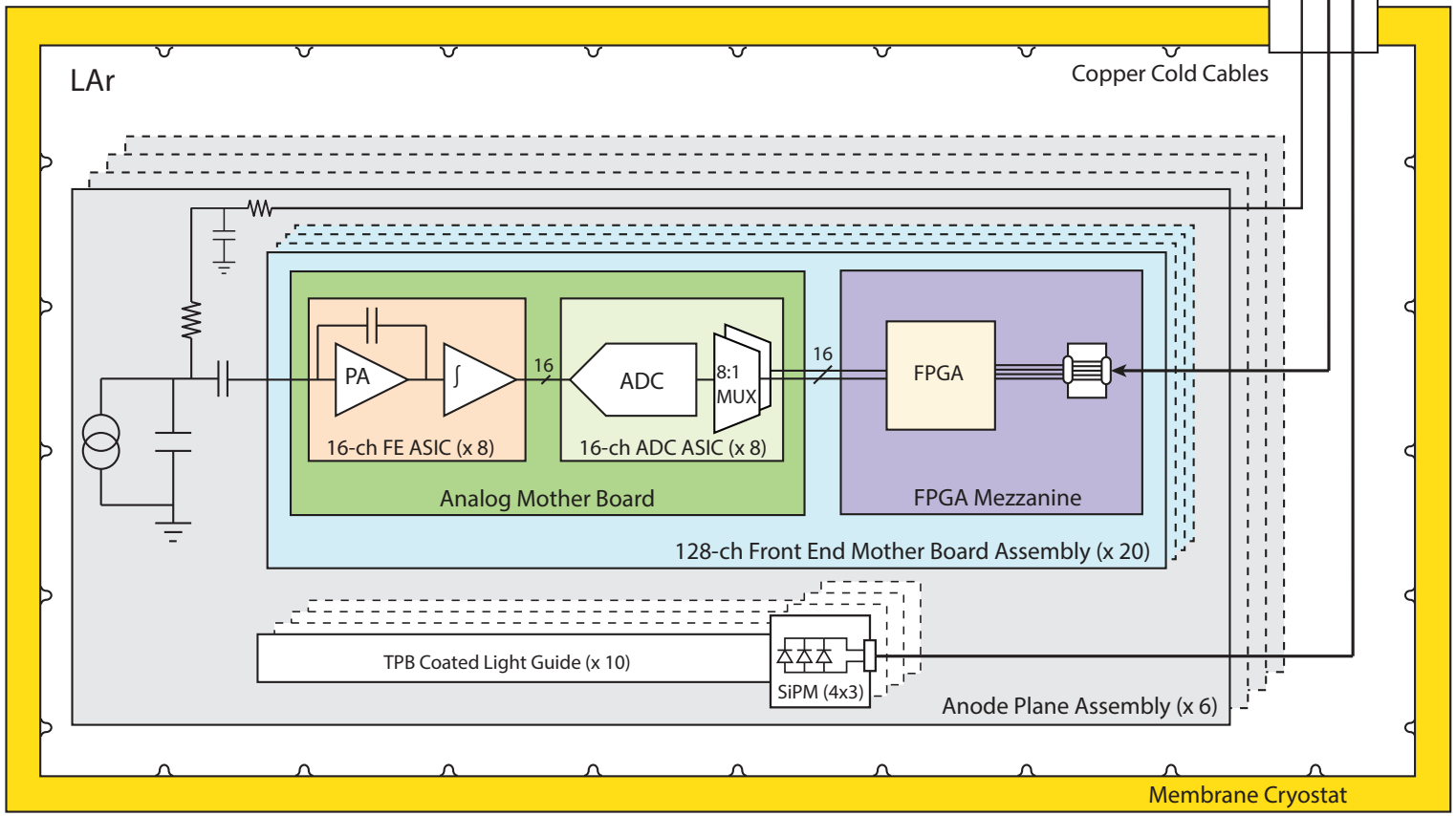


- Single-phase TPC prototype
  - Will sit in H4 beam line @ CERN
  - Consisting of 6 full-size APA's plus CPA's → 2 x 3.6m drift regions
  - Total 15,360 TPC channels
  - Will install photon detectors of different fabrication methods
  - Plan for operation in 2018
- Will be a key test of:
  - Components
  - Construction methods
  - Installation procedures
  - Commissioning
  - Detector response to particles

ProtoDUNE-SP TPC Readout Electronics

- ***Front End Electronics System***
  - ***960 FE ASICs/960 ADC ASICs/120 Cold FPGAs***
  - ***120 Front End Mother Board assemblies***
  - ***6 sets of cold cable bundles, 6 sets of signal feed-throughs***
  - ***~36 boards in warm interface electronics crate***





SBND and ProtoDUNE-SP Cold Electronics System

- SBND Cold Electronics System
  - 704 FE ASICs
  - 704 ADC ASICs
  - 88 Cold FPGAs
  - 88 Front End Mother Board assemblies
  - 4 sets of cold cable bundles
  - 4 sets of signal feed-throughs
  - 24 warm interface boards (WIB)
  - 4 power timing cards (PTC)
  - 1 power timing baseplane (PTB)
- ProtoDUNE-SP Cold Electronics System
  - 960 FE ASICs
  - 960 ADC ASICs
  - 120 Cold FPGAs
  - 120 Front End Mother Board assemblies
  - 6 sets of cold cable bundles
  - 6 sets of signal feed-throughs
  - 30 warm interface boards (WIB)
  - 6 power timing cards (PTC)
  - 1 power timing baseplane (PTB)

SBND and ProtoDUNE-SP Cold Electronics System

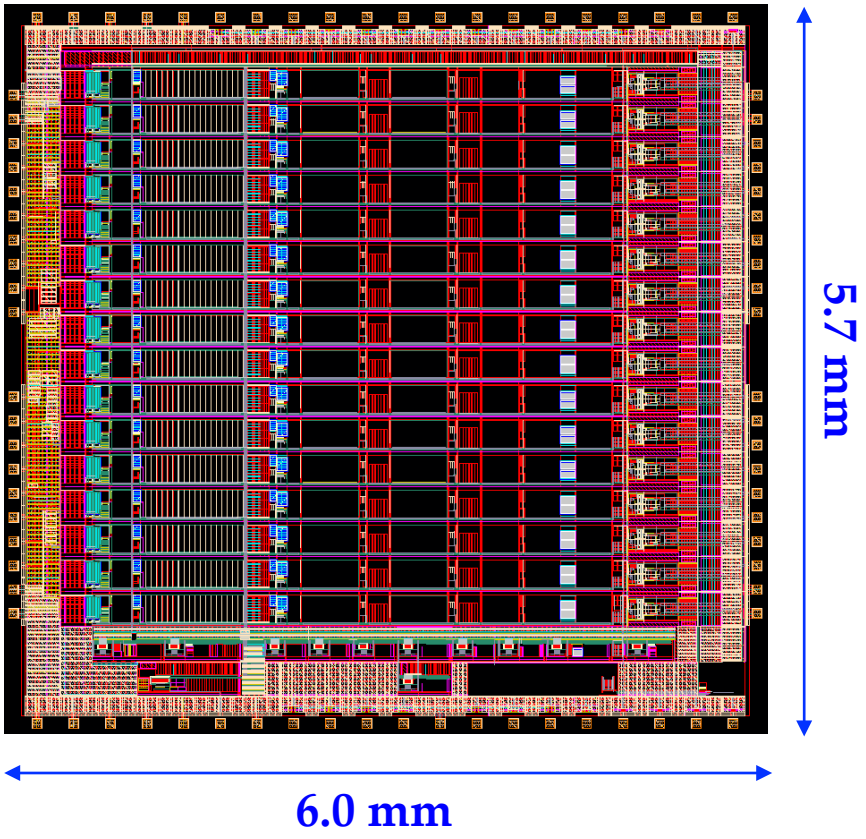
	SBND	ProtoDUNE-SP	Comparison
FEMB	Horizonal & Vertical	Horizontal Only	***Similar***
Cold Cable	3M Data + Samtec Power	Samtec Data + Samtec Power	***Similar***
Feed-through	Custom Flange and Board	Custom Flange and Board	***Similar***
Warm Interface Electronics	WIB+PTC+PTB in Faraday Crate	WIB+PTC+PTB in Faraday Crate	***Similar***
Back End Electronics/DAQ HW	Nevis	RCE/FELIX	***Different***

- SBND and ProtoDUNE-SP share many common development of cold electronics system
- Development of SBND cold electronics system started in early 2015, which provides a head start to ProtoDUNE-SP cold electronics system design

SBND and ProtoDUNE-SP Cold Electronics System

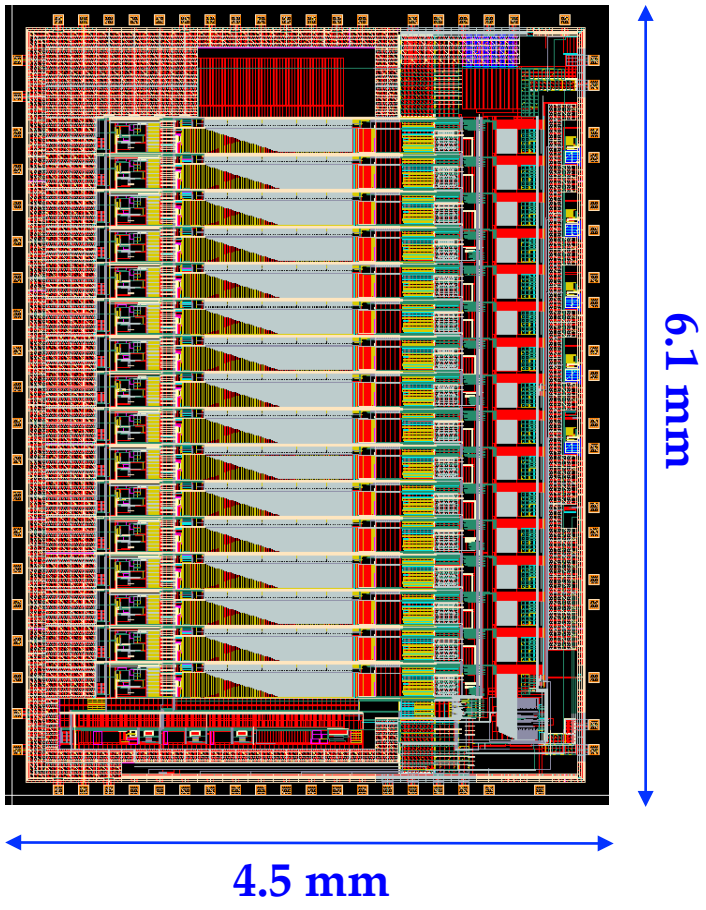
	SBND	ProtoDUNE-SP	Comparison
FEMB			
AM - Analog Mother Board	Horizonal & Vertical	Horizontal Only	***Similar***
FE ASIC	Version P2	Version P2	***Identical***
ADC ASIC	Version P1/P2	Version P1	***Similar***
Cold Voltage Regulator	TPS74201	TPS74201	***Identical***
FM - FPGA Mezzanine	MiniSAS Connector	Samtec Connector	***Similar***
Cold FPGA	ALTERA Cyclone IV GX	ALTERA Cyclone IV GX	***Identical***
Cold Voltage Regulator	TPS74201	TPS74201	***Identical***
Cold Cable			
Data Cable	3M MiniSAS Cable	Samtec Twin-axial Cable	***Different***
Power Cable	Samtec Twisted Pair Cable	Samtec Twisted Pair Cable	***Similar***
Feed-through			
Conflact Flange	Custom Designed	Custom Designed	***Identical***
Flange Board	1 PTC Slot + 6 WIB Slots	1 PTC Slot + 5 WIB Slots	***Similar***
Warm Interface Electronics			
WIB - Warm Interface Board	ALTERA Arria V GX	ALTERA Arria V GT	***Similar***
PTC - Power Timing Card	Unidirectinal Timing System	Bidirectinal Timing System	***Similar***
PTB - Power Timing Backplane	Custom Designed	Custom Designed	***Identical***
WIEC - Warm Infc Electronics Crate	Custom Designed Faraday Cage	Custom Designed Faraday Cage	***Identical***
Back End Electronics/DAQ HW	Nevis	RCE/FELIX	***Different***

Cold FE ASIC



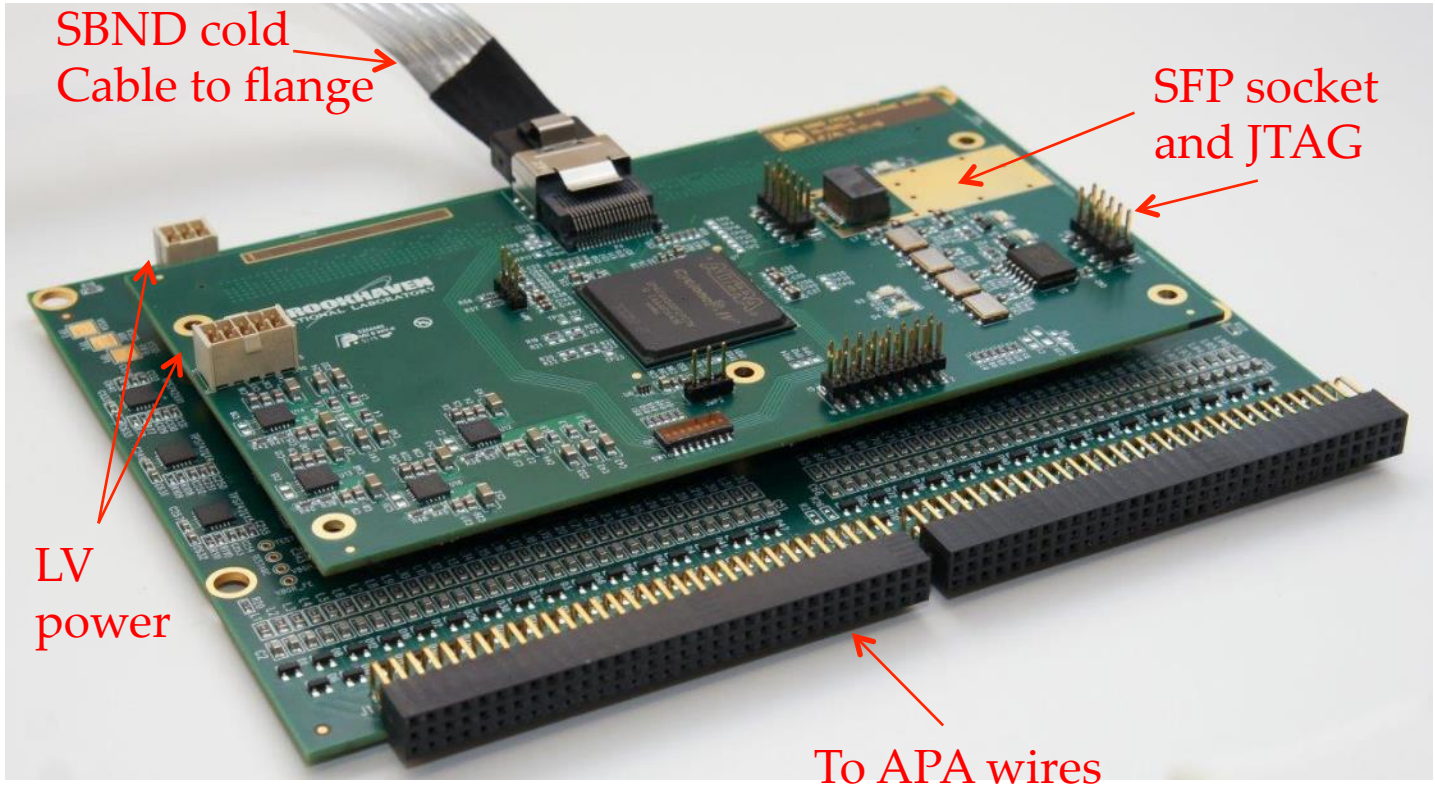
- 16 channels low power (~5.5mW/ch) and low noise analog front end ASIC
- P1 FE ASIC was submitted to MOSIS in early February
- Main new features
  - Integrate internal pulse generator with 6-bit DAC
  - Increase the buffer-off drive capability of last stage
  - Increase front-end bias current (1nA and 5nA) capability
  - Implement smart reset and increase ESD protection
  - Revise GBR start-up circuit and configuration interface
- 240 P1 FE ASICs were delivered in the first week of June
  - Evaluation test started since then
  - Data sheet is on the review page

Cold ADC ASIC



- 16 channels low power (~4.5mW/ch) and 12-bit 2Msps ADC ASIC
- P1 ADC ASIC was submitted in early July
- Main new features
  - Improve ADC INL/DNL
  - Address the early saturation and roll-back
  - Extend soft-control functions
  - Implement power-on default configuration
  - Modify configuration interface and increase ESD protection
  - Revise GBR start-up circuit
- 240 P1 ADC ASICs are expected to be available this week
  - Test platform is ready and being used to test the first wired bonded die
  - Data sheet is on the review page

Front End Mother Board



- 128 channels of digitized TPC wire readout
  - Analog motherboard: 8 FE ASICs/8 ADC ASICs
  - FPGA mezzanine is used for multiplexing and readout of digitized detector signals

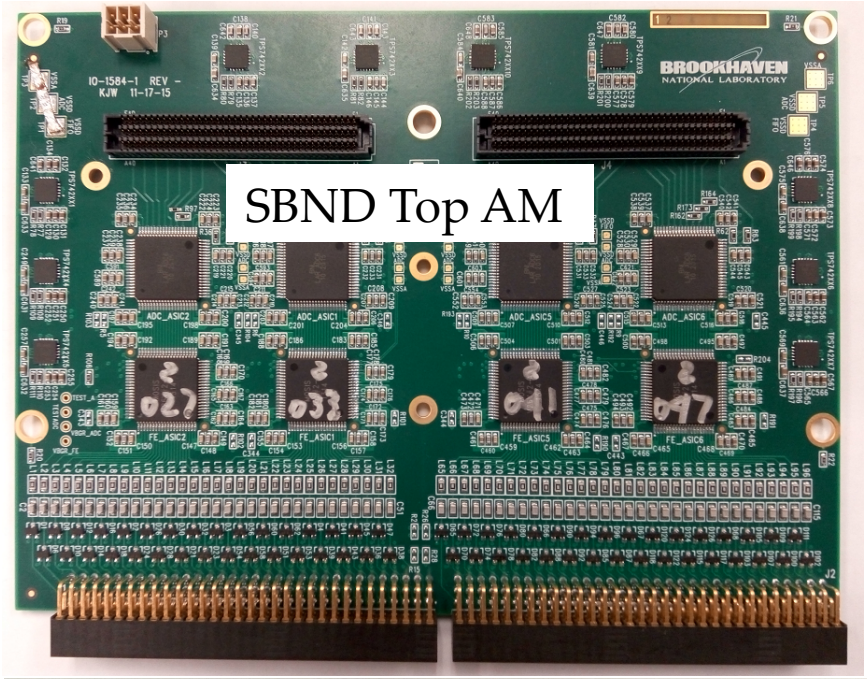
Analog Mother Board

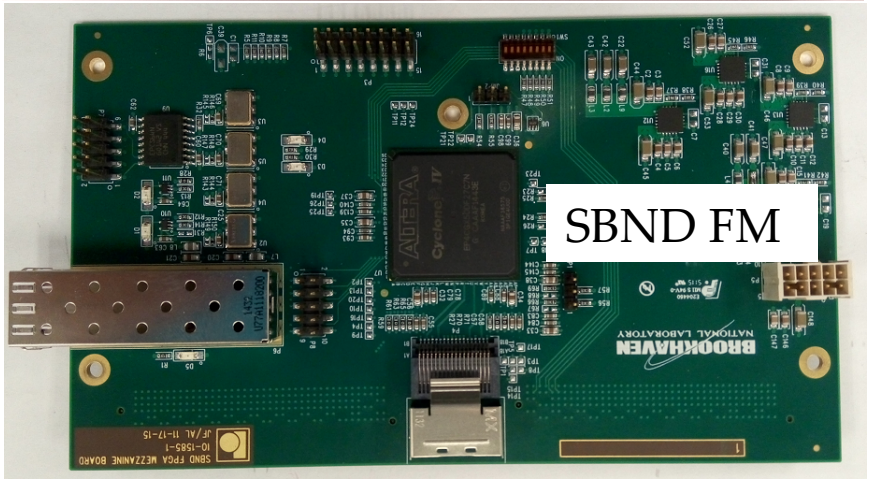
- AM: Analog Mother Board
  - 8 FE ASICs & 8 ADC ASICs
  - 128 FE readout channels
  - Cold voltage regulators: TI TPS74201
- SBND has two versions of analog mother board
  - Top (horizontal) AM: right angle mating connector to geometry board
  - Side (vertical) AM: straight mating connector to geometry board
- ProtoDUNE-SP has one type of analog mother board
  - With straight mating connector to CR board
- SBND side AM and ProtoDUNE AM share the same design
  - ***Two AM designs*** to cover both SBND and ProtoDUNE

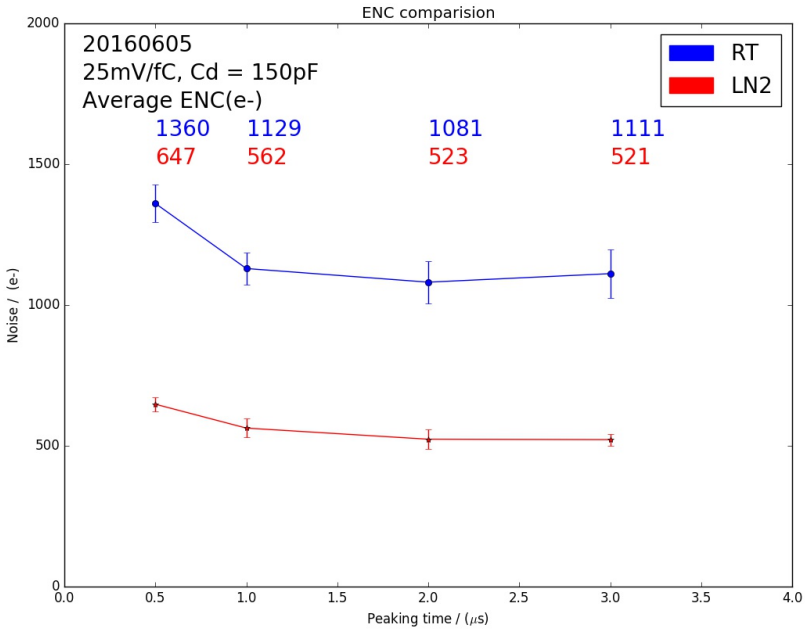
FPGA Mezzanine

- FM: FPGA mezzanine
  - One Cyclone IV GX FPGA
  - 4 serial links @ 1Gb/s to transmit 128 FE readout channels of data
  - Cold voltage regulators: TI TPS74201
  - On board SFP cage for warm test over GbE, not used in the cold
  - Output data connector is mating with the cold cable for data transmission out of cryostat
- SBND FM uses Molex miniSAS connector
  - SBND requires 7 meters of cold cable
  - 3M miniSAS cable is used as data cable
- ProtoDUNE-SP FM uses Samtec HSEC8 connector
  - DUNE far detector requires up to 25 meters of cold cable
  - ProtoDUNE-SP requires 7 meters of cold cable, which shares the same design of the 25 meters of cold cable
  - Samtec custom twin-axial cable assembly is used as data cable

Noise Measurement of FEMB

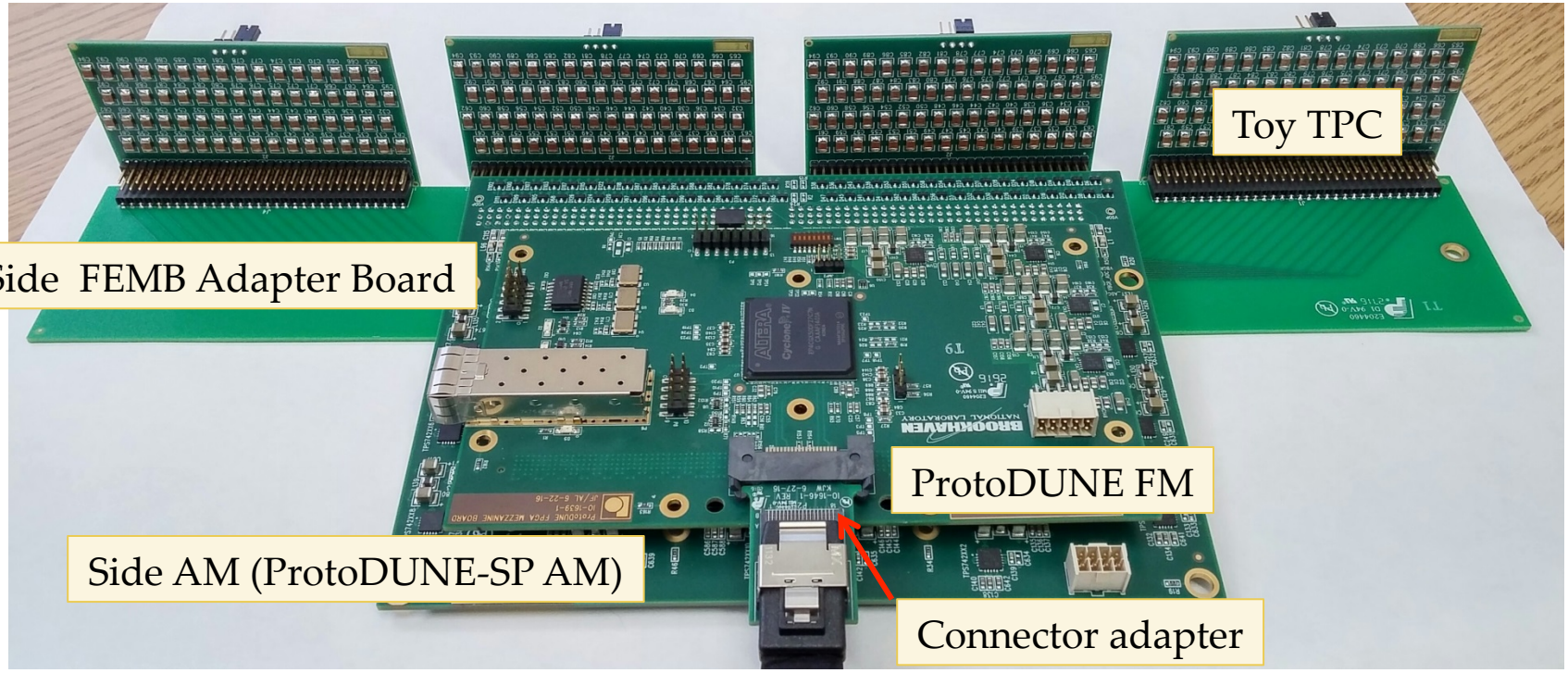






- AM: Analog Mother Board
  - 8 FE ASICs & 8 ADC ASICs
  - 128 FE channels
  - Cold regulators: TI TPS74201
- FM: FPGA mezzanine
  - Cyclone IV GX FPGA
  - MiniSAS connector for SBND
  - Samtec HESC8 connector for ProtoDUNE-SP

Side FEMB

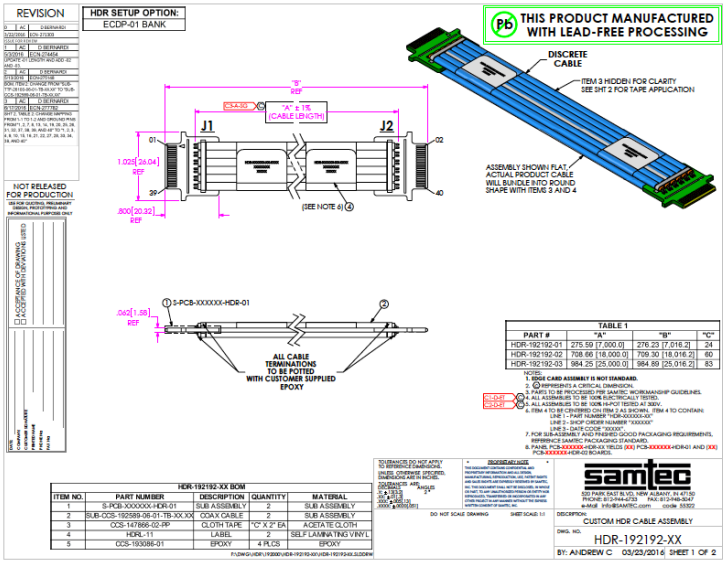


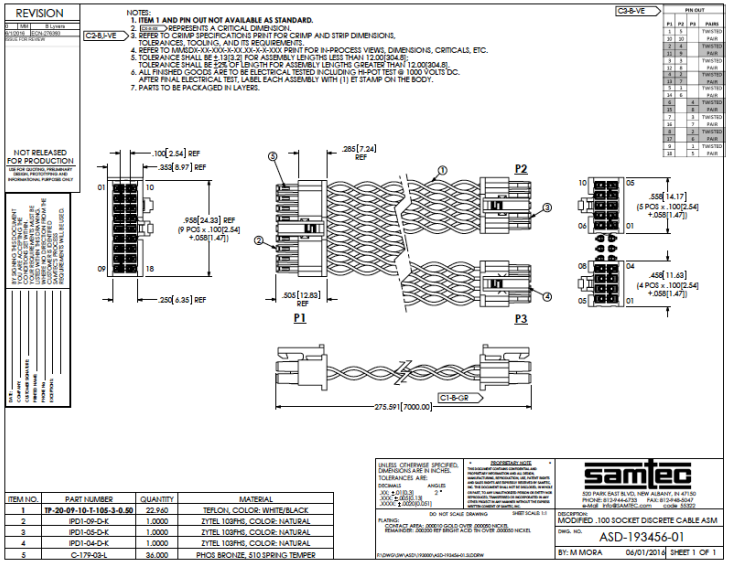
- SBND Side AM
  - Same size of top AM, only difference is the input mating connector
  - Same design as (Proto)DUNE-SP AM
- Side FEMB Adapter board
  - Passive board with only mating connectors
- Toy TPC has been developed to emulate detector capacitance
  - Together with FEMB and adapter board to form a complete cold electronics assembly

Cold Cable

- SBND requires 7 meters of cold cable
- Data cable
  - 3M miniSAS cable has been identified as a good candidate for cold signal cable
  - 7 meters long, 8 twinax pairs and 8 single ended signals
- Power cable
  - Twisted pair 22AWG 2x8 Teflon cable assembly from Samtec
- Cable materials have been tested to verify the LAr compatibility successful at Fermilab MTS

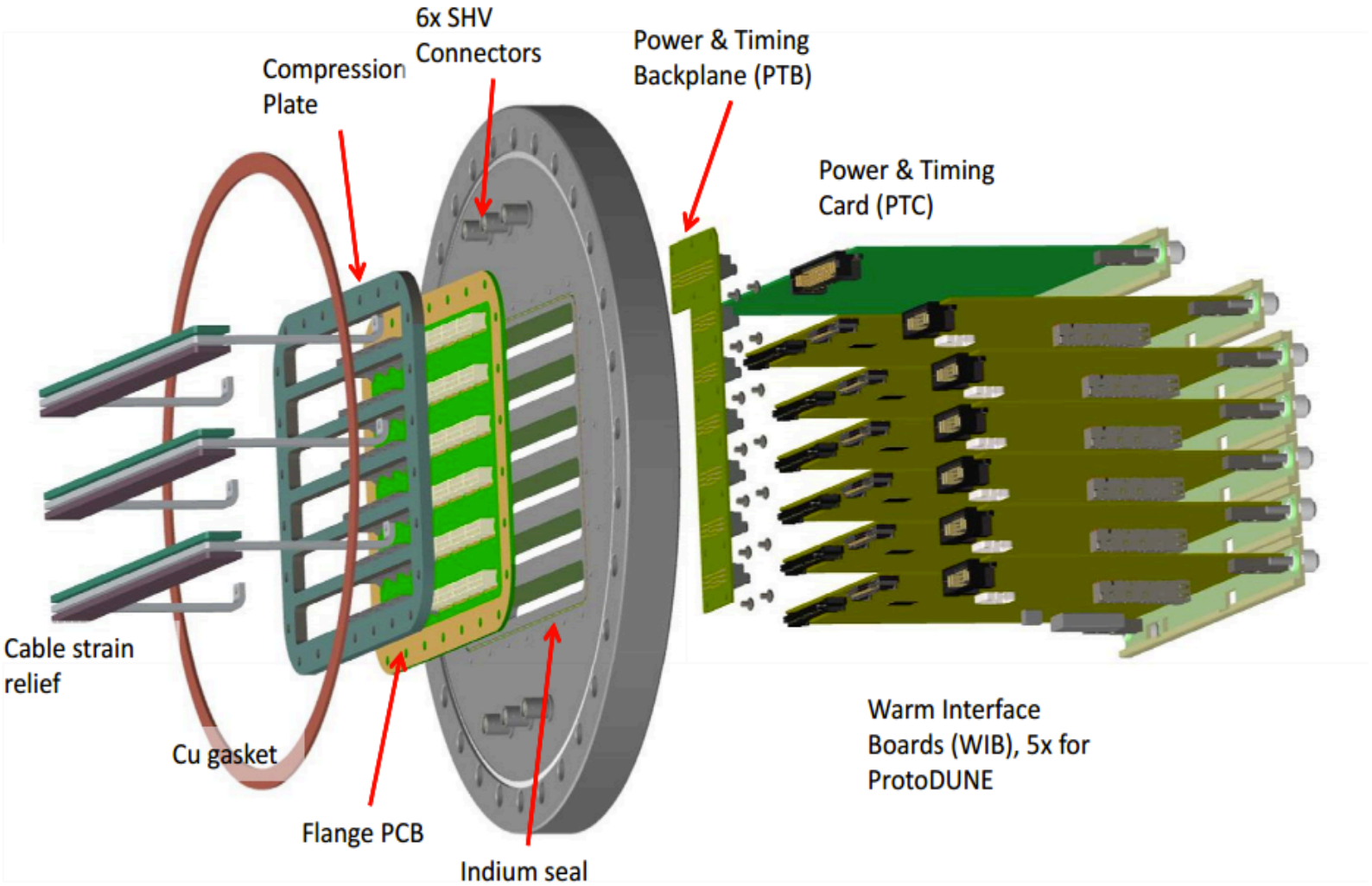
Cold Cable



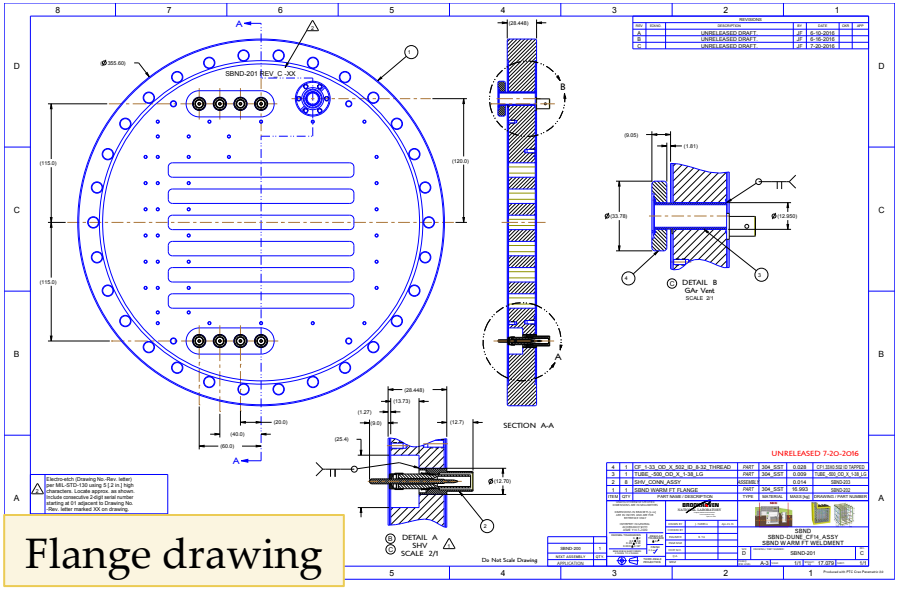


- DUNE far detector requires up to 25 meters of cold cable
  - ProtoDUNE-SP requires 7 meters of cold cable, which shares the same design of the 25 meters of cold cable
- Data cable
  - 12 pairs of 26 AWG copper twin-axial cable from Samtec
  - Viable candidate for all lengths (up to 25 meters) of cable required in DUNE FD
- Power cable
  - Twisted pair 20AWG 2x9 Teflon cable from Samtec
- Cable materials have been tested to verify the LAr compatibility successful at Fermilab MTS

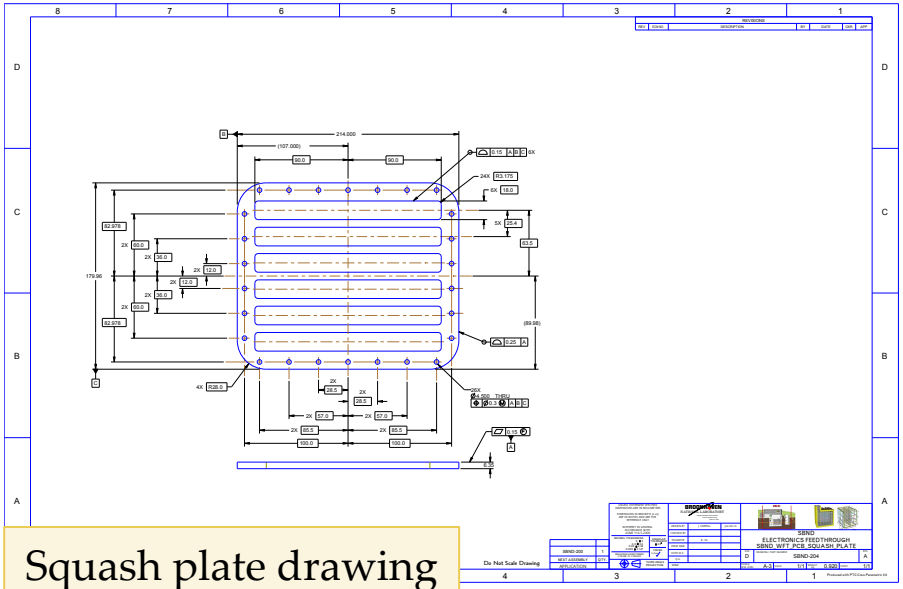
Signal Feed-through



Signal Feed-through



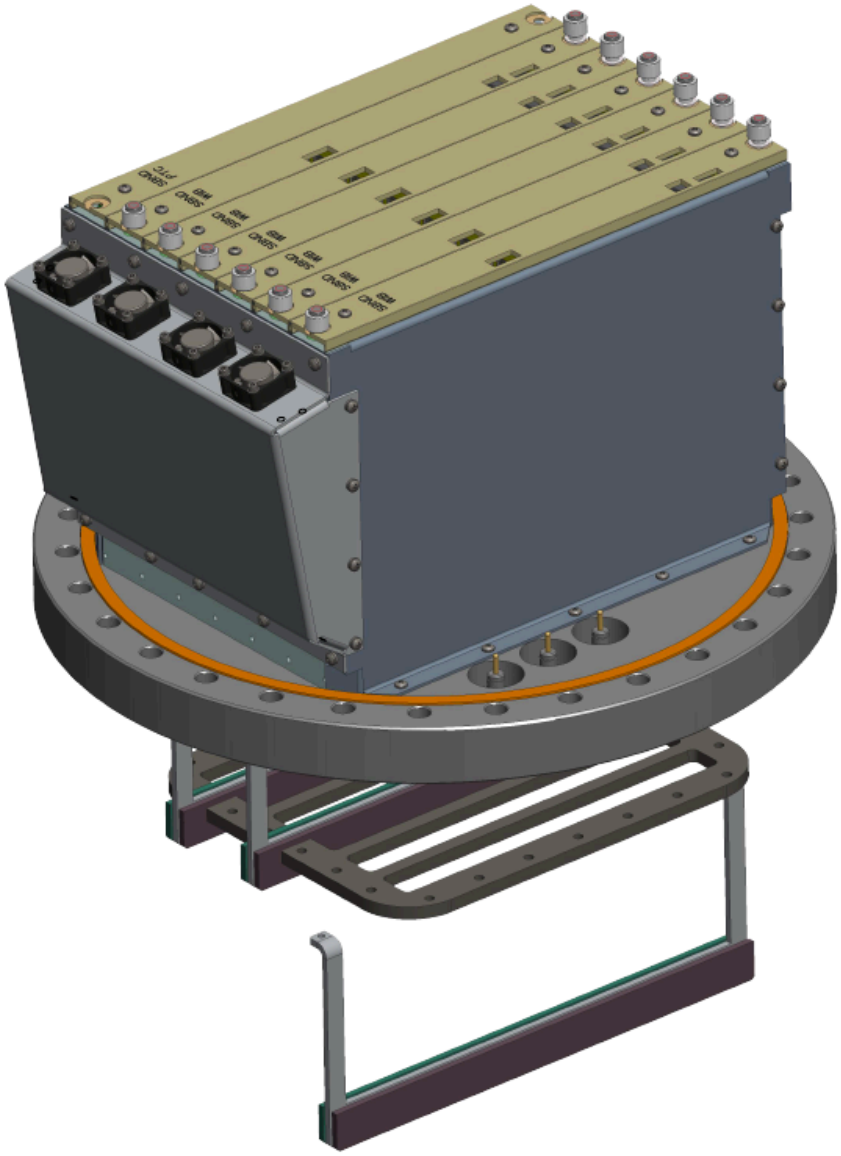
Flange drawing

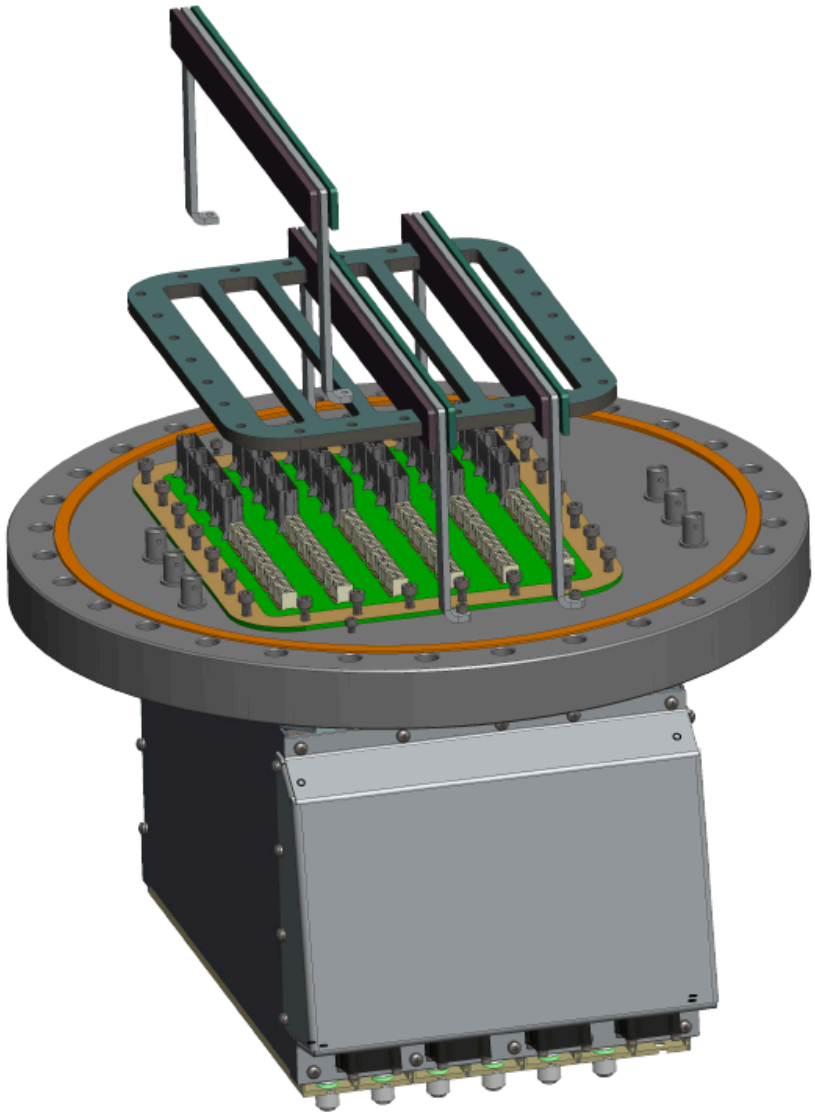


Squash plate drawing

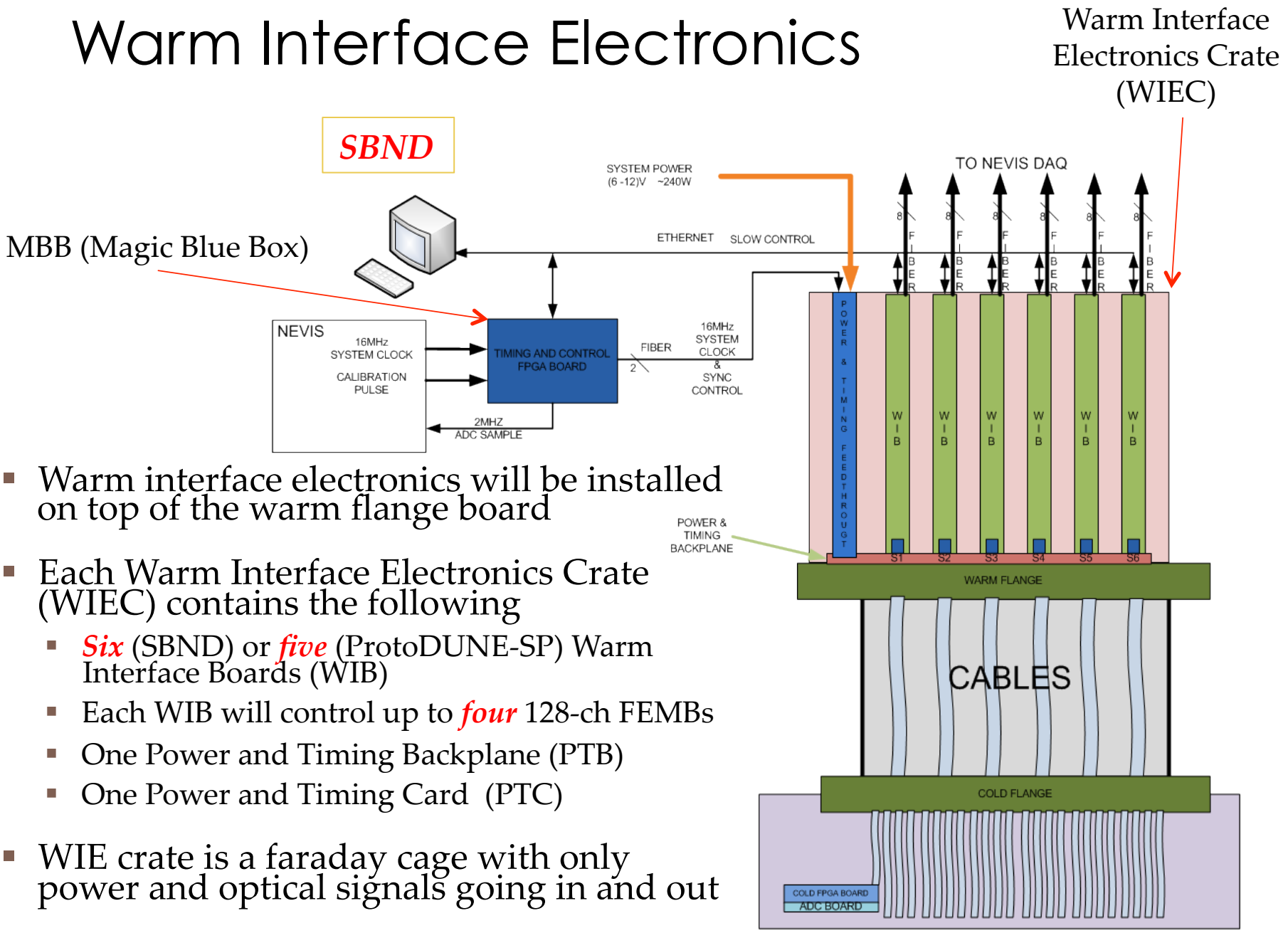
- Both SBND and ProtoDUNE-SP will use single warm flange configuration
  - Warm flange board PCB sealed with indium and squash plate to flange
  - Warm interface electronics is installed inside a faraday crate on the top of the signal feed-through
- Signal feed-through design is finalized
  - 8 SHV connectors for bias will be welded on the flange
  - Vent port is available on the flange
  - Prototype order is being fabricated

Warm Interface Electronics on Signal FT



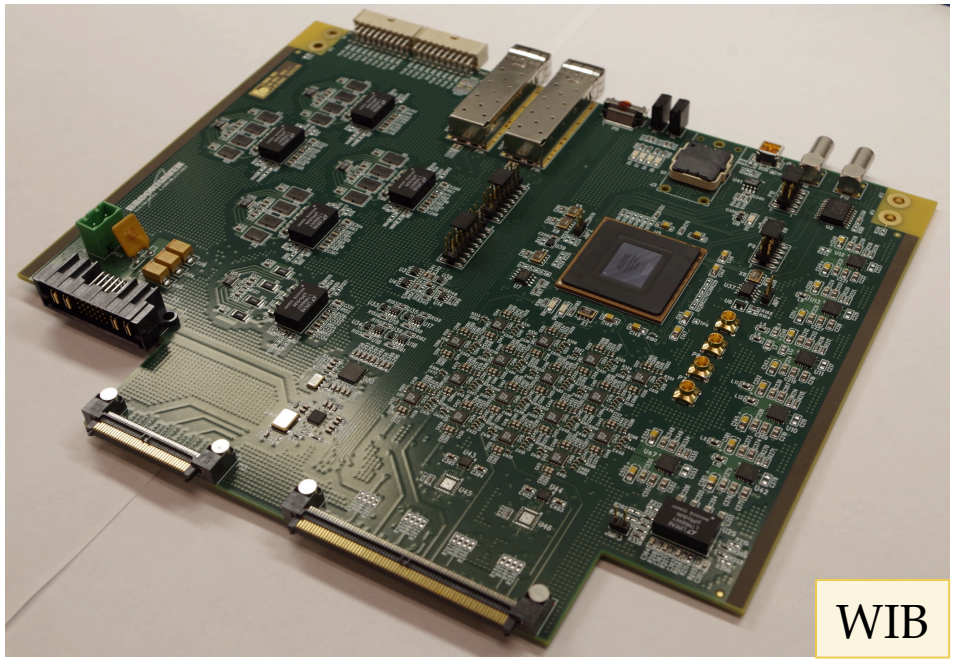


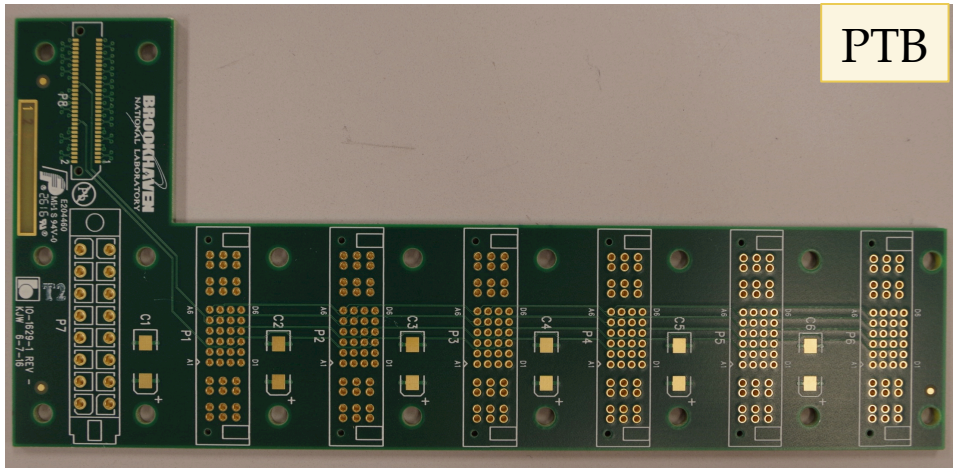
Warm Interface Electronics



- Warm interface electronics will be installed on top of the warm flange board
- Each Warm Interface Electronics Crate (WIEC) contains the following
  - ***Six*** (SBND) or ***five*** (ProtoDUNE-SP) Warm Interface Boards (WIB)
  - Each WIB will control up to ***four*** 128-ch FEMBs
  - One Power and Timing Backplane (PTB)
  - One Power and Timing Card (PTC)
- WIE crate is a faraday cage with only power and optical signals going in and out

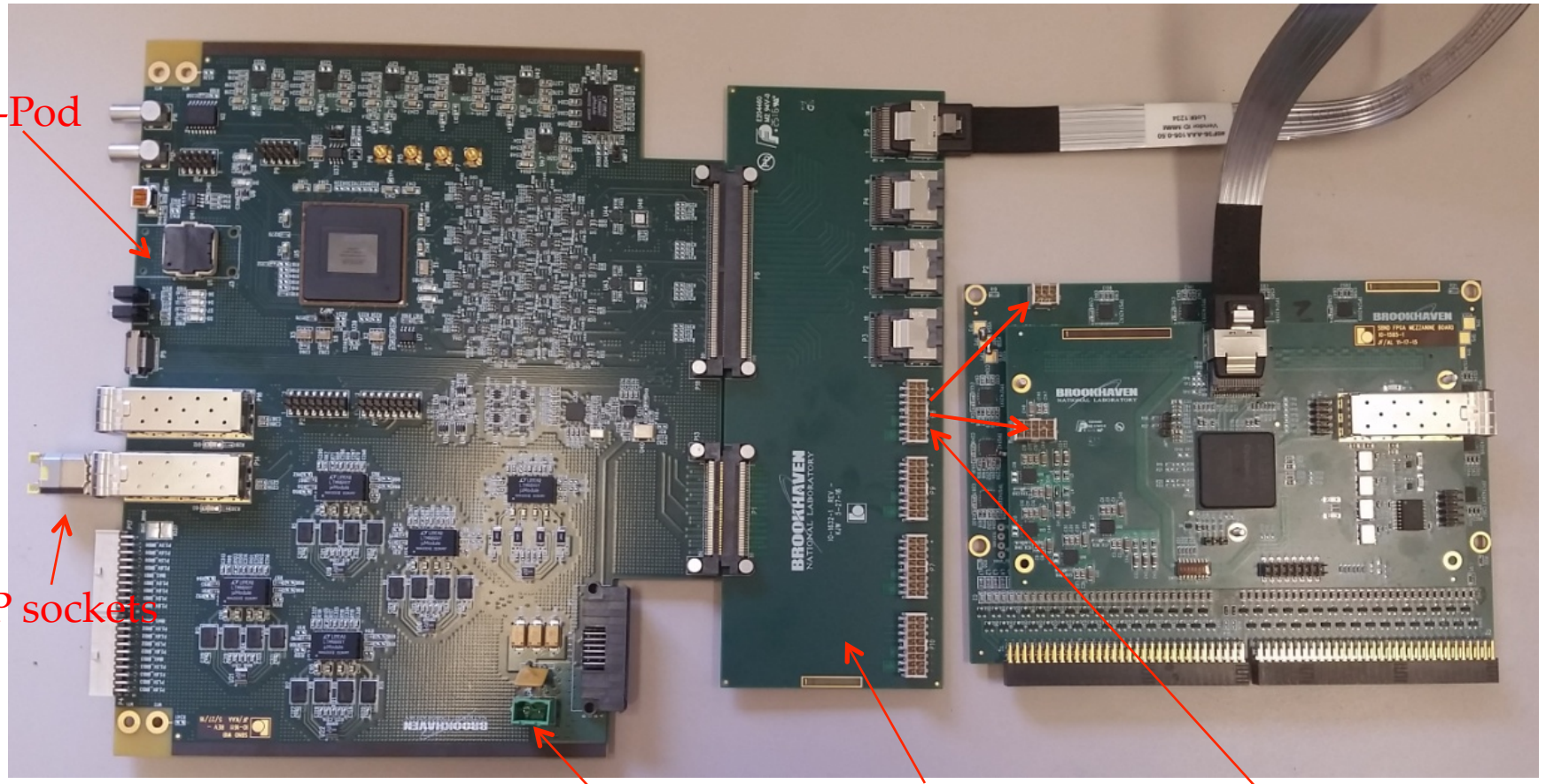
Warm Interface Electronics





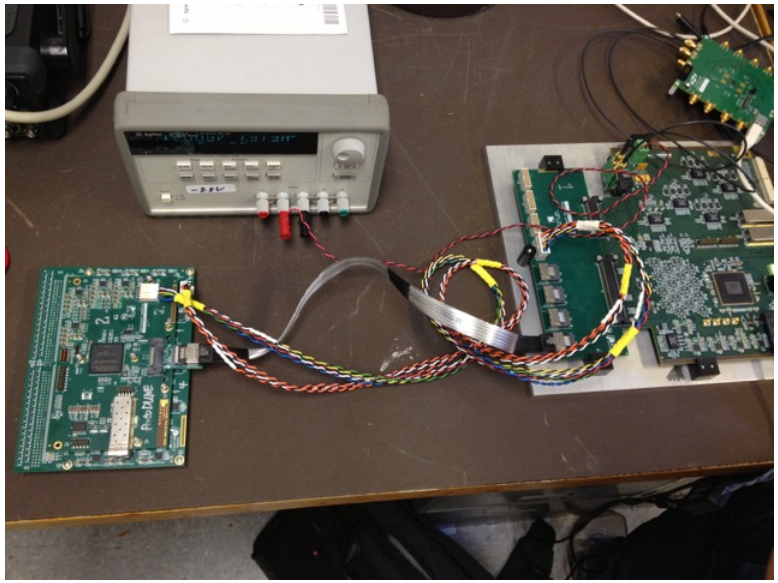
- WIB
  - SBND WIB has been fabricated and assembled
  - Preliminary tests show the power, FPGA and GbE communication are working well
  - Successful integration test with Nevis electronics on Sept 22nd
  - ProtoDUNE-SP WIB design is being finalized
  - SBND WIB is being used for ProtoDUNE-SP firmware development
- PTB
  - First prototype is available and being tested
  - A minor revision to fix one mating connector has been finalized
- PTC
  - SBND prototype is available and being tested
  - ProtoDUNE-SP design is being finalized (UC Davis) and will be fabricated this week

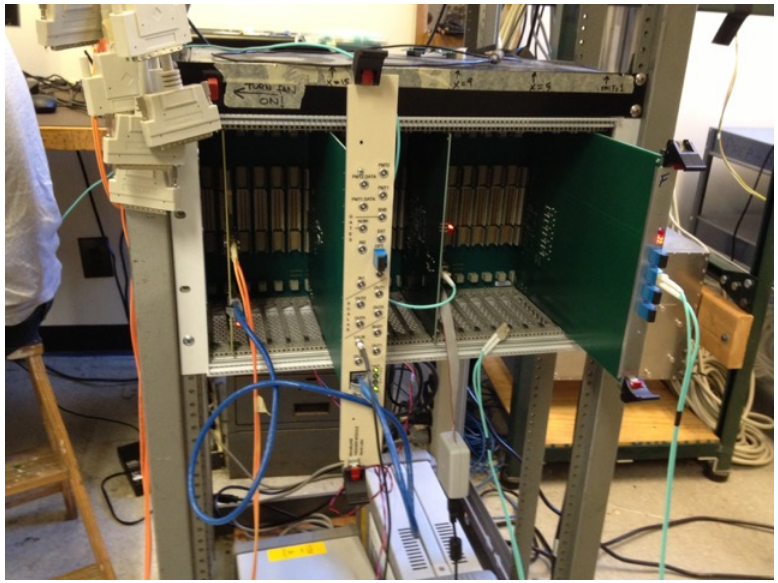
SBND WIB + FEMB



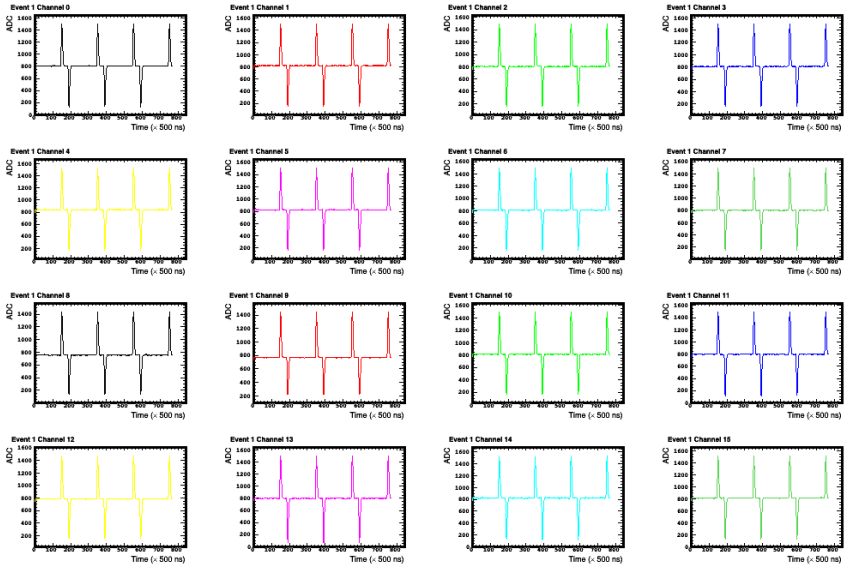
- Test platform can be set up without signal feed-through

SBND Integration Test





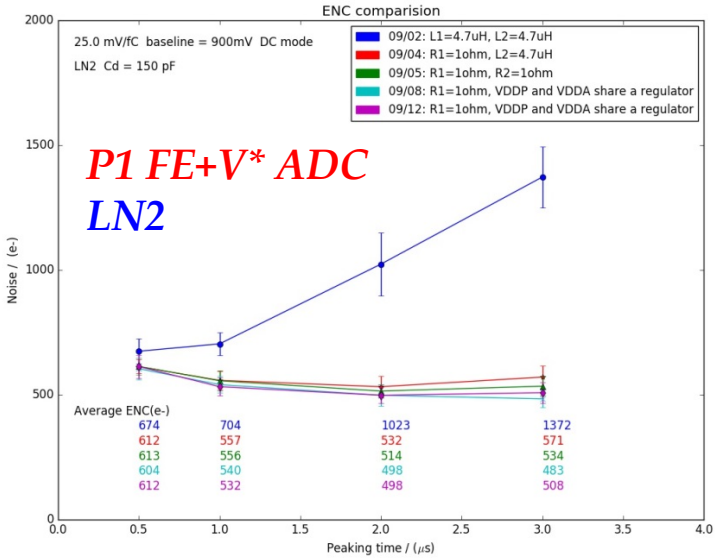
- Integration test of SBND full readout chain took place at Nevis labs on Sept 22nd
  - Successful data flow from FEMB → WIB → FEM → Ctrl → DAQ PC
  - Stable optical link was established between WIB and FEB
  - Calibration data was acquired and displayed on DAQ PC successfully
- Next integration test is planned in the week of Nov 7th to include timing distribution



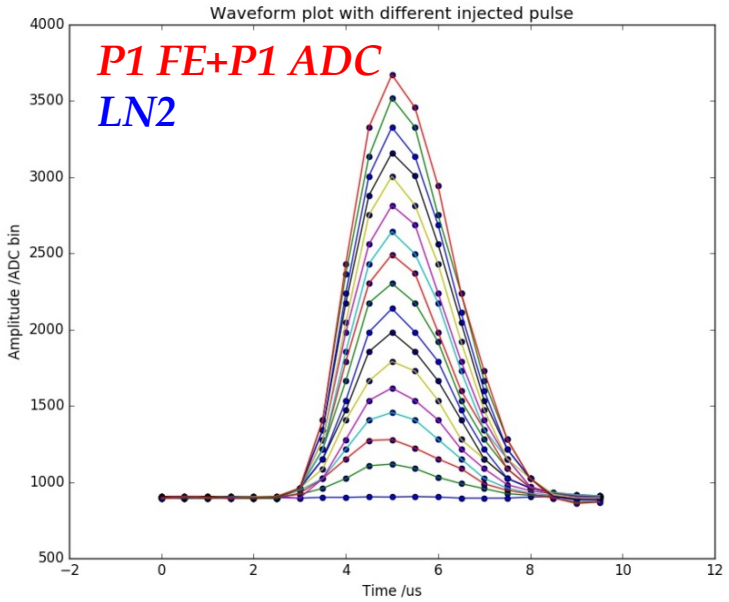
Cold ASICs Development – Current Status

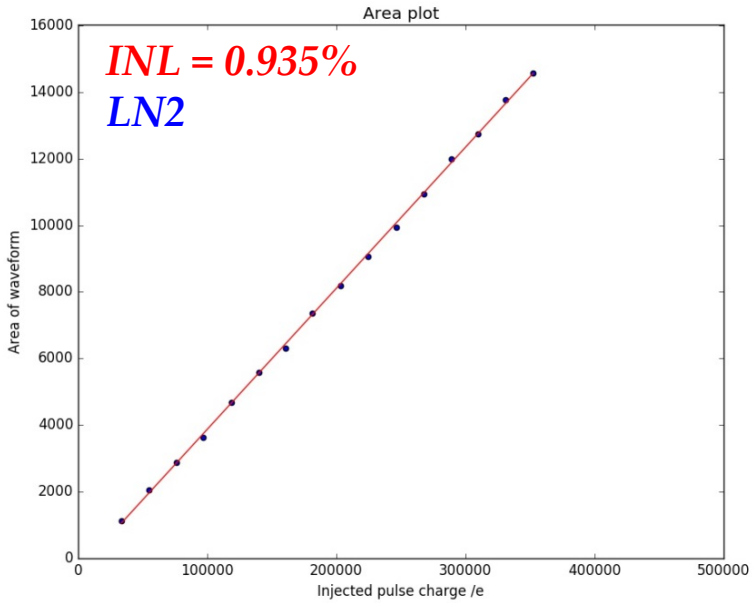
- FE ASIC
  - P1 FE ASIC has been tested on FEMB with satisfactory noise performance (< 600 e^- with τ_p = 1us and C_d = 150pF)
  - Two design issues to be addressed
    - Glitch of bias current design, 1GOhm resistor is necessary to bring channels up
    - Imperfect pole-zero cancellation in cold operation
  - One package issue to be addressed
    - Distortion of baseline is caused by excessive stress from package in cold operation
- ADC ASIC
  - One P1 ADC ASIC die has been tested in past weeks
  - Packaged P1 ADC ASICs have just arrived, evaluation test will start
  - Preliminary test results from P1 ADC die shows stuck code (DNL issue) is still existed
  - More evaluation tests will be necessary to have a quantitative assessment of P1 ADC performance

Performance of P1 FE and ADC ASICs



- P1 FE ASIC has been characterized with V* ADC on FEMB extensively
  - Satisfactory noise performance (< 600 e^- with τ_p = 1us and C_d = 150pF) in LN2
- Only one P1 ADC die has been tested so far
  - Preliminary test results with P1 FE ASIC shows reasonable INL despite of the residue stuck codes
- More details will be discussed in the parallel session tomorrow morning





Cold ASICs Development – Next Step

- FE ASIC
  - P2 FE ASIC has been submitted in late August, will be back in early November
  - Two design issues have been addressed in the P2 FE design
  - Package issue is being followed up with three different packaging houses
    - Chips packaged by Quik-Pak shows improved baseline distortion
    - Chips packaged by MOSIS/ASE have just arrived, evaluation test will start
    - Chips packaged by Novapak will be available for test in coming weeks
    - One packaging house will be selected to package P2 ASICs after evaluation tests
- ADC ASIC
  - Evaluation test of P1 ADC ASICs will soon start with packaged chips
  - Quantitative comparison of P1 ADC and V* ADC will be performed. V* ADC has been used on FEMB prototype so far
  - Simulation studies of ADC stuck code in event reconstruction is being carried out
  - Mitigation of stuck code in detector operation is being explored

Cold ASICs Development – Next Step

- ProtoDUNE-SP
  - Very tight schedule will allow no new submission of cold ASICs
  - Based on test results, P2 FE ASIC and P1 (or V*) ADC ASIC will be used to instrument APA
- SBND
  - Slightly relaxed schedule allows for one more cold ASIC submission in Spring 2017
  - Evaluation test of P1 ADC ASIC and simulation studies will provide inputs to the next iteration of cold ADC design
- DUNE far detector
  - A strong collaboration is being built up between Fermilab and BNL ASIC design teams
  - Cold ADC design will be studied and optimized to meet requirements of 10kt far detector

Prototype Status of SBND CE System

SBND Prototype		Design	Fabrication	Test
Cold Electronics	FE ASIC	✔	✔	Ongoing
	ADC ASIC	✔	✔	Ongoing
	Top FEMB	✔	✔	✔
	Side FEMB	✔	✔	Ongoing
Cold Cable	Data Cable	✔	✔	Ongoing
	Power Cable	✔	✔	Ongoing
Signal Feed-through	Flange	✔	Ongoing	
	Flange Board	✔	Ongoing	
	WIE Crate	✔	✔	Ongoing
Warm Interface Electronics	WIB	✔	✔	Ongoing
	PTB	✔	✔	Ongoing
	PTC	✔	✔	Ongoing
	MBB	✔	Ongoing	

Prototype Status of ProtoDUNE –SP CE System

ProtoDUNE-SP Prototype		Design	Fabrication	Test
Cold Electronics	FE ASIC	✔	✔	Ongoing
	ADC ASIC	✔	✔	Ongoing
	FEMB	✔	✔	Ongoing
Cold Cable	Data Cable	✔	✔	Ongoing
	Power Cable	✔	✔	Ongoing
Signal Feed-through	Flange	✔	Ongoing	
	Flange Board	✔	Ongoing	
	WIE Crate	✔	✔	Ongoing
Warm Interface Electronics	WIB	Ongoing		
	PTB	✔	✔	Ongoing
	PTC	✔	Ongoing	

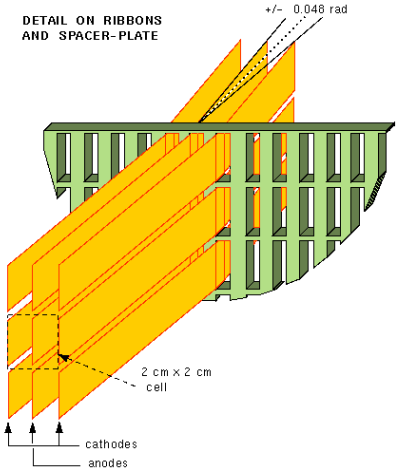
Conclusion

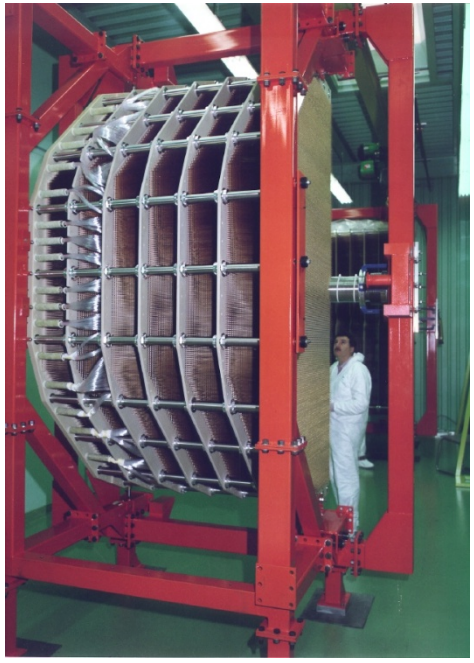
- R&D of CMOS cold electronics started in 2008
  - This was before most of projects using cold electronics were anticipated or in existence
    - MicroBooNE, ARGONETUBE, CAPTAIN, LArIAT, DUNE 35 Ton, ICARUS 50l TPC at CERN, SBND, ProtoDUNE-SP, DUNE Far Detector etc.
  - In parallel, studies of CMOS lifetime and reliability at 77 K have been conducted
    - *"LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Trans. on NSci, 60, No: 6, Part: 2, p4737(2013)*
- Cold electronics development shares common features of R&D project
  - It has high impact, but not risk free and needs continuous advancement
  - Integration test (as planned at BNL, Nevis, Fermilab and CERN etc.) and QA/QC test serve as importance steps to ensure the success of experiment
- A much boarder user community and larger development team (BNL, Fermilab, MSU, BU, LSU, UTA etc.) have been formed in past years
  - Near term goal is to instrument ProtoDUNE-SP and SBND APA in 2017/2018
  - Cold electronics will continue to be optimized to meet requirements of various experiments, with final goal to instrument the first 10 kt far detector

Backup Slides

Cryogenics Front-End based on JFET

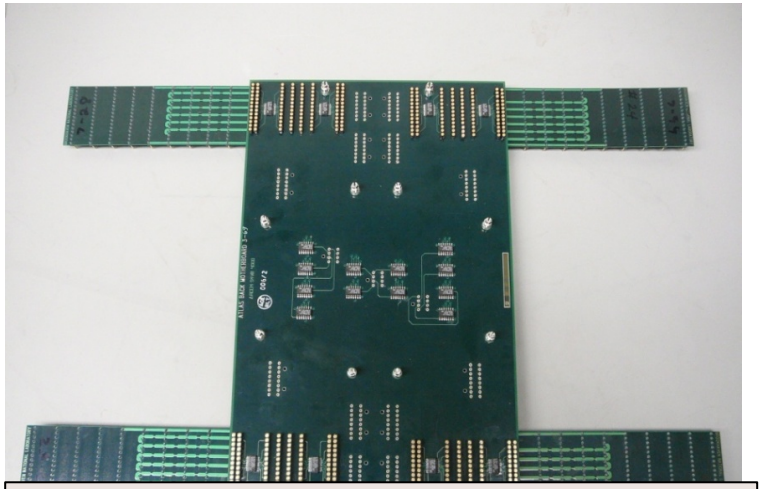
- NA48/NA62
  - Liquid Krypton calorimeter
  - Preamplifiers in LKr: **13,212** channels; surface mounted components
  - Operated at very high voltage
    - Tested up to 7kV, operated in 3kV
  - Failures
    - ~50 because of a HV accident in 1998
    - ~25 cold electronics failures after 1998
    - failure rate is < 0.2% in 18 years
    - The last failure recorded was more than 8 years ago
  - Always kept at cryogenic temperature since 1998
  - Operation
    - **18 years** so far
    - Plan to run until 2018, expected to be in operation for **20 years**



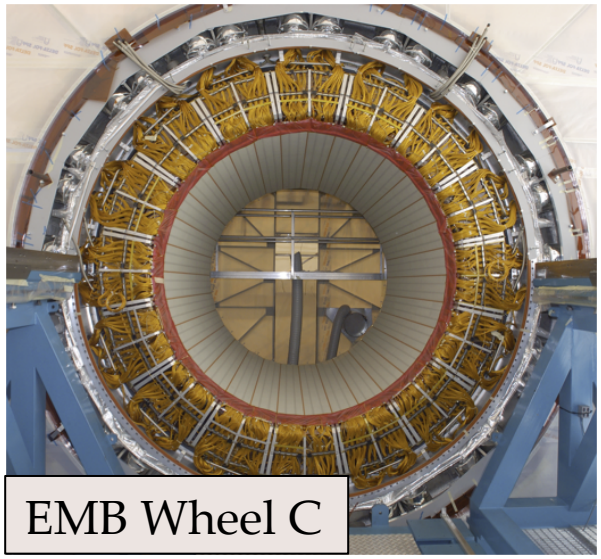


Reliability of Cold Electronics *wrt* thermal contraction-expansion PCB and Cold Electronics in ATLAS

- ATLAS LAr Calorimeter
  - 182,468 readout channels
- EM Barrel Mother Board and Summing Board
  - EMB has ~110,000 detector channels read out by 896 128-ch FEBs
  - 960 Mother Boards, 15 different types
  - 7,168 Summing Boards, 4 different types
  - 20,480 resistor network chips on Mother Boards, 5 different types
  - ~110,000 protection diodes on MB/SB assembly
- EM Barrel Calorimeter has been cooled down since 2004
  - Operation: 12 years so far
  - MB/SB will remain in operation without upgrade for HL-LHC
- 'Inoperative' channels <0.5%, as of 2016 (outside the cryostat)
- Dead channels in the cryostat ~0.02% since 2008



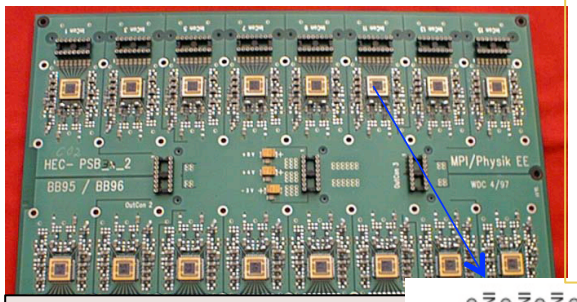
EMB Mid/Back MB+SB Assembly



EMB Wheel C

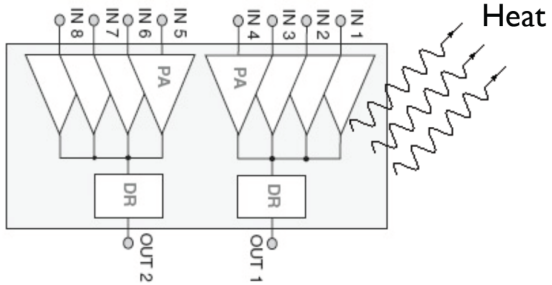
PCB and Cold Electronics in ATLAS

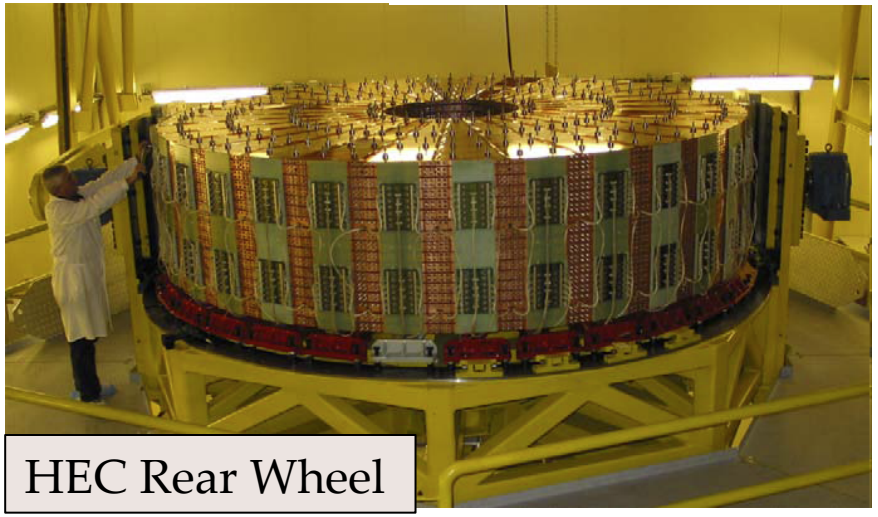
- ATLAS LAr Calorimeter HEC preamplifier ASIC based on GaAs
  - HEC has 5,632 detector channels read out by 48 128-ch FEBs
  - 320 PSBs installed on HEC wheels, 5 different types
  - Total 35,840 cold preamplifier channels, 8,960 summing amp. Each preamplifier ASIC has 8 channels
- HEC Calorimeter has been cooled down since 2005
  - In 2005 first commission in cold: 5 deal channels (< 0.1%). None due to preamps. Two due to sum amp (already at warm)
  - In 2016 still 5 dead channels: stable after 11 years of operation
  - HEC cold electronics will remain in operation without upgrade for HL-LHC



HEC Type C PSB

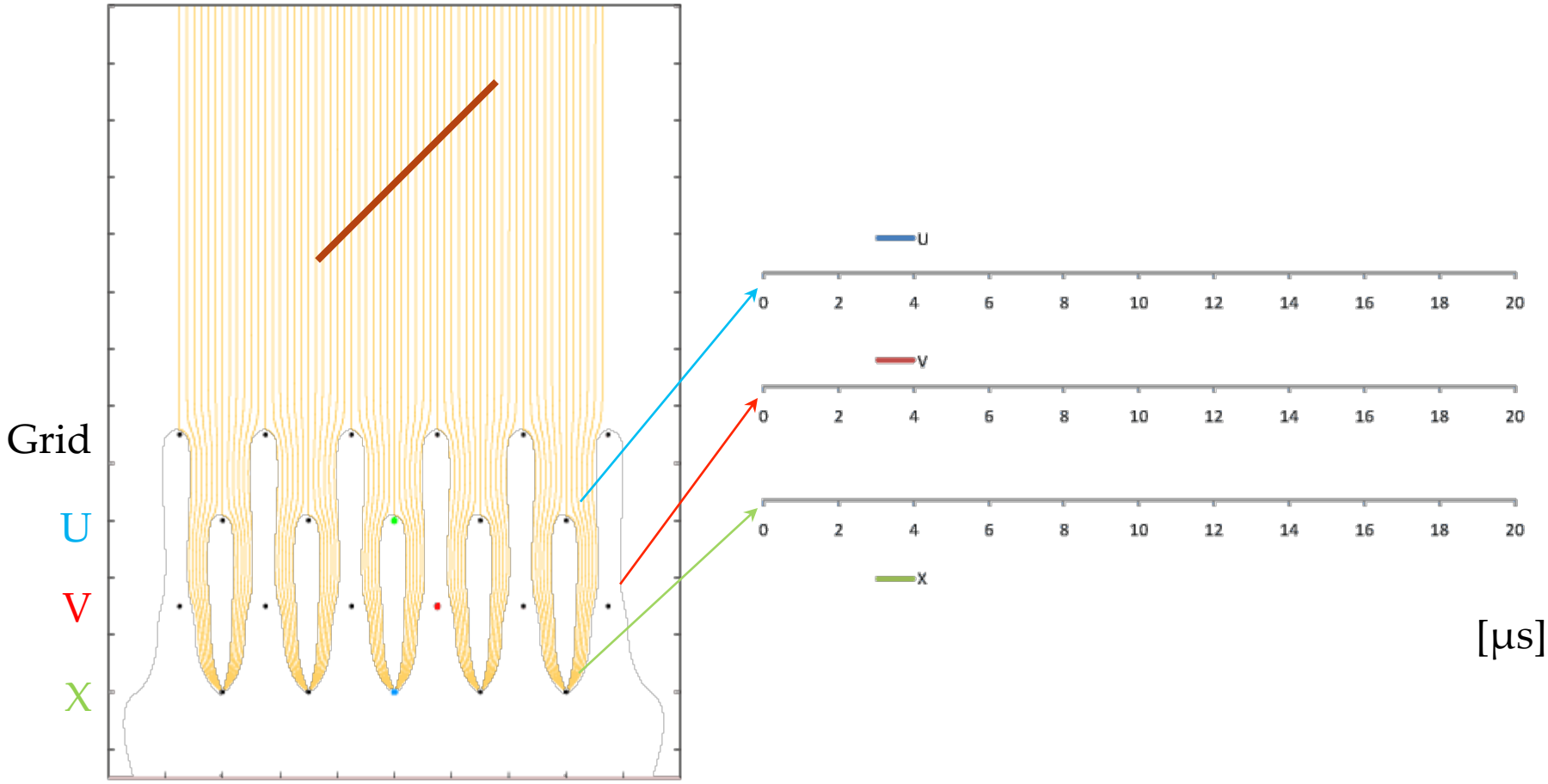
GaAs TriQuint QED-A 1um Stable operation at cryogenic temperatures





HEC Rear Wheel

Signal Formation: Induced Signals from a Track Segment



DUNE style wire arrangement: 3 instrumented wire planes + 1 grid plane
Raw current waveforms convolved with a 0.5μs gaussian (~1/2 drift length) to mimic diffusion

Principal findings and design guidelines

- A study of hot-electron effects on the device lifetime has been performed for the TSMC NMOS 180nm technology node at 300K and 77K. Two different measurements were used: accelerated lifetime measurement under severe electric field stress by the drain-source voltage (Vds), and a separate measurement of the substrate current (Isub) as a function of $1/V_{ds}$. The former verifies the canonical very steep slope of the inverse relation between the lifetime and the substrate current , $\tau \propto I_{sub}^{-3}$, and the latter confirms that below a certain value of Vds *a lifetime margin of several orders of magnitude can be achieved for the cold electronics TPC readout. The low power ASIC design for MicroBooNE and DUNE falls naturally into this domain, where hot-electron effects are negligible*

- *Lifetime of digital circuits (ac operation) is extended by the inverse duty factor* $4/(f_{clock}t_{rise})$ *compared to dc operation.* This factor is large (>100) for deep submicron technology and clock frequency needed for TPC

Analog ASIC for DUNE: I_{sub} and $1/V_{ds}$ distribution for all transistors (TSMC 180nm, 1.8V node)

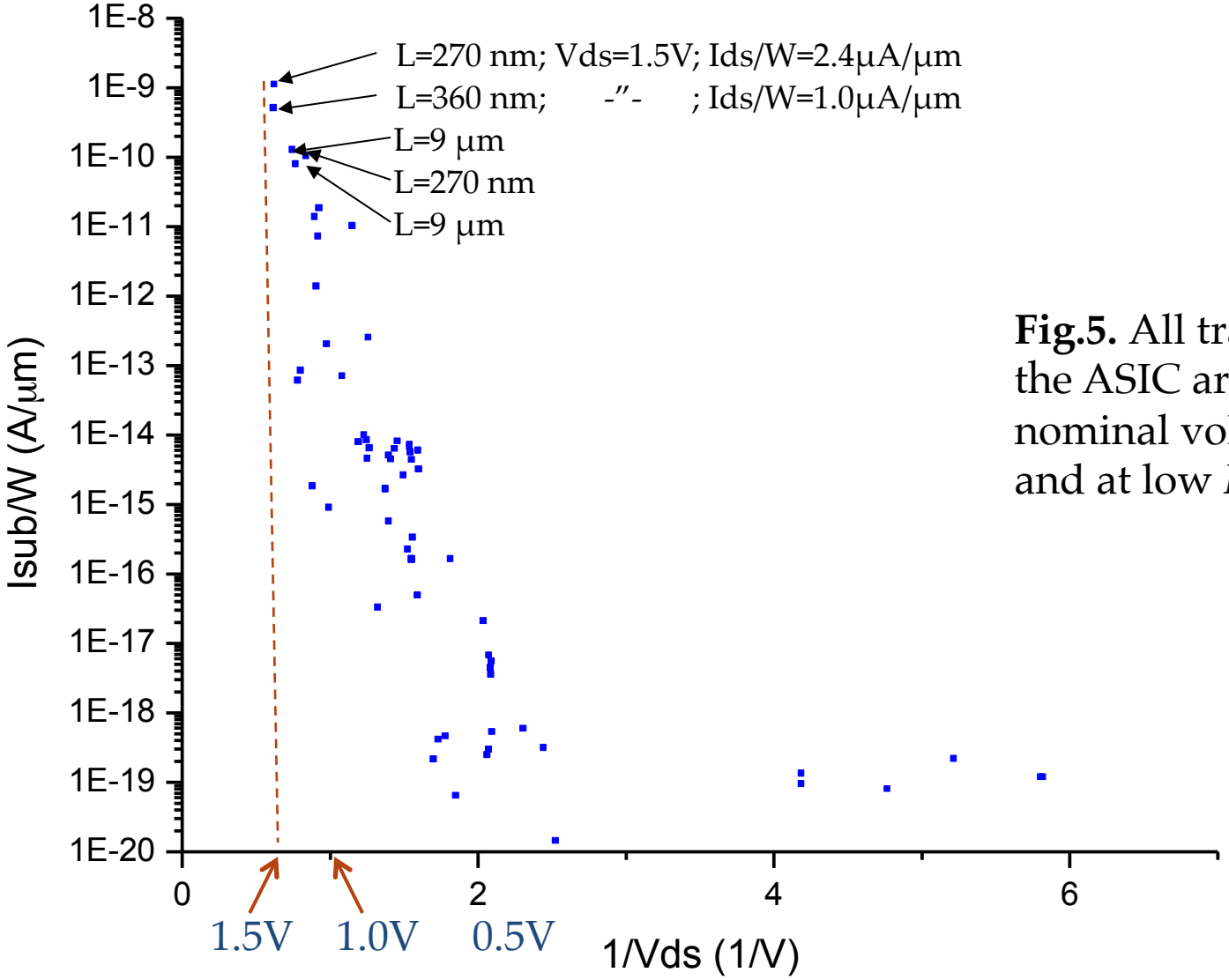


Fig.5. All transistors in the ASIC are well below nominal voltage of 1.8V and at low I_{sub}

Designing CMOS for low power = long lifetime

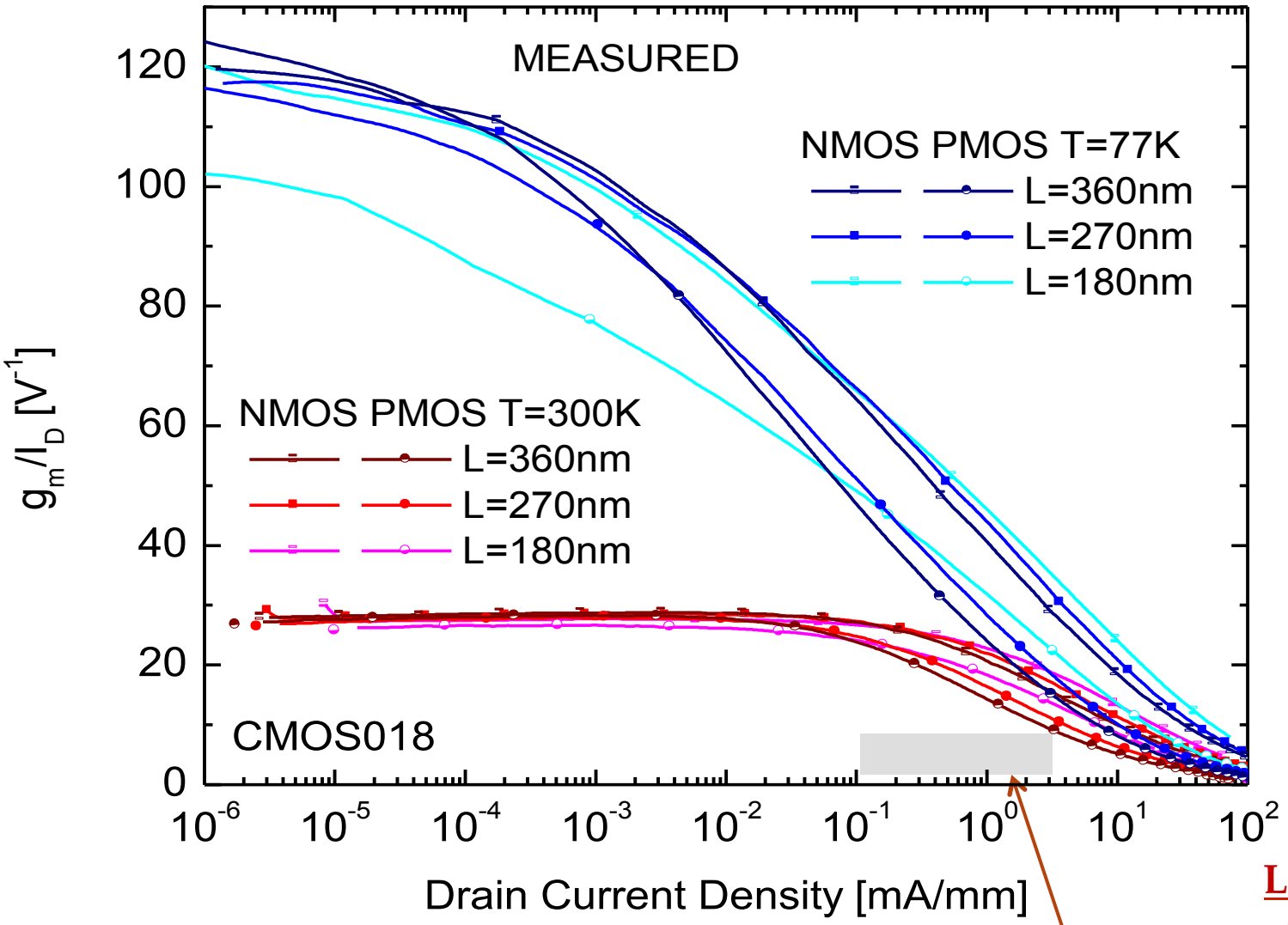
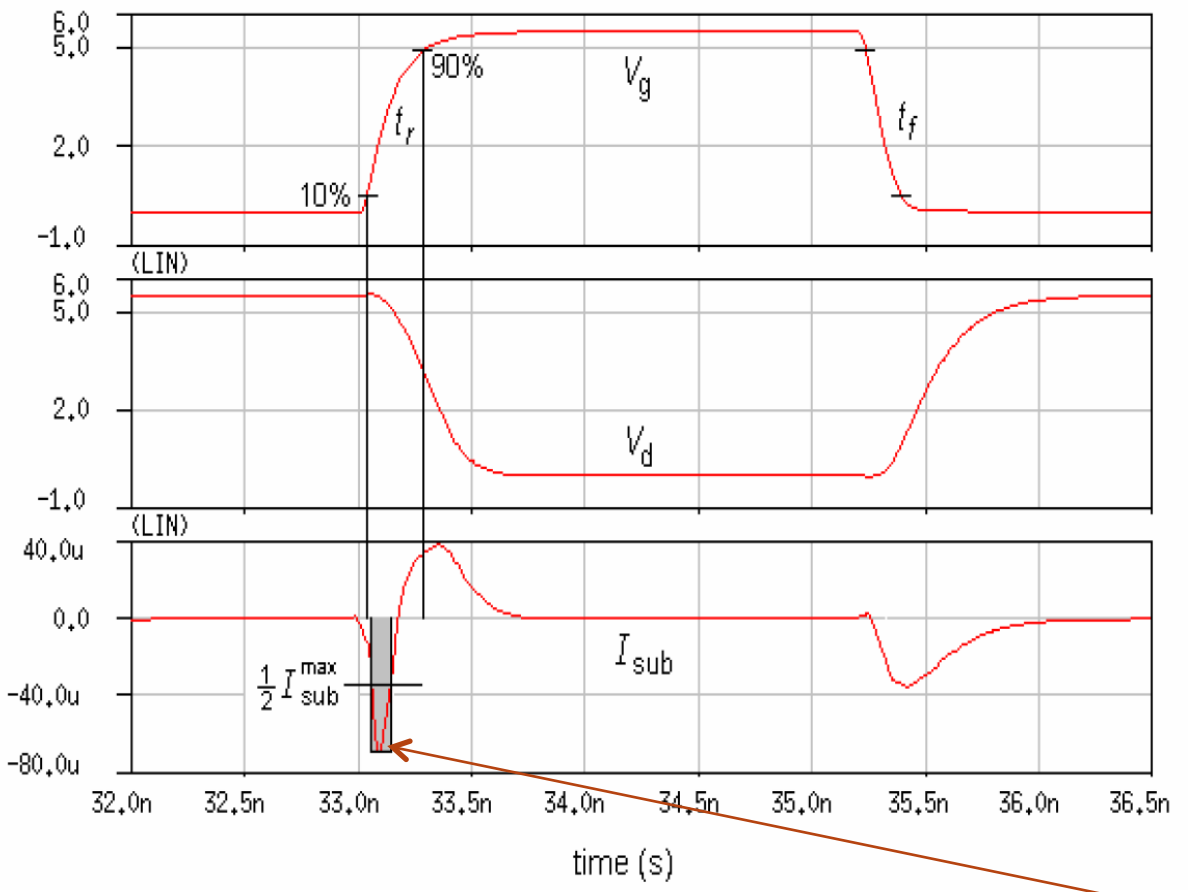


Fig.6.

Design region (approx.) for *low power* and *long lifetime* at 77K (moderate inversion)

Life time testing (stress) region (V_{ds}>1.8V)

Effective Stress Time is a small fraction of the Clock Cycle:



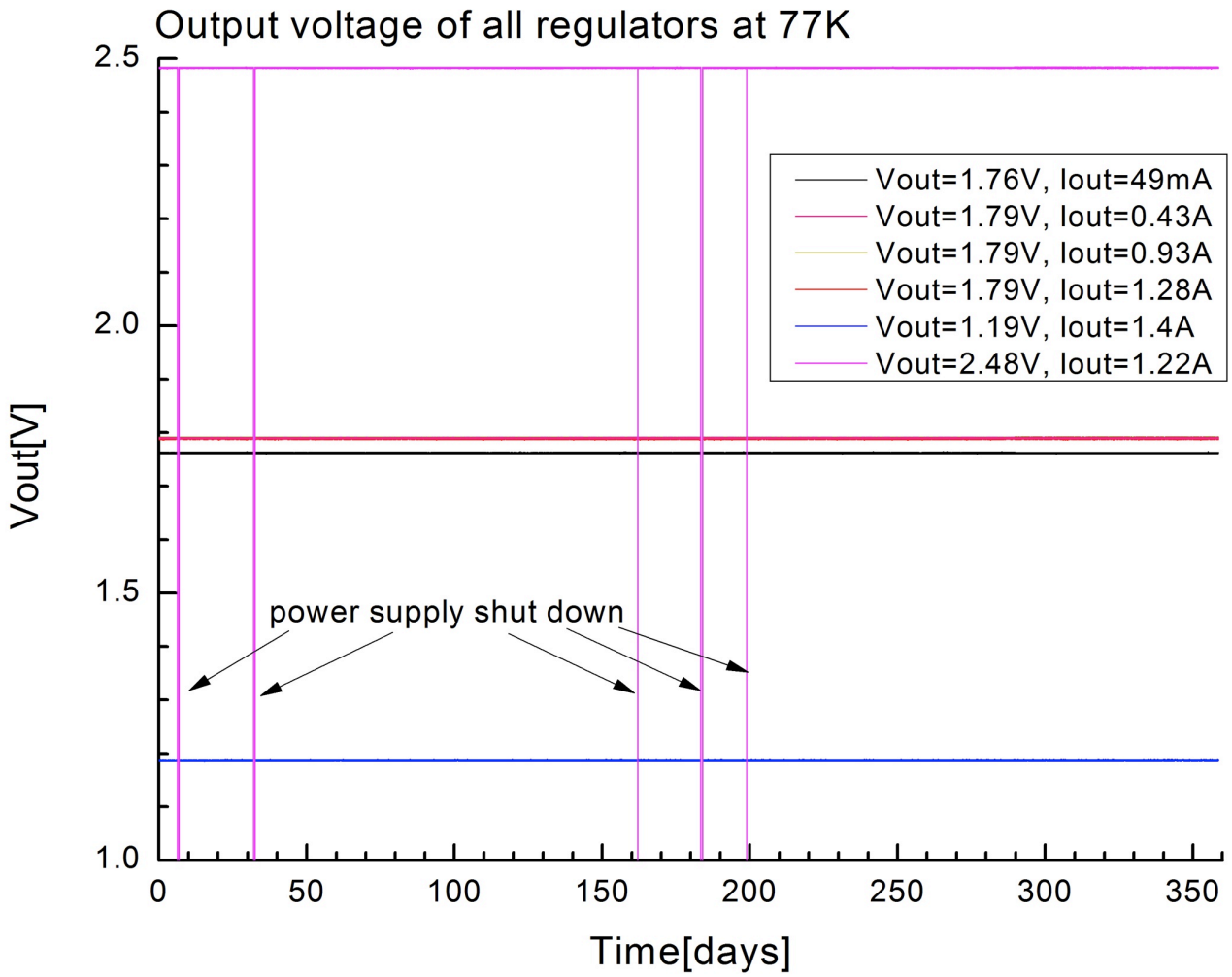
$$\left[\frac{ac\ stress\ time}{dc\ stress\ time}\right] \approx \left(f_{clock} t_{rise}\right)/4$$

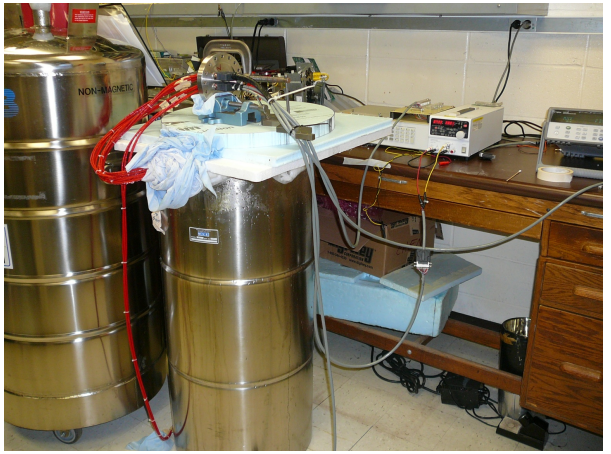
Standard method for accelerated stress testing of FPGAs: ***Observe ring oscillator frequency under severe Vds stress.***

(Degradation of Ids leads to increased rise (propagation) time and reduced ring oscillator frequency.)

Hot-carrier induced degradation occurs only when the *substrate current* is high, i.e., nominal Vds and high Ids.

Cold Regulator - Lifetime



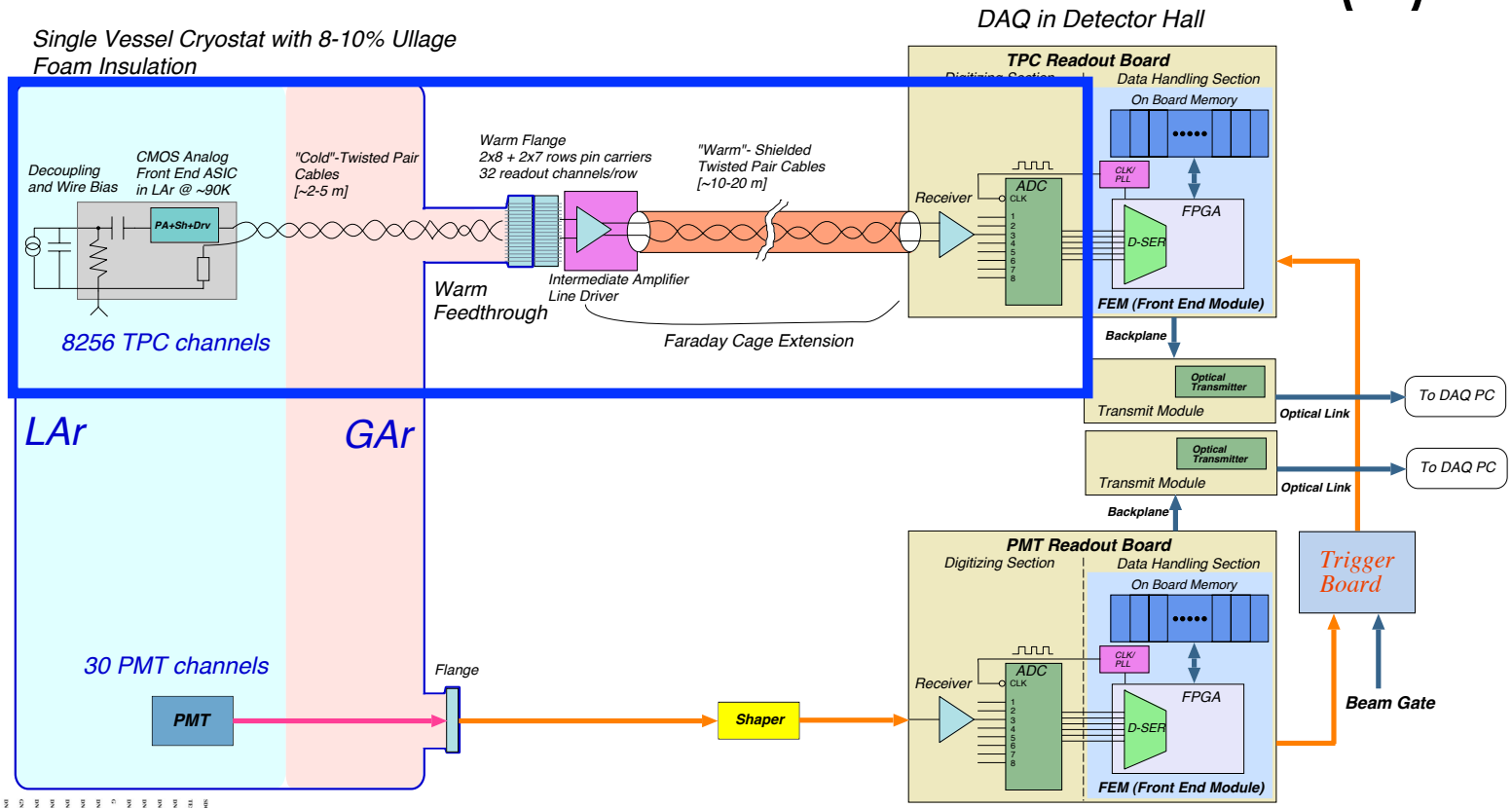


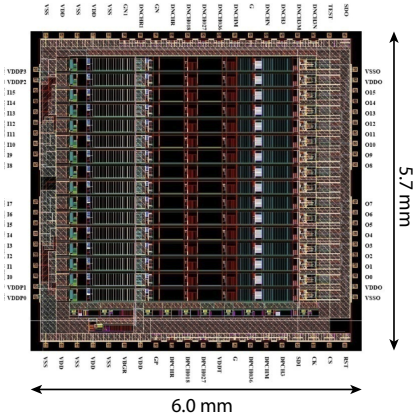
- A long term test of several **TPS74201 in LN2** has been going on **since June 24th, 2013**
- Voltage regulators are working normally for ~ 24 months, the test has been wrapped up in June 2015

Neutrino Experiments using Cold Electronics

- Projects using, and potentially will be using cold electronics:
  - MicroBooNE
  - ARGONETUBE
  - CAPTAIN
  - LArIAT
  - DUNE 35 Ton
  - ICARUS 50l TPC at CERN
  - SBND
  - ProtoDUNE-SP
  - DUNE Far Detector
- ***R&D on cold electronics started before most of these projects were anticipated or in existence***

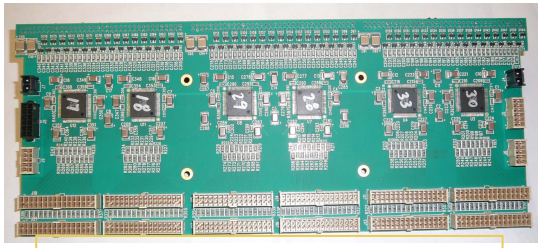
MicroBooNE Front End Electronics (1)



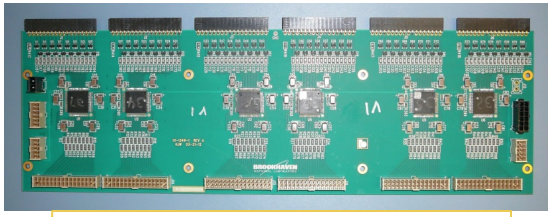


- BNL designed front end readout electronics system for MicroBooNE experiment
- Analog front end ASIC designed in 180 nm is running in LAr (~89 K) to achieve optimum signal to noise ratio
- MicroBooNE is the first experiment instrumented with cold CMOS ASICs

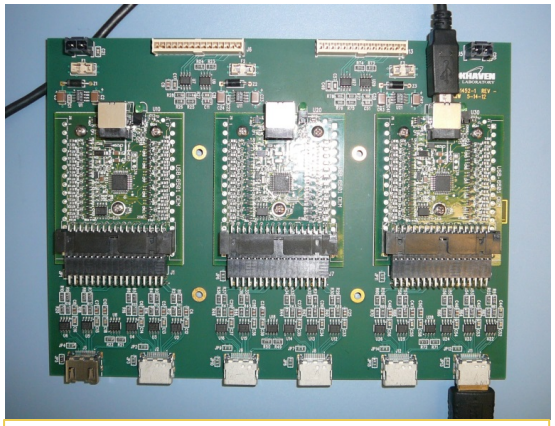
MicroBooNE Front End Electronics (2)



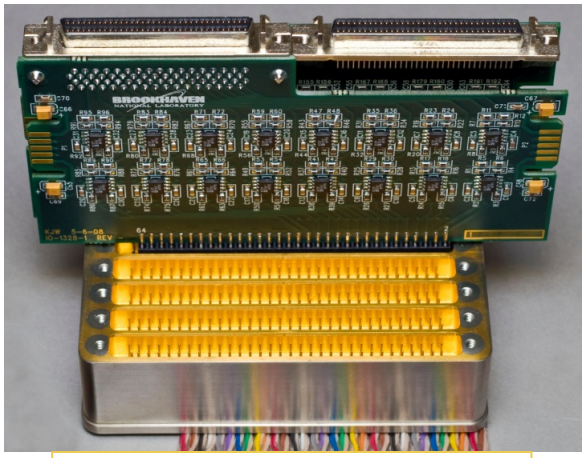
H. Cold Mother Board



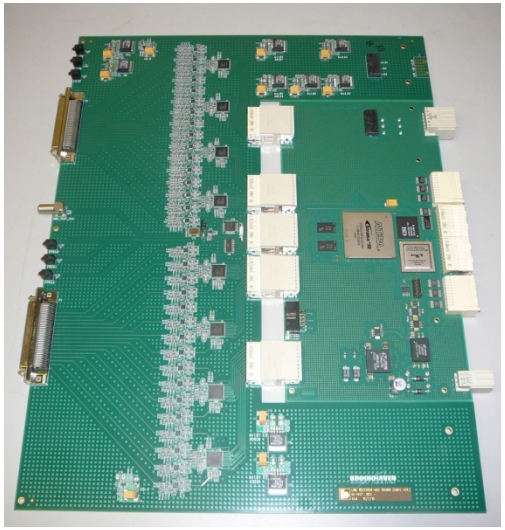
V. Cold Mother Board



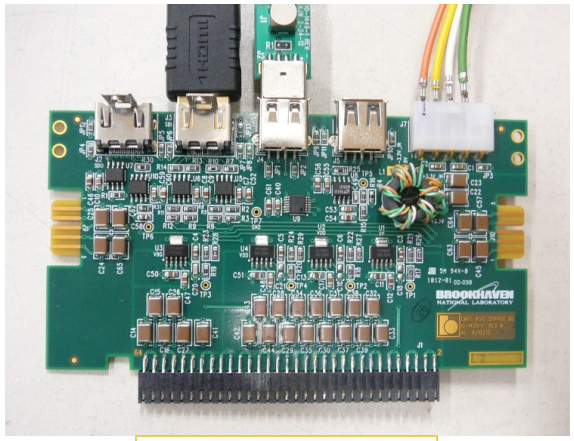
ASIC Configuration Board



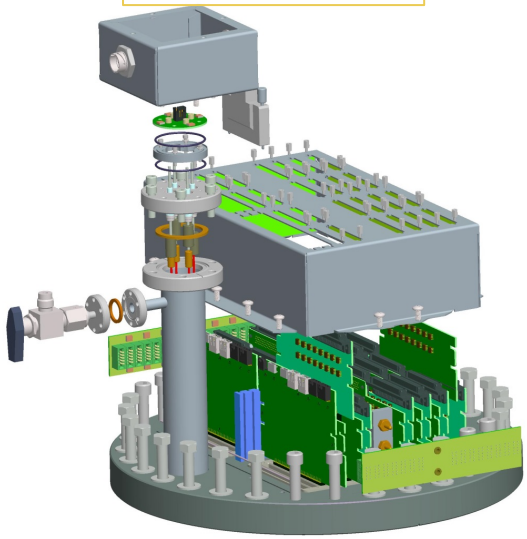
Intermediate Amplifier



Receiver ADC Board

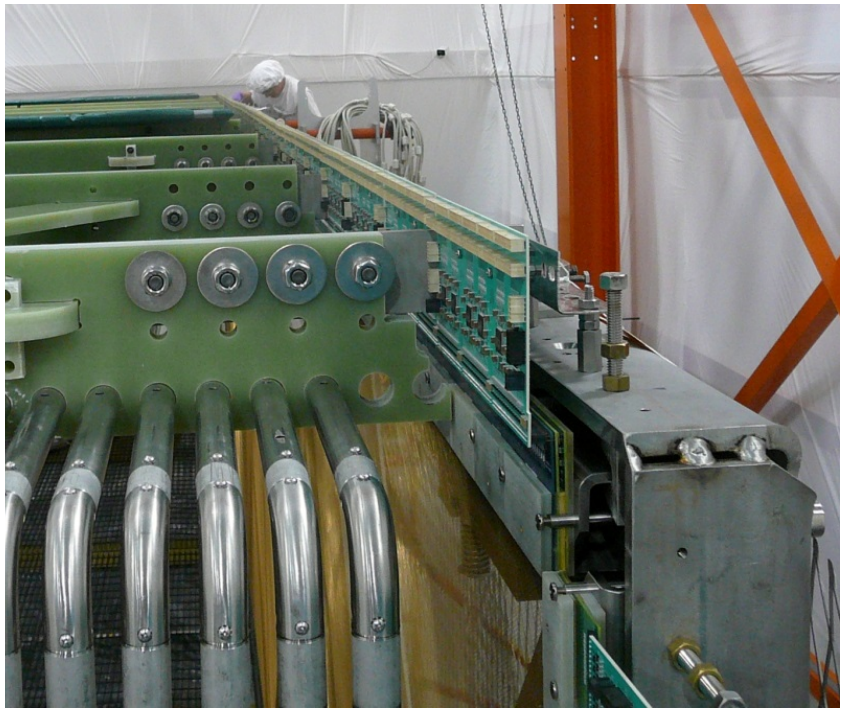


Service Board



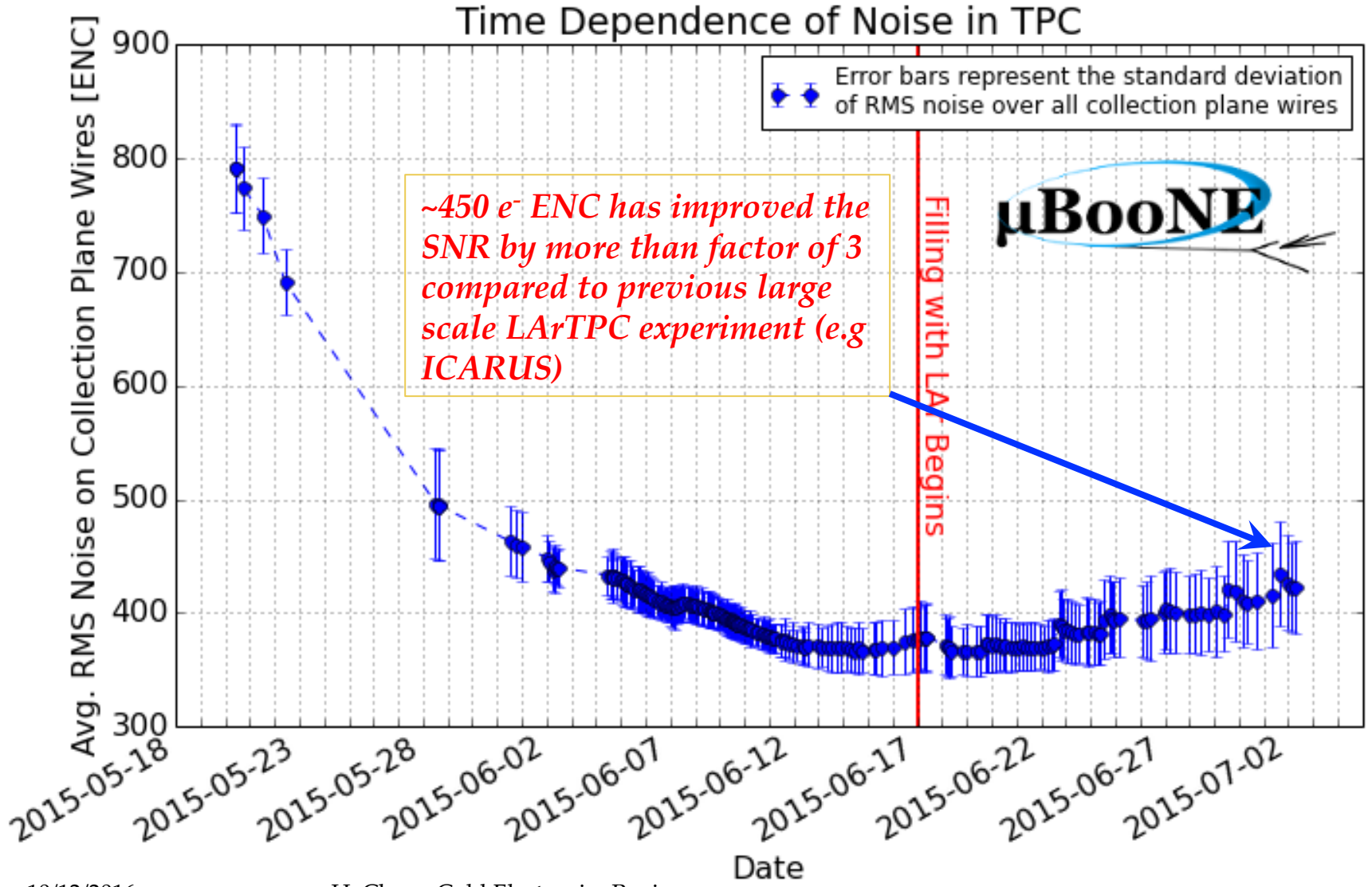
Signal Feed-through Assembly

MicroBooNE Front-end Electronics (3)

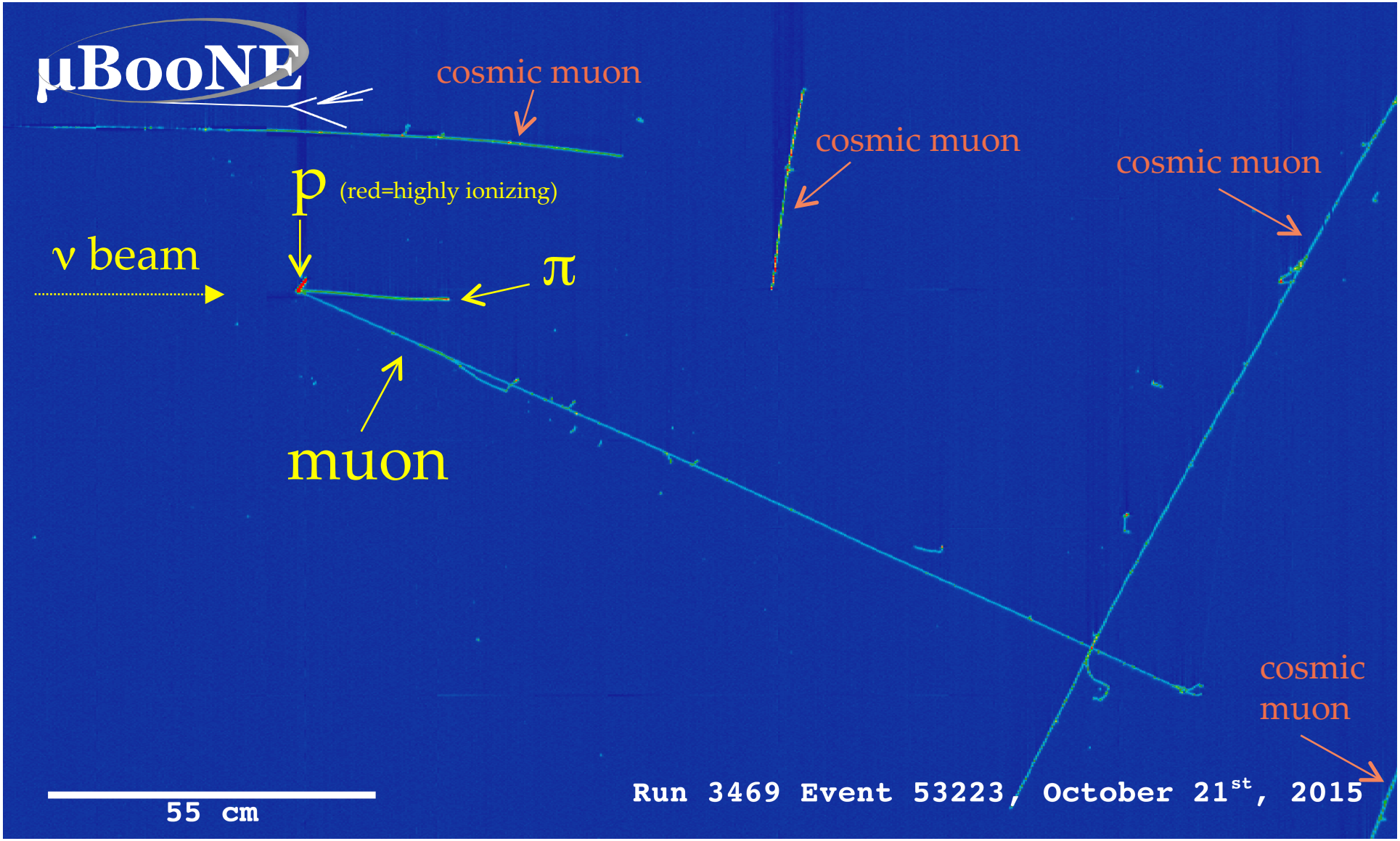


- **50 cold mother boards (8,256 channels)** are installed on MicroBooNE TPC, all channels tested successfully
- The full chain of front-end readout electronics has been installed in cryostat and tested successfully in January 2014
- Detector was moved to experimental hall in June 2014

MicroBooNE Cold Electronics Temperature Dependence of Noise in TPC



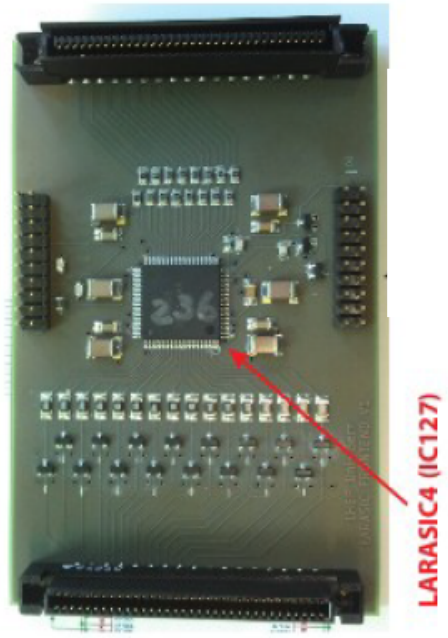
Start of Operations → First Neutrinos: October 15, 2015

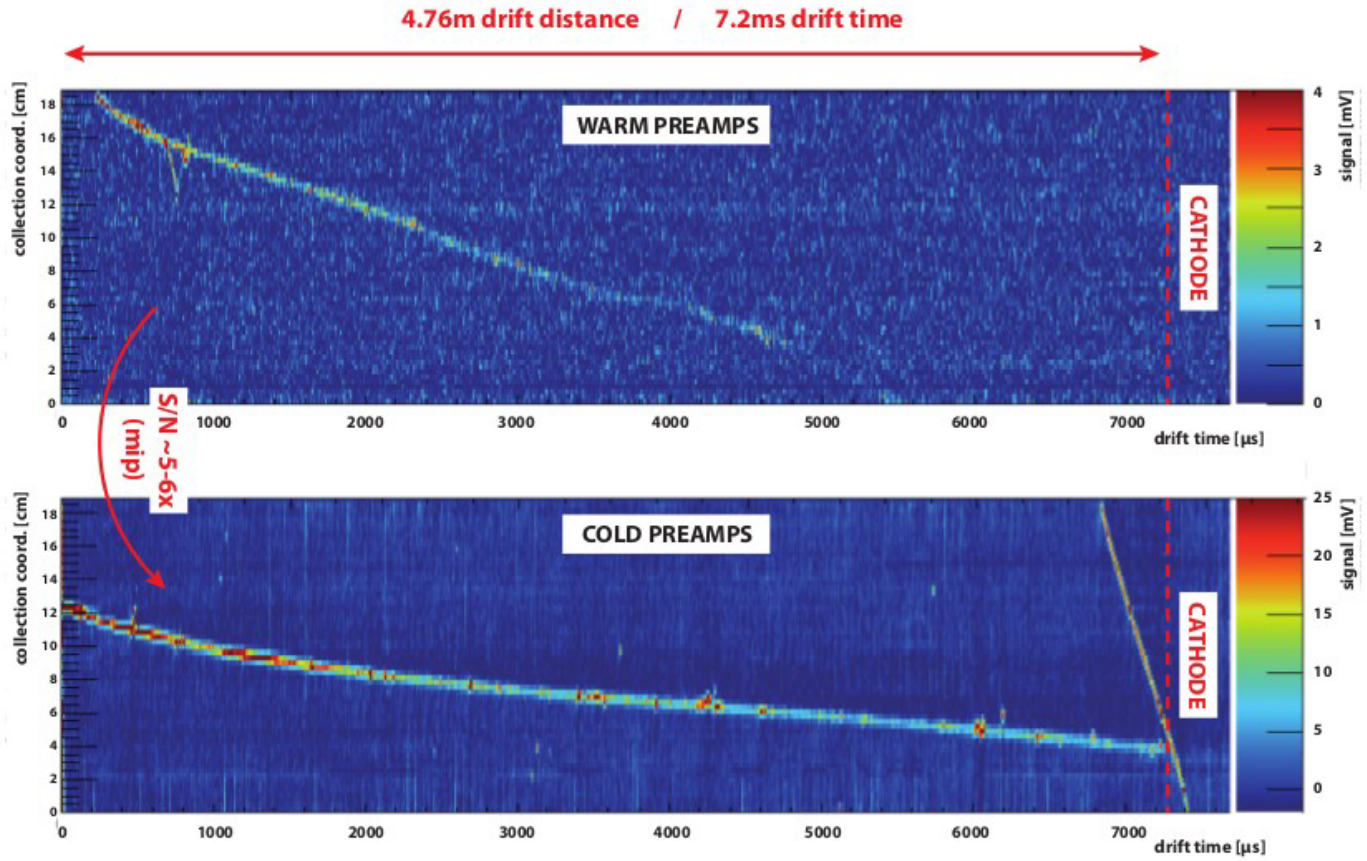


more images here: http://www-microboone.fnal.gov/first-neutrinos/index.html

Analog FE ASIC in ARGONTUBE (Bern)

5-6x Improvement on S/N



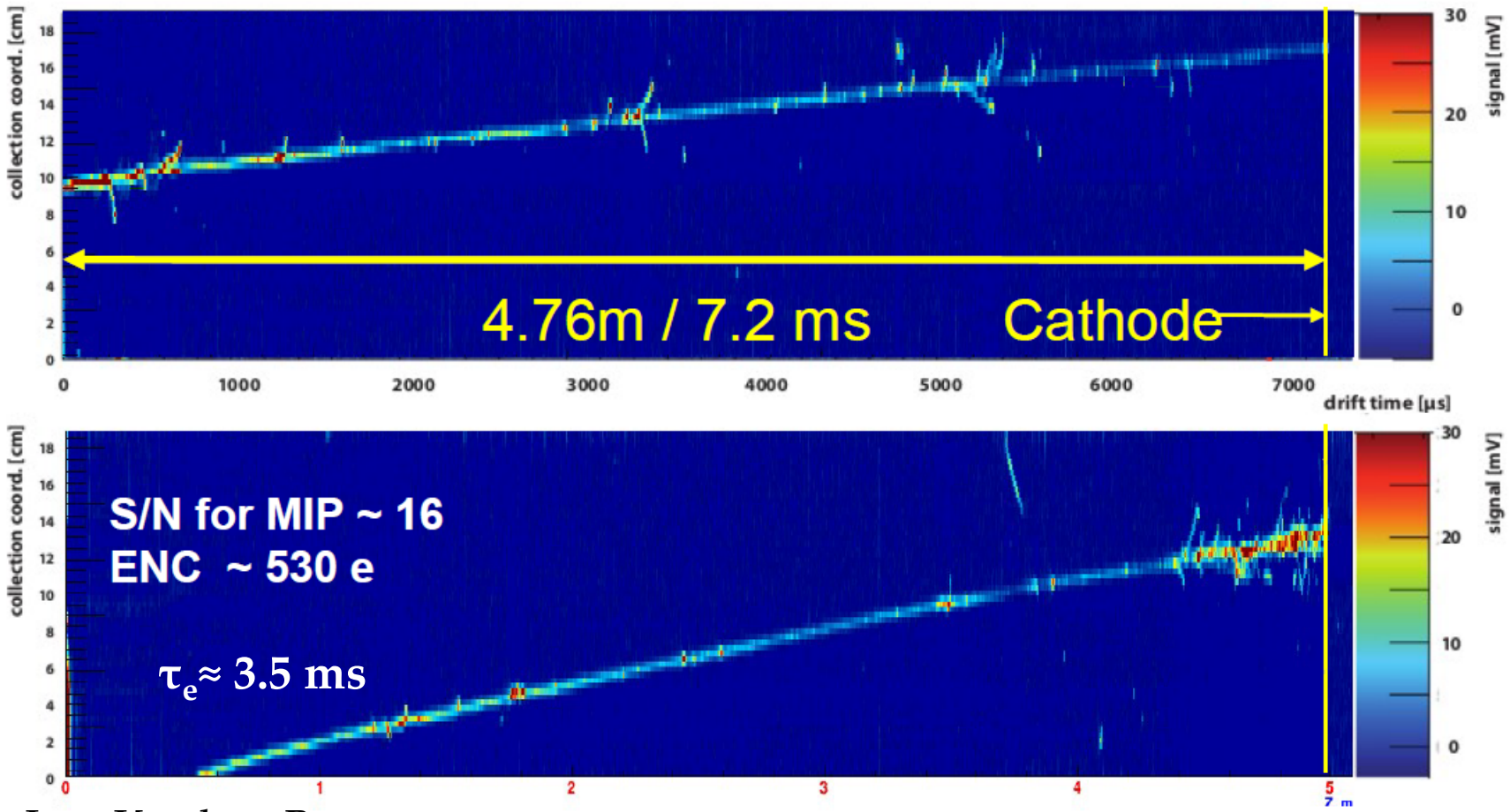


- N.B. different color scale on two plots
- Courtesy of Igor Kreslo @ University of Bern

Testing MicroBooNE cold preamps with ARGONTUBE

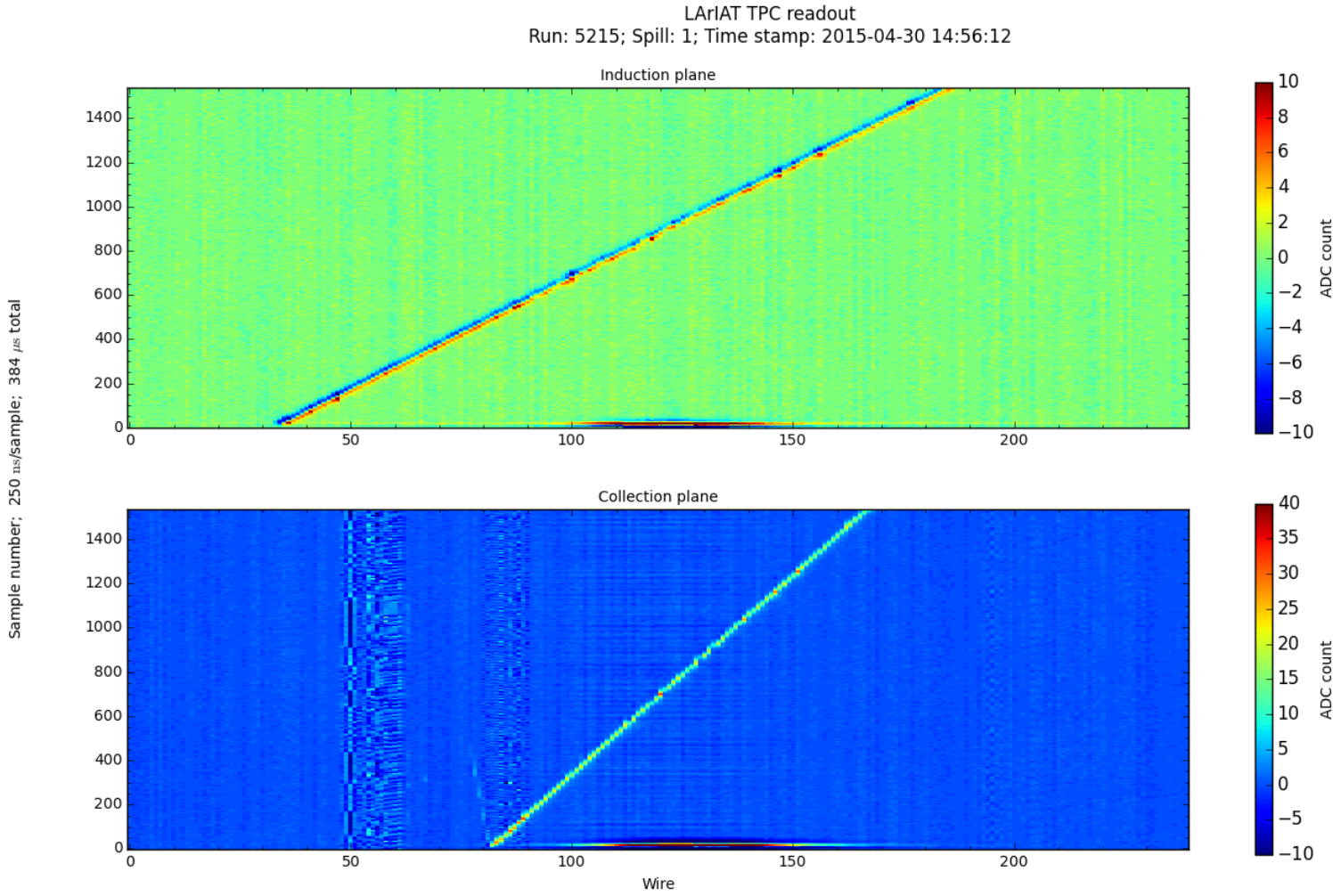
~ 5 m long electrons drift in LAR: first time!

twice MicroBooNE drift lentgh, < ½ E-field



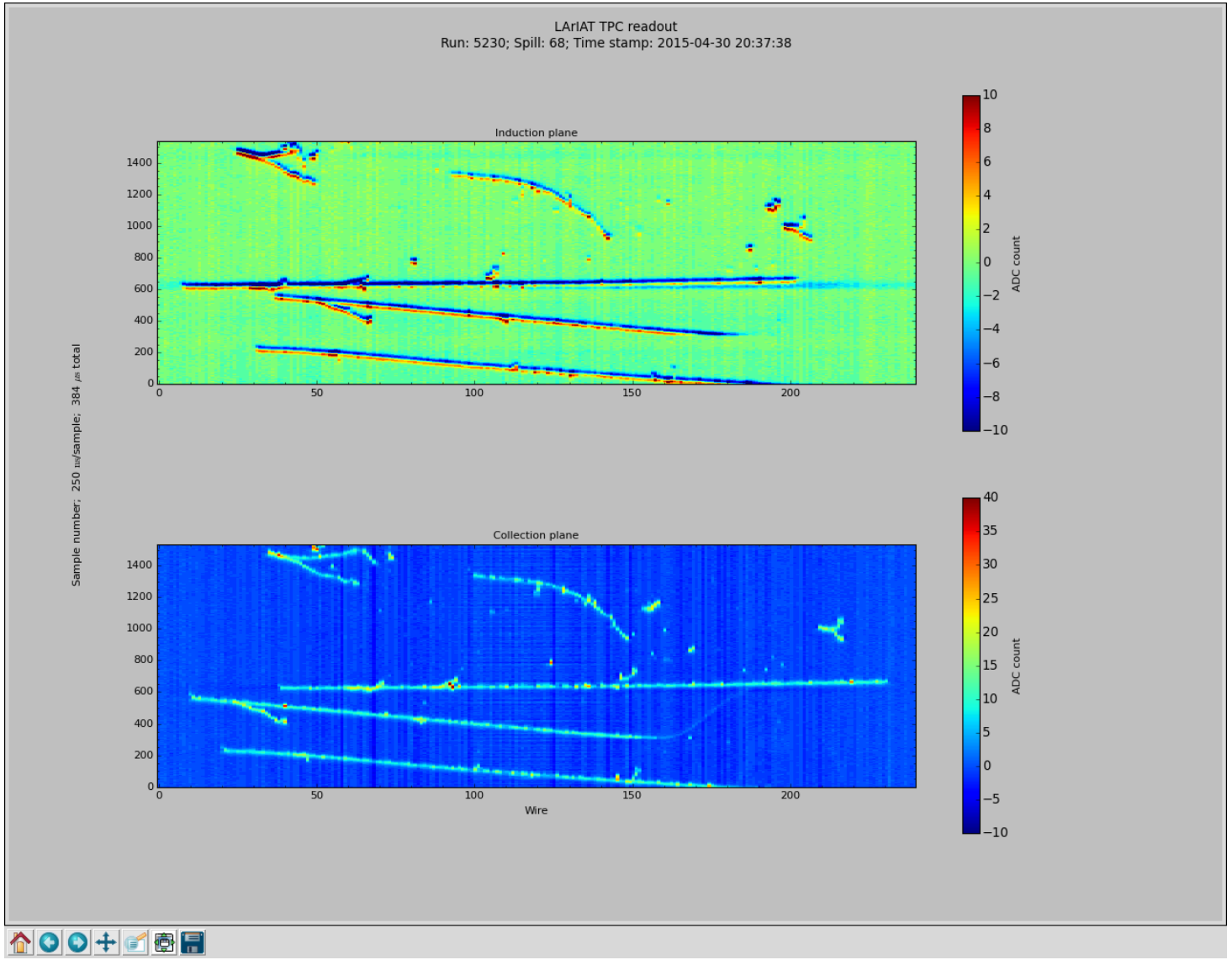
From: Igor Kreslo @ Bern

Analog FE ASIC in LArIAT



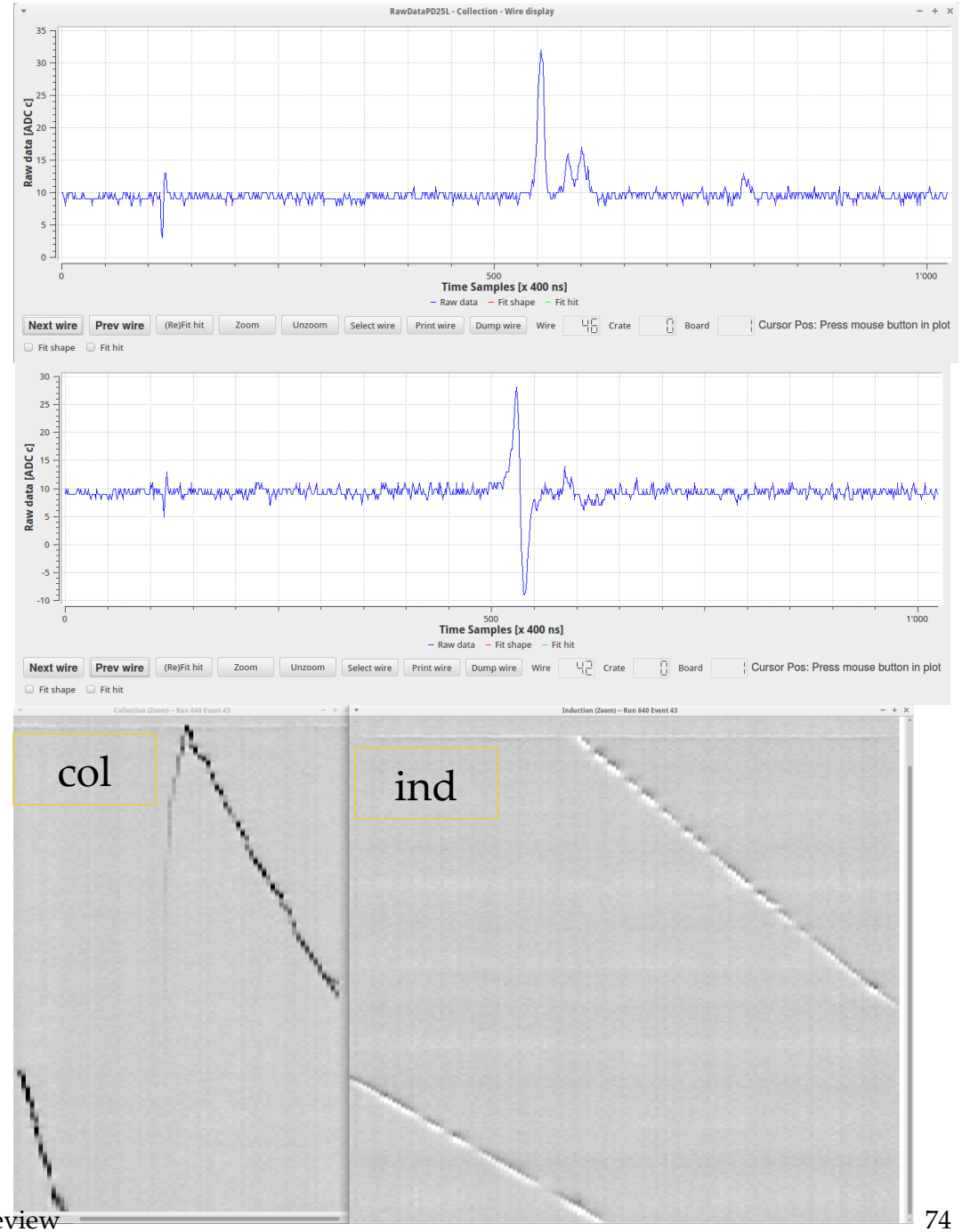
- S/N reaches ~50/1 (from Carl Bromberg @ MSU)

LArIAT Beam Event

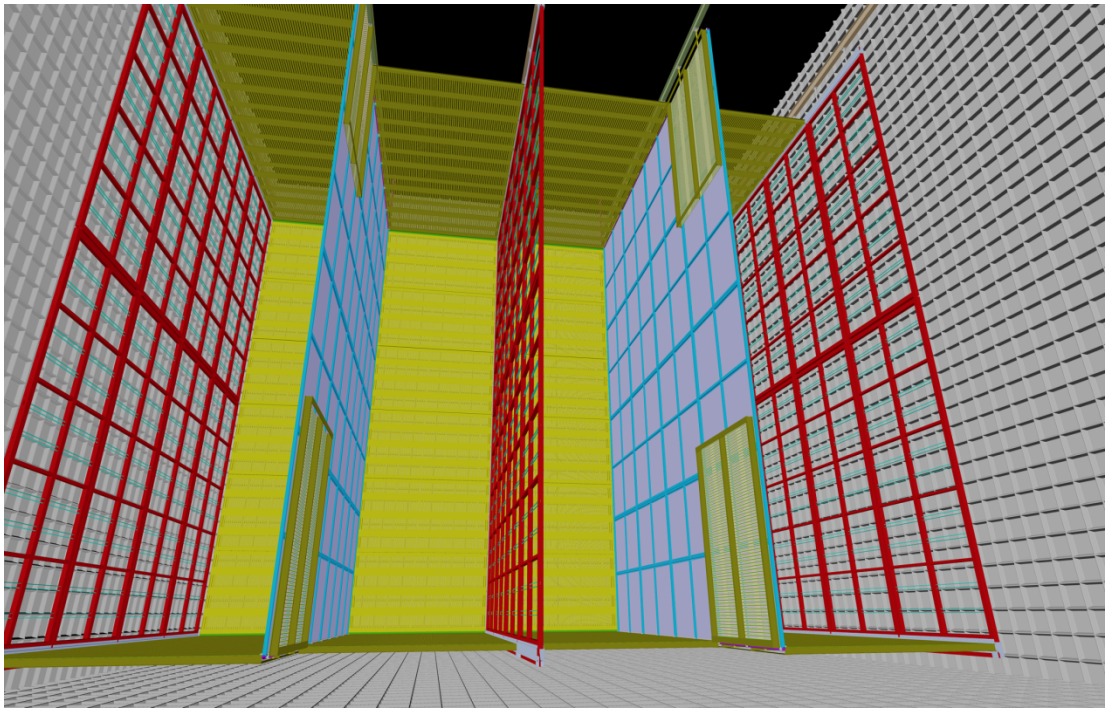


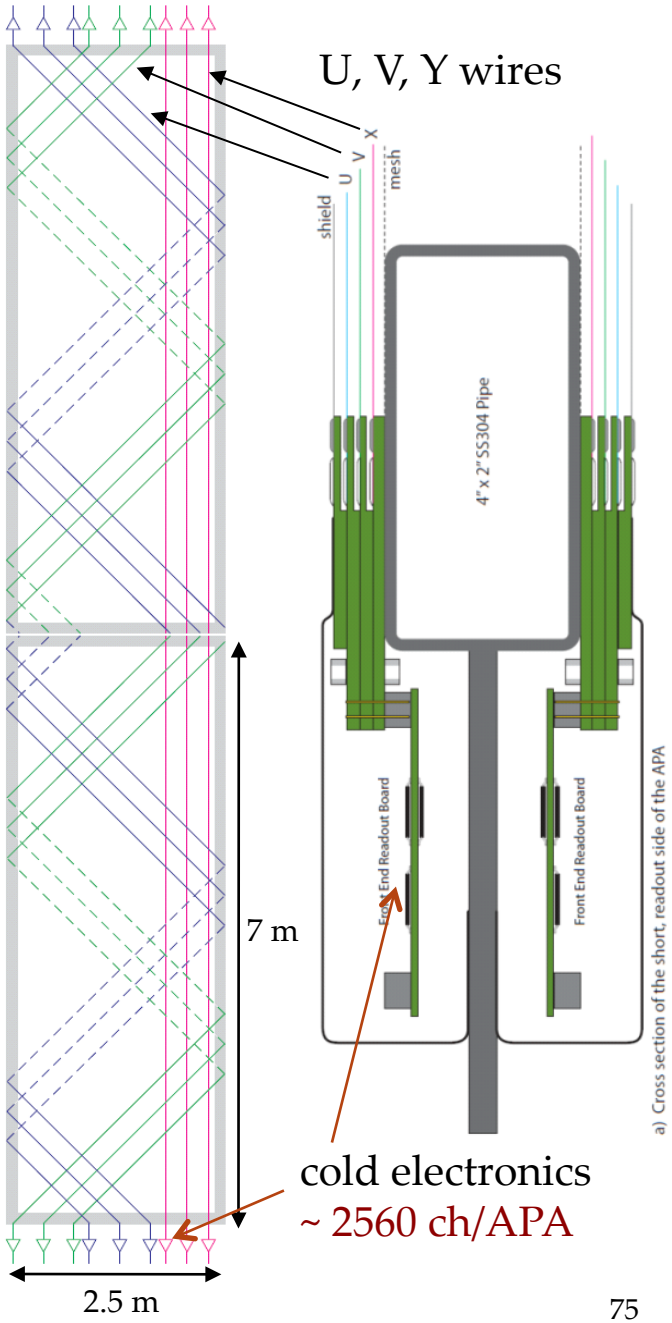
Analog FE ASIC in ICARUS 50l TPC

- ICARUS 50l TPC
  - Warm integration test in the week of March 30th at CERN
  - Cold data taking in the week of April 20th at CERN:
    - **The signals were observed and the tracks reconstructed on the first day of cooling down!**



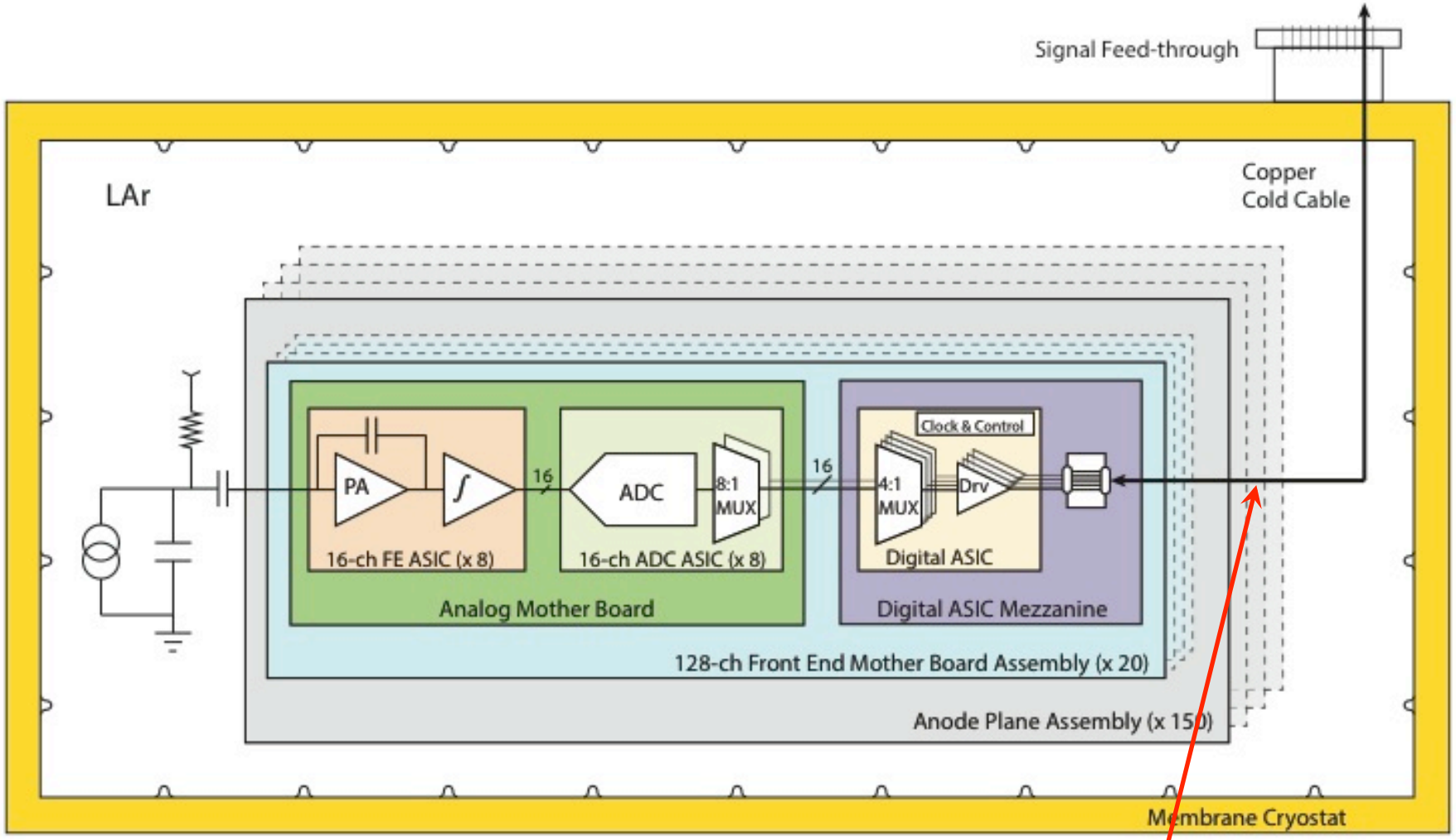
Cold Electronics for DUNE Far Detector





- BNL is developing APA & front end cold electronics system for DUNE far detector
- DUNE 10 kt Far Detector
  - ***384,000 channels***
  - 24,000 FE ASICs/24,000 ADC ASICs
  - 6,000 COLDATA ASICs (FNAL)
  - 3,000 Front End Mother Board assemblies

DUNE FD TPC Readout Electronics



SBND and ProtoDUNE-SP Cold Electronics System

- SBND and ProtoDUNE-SP share many common development of cold electronics system
  - SBND: 11,264 channels vs. ProtoDUNE-SP: 15,360 channels
  - Cold FE ASIC and ADC ASIC are identical
  - The functionality of the FEMB (Front End Mother Board) will be the same
    - Small differences in layout are required due to the wire spacing differences and readouts in the two detectors
    - FPGA mezzanine has minor difference on connectors due to the choice of cold cable
  - The feed-throughs are similar from an electrical connection point of view, but different in the flange board layout for cold cable interface
  - The Warm Interface Electronics is similar with small differences in the way the timing protocols and DAQ interface are handled.

Comparison of SBND and ProtoDUNE-SP Cold Electronics System

	SBND	ProtoDUNE-SP	Comparison	Note
FEMB	Horizonal & Vertical	Horizontal Only	***Similar***	Difference accounts for different wire pitch, attachment, cold cable
AM - Analog Mother Board	Horizonal & Vertical	Horizontal Only	***Similar***	SBND Vertical AM and ProtoDUNE-SP AM share the same design
FE ASIC	Version P2	Version P2	***Identical***	
ADC ASIC	Version P1/P2	Version P1	***Similar***	SBND schedule allows for a new submission
Cold Voltage Regulator	TPS74201	TPS74201	***Identical***	
FM - FPGA Mezzanine	MiniSAS Connector	Samtec Connector	***Similar***	Difference accounts for different cold cable
Cold FPGA	ALTERA Cyclone IV GX	ALTERA Cyclone IV GX	***Identical***	
Cold Voltage Regulator	TPS74201	TPS74201	***Identical***	
Cold Cable	3M Data + Samtec Power	Samtec Data + Samtec Power	***Similar***	Difference accounts for different requirements (up to 25 meters) of DUNE far detector
Data Cable	3M MiniSAS Cable	Samtec Twin-axial Cable	***Different***	30AWG SBND cable vs. 26AWG ProtoDUNE-SP cable
Power Cable	Samtec Twisted Pair Cable	Samtec Twisted Pair Cable	***Similar***	22AWG 2x8 SBND cable vs. 20AWG 2x9 ProtoDUNE-SP cable
Feed-through	Custom Flange and Board	Custom Flange and Board	***Similar***	Difference accounts for different cold cable and number of WIBs
Conflact Flange	Custom Designed	Custom Designed	***Identical***	
Flange Board	1 PTC Slot + 6 WIB Slots	1 PTC Slot + 5 WIB Slots	***Similar***	Difference accounts for different cold cable and number of WIBs
Warm Interface Electronics	WIB+PTC+PTB in Faraday Crate	WIB+PTC+PTB in Faraday Crate	***Similar***	Difference accounts for different WIB and PTC
WIB - Warm Interface Board	ALTERA Arria V GX	ALTERA Arria V GT	***Similar***	Difference accounts for different optical link speed, FPGA and optical transmitter
PTC - Power Timing Card	Unidirectinal Timing System	Bidirectinal Timing System	***Similar***	Difference accounts for different timing system, Nevis + MBB for SBND, Bristol for ProtoDUNE-SP
PTB - Power Timing Backplane	Custom Designed	Custom Designed	***Identical***	ProtoDUNE-SP has one WIB slot not populated and slightly different pinout definition
WIEC - Warm Infc Electronics Crate	Custom Designed Faraday Cage	Custom Designed Faraday Cage	***Identical***	ProtoDUNE-SP has one WIB slot not populated
Back End Electronics/DAQ HW	Nevis	RCE/FELIX	***Different***	Nevis design is based on MicroBooNE experiment, which has secured funding and is a proven design