Cold Electronics QA/QC plan

For the DUNE/SBND Cold Electronics Design Review
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Dean Shooltz (Michigan State University)

On behalf of the ProtoDUNE-SP and SBND Cold Electronics Working Group

Some indicators of the critical nature of Cold Electronics and QA/QC:

– CE to be installed in a system with expected 20 years lifetime and no access for service
– QA/QC plan is being prepared as a separate document to accompany TDR
– Two items from the CE design review directly relate to CE QA/QC

Conclusion: We must take QA/QC very seriously.

This presentation: Our own critical review of the ProtoDUNE/SBND QA/QC approach

Presentation structure
Build this presentation around the appropriate questions from the review committee charge letter:

Question 8:

Are the proposed integrated system tests sufficient to assure that the systems will meet the performance requirements for ProtoDUNE-SP and SBND?

Have applicable lessons-learned from previous LArTPC detectors been documented and implemented into the QA plan?

Question 9:

Is the CE design robust enough and the quality control plan and testing program sufficiently comprehensive to assure the dead/bad channel requirements for ProtoDUNE-SPand SBND are achieved?

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Answer: Meeting the detector requirements requires **many** different items:

– Need to produce enough robust and fully functional FEMB (Front End Mother Boards)

– FEMB need to perform well in real system (integrated test stands are best mimic- see other presentations)

– Need good cabling plant

– Need to get through installation procedures without damage to CE

– Requires no faults in wires, CR boards, HV systems, structure.

– Requires that we don't have premature aging effects

Most of these items are deal with in other presentations.

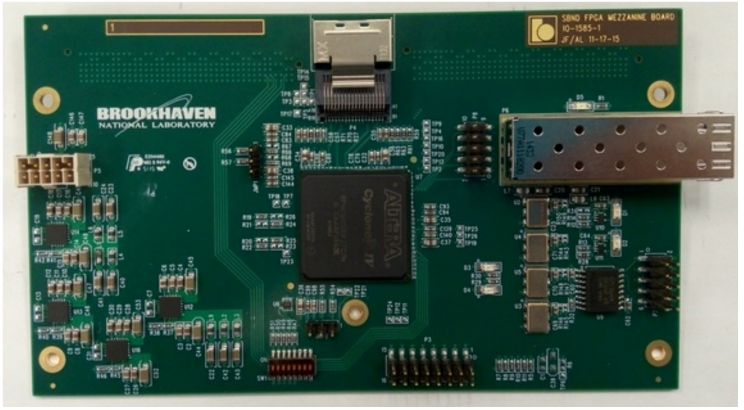
This presentation will focus on the **FEMB** as the functional unit of the cold electronics while noting that overall success depends on many subsystems.

Question: can we predict the success rate for producing 100% functional FEMBs?

Approach: Look at the FEMB as a collection of components that must work together:

FPGA
Regulators
Oscillators
Memory
Connectors
Passive components
PCB structure
PCB traces
PCB vias
Solder connections

FPGA mezzanine



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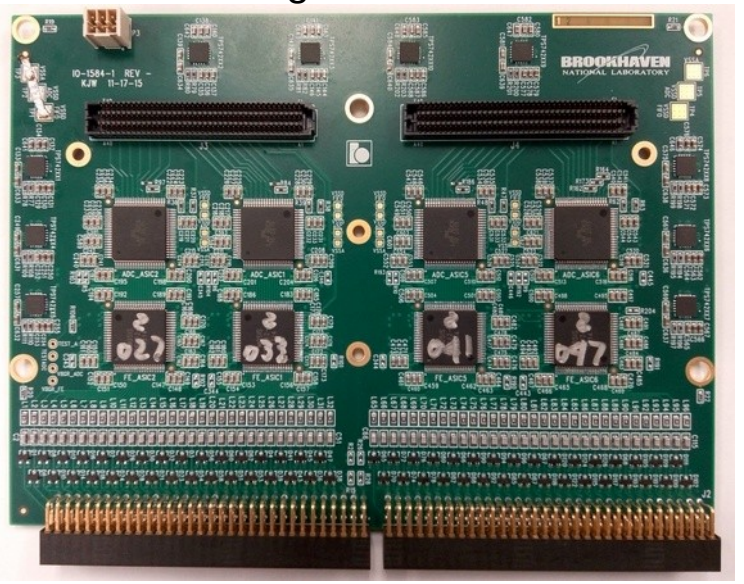
Analogue motherboard



Commercial parts:

Foundry → Packaging → QA/QC → Purchaser
For the commercial parts we are shielded from the QA/QC process.
* not really: commercial parts are not tested in cryo conditions
* we are responsible for validating performance in cryo
* we are exposed to batch variations and even unadvertised design changes not affecting manufacturer's QA/QC

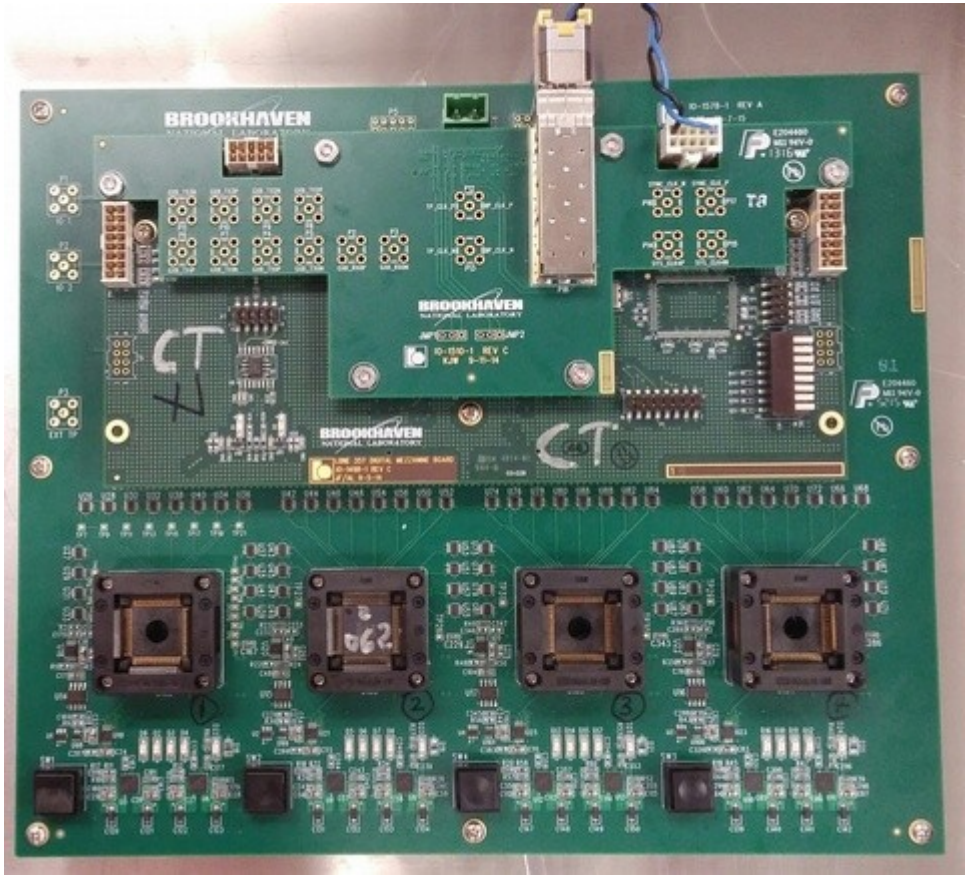
Custom parts (FE-ASIC and ADC-ASIC, and PCB itself):

Foundry → Packaging → Purchaser
* we are fully responsible for design validation and QA/QC
* QA: feeds back into design validation
* QC: we must determine acceptance threshold and corresponding yield of good chips

On next slide: focus on QA/QC of the ASIC components of the FEMB.

But we note that many other parts are also vital and some may require cryo validation at the batch level.
Example: the oscillators on the FPGA were identified as a risk for 35t and were pre-tested before assembly

FE-ASIC testing station



Initial 4-station tester is shown

Allows for full functional testing of FE-ASIC

High-speed operation and high-quality data output

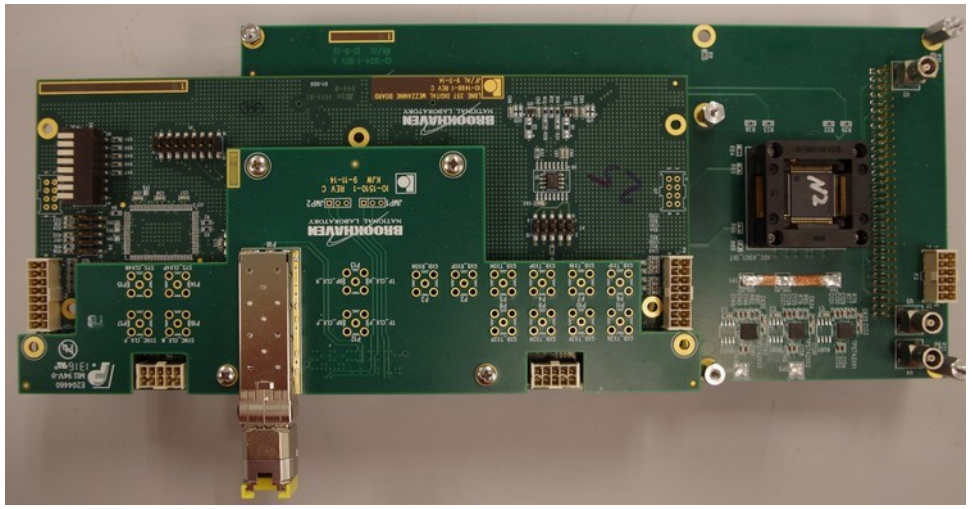
Comprehensive testing done in minutes per chip

Automated user interface is in development

<u>Updated version is in development</u>
– Tailored for newest version FE-ASIC features
– Include current draw measurements
– Add shielding for ASIC noise tests

<u>Cryo-compatible version also under development</u>
– One step behind as we develop cryo cycling technology (cryo plan on later slides)

ADC-ASIC testing station



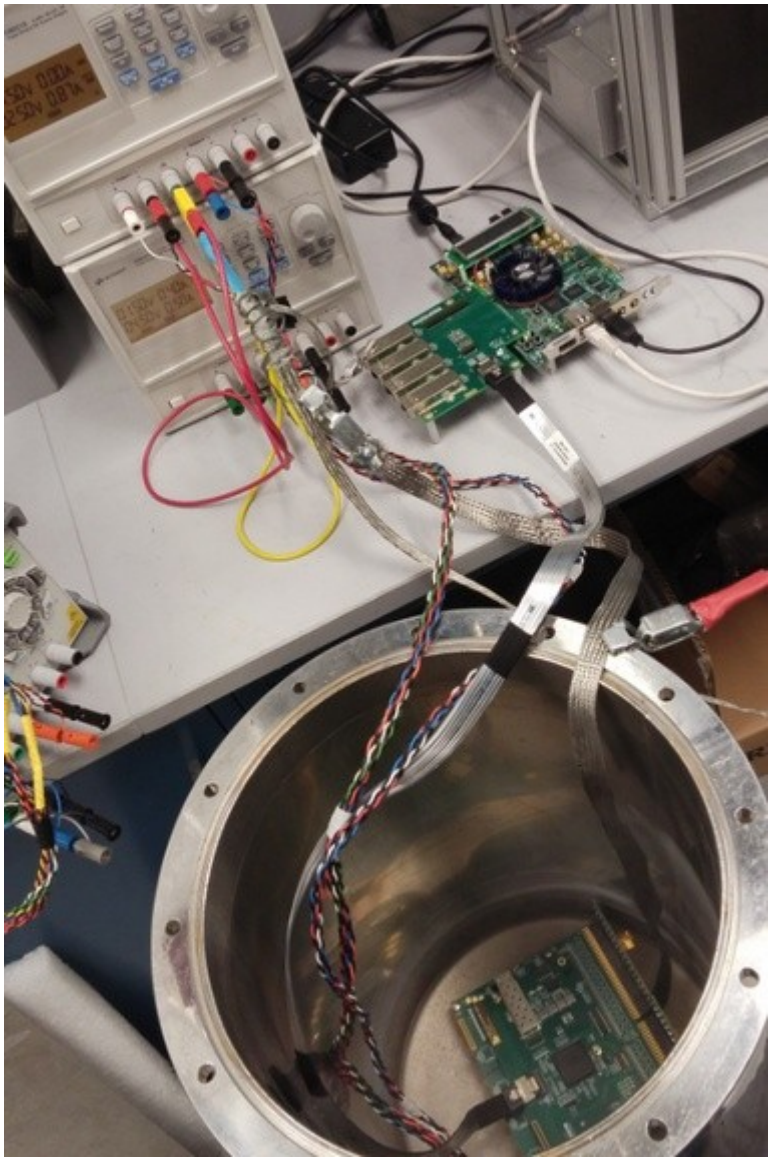
Early version shown

Four-station tester version is in development

Same idea as FE-ASIC tester:
– fully test ADC-ASIC in a short time

A cryo-compatible version is also envisioned
(cryo plan on later slides)

FEMB testing station



Early testing methods are shown

Problem: these is no way to completely eliminate condensation on the FEMB upon removal from dewar

Problem: not designed for testing hundreds of FEMBs

We are working to design an updated system with the following requirements:

– Appropriate shielding
– Controlled cryo cycling: warm → cold → warm
– Minimize cryo cycle time
– Prevent condensation on device under test
– Improved handling of device under test

Question: is cryo-testing of the FEMB components (esp. ASICs) necessary?

Points to consider:

– ASICs must run in cryo temperatures with 20+ year lifetime

– Some ASIC problems and properties that are evident only in the cold
  – Failure to start up (known possibility)
  – Pole zero cancellation / baseline restoration (unexpected/unrecognized problem)
    – This is a case of closing the QA / design validation loop with downstream physics data:
      – First given attention as a result of LArIAT TPC data
      – Issue has been communicated back to ASIC design team, effect verified at BNL, design changes are in progress
      – Will result in additions to the QA/QC plan at the ASIC level
      – More thorough initial QA/QC testing might have caught this much earlier

– But cryo testing is much more difficult than warm testing:
  – esp. at the component level, need to completely avoid water condensation
  – cycle time for (warm → cryo → warm) can be a problem for schedule

Answer: It really depends on how well the warm performance of the ASICs predicts the cryo performance.

Question: How well does warm performance predict cryo performance?

Answer drawn from supporting documentation on CE review page (Lessons Learned: Experience from MicroBooNE and 35ton)

~5% of FE-ASICs were replaced for failures in cryo conditions.

This illustrates failures that could not be predicted from warm testing.

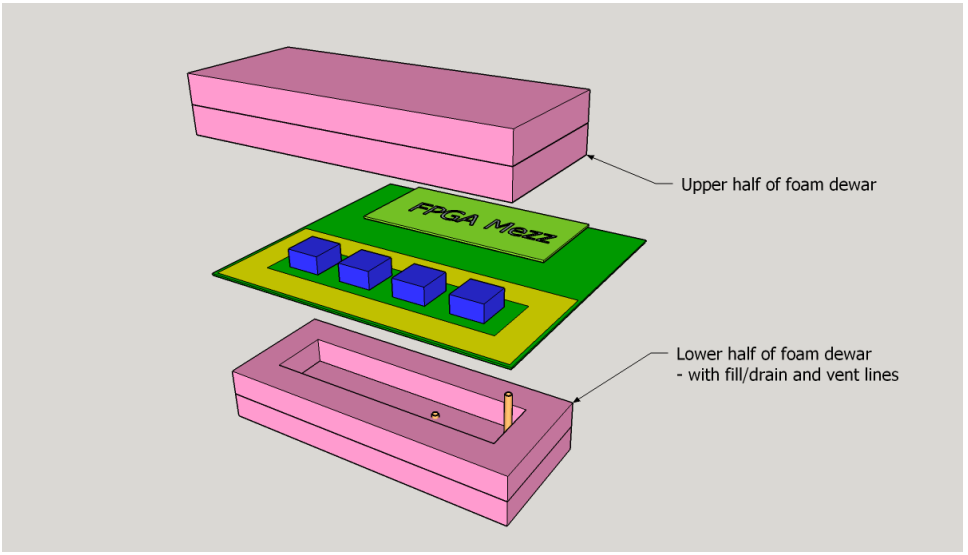
This presents a big risk for FEMB production and schedule:

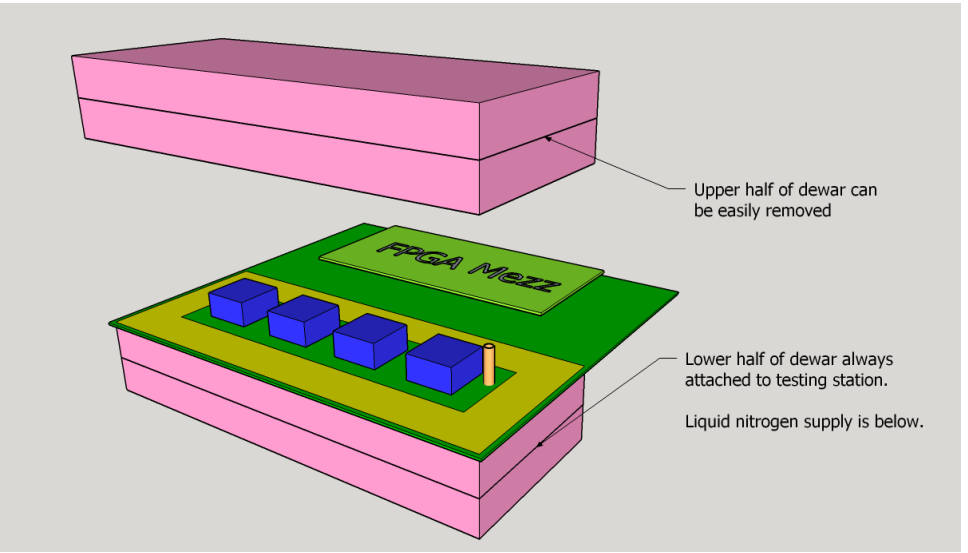
Cryo yield of FE-ASICs that are good in warm	Upper limit of good FEMBs with 8 FE-ASICs per board	Expected fraction of FEMBs that will require rework due to FE-ASIC
100%	100%	none
99%	92%	8%
98%	85%	15%
95%	66%	34%

It is HIGHLY desirable to avoid unnecessary FEMB rework cycles.
→ risk to quality
→ risk to schedule

Answer: We must be *prepared* to perform cryo testing of all ASICs, and maybe batch sampling will be sufficient.

Cryo cycling system design status page 1:
Dewar structures built around testing system





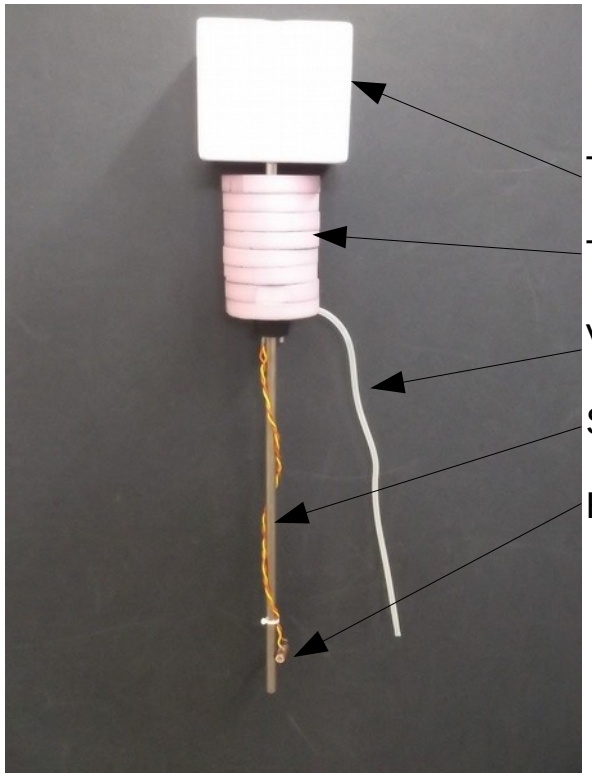
This work is in the initial design stages

Current designs are focused on foam-based dewars
– Other designs are also being considered

There are two general topologies:
– fixed, non-moving testing board
– vertical test board that can be dunked into LN2

Some preference for stationary test stand
– better setup for production testing

Cryo-cycling system design status page 2: Methods for dewar fill and drain



We received advice from condensed-matter physics colleagues

They have used this technique at times their own research

The heater is used to build a slight pressure in the storage dewar

The pressure pushes LN2 into the test dewar

Opening the vent line lets the LN2 fall back into the storage dewar

Heaters inside the test dewar have two purposes:
– reduce warmup time for acceptable overall cycle time
– boil off residual nitrogen to prevent exposure of cold CE to atmosphere
– Thus no condensation on devices under test

Initial tests with this very crude prototype are encouraging

Committee charge- Question 9:

Is the CE design robust enough and the quality control plan and testing program sufficiently comprehensive to assure the dead/bad channel requirements for ProtoDUNE-SPand SBND are achieved?

Answer:

For FEMB we think we have a sufficient approach: full comprehensive testing of all FEMB assemblies in cryogenic temperatures before installation onto TPC system. This is the final FEMB QC step.

We have also identified a need for cryo-testing the components to be installed on the FEMB, and we and we are working on creating the necessary test stands. Without cryo-testing at the component level we are exposed to a risk of significant rework tasks at the FEMB level. Reworking the FEMBs opens a risk of schedule slippage and quality issues related to handling and rework.

We have also identified a need to develop a database to handle the QA/QC data, and we are working on developing an appropriate database system.

We also recognize that the scope of CE QA/QC for ProtoDUNE-SP and SBND extends beyond the need to generate robust and functional FEMBs. Other components requiring good QC include: connectors, CR boards, cabling plant and bias voltage distribution.

Committee charge- Question 8:

Are the proposed integrated system tests sufficient to assure that the systems will meet the performance requirements for ProtoDUNE-SP and SBND?

Have applicable lessons-learned from previous LArTPC detectors been documented and implemented into the QA plan?

Reference point:

supporting documentation on CE review page (Lessons Learned: Experience from MicroBooNE and 35ton)

35t Lessons Learned:

Of 19 FEMBs produced for 35ton, 16 passed final QC. All 16 were required, leaving no spare inventory.

Among the consequences of having insufficient spares:

There was a reluctance to repeatedly cryo-cycle any FEMBs. It was considered too much of a risk due to limited stock.

Importantly, there are different classes of cryo problems that were found in 35ton:
– parts that did not work in the cold
– parts that worked intermittently in the cold
– parts that were initially good and then became unstable over time

Thus there is a clear QC benefit to multiple cycles of cryo-testing.
This would improve QC by reducing the chances of putting bad CE into the detectors where they are inaccessible.
But there is also probably a point where repeated cryo-cycling causes more harm than benefit.

Conclusion: *We could use more information to help determine the balance point for cryo-cycling FEMBs during QC*

Actions based on lessons learned:

Need to budget for sufficient spare FEMBs

Should cryo-cycle an FEMB enough times to learn about the balance of improving QC and risking damage.

Testing to failure will also help us identify any weak points in the design (a *design validation*)
– Critical components, critical PCB vias, critical connectors?
– Single Point Failures?
– Cost is small compared to value of the information- and there is no other way to get this information

We could start immediately: There are a few uncommitted FEMBs recovered from the 35t detector.
These could be cold-cycled multiple times in an attempt to identify failure modes related to cryo-cycling.

35t Lessons Learned:

The strength of the 35t QA/QC effort was compromised by limited available resources (time, manpower).

These limitations, along with insufficient cryo-testing capability, led to a bypass of ASIC-level cryo QC.
– That further led to an increase of FEMB rework cycles. Some boards were reworked multiple times.

The FEMB final QC approach was not fully developed. A balance between multiple cryo-testing cycles and wear on the boards was not established. A tougher final QC might have shaken out more problems before installation on the TPC.

How this relates to ProtoDUNE-SP and SBND:

We are now facing a need to develop a comprehensive QA/QC system and again with limited time remaining.

A somewhat similar situation

This situation has risk- adequate QA/QC is a critical and central part of the CE production.

This risk is mitigated by the added manpower of more institutions (Fermilab, MSU, Penn, LSU, and UTA).

Improvements in QC (at FEMB in particular) reduce the risk of installing bad or flaky parts into the detectors.

More Lessons Learned:

There are also examples where the CE designs have taken us into new LarTPC performance territory:

MicroBooNE and LArIAT- commissioned and active and taking data with unprecedented S/N

How this relates to ProtoDUNE-SP and SBND:

This shows that with careful implementation we can certainly succeed in pushing LarTPC performance to the next level.

Whereas MicroBooNE and LarIAT have warm ADCs, ProtoDUNE-SP and SBND have moved this function into the cryostat. This is enabling in terms of handling DUNE-scale channel count and in terms of further increasing S/N.

Along with this added power comes added responsibility- what goes in to the cryostat must be of the highest quality. With more of the system moved into the cryostat and beyond access for repair or upgrade we must be correspondingly more careful.

Conclusions:

LArTPC detectors require good and stable components- there is no opportunity to service after installation.

These detectors (and later DUNE) are of enormous scale and cost. We cannot afford any weaknesses in our QA/QC methods.

Part of ProtoDUNE's mission is to qualify our ability to succeed at DUNE
– Highest-quality QA/QC is central to this mission- our methods should show how we will do this in DUNE

The bottom line:

QA/QC testing stations need to be ready prior to the arrival of a few thousand ASICs in Spring 2017

Ideally the overall QA/QC systems in Spring 2017 will be:
– Capable of fully qualifying components for 20 years of operation in cryo conditions
– Automated to the point of being usable by shifters
– QC information will be fed to a central database

Getting to this status earlier than the last minute is desirable for many reasons:
– More time for more people to explore the device characteristics (for QC and QA and design validation)
– More time to develop the procedures and further automate the testing
– More cushion against unexpected hurdles (for instance the cryo setups)
– More time to analyze the device data and search for unexpected problems