Cold Electronics Introduction and Requirements

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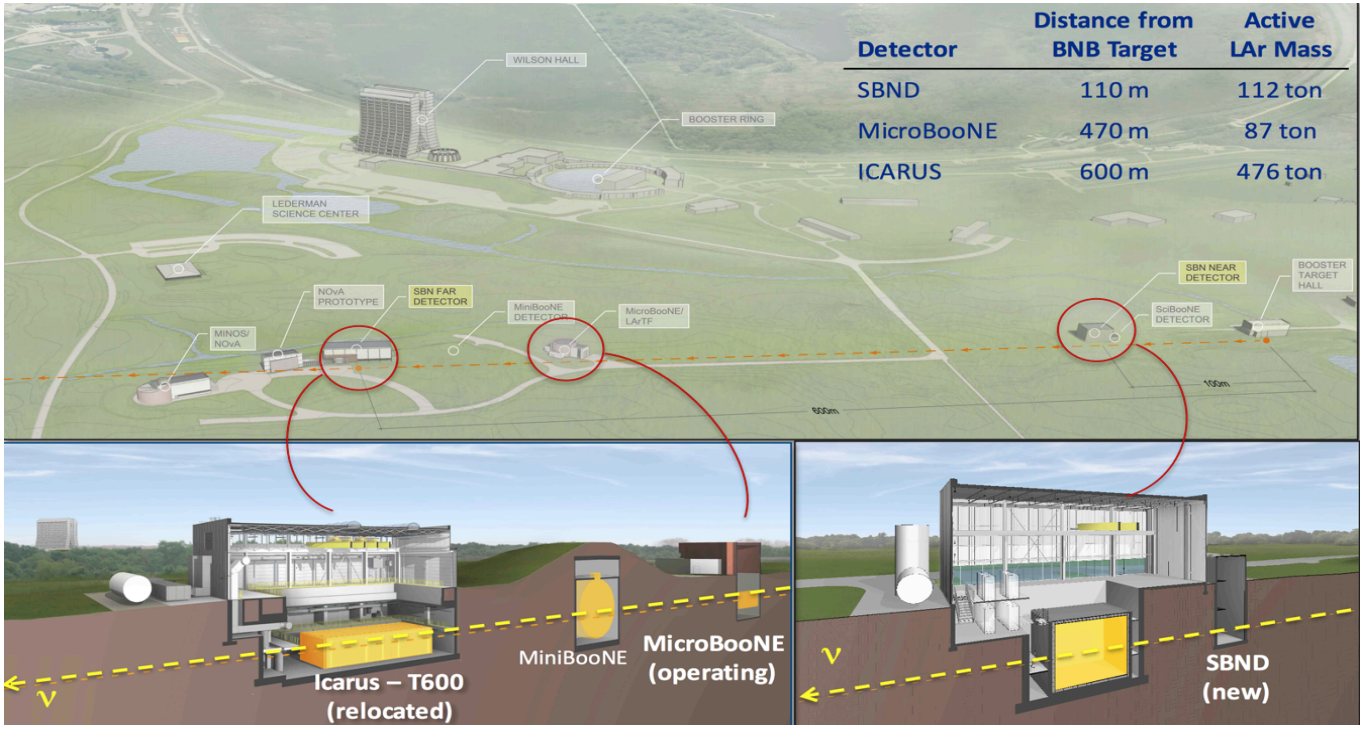
Cold Electronics Review
October 12, 2016

Outline

- SBND and DUNE physics
- Single phase TPC and cold electronics
- Cold electronics organization
- Requirements
- Conclusions
- Review organization and charge matrix

SBND Physics

- The Short Baseline Neutrino Detector (SBND) will take neutrino beam data in the Fermilab Short Baseline Neutrino Program starting in 2019

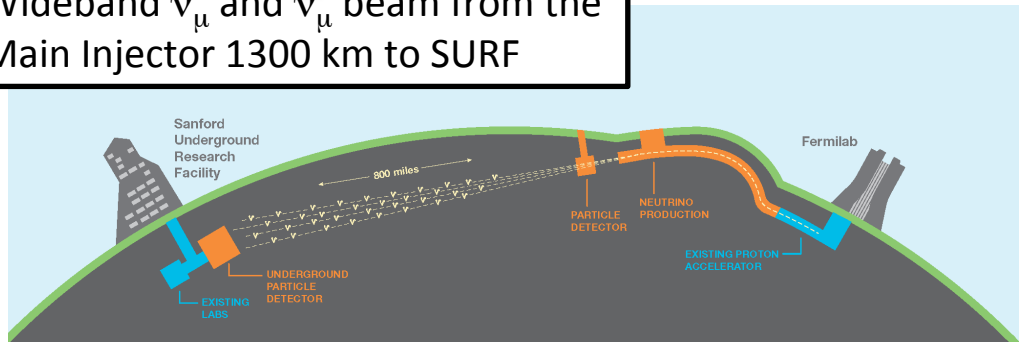


- Measure ν_e and ν_μ interactions with high-statistics
  - High-precision ν–Ar measurements: 1.5×10^6 ν_μCC and 1.2×10^4 ν_eCC interactions/year
  - Sterile neutrino oscillation search

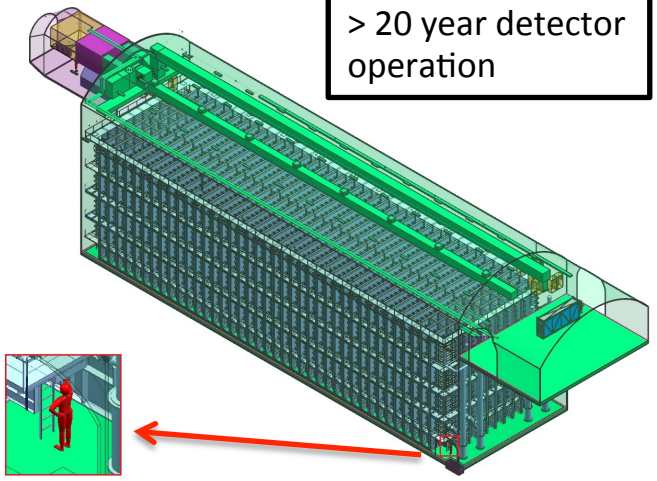
DUNE Physics

- The Deep Underground Neutrino Detector (DUNE) will take neutrino beam data from Fermilab in the Long Baseline Neutrino Facility (LBNF) starting in 2026

Wideband ν_μ and $\overline{\nu}_\mu$ beam from the Main Injector 1300 km to SURF



> 20 year detector operation

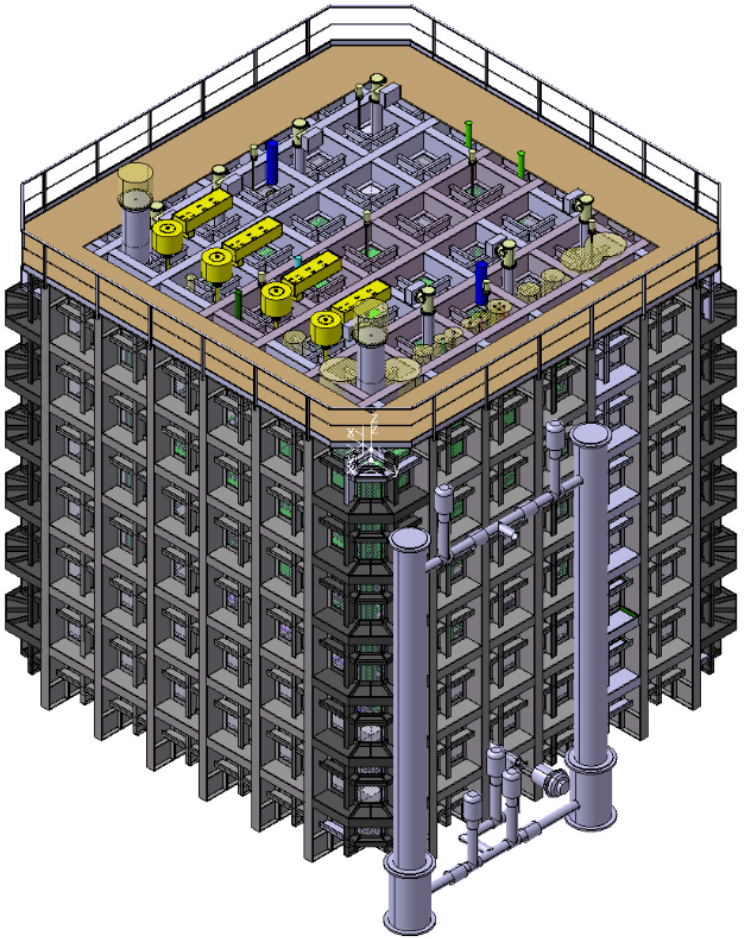


DUNE single phase far detector module
10 kton fiducial volume LArTPC at 4850L

- Measure ν_e appearance and ν_μ disappearance
  - Sensitive to MH, CPV, and neutrino mixing parameters
  - Order 1000 ν_e appearance events detected via ν_e charged current (CC) interactions in ~7 years of equal running in neutrino and antineutrino mode
- Nucleon decay:
  - $p \rightarrow \overline{\nu} K^+$ in DUNE has ~97% signal efficiency with ~1 background event/Mt-year
- Supernova burst neutrinos: ν_e-Ar CC absorption

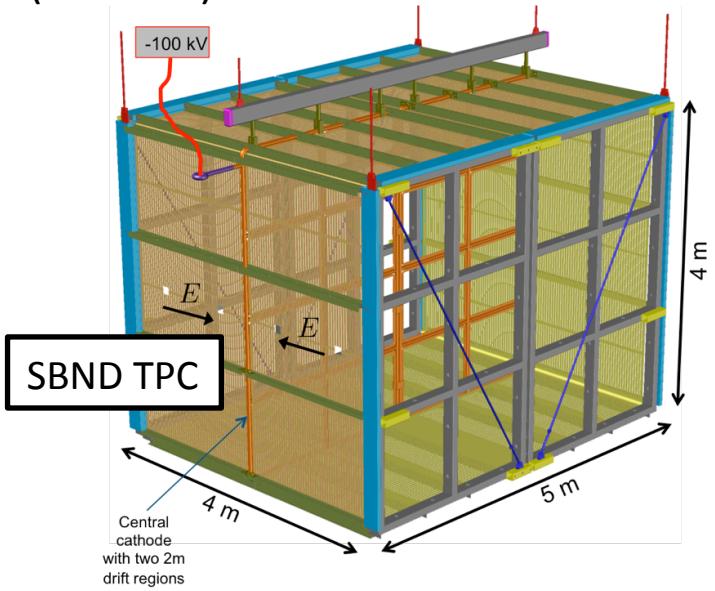
Single-Phase ProtoDUNE

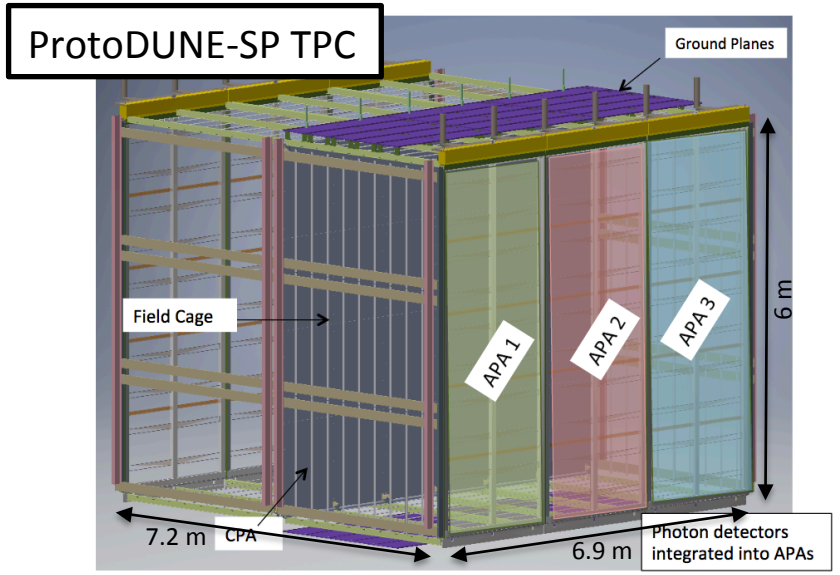
- 700 ton LAr TPC
  - Prototype using full scale components of DUNE far detector module
- Will take data from charged particle beam in the CERN neutrino platform
  - Schedule driven by CERN long shutdown in Oct 2018
  - Detector commissioning in summer of 2018
  - Cold electronics installed from August-December 2017
- Goals
  - Measure detector response to known particles
  - Confirm modeling and simulation
  - Validate mechanical and electrical design and interfaces
  - Demonstrate performance of cold electronics at a scale 10x larger than previous prototype(s)



LArTPC

- Single-phase ProtoDUNE and SBND are liquid Argon Time Projection Chambers (LArTPCs)



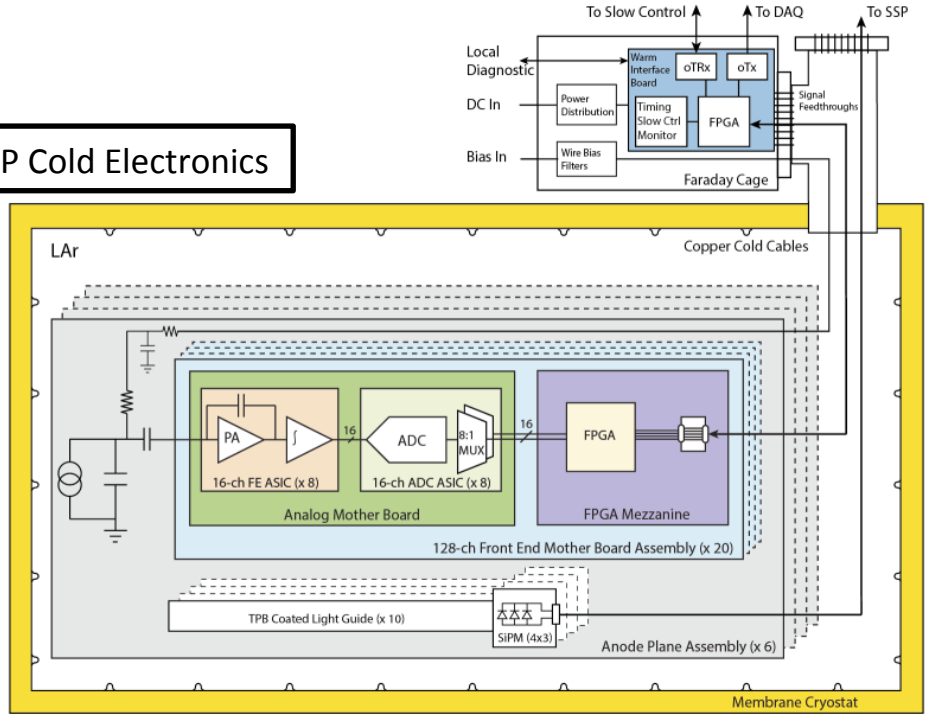


- Electrons from ionizing particles drift in an electric field to wire Anode Plane Assemblies (APAs) where the e^- charge is measured
- Design choices for the TPC directly impact the design of the cold electronics
  - Wire spacing and length
  - Drift length and drift electric field
  - Argon purity (electron lifetime)

Cold Electronics

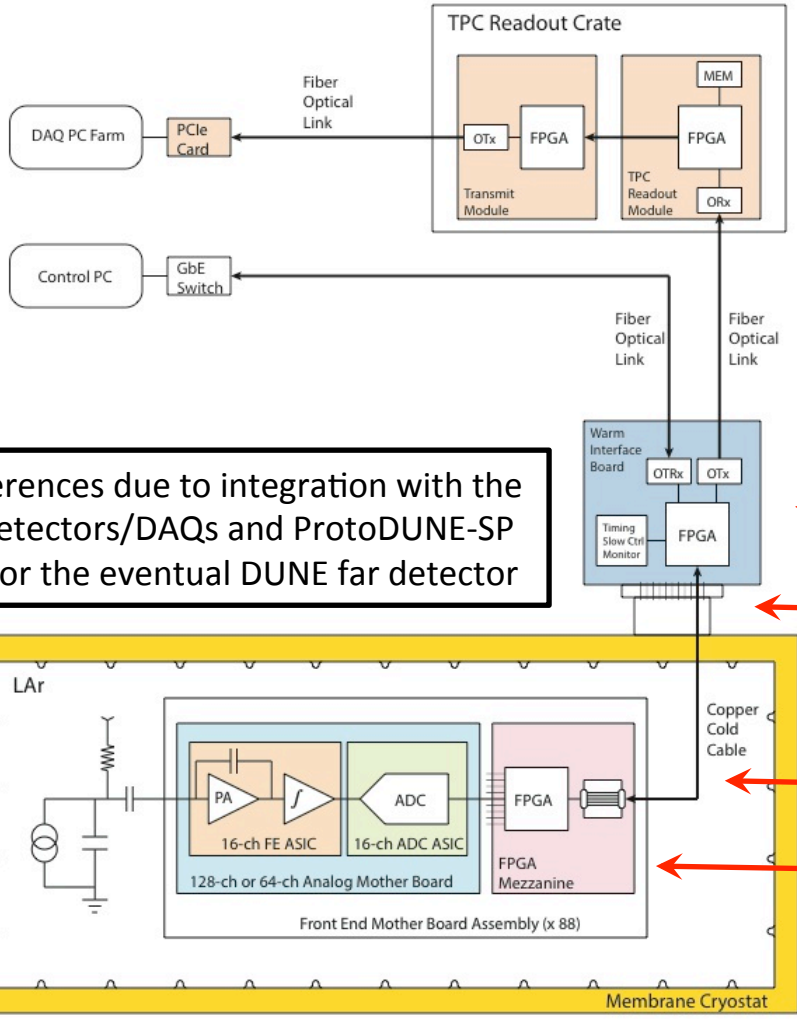
- The function of the Cold Electronics (CE) is to process the charge induced/collected on the APA wires, digitize, and transmit the digitized data from the LAr to the DAQ

ProtoDUNE-SP Cold Electronics



- Objectives:
  - Minimize noise by placing amplification as near as possible to the TPC wires
  - Minimize cryostat penetrations by placing the digitization and multiplexing inside the cryostat
  - Transmit all TPC wire data without significant loss of fiducial volume or detector performance

SBND Cold Electronics



TPC Readout Electronics

Back End Electronics

Front End Electronics

Warm Interface Electronics

Signal Feed-through

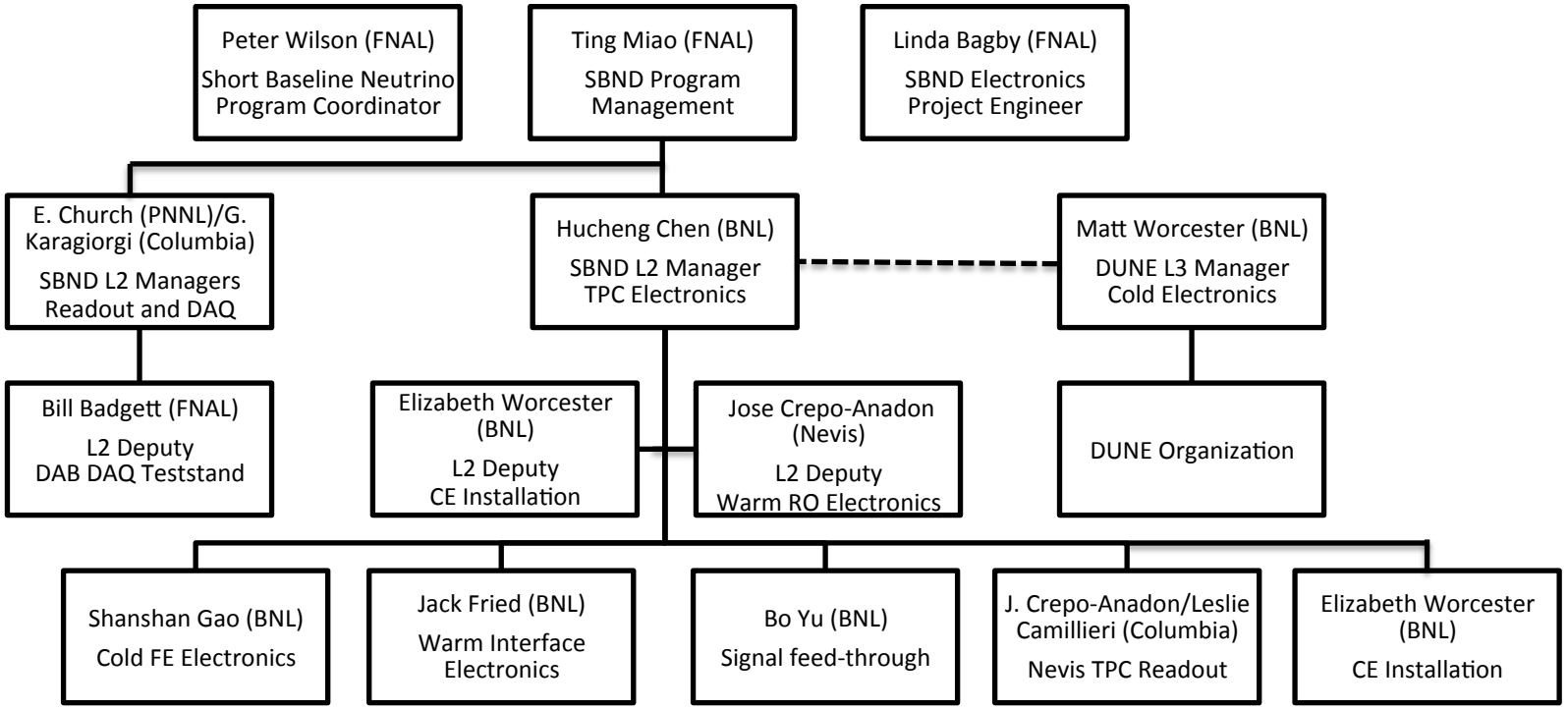
Cold Cable

Cold Electronics

Minor differences due to integration with the different detectors/DAQs and ProtoDUNE-SP designing for the eventual DUNE far detector

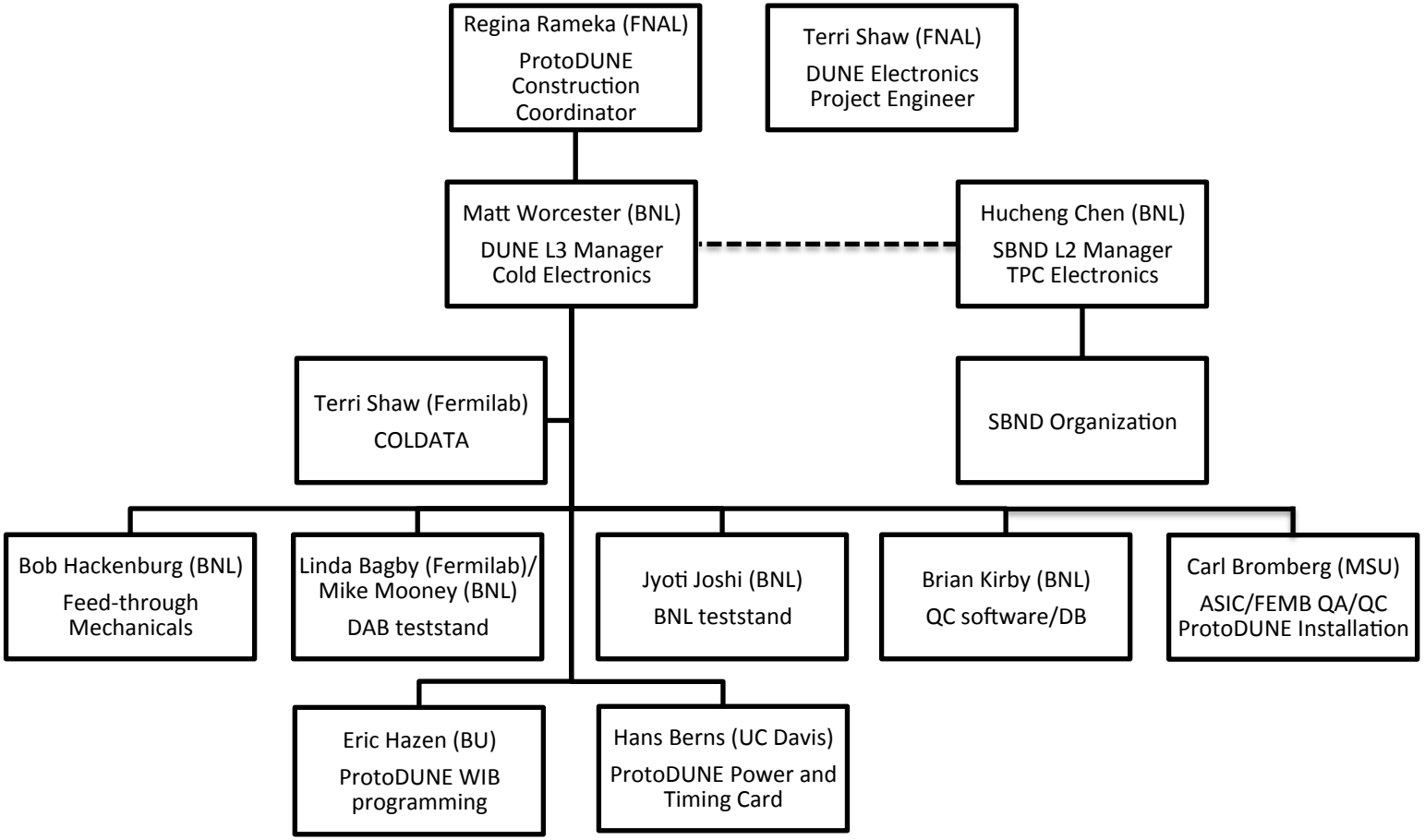
SBND Organization

- Cold electronics is a joint project between SBND and ProtoDUNE-SP



- Decision in 2015 to use already ongoing SBND design for ProtoDUNE-SP
  - Cold ASICs identical between experiments
  - Front End Motherboards functionally identical
  - Cryostat signal feed-through and warm electronics concepts the same

DUNE Organization



- DUNE L3 Managers for APA, CE, Photon Detectors, FC/CPA/HV, DSS and integration now managed by a ProtoDUNE-SP Construction Coordinator
- Many tasks listed under DUNE directly benefit SBND and vice versa

Cold Electronics Team

- ProtoDUNE:
  - BNL:
    - System design, cold ASICs, FEE, cold cable, signal feed-through, warm electronics
    - > 25 designers, engineers, technicians, and physicists
  - MSU:
    - ASIC/FEMB QA/QC
    - Leadership for CE installation at CERN
    - Engineering for installation/integration at CERN
  - Penn:
    - FEMB testing
  - Boston:
    - Firmware for WIB
    - DAQ/CE integration
  - UC Davis
    - Power and Timing Card
  - LSU:
    - Physicists for QC and installation/integration at CERN
  - Fermilab
    - DUNE electronics project engineer
    - Grounding and shielding committee
    - Power and warm cable
- SBND:
  - BNL:
    - System design, cold ASICs, FEE, cold cable, signal feed-through, warm electronics
    - > 25 designers, engineers, technicians, and physicists
  - UT Arlington
    - Integration testing (baby TPC)
    - Student/postdoc for QC and installation/ integration at Fermilab
  - Penn
    - Students for QC and installation/integration at Fermilab
  - Fermilab
    - Vertical slice test stand (DAB)
    - Postdoc for integration testing and installation/ integration
    - Faraday cage test (F0)
    - SBND electronics project engineer

Requirements

- DUNE requirements
  - DUNE global objectives drive the science requirements
    - Measure MH, CPV ➔ CC energy resolution and multiple track separation
    - Proton decay sensitivity
    - Supernova burst neutrino detection
  - Science requirements set the Far Detector requirements, which in turn set the cold electronics TPC readout requirements
  - DUNE-doc-1807 gives the flow from CE parameters up to the DUNE global objectives
- Cold electronics requirements set the parameters defined in the following tables
- DUNE cold electronics requirements are sufficient for
  - SBND physics goals
  - ProtoDUNE-SP prototyping goals

Cold Electronics Requirements

ID	Parameter	Value	Requirement	Rationale
1.1	Electronics Lifetime	25 years	All components of the electronics chain inside the cryostat shall have lifetime corresponding to the expected running time of the DUNE detector.	Detector lifetime is expected to be >20 years.
2.1	Channel Reliability	< 0.6% dead channels	The fraction of dead channels shall not adversely affect the fiducial volume of the detector for the 4 primary physics goals.	Fiducial volume must not be reduced by more than 2%.
3.1	Minimize Mechanical Feedthrough	32:1 channels per link	The overall electronics design shall minimize the heat and noise input into the cryostat.	Reduce number of feed-throughs and feed-through size by inserting digititzation, control, and multiplexing inside the LAr cryostat
6.1	Electronics S:N Budget Collection Wire	1300 e-	Total equivalent noise charge (ENC) at the output of the FE pre-amplifier shall be less than 1/9 of the expected worse case instantaneous charge arriving at the APA from a MIP	Accounts for wire pitch, electron losses due to recombination and drift; includes the requirement on electron lifetime of 3 ms; recombination and drift time are a function of drift HV; Total equivalent noise charge (ENC) at the output of the FE pre-amplifier shall allow less than 0.1% of MIP energy deposits on the collection wires to be lost below threshold.
6.2	Electronics S:N Budget Induction Wire	650 e-	Total equivalent noise charge (ENC) at the output of the FE pre-amplifier shall be 0.5 the collection wires	The FE pre-amplifier is to be the same for both collection and induction wires, equivalent MIP charge on the induction plane is expected to be <0.5 of the collection plane.
7.1	Charge Resolution	1%	Charge resolution in a single channel for the collection wires shall not be a contributing factor to the measurement of energy deposition.	The Landau fluctuation is expected to be 14% sigma for 5 mm thick restricted energy loss for MIP. The charge resolution must be much smaller than this. We set it to be 1%

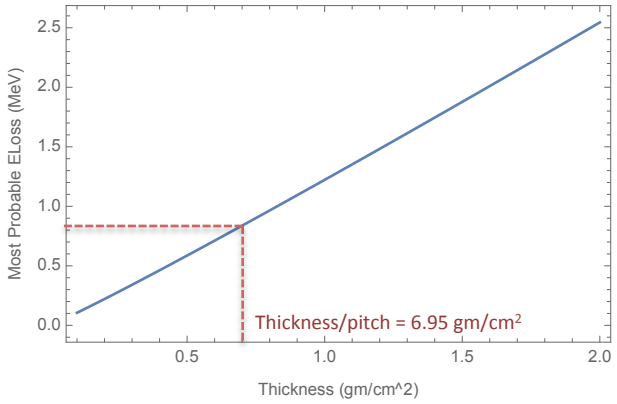
Signal to Noise

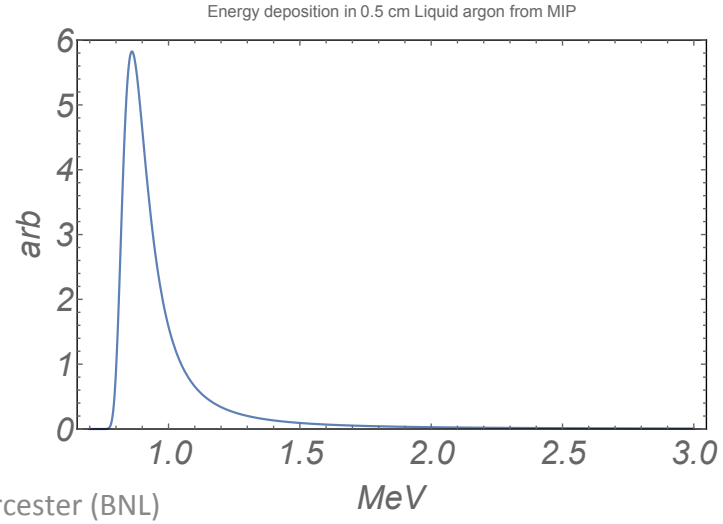
Total equivalent noise charge (ENC) at the output of the FE pre-amplifier shall be less than 1/9 of the expected worse case instantaneous charge arriving at the APA from a MIP.

- Driven by far detector S:N requirement to "distinguish a Minimum Ionizing Particle (MIP) track cleanly from electronic noise everywhere within the drift volume."
- Simple calculation of charge from a MIP track at the cathode parallel to the wire spacing:

$$\frac{E_{loss}\ (0.5\ cm)}{LAr\ E_{ee}} \times \frac{Recombination}{(500\ V/cm)} \times e^{-\frac{DL/velocity}{e^- lifetime}} = \frac{0.83\ MeV}{23.6\ eV} \times 0.7 \times e^{-\frac{3.6m/1.6\ m/ms}{3\ ms}} = 11{,}629\ e^-$$

- Sets the collection wire noise parameter at ENC < 1300 e^-
- Equivalent charge on the induction wires is expected to be 0.5 x collection wire charge
- Induction wire noise parameter ENC < 650 e^-

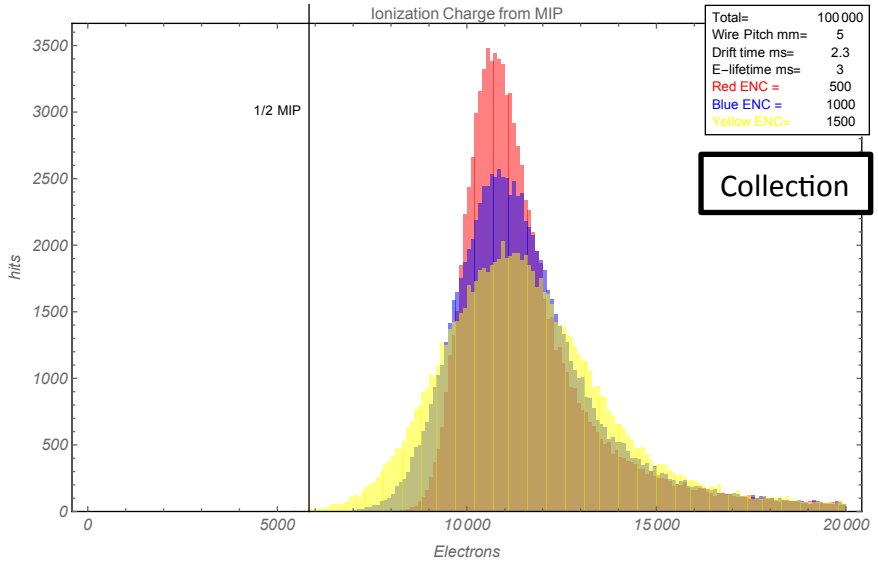




Signal to Noise

ENC at the output of the FE pre-amplifier shall allow less than 0.1% of MIP energy deposits on the collection wires to be lost below threshold.

- Model the ionization charge at the collection wire with a Landau Gaussian
- Set the threshold to ½ of a MIP charge at the wire



Noise (e-) (induction)	% MIP single deposit loss	σ (mean-threshold)
500	0.02	3.7
600	0.06	3.4
700	0.16	3.2
800	0.37	2.9
900	0.72	2.7

Calculation for induction (0.5 collection) wires with Gaussian approximation for Landau peak.

- Integrate the fraction of MIP single deposits that fluctuate below the threshold
- Collection/induction wire noise parameter ENC < 1300/650 e^-

FE ASIC Requirements

ID	Parameter	Value	Requirement	Rationale
100	FE ASIC technology	180 nm	FE ASIC shall be 180 nm CMOS integrated circuit.	Defines the power consumption, 1.8V bias, and 1.4V maximum output per channel. 16,000 transistors in current design.
100.1	Power Consumption	< 10 mW per channel	The heat loss due to electronics in the LAr shall not dominate the total heat load on the cryogenic system.	Current budget is maximum 10 mW per Front End channel.
100.2	Filter peaking time	1.0 µsec	The CE FE ASIC shall provide a shaper peaking time option equal to the specified parameter for optimal performance.	1.0 µs corresponds to an average electron diffusion of ~1.4 mm expected for the nominal electric field of 500V/cm.
100.3	Minimum peaking time	0.5 µsec	The CE front end shall provide the option for a minimum shaping time specified by the parameter.	Physics goals may require optimization of the electronics response.
100.4	Maximum peaking time	3 µsec	The CE front end shall provide the option for a maxium shaping time specified by the parameter.	Physics goals may require optimization of the electronics response.
100.5	Gain	6	The CE FE ASIC shall provide programmable gain settings over a dynamic range specified by the parameter. 4.7, 7.8, 14, and 25 mV/fC per independent channel.	Physics goals may require optimization of the electronics response.
100.9	Calibration	1%	The FE ASIC shall contain a test capacitor sufficiently accurate to calibrate the gain to 1%.	Measure charge resolution to 1%. Each FE channel can also receive a voltage from an external source.

ADC ASIC Requirements

ID	Parameter	Value	Requirement	Rationale
200	ADC ASIC technology	180 nm	ADC ASIC shall be 180 nm CMOS integrated circuit.	Defines the power consumption. 320,000 transistors in current design.
200.1	Power Consumption	< 8 mW per channel	The heat loss due to electronics in the LAr shall not dominate the total heat load on the cryogenic system	Current budget is maximum 8 mW per ADC channel.
200.2	Sampling rate	< 2 MHz	The charge pulse shall be recorded with sampling frequency that is higher than the frequency corresponding to the typical charge diffusion time for an instaneous deposit of charge in the LAr	The average electron longitudinal diffusion over a drift distance of 1.8m is 1.2 mm = 0.75 usec for drift electric field of 500 V/cm; the minimum sampling rate of the system shall be 2/(pulse width) = 2/2x0.75 = 4/3 MHz
200.3	Dynamic range	1-3836 count	The requirement to observe in the induction plane a MIP produced at the far end of the TPC determines the lower end of the dynamic. The need to collect charge from a highly ionizing stopping proton without suffering saturation effects sets the upper end.	~1% of 11.6k e- sets the lower limit of 116 e- per count. The upper limit is set by energy deposited in one voxel by 2 highly-ionizing protons = 445k e-.
200.4	Number of bits	12 bits	The ADC shall resolve the full dynamic range, including noise requirements.	For induction wires: ENC < 700 e-, and 1% of 11.6k e- gives 116 e-/count, then we find ADC < Log2(700/116) < 2.6 counts used for noise. 12 bits = 4096 counts > 3836+3.

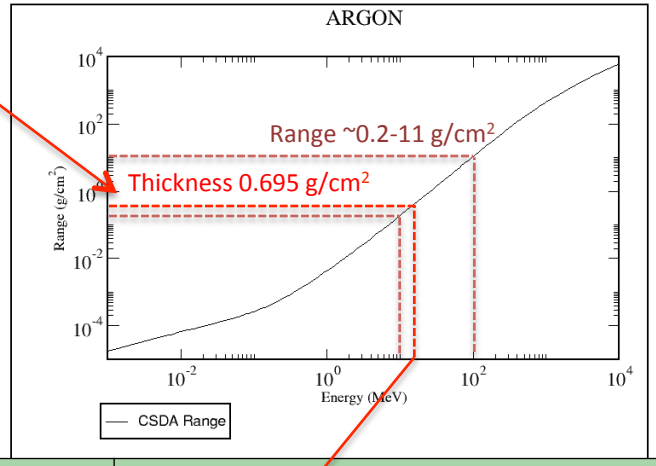
Dynamic Range

The requirement to measure a MIP-size charge from the cathode with a precision of 1% in the collection plane determines the lower end of the dynamic range. The need to collect charge deposited at the vertex of a neutrino event (mainly by protons) without suffering saturation sets the upper end.

- Lower end calculation
  - To obtain 1% charge resolution requires 1% of 11.6k e-: ~116 e- per ADC count
- Upper end calculation
  - Proton energy distribution is isotropic in the range 10-100 MeV
  - Worst case assumption: all energy deposited in one 0.5cm voxel!
  - Proton at wire plane: no drift losses, instantaneous deposition

$$\frac{E_{loss}\ (0.5\ cm)}{LAr\ E_{ee}} \times \frac{Recombination}{(500\ V/cm)} = \frac{21\ MeV}{23.6\ eV} \times 0.25 = 222.5k\ e^-$$

  - For CC ν_e–Ar interactions assume a mean of 2 protons/vertex
  - 445k e- maximum charge ÷ 116 e-/count = 3,836 counts
- Noise: ADC < Log2(650/116) < 2.5 counts



Dynamic range
ADC < 1-3836 + 3 counts

- 12 bits is sufficient

(required) Kinetic Energy (MeV)	Stopping Power (MeV cm²/g)			Range		
	Electronic	Nuclear	Total	CSDA (g/cm²)	Projected (g/cm²)	Detour Factor Projected / CSDA
2.00E+01	1.79E+01	7.60E-03	1.79E+01	6.34E-01	6.30E-01	0.9946
2.50E+01	1.51E+01	6.19E-03	1.51E+01	9.39E-01	9.34E-01	0.9949

CE Component Requirements

ID	Parameter	Value	Function	Rationale
301	Cold Cable Plant	20 per APA	The cold cable plant shall provide LV power, HV wire bias, control and output analog and digital signals from the LAr electronics to the cryostat signal feed-through without loss of CE performance.	Does not introduce noise from the cables or loss of data in transmission.
302	Cryostat Signal Feed Through	1 per APA	The cryostat signal feed-through shall allow connections from the cold cable plant to warm components of the TPC wire-related components housed in the Warm Electronics Crate.	Allow signal penetration while maintaining cryostat pressure and flow rate.
303	Warm Electronics Crate	1 oer APA	The Warm Electronics Crate shall contain the warm interface electronics which provide control, clock and data communcation between the LAr cold electronics and the timing and DAQ systems.	Does not introduce noise into the cryostat at the flange or loss of data in the warm electronics.
304	Warm Cable Plant	1 per APA	The warm cable plant shall provide HV wire bias, LV power, optical fiber to DAQ and slow control, ethernet local monitoring from the cryostat signal feed-through without loss of CE performance.	Does not introduce noise in the cable or loss of data in the fiber.
305	High Voltage Wire Bias (HVWB)	< 2000 V	The HV wire bias power supplies shall provide HV power to the APA.	Wire bias is required for the electron diverters and transparency of the wires to the drift electrons.
306	Low Voltage Power (LV)	12 V	The LV power supplies shall provide LV power to the warm and cold electronics units.	LV power is required by the warm interface electronics and cold front-end electronics.

Conclusions

- SBND and ProtoDUNE-SP are LArTPCs read out by the same cold electronics design
  - Cold FE and ADC ASICs are identical between detectors
  - Minor differences due to implementation
- DUNE and SBND have established a management and team to deliver cold electronics for both detectors
- The DUNE far detector requirements will allow DUNE to meet the global science objectives

> Are the requirements for the proposed ProtoDUNE-SP and SBND CE systems sufficiently complete and clear?

- The cold electronics system parameters (set by the DUNE far detector requirements) are sufficient to design the cold electronics system
  - Sufficient for SBND physics and ProtoDUNE-SP goals

Review Organization

- Day 1
  - Plenary talks in the Instrumentation Large Conference Room (here)
- Day 2
  - Morning: parallel sessions for System Design (Large Conference Room) and ASICs (OASIS Room – down the hall)
  - Afternoon: plenary talks in the Large Conference Room
- Day 3
  - Committee writing and close-out in the Large Conference Room
  - Working lunch for the committee will be provided
- Review documentation

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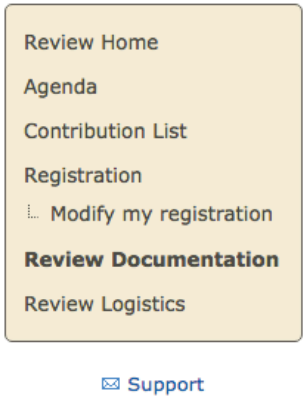


Electronics Review documentation

Primary Documentation

ProtoDUNE-SP Cold Electronics Design
ProtoDUNE Technical Design Report
Joint SBN Program Proposal

Cold Electronics Requirements
Cold Electronics QA/QC Plan

Supporting Documentation

DUNE/LBNF CDR Vol. 2: The Physics Program for DUNE at LBNF
DUNE/LBNF CDR Vol. 4: The DUNE Detectors at LBNF

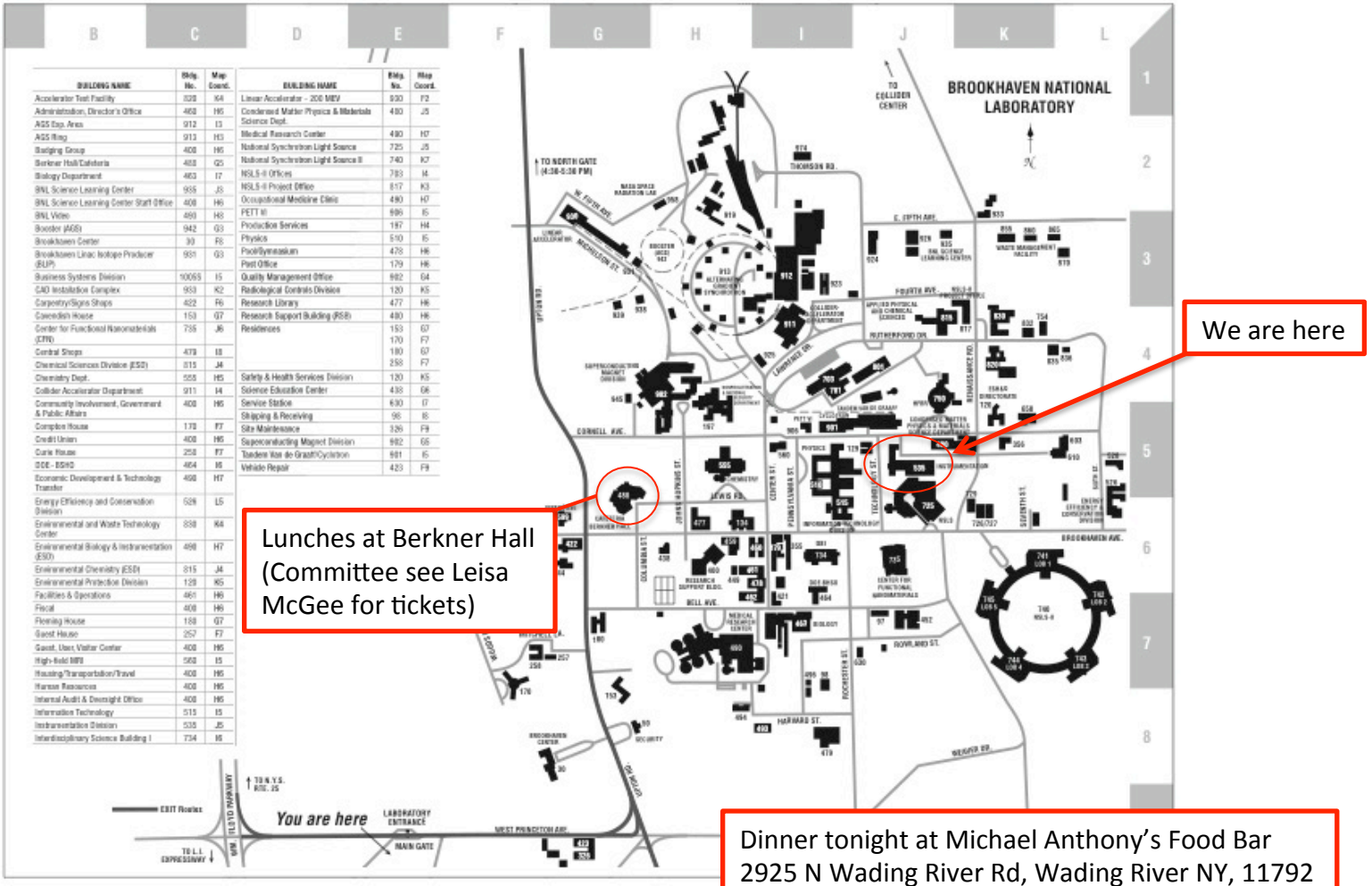
FE ASIC Design and Digitization
FE ASIC Datasheet
ADC Design/Performance Study
ADC ASIC Datasheet

DUNE Prototype Front End Mother Board Design
SBND Prototype Warm Interface Electronics Design

CE to DAQ Proposed Protocols
DUNE Grounding and Shielding
SBND Grounding and Shielding
Lessons Learned: Experience from MicroBooNE and 35ton

SBN: reviewer
Review-sbn
DUNE: review
nurev2pass

BNL Campus


BROOKHAVEN NATIONAL LABORATORY
We are here
Lunches at Berkner Hall (Committee see Leisa McGee for tickets)
Dinner tonight at Michael Anthony's Food Bar
2925 N Wading River Rd, Wading River NY, 11792
You are here
LABORATORY ENTRANCE
MAIN GATE

Charge Matrix Plenary I

	Charge Question	Matt (I)	Yu	Chen	Bagby	Li	Gao	Radeka (I)	Matt Shaw	Matt (II)	Radeka (II)	Dean	Matt (III)
1	Are the requirements for the proposed ProtoDUNE-SP and SBND CE systems sufficiently complete and clear?	✓											
2	Does the conceptual design for the CE systems meet the requirements?			✓									
3	Are justifications for each of the specific technical design choices sufficiently documented?			✓		✓							
4	Does the design as presented represent a good development path toward DUNE and are there opportunities for incorporating potential advances in the CMOS technology over the DUNE time scale?			✓		✓							
5	Are the CE interfaces to other detector subsystems including TPC, DAQ, and cryostat well-defined and documented?												
6	Is the grounding and shielding plan for the detectors and its impact on the CE systems understood and adequate?				✓			✓					
7	Does the proposed CE design adequately address potential catastrophic failure modes, such as large HV discharges?										✓		

Charge Matrix Plenary II

	Charge Question	Matt (I)	Yu	Chen	Bagby	Li	Gao	Radeka (I)	Matt Shaw	Matt (II)	Radeka (II)	Dean	Matt (III)
8	Are the proposed integrated system tests sufficient to assure that the systems will meet the performance requirements for ProtoDUNE-SP and SBND? Have applicable lessons-learned from previous LArTPC detectors been documented and implemented into the QA plan?							✓	✓			✓	
9	Is the CE design robust enough and the quality control plan and testing program sufficiently comprehensive to assure the dead/bad channel requirements for ProtoDUNE-SP and SBND are achieved?			✓								✓	
10	Is the proposed joint ProtoDUNE-SP/SBND production, installation, and commissioning plan reasonable?												✓
11	Are sufficient technical resources assigned to complete the design and production of the CE systems for ProtoDUNE-SP and SBND?	✓		✓									
12	Are the technical risks associated with the development and implementation of the CE systems recognized and understood and is there a plan for managing and mitigating these risks?									✓			

Charge Matrix Parallel Sessions

	Charge Question	Yu	Fried	Hazen	Bagby Shaw	Matt	Elizabeth	ASICs
2	Does the conceptual design for the CE systems meet the requirements?	✓	✓	✓				✓
3	Are justifications for each of the specific technical design choices sufficiently documented?	✓	✓	✓				✓
4	Does the design as presented represent a good development path toward DUNE and are there opportunities for incorporating potential advances in the CMOS technology over the DUNE time scale?							✓
5	Are the CE interfaces to other detector subsystems including TPC, DAQ, and cryostat well-defined and documented?				✓			
10	Is the proposed joint ProtoDUNE-SP/SBND production, installation, and commissioning plan reasonable?					✓	✓	