

Noise “Phenomena” in MicroBooNE

- Relevance to test stands and other TPCs

V. Radeka

March 2: reduced and updated June 27, 2016

1. “noisy wires after applying the wire bias” - wires in contact
2. “chirping noise” - FE ASIC saturation due to wire motion
3. “zig-zag noise” - “pickup” burst noise
4. “10-30 kHz noise” - low voltage regulator noise
5. “drift HV noise” - cathode→anode HV supply ripple

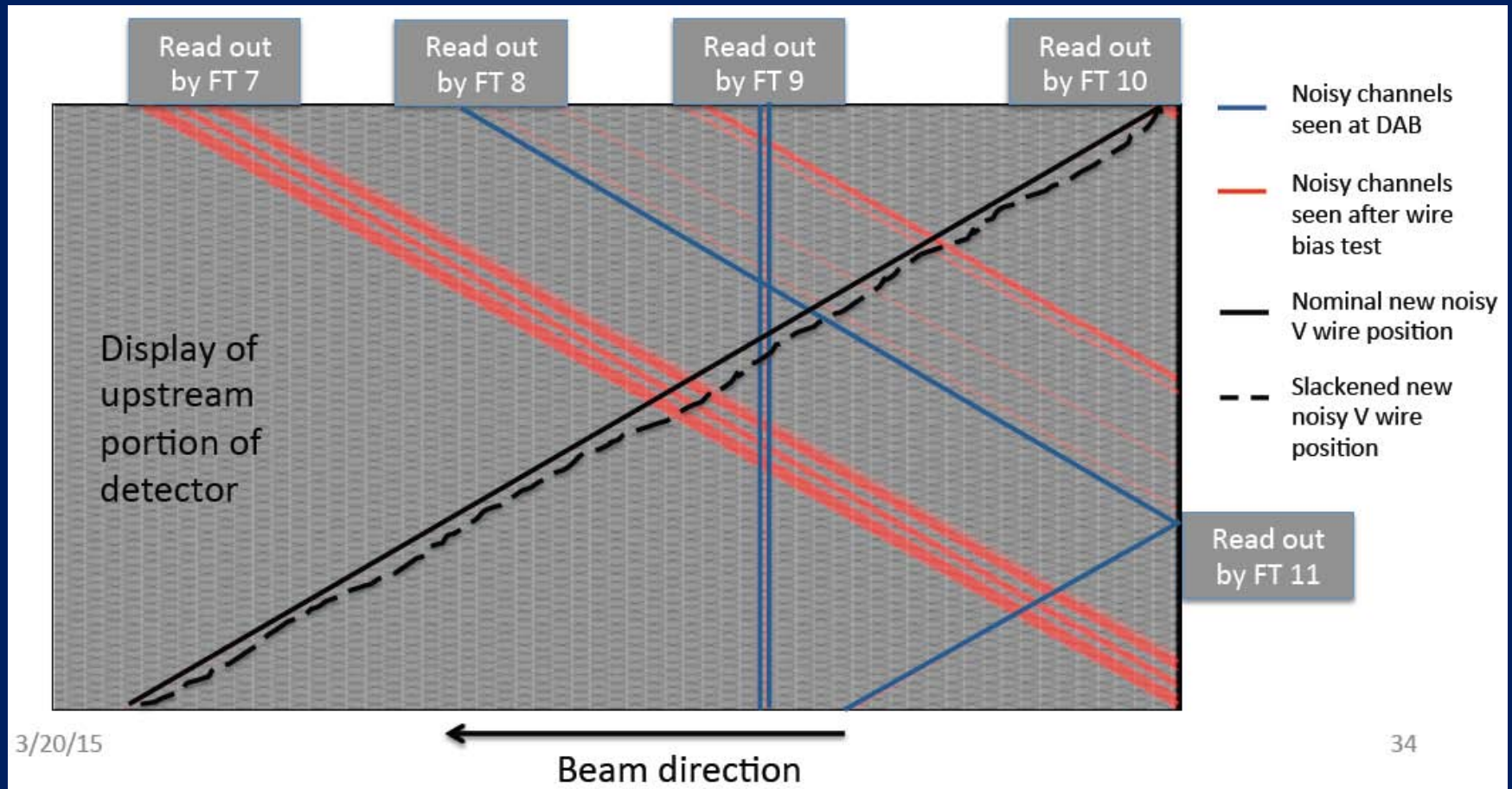
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Based on numerous measurements and observations during commissioning and operation March 2015 by collaborators and contributors: J. Asaadi, L. Bagby, D. Caratelli, h. Chen, G. De Geronimo, M. Johnson, J. Joshi, D. Kaleko, W. Ketchum, B. Kirby, M. Mooney, S. Rescia, K. Terao, M. Toups, Y.-T. Tsai, B. Yu

1. “noisy wires after first application of wire bias”

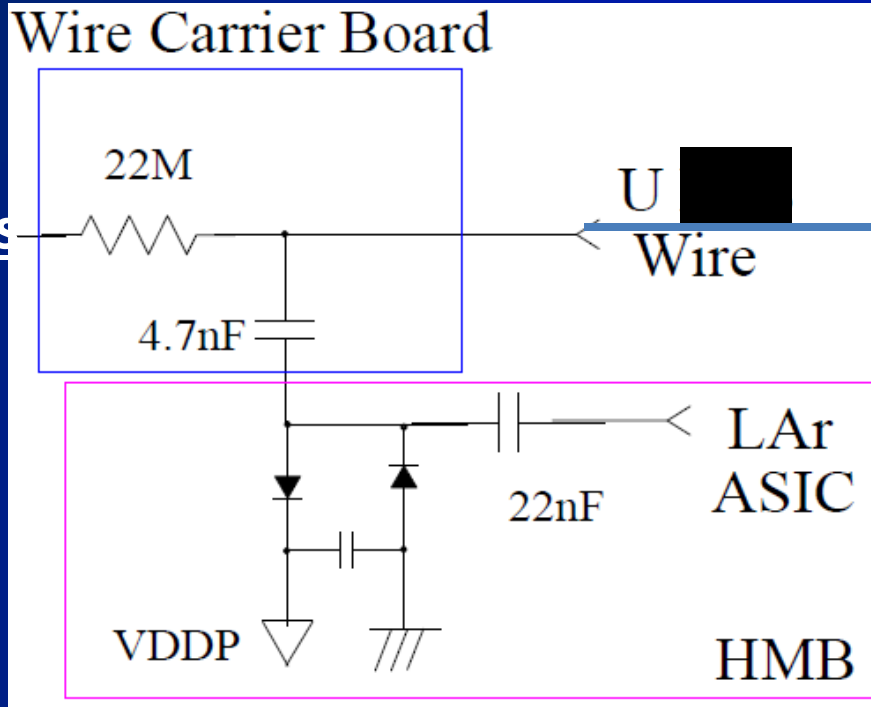
dc bias current on FT 7,8,9; dc current between them - none should exist!

A loose **v-wire** fits best very detailed analysis of all symptoms
(described in: MB docdb 4209-2 and 4212-v5)

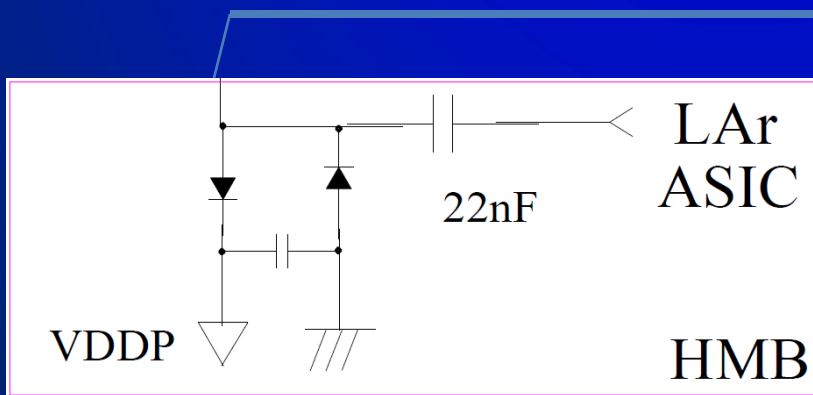
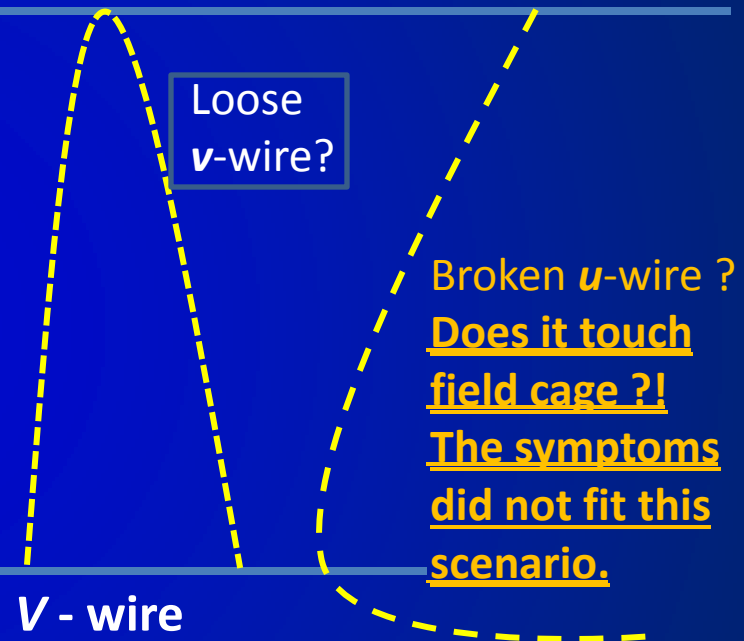


Wires in contact changing in time; after filling with Lar; ~ 50 wires in contact .

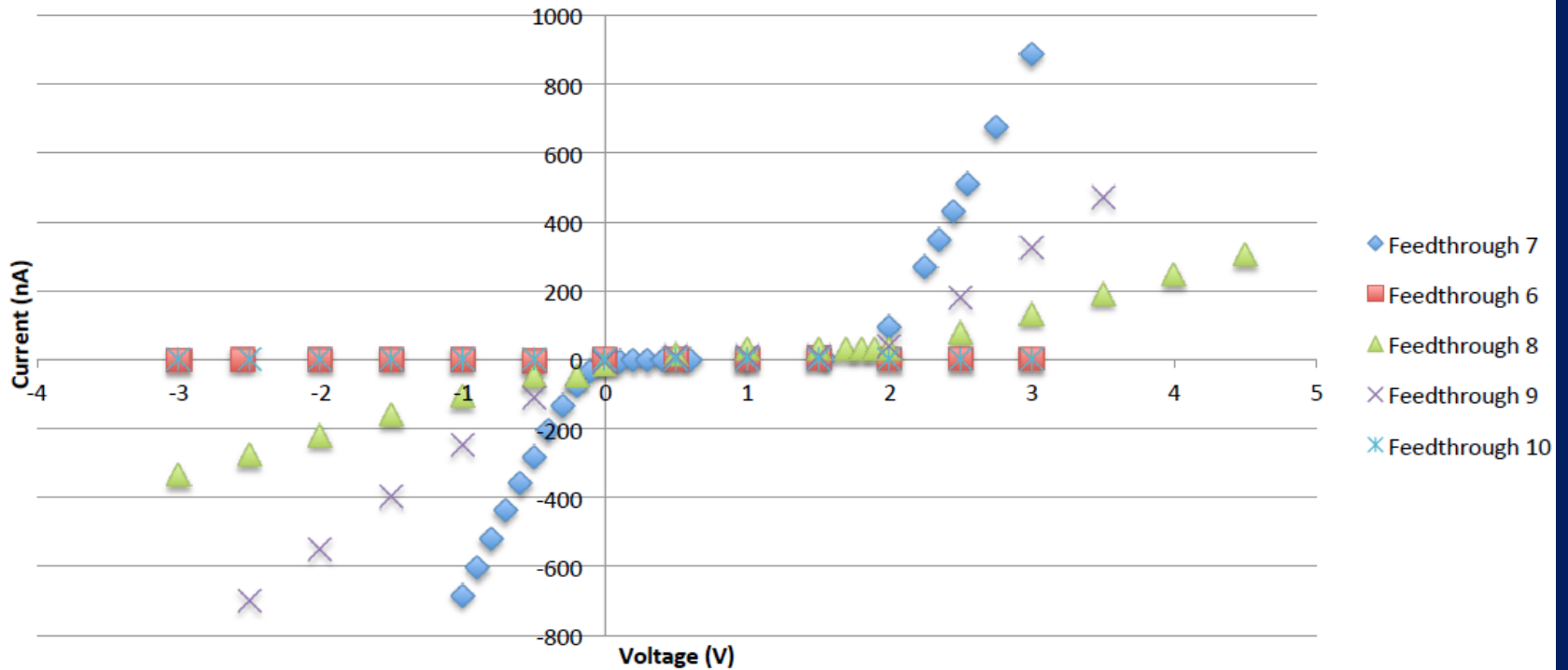
Sense wire bias circuits



U-bias



Current Vs. Voltage For Negative Wire Bias Input Lines



3/20/15

Resistance [Mohm]	Bias Voltage Test - 2015/03/10	SMU Test - 2015/03/16	U/V Short Hypo - 2015/03/18
FT7	1.13	1.22	1.13
FT8	8.36	8.76	8.45
FT9	3.36	3.40	3.25

wires in contact with v-wire:

21.
3
7

Signal and noise on “good” and “noisy” wires (at 300K)

Noise Signal

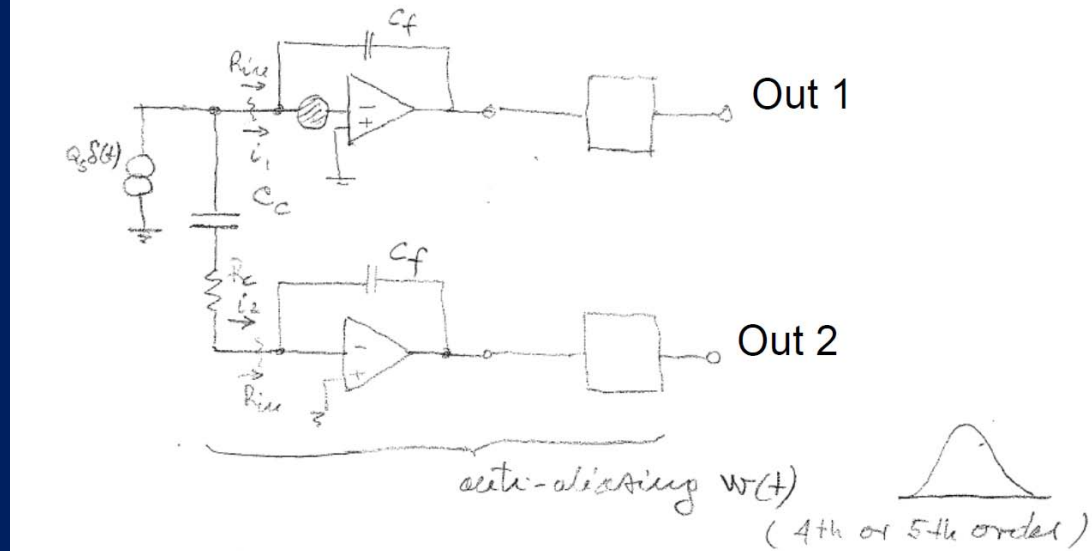
4.26 amplitude	1126.59,
3.94 amplitude	1126.30,
4.39	
amplitude	1116.48,
3.47 amplitude	1146.68,
3.50	
amplitude	1119.26,
4.03 amplitude	1122.80,
3.38	
amplitude	1141.81,
4.23	

1 ADC count
=200 e

amplitude	877.15
81.98	
amplitude	901.69
83.21	
amplitude	910.59
85.17	
amplitude	909.57
83.58	
amplitude	932.52
84.51	
amplitude	919.72
83.57	
amplitude	882.80
81.68	
amplitude	860.61
81.98	
amplitude	856.98
83.45	

Noise increase ~ **x21**
Signal decrease ~ **x0.7**
Remarkably uniform

Microboone Broken Wire Model

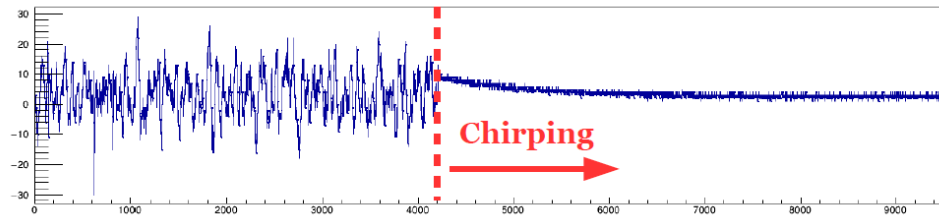


Simulations confirm the observations:
Input transistor noise greatly magnified when connected to another low impedance input, instead of just to wire capacitance.

2. “chirping”: What is it and how it got resolved? (from MB docdb 5117)

MicroBooNE has long had an issue with channels “chirping”

- Intermittent dead regions on waveform (10-15% of channels/event)
- Happens only with wire bias HV on, changes event to event



Numerous observations, analysis and studies of the incidence and properties of “chirping” have been done starting in March-April in air, gaseous argon and since July in Lar, and it took until October to resolve it. This work has been reported through MB means of internal communication as it was performed.

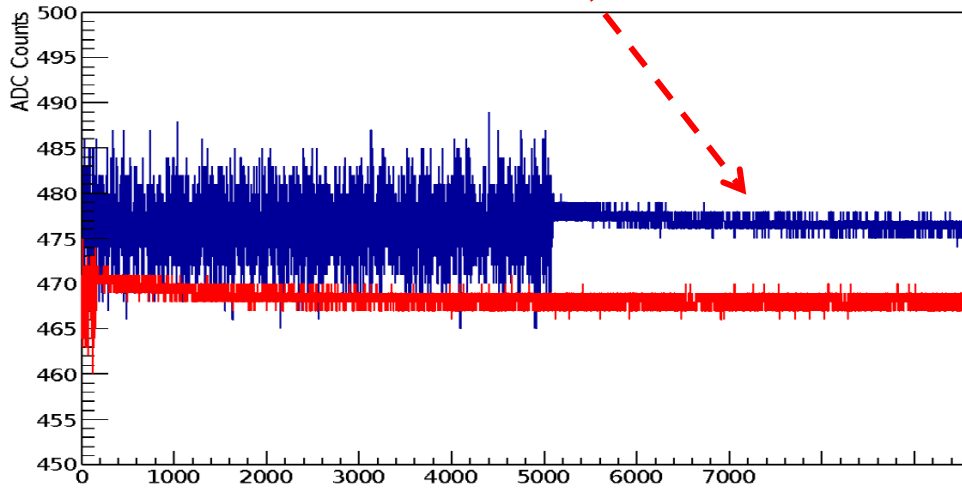
Information has been collected by:

J. Asaadi, L. Bagby, D. Caratelli, J. Joshi, D. Kaleko, W. Ketchum, B. Kirby, M. Mooney, K. Terao, M. Touns, Y.-T. Tsai, with participation by others.

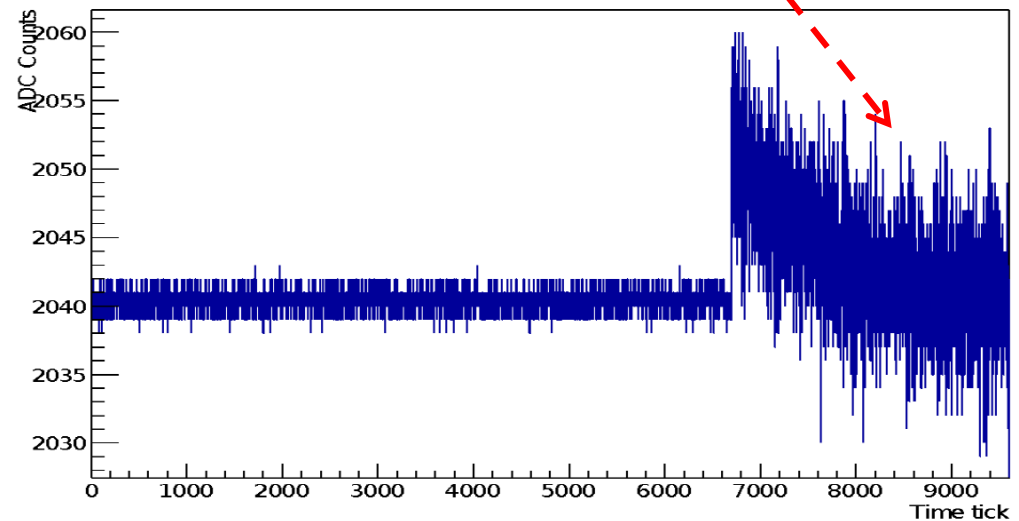
Slides in this section have been adapted from their reports.

Noise waveforms indicating onset of ASIC saturation and of normal state

Pulses Run 150, Subrun 2, Event 1: Example FT 10 Y channels



Pulses Run 150, Subrun 2, Event 1: Example FT 11 V channel

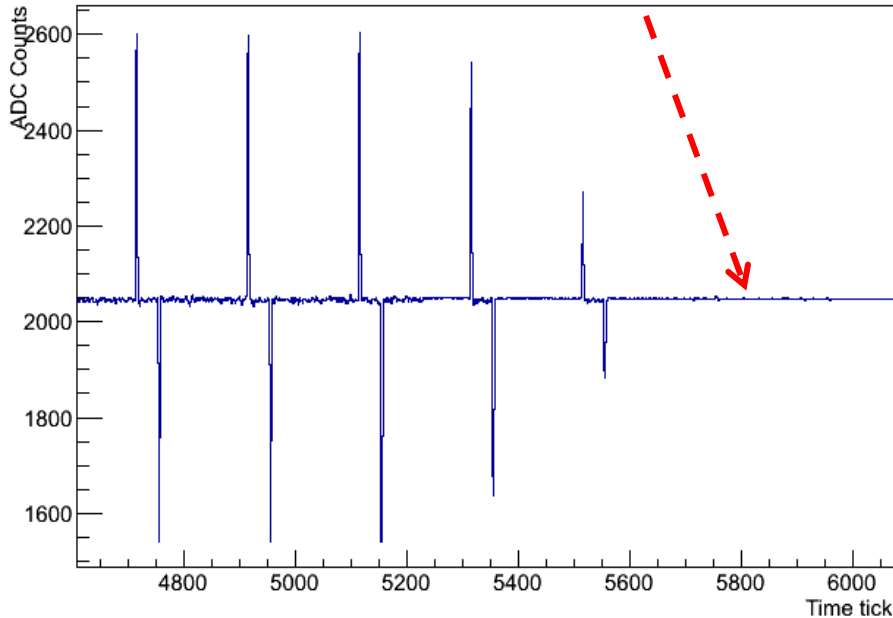


Time tick=0.5 μ s

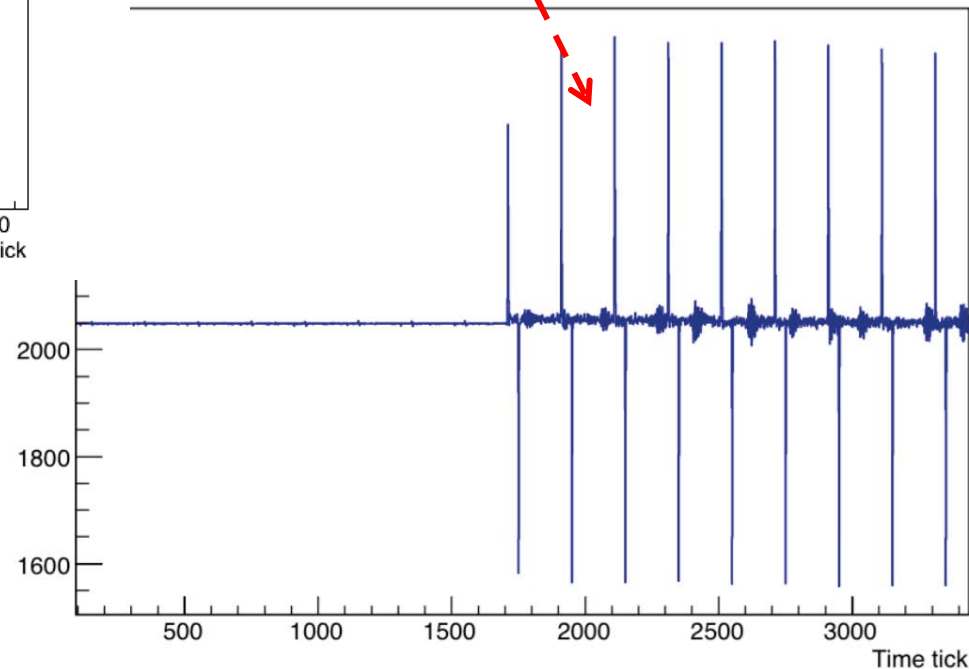
The recordings, as limited by DAQ, were too short (~4.5ms) to determine the period (frequency) of saturation intervals, which was clearly much lower than $1/(4.5 \text{ ms})$

Pulsar response waveforms indicating onset of ASIC saturation and of normal state

(Crate,Slot,Ch)=(7,10,6), Zoom on quiet region



Pulse from Crate 4, Card 2, Channel Number 19



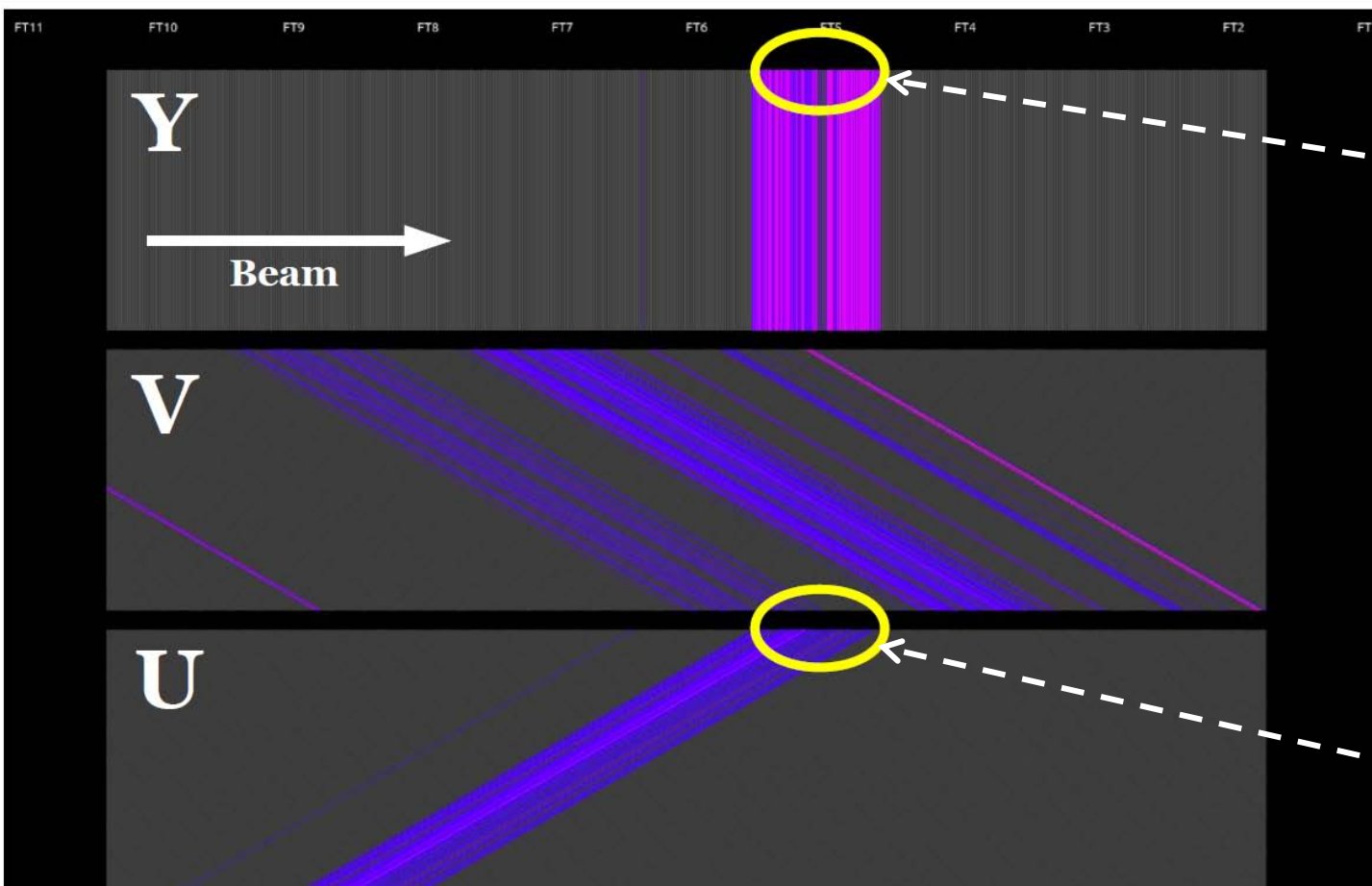
Pulsar response and noise rms in normal state were as expected: “chirping” did not mean increased noise, but it did cause disruption of data.

Time tick=0.5 μ s

v- sense wires at zero potential show incidence of saturation with bias on u- and y-wires



Chirpiness for Run 161+162



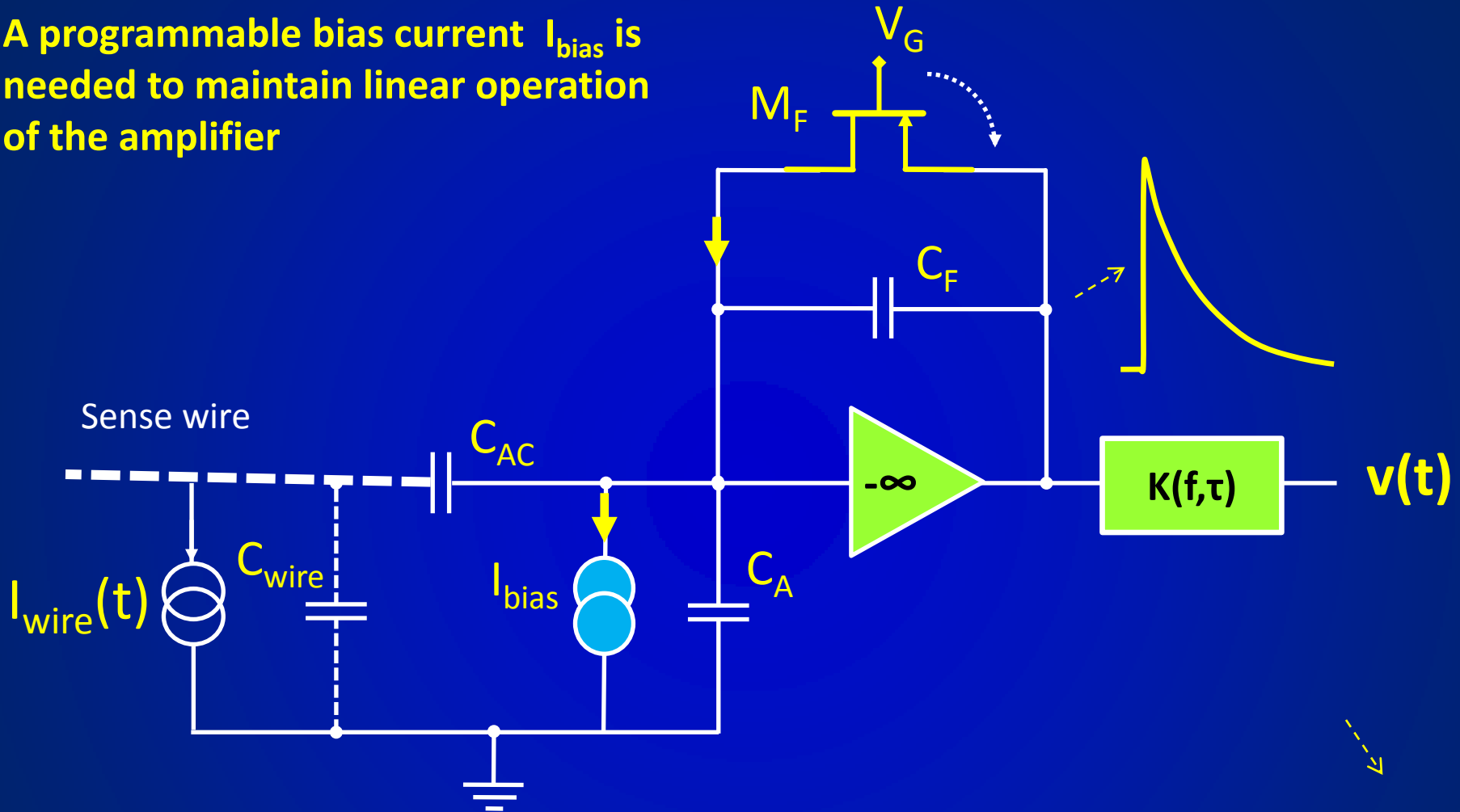
Biased
y-wires

v-wires
saturation
(zero bias!)

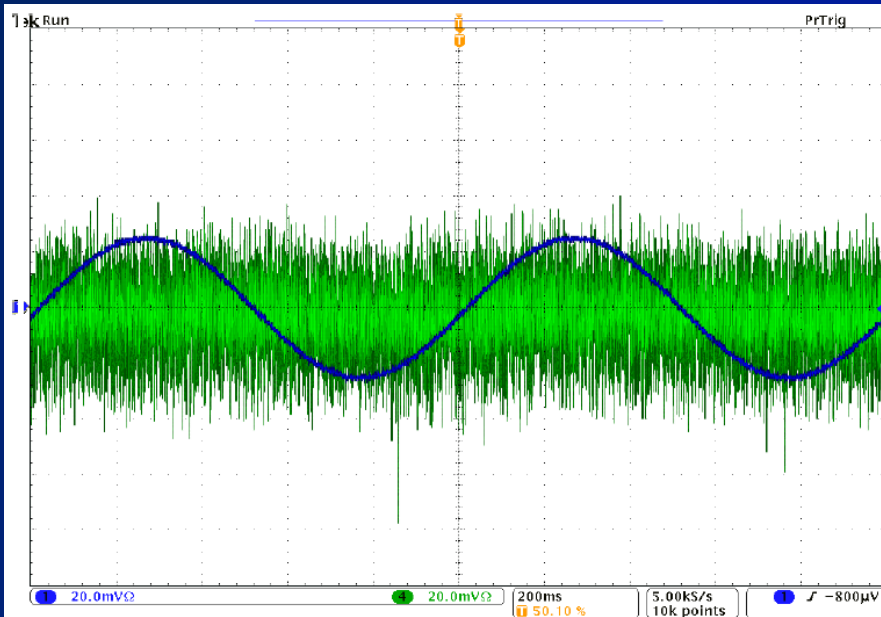
Biased
u-wires

Reset in AC-coupled front-end ASICs

A programmable bias current I_{bias} is needed to maintain linear operation of the amplifier



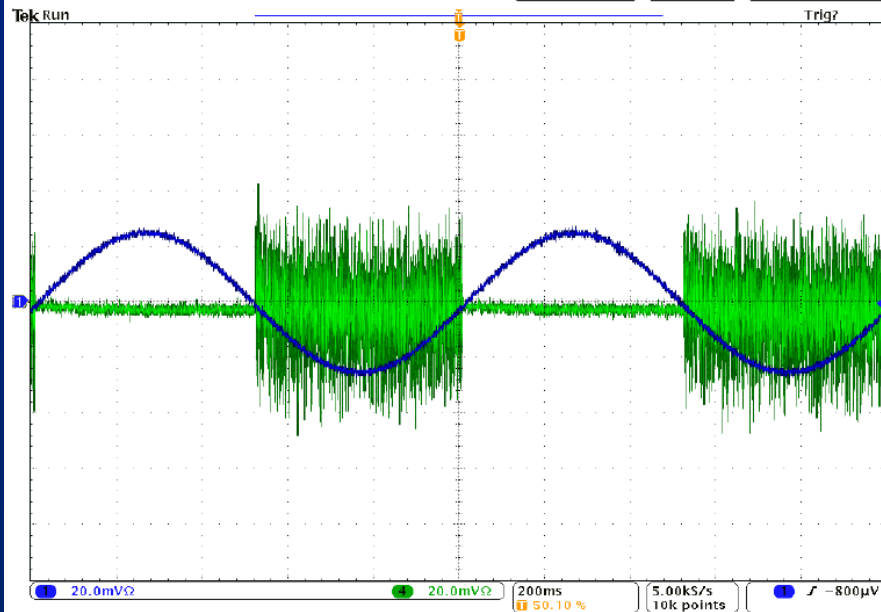
In LAr FE ASIC I_{bias} is programmable as 100pA or 500pA (default 500pA gives $\sim 60e$ -noise). In the new version 1nA and 5nA will also be available.



Bias
Current
Setting:
500 pA

Current sine wave at 1Hz
and peak amplitude **225pA**
injected into the ASIC input

No saturation at
bias current of
500pA



Bias
Current
Setting:
100 pA

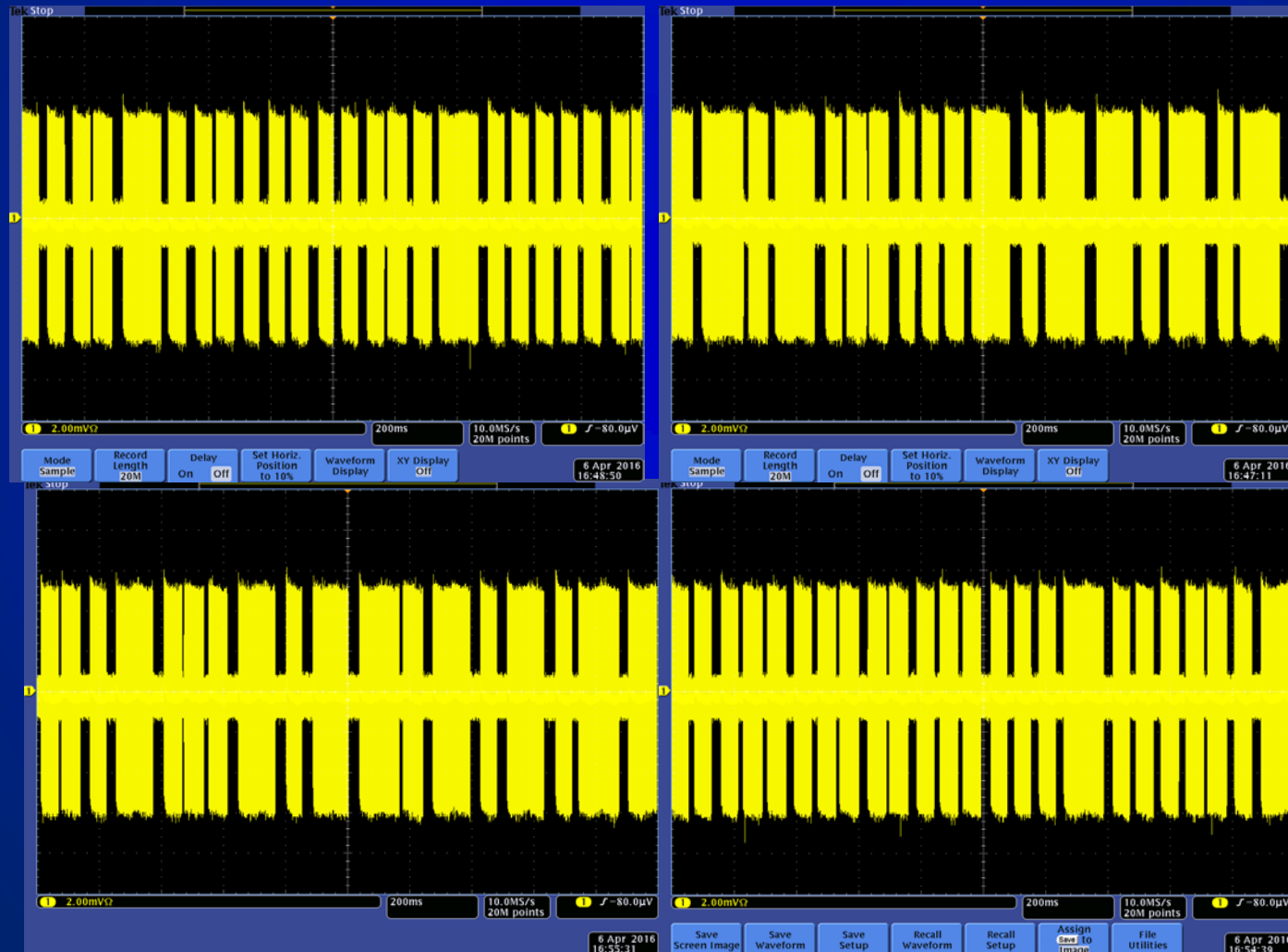
Saturation for half
a period at bias
current of **100pA**

Frequency: 1 Hz Gain: 14 mV/fC Peaking Time: 3 μ s
Input Current: 225 pA Zero to Peak

Measurement of Saturation by Oscilloscope

- FT5.B-6: C.4.S15.P1 on 04/06/2016

Very low frequency, varying from wire to wire between ~ 0.5 and ~ 10 Hz



Saturation (“chirping”) incidence vs wire bias at 100pA ASIC current bias

Wire plane	Bias #3423 [V]	Number of chirping wires per event	Bias #3428 [V]	Number of chirping wires per event	Bias #3445 [V]	Number of chirping wires per event
u	-158	~ 209	-110	~ 141	-110	~ 118
v	0	~ 566	0	~ 429	0	~ 220
y	237	~ 65	230	~ 57	110	~ 8
Total (abs.)	395V	~ 840	340V	~ 627	220V	~ 346

- zero bias on *u*- and *y*-wires: no saturation!
- saturation incidence increases with total (abs.) wire bias (the effect on v-wires of biases of opposite polarity on *u*- and *y*-wires adds up – while *v*-wire bias is zero).

Elimination of saturation by proper current bias setting in the ASIC (*Chen!*)

Saturation (“chirping”) incidence at operating wire bias and 500pA ASIC current bias:

U:	~4/event
V:	~14/event
Y:	~0/event
Total:	~18/event

ASIC saturation is essentially eliminated with correct current bias (run #3438).

Charge on Wires vs Wire Displacement

$E_{\text{drift}}=250\text{V/cm}$
 Wires: 0.15mm
 @ 3mm
 Wires in vacuum

dQ/dx

	u (-100V)	v (0V)	y (220V)
dQ/du	4.1E-10	-8.2E-11	-1.1E-11
dQ/dv	-5.1E-11	6.2E-10	-1.3E-10
dQ/dy	-1.8E-11	-1.2E-10	3.6E-10

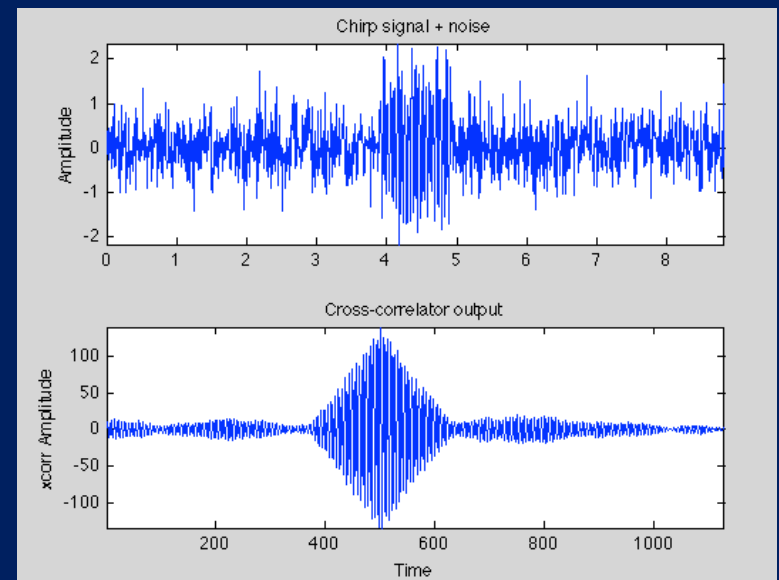
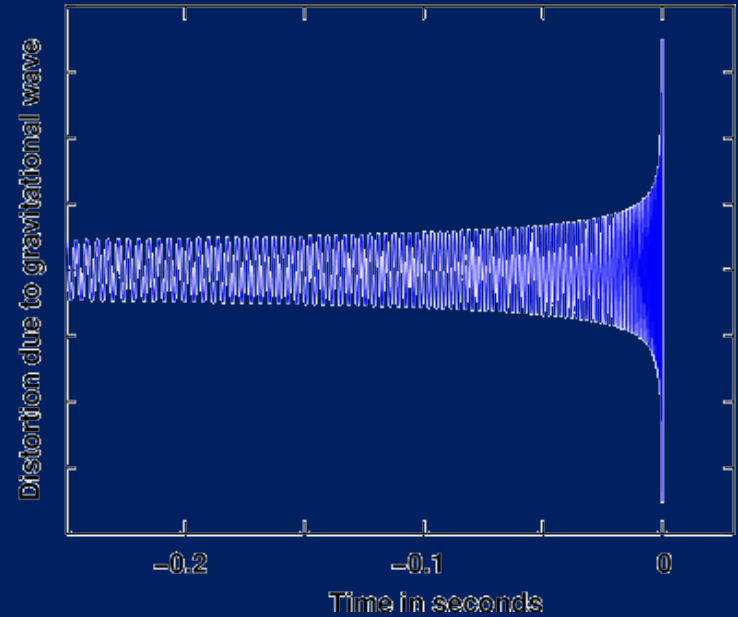
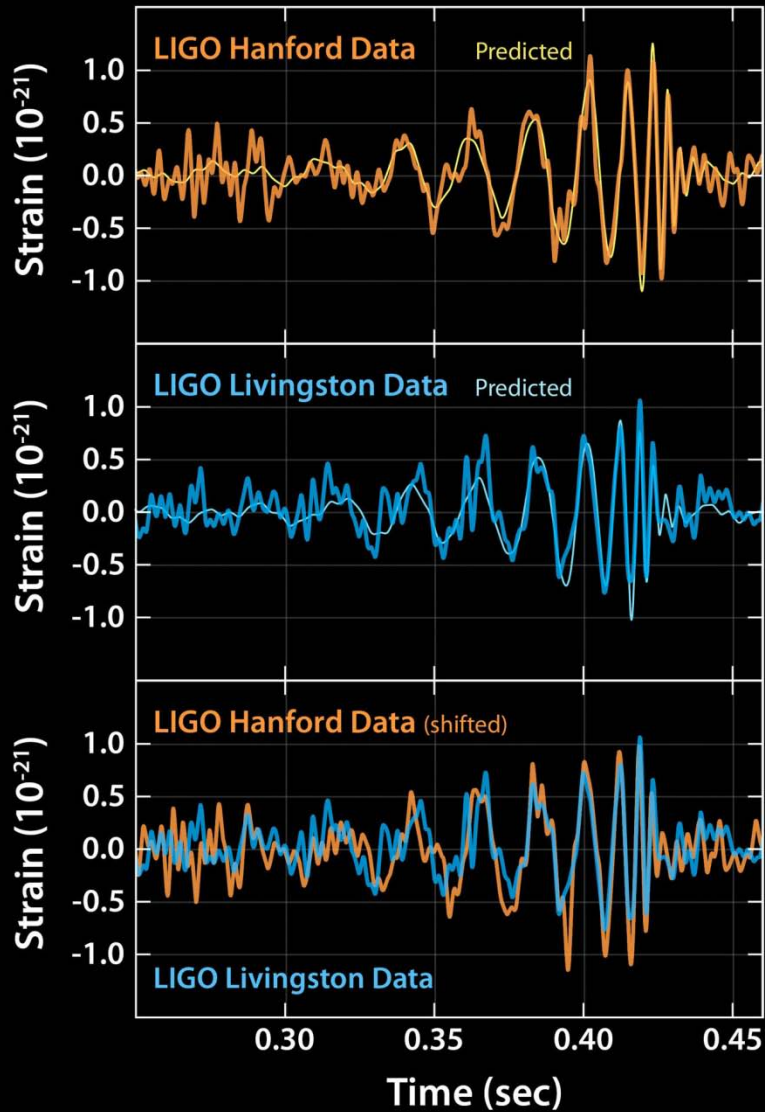
Unit: **Coulomb/m per mm** wire displacement

- We need to multiply the charge per unit length by the displaced (effective) wire length ℓ , and by 1.5 (LAr), to get the charge on each wire. Charge is proportional to the voltages/fields scaled by the same factor from the values in the table.
- **To induce a charge of >50pC to saturate the ASIC biased at 100pA at frequencies in the range $1\text{Hz} < f < 20\text{Hz}$, a v-wire displacement well below $100\mu\text{m}$ (less than the wire diameter) is sufficient.**
- Wire displacement is proportional to ℓ^n , where $n=2-3$ depending on the displacement force distribution.
- v -wires are most prone to cause ASIC saturation, with u -wires less so, and the shorter y -wires the least, in general agreement with the trend in slide 13.

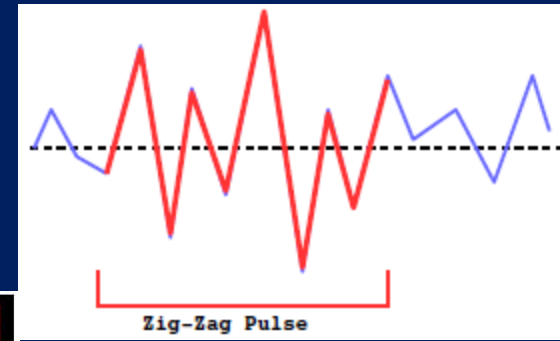
Summary on saturation

- Front end ASIC saturation was observed in MicroBooNE, both in air and in LAr, at incorrect ASIC bias current setting of 100pA. At the setting of 500pA, planned for the experiment, the saturation incidence is reduced to negligible level. A most likely cause is minute wire motion (see slide 15). There is no evidence that saturation is related to any other excess noise.
- No saturation (“chirping”) has been observed in 35ton prototype. Note: 35 ton has shorter sense wires than MB.
- Tentative conclusions for future LAr TPC projects:
 1. Higher programmable values of ASIC bias current (1 and 5 nA being implemented). Note: at $\geq 1\text{nA}$ the noise contribution becomes significant. 500 pA should be sufficient, in view of 2.
 2. Unsupported wire length should be limited to minimize wire displacement, and more importantly, to prevent contact of any broken wire with the field cage.
 3. For diagnostic purposes waveforms on individual wires should be observable on much longer time scale (seconds) than the electron drift time (need “oscilloscope trace”). This is being implemented in SBND project.

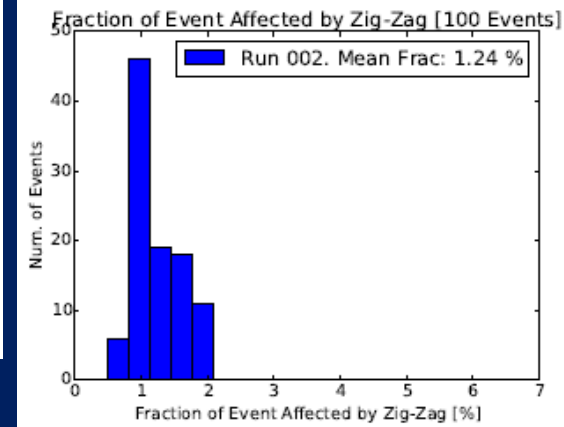
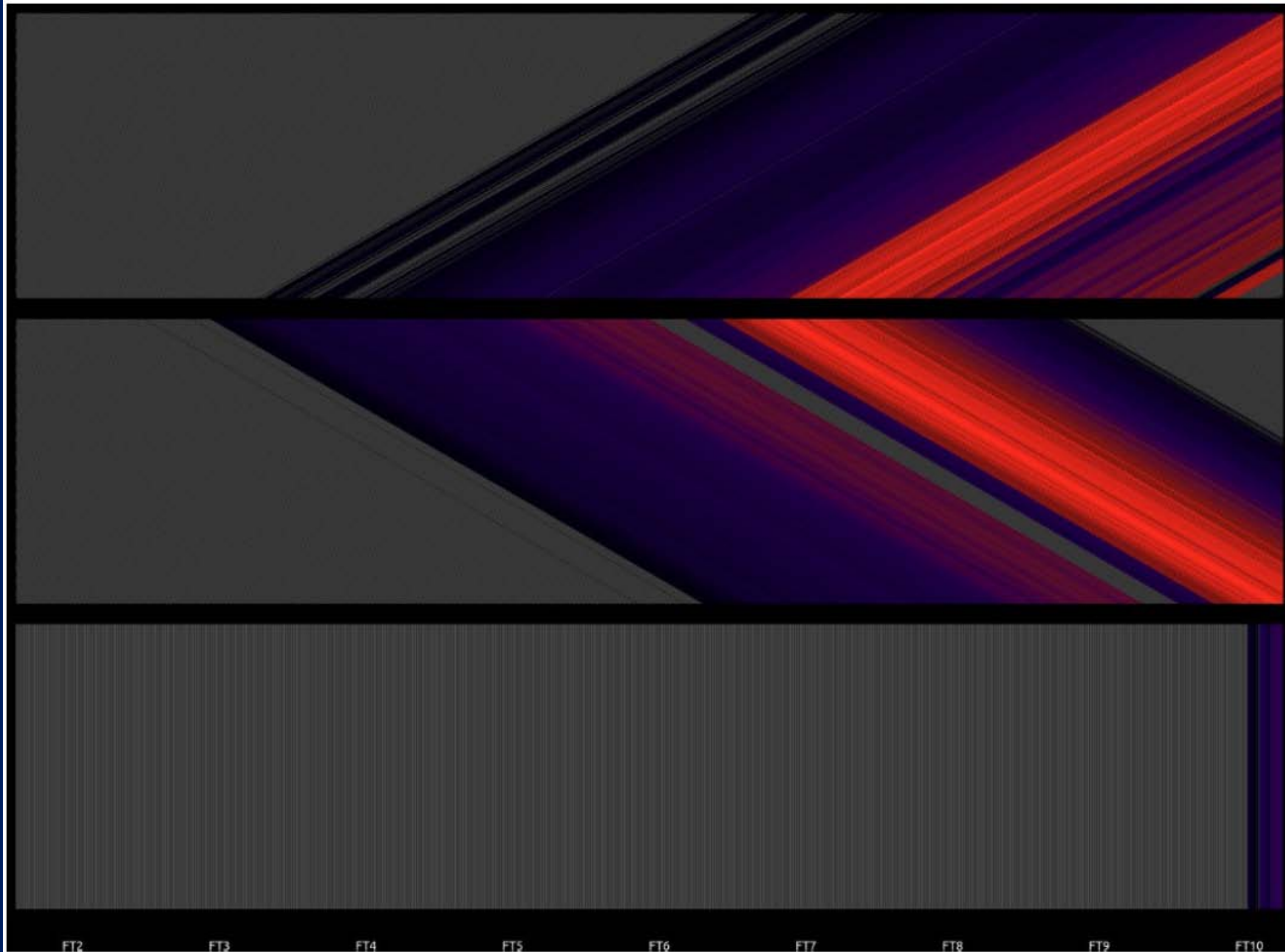
What is a Chirp?



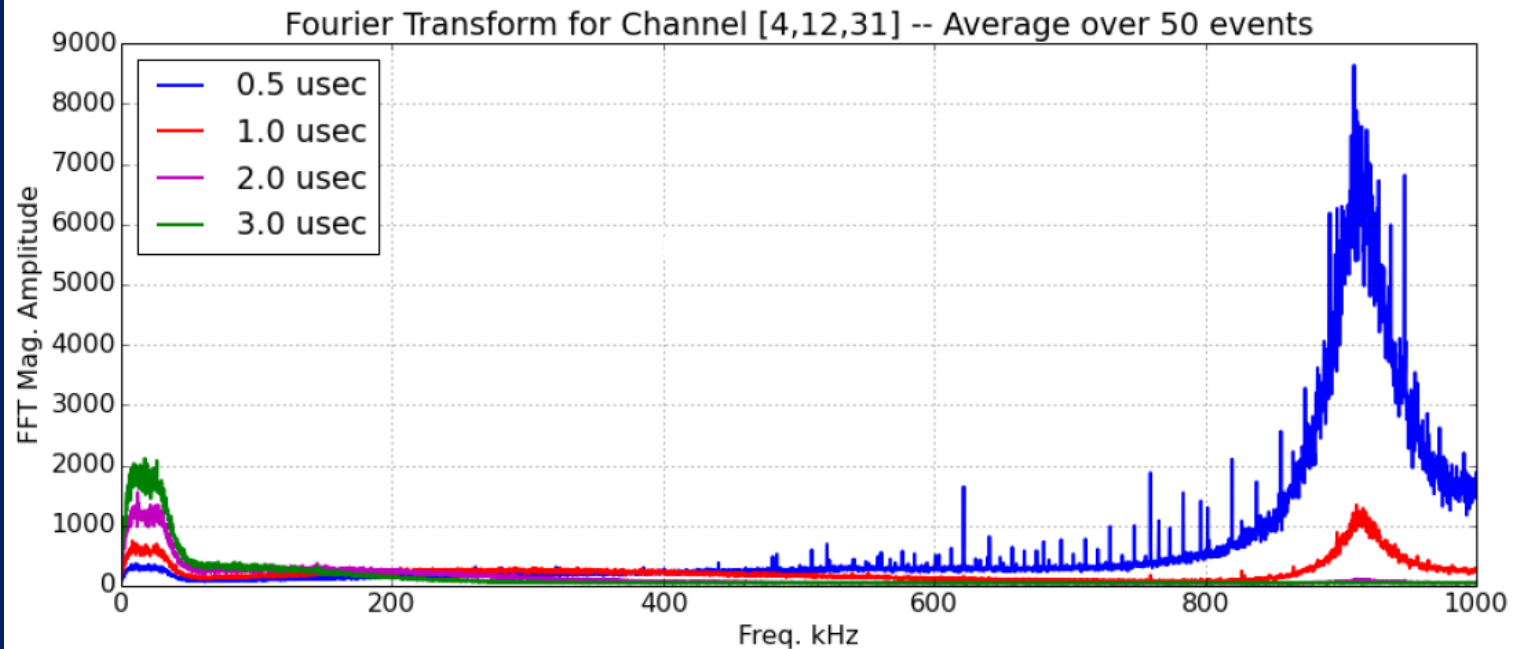
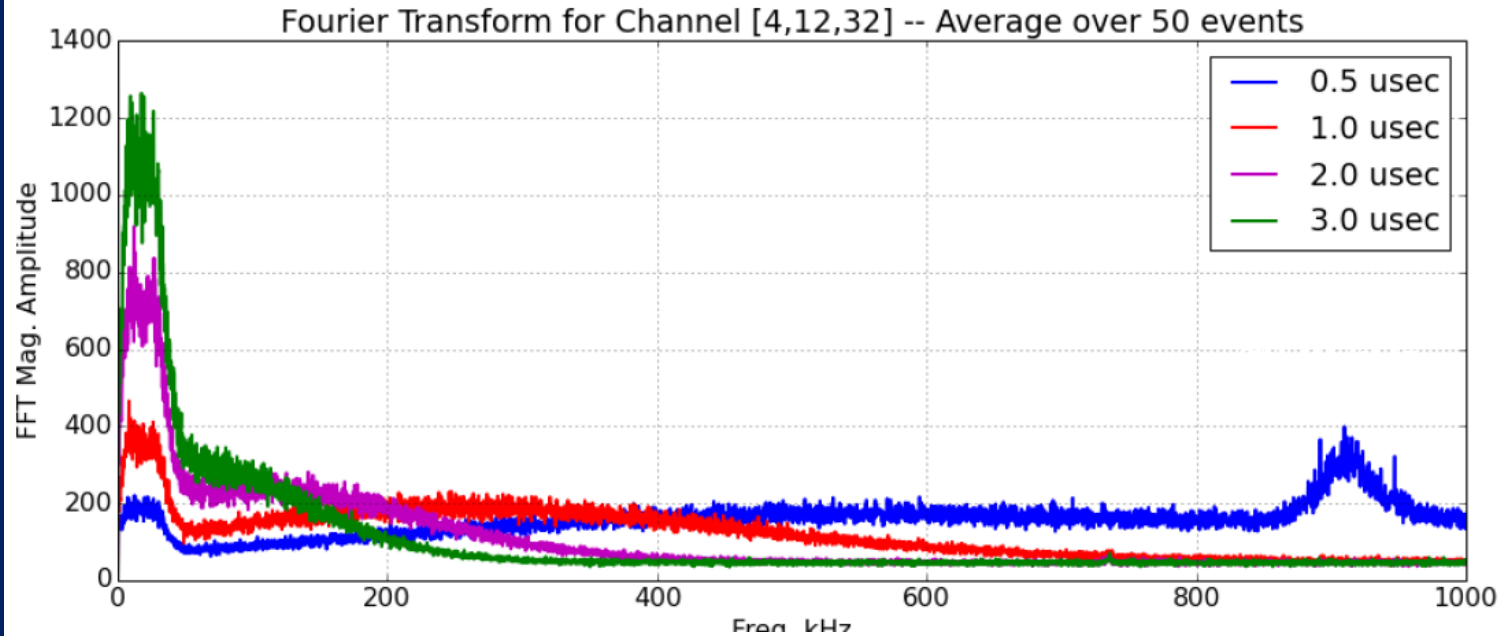
3. “zig-zag noise” (ref.: MB docdb 4293)



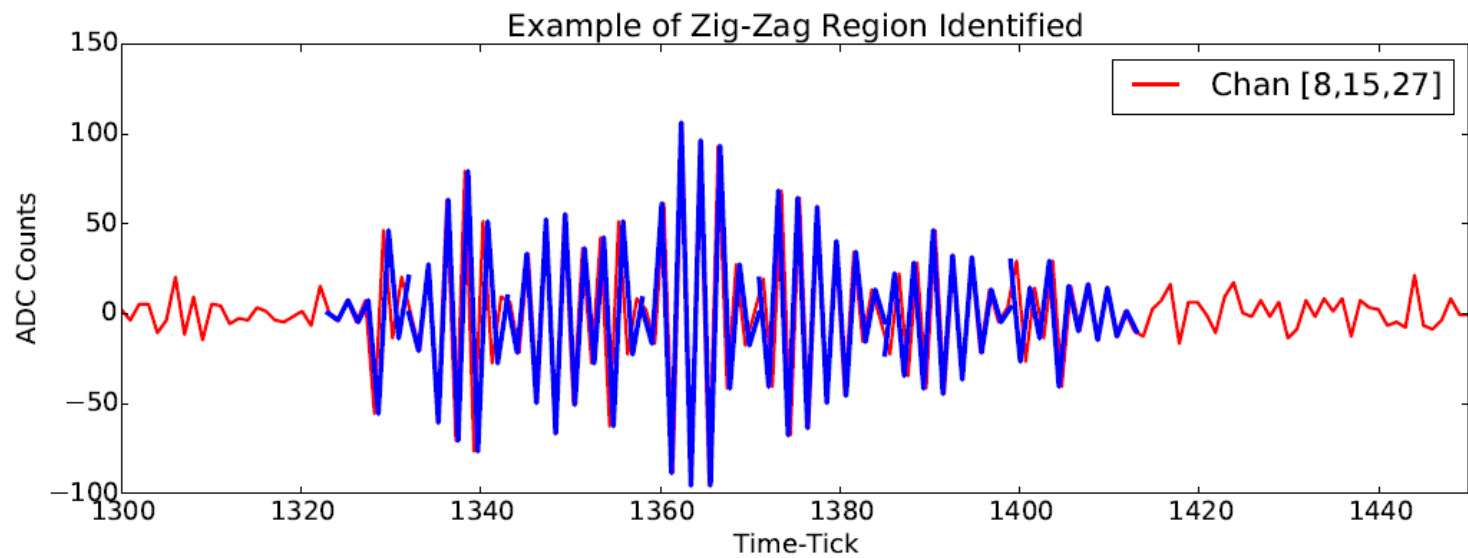
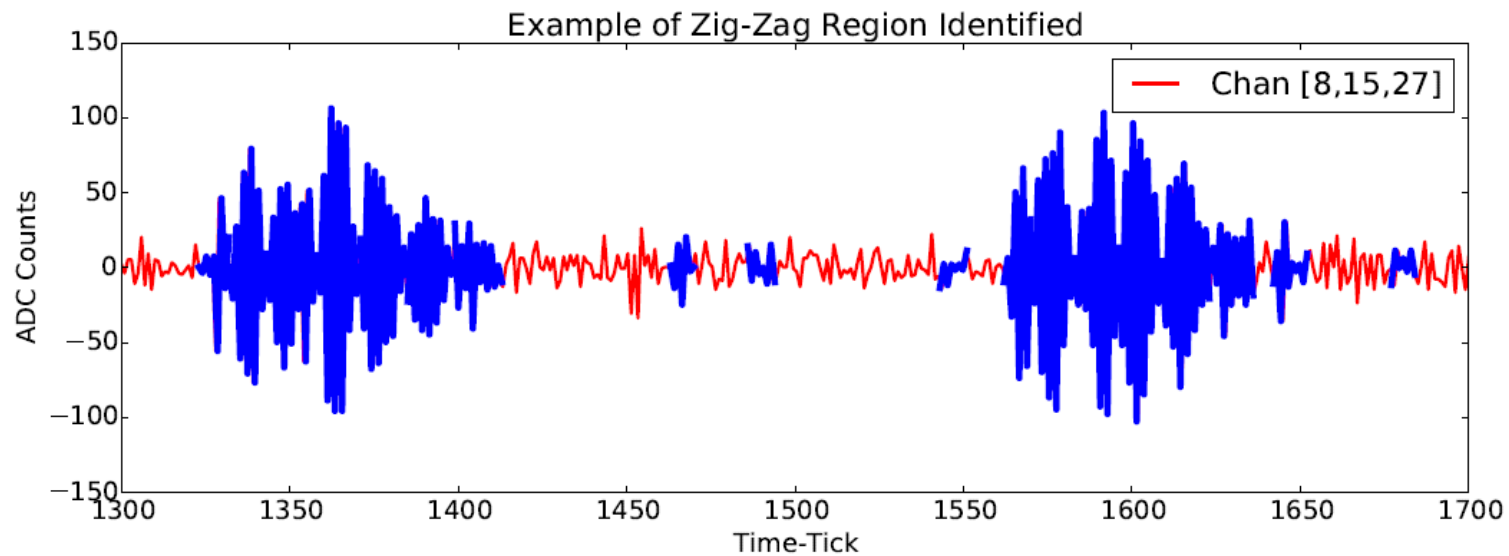
Each wire is colored based on the relative amount of zig-zag pulses seen



Zig-zag noise in frequency domain (FFT)



Zig-zag waveforms



Correlation

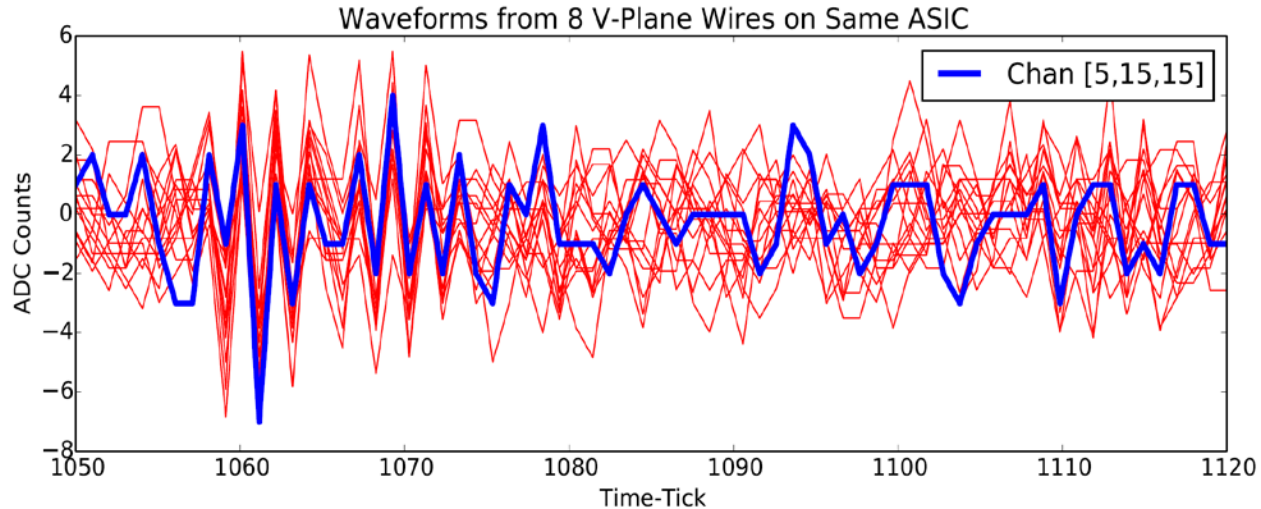
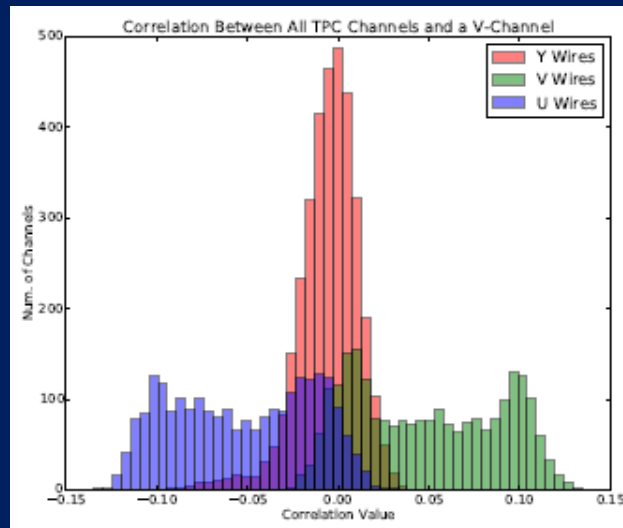
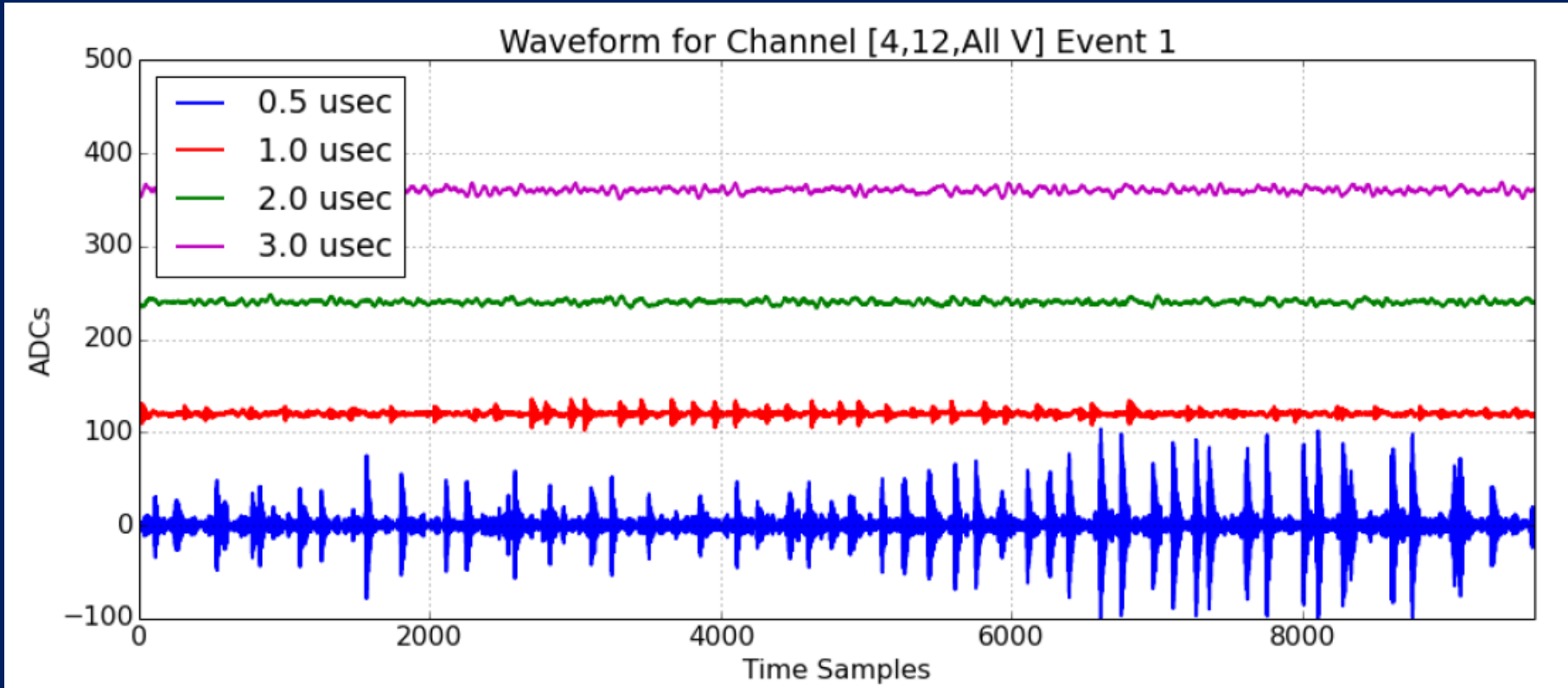


Figure 20: Noise pattern on 8 V-Plane channels on the same ASIC. In the zig-zag region the noise is strongly correlated across all 8 channels. Outside of the noise region there is no noticeable noise correlation



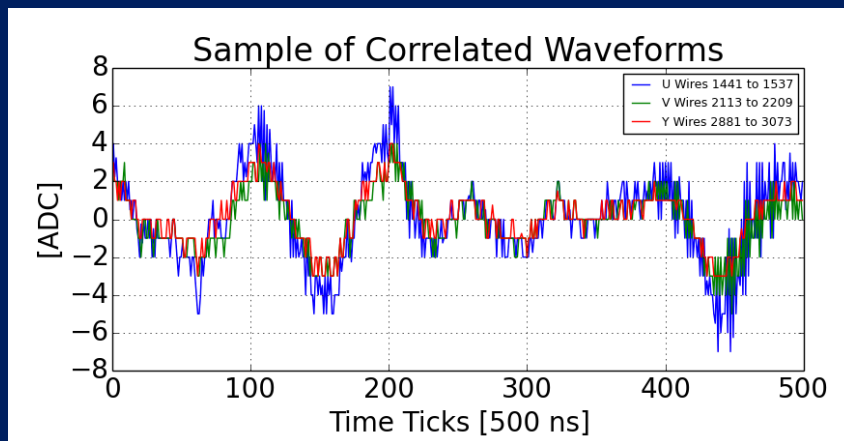
zig-zag noise (occasional large amplitude)



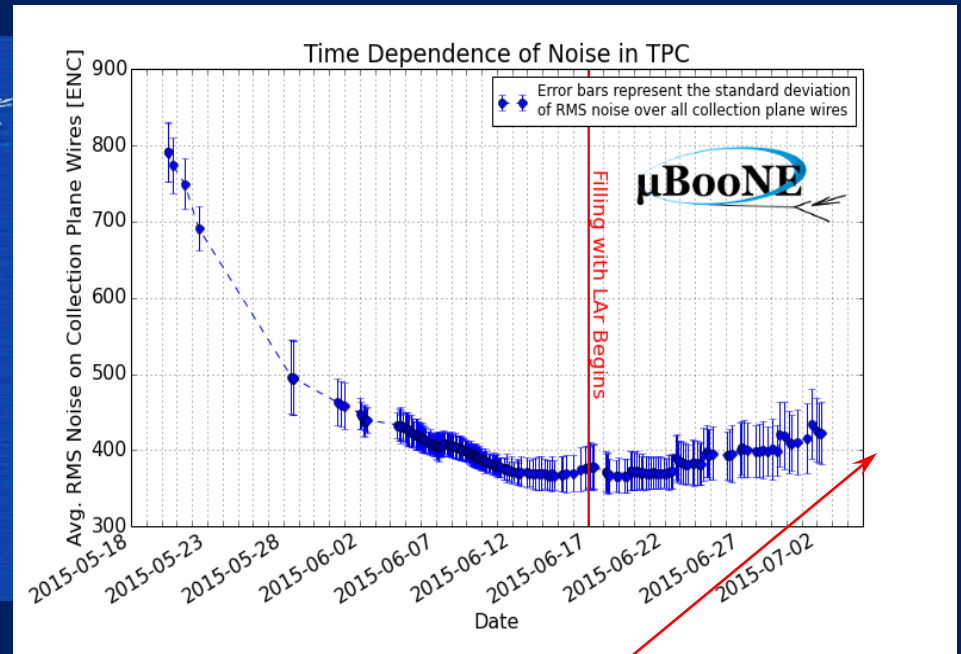
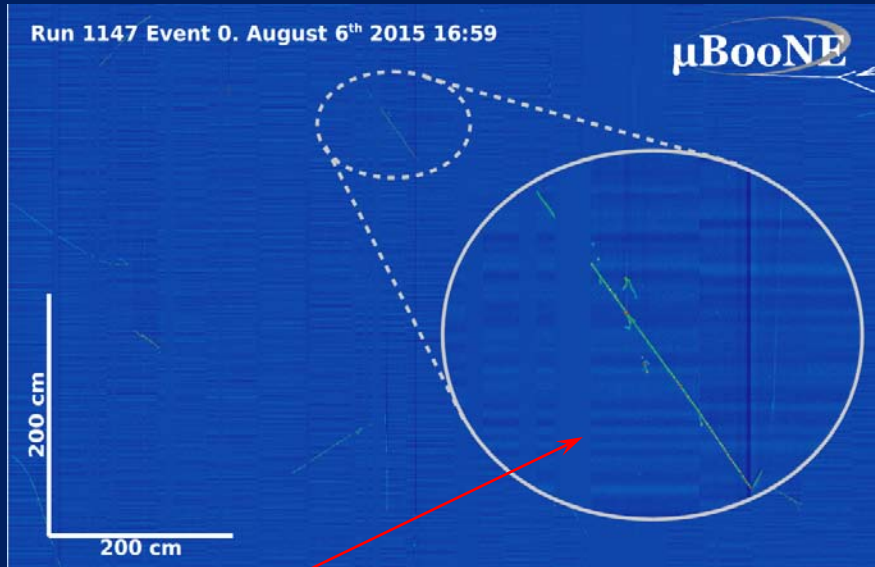
- Not known where it comes from; it occurs in the downstream part of the cryostat; it is intermittent and changes in time; not related to any other noise.
- Its effect on the experiment is negligible: At 0.5 μ s it affects <1.5% of events, very few at 1 μ s, none at 2 μ s. Easily filtered out without affecting the signal.

4. "10-30 kHz noise" – LVR noise

- Low frequency noise has been observed on MicroBooNE TPC
 - ~10kHz – 30kHz wide spectrum noise
 - Contributes little to the ENC at the ~500 e⁻ rms level, but visible as "waviness" after reconstruction
 - Characterized by waviness proposed by M. Mooney
 - Coherent noise in a group of mother boards on half feed-through
 - No dependency on the wire bias
 - Dependency on wire length (wire capacitance)
 - Confirmed by measurement of IA output with spectrum analyzer

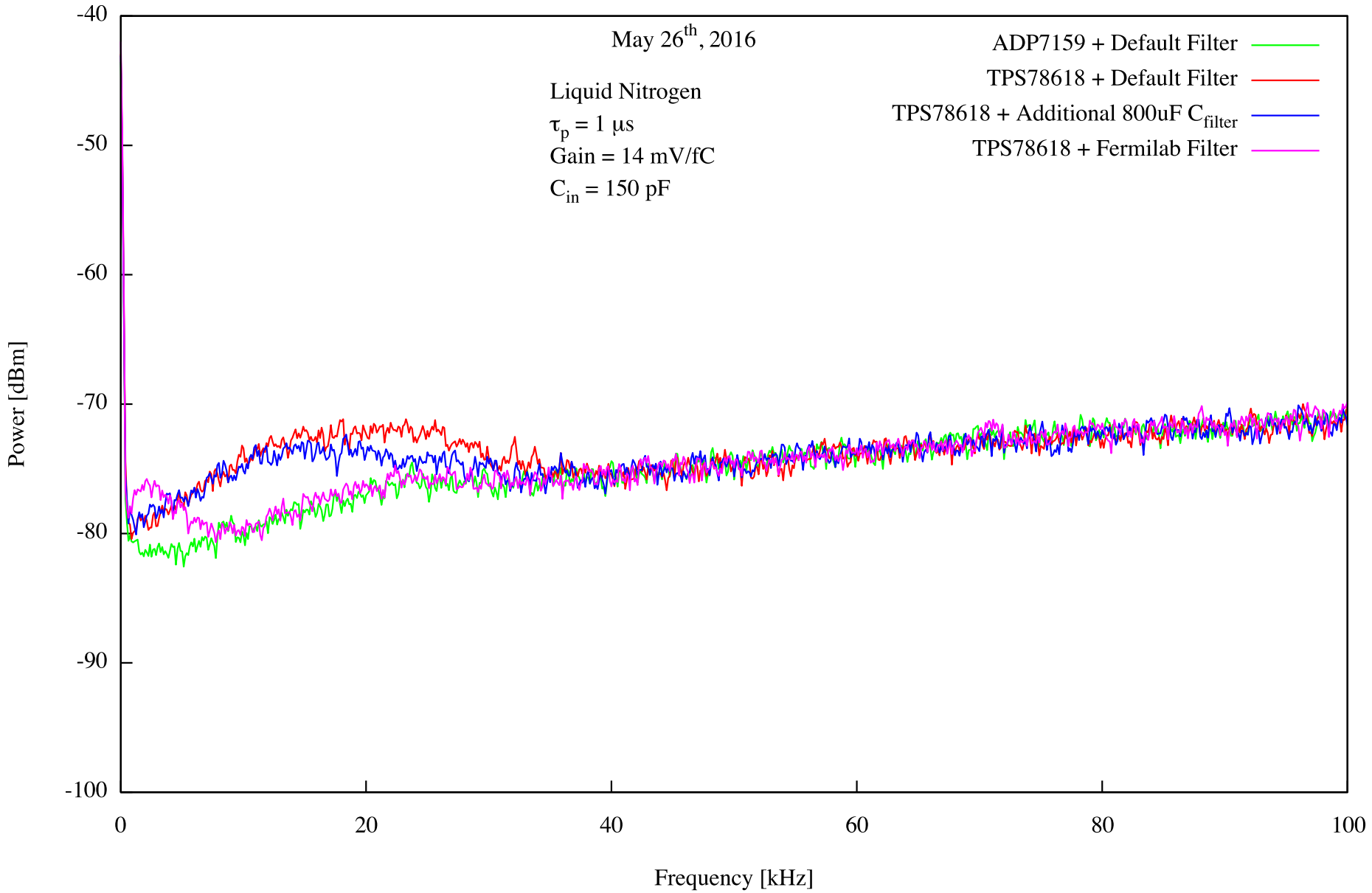


Low Frequency Noise



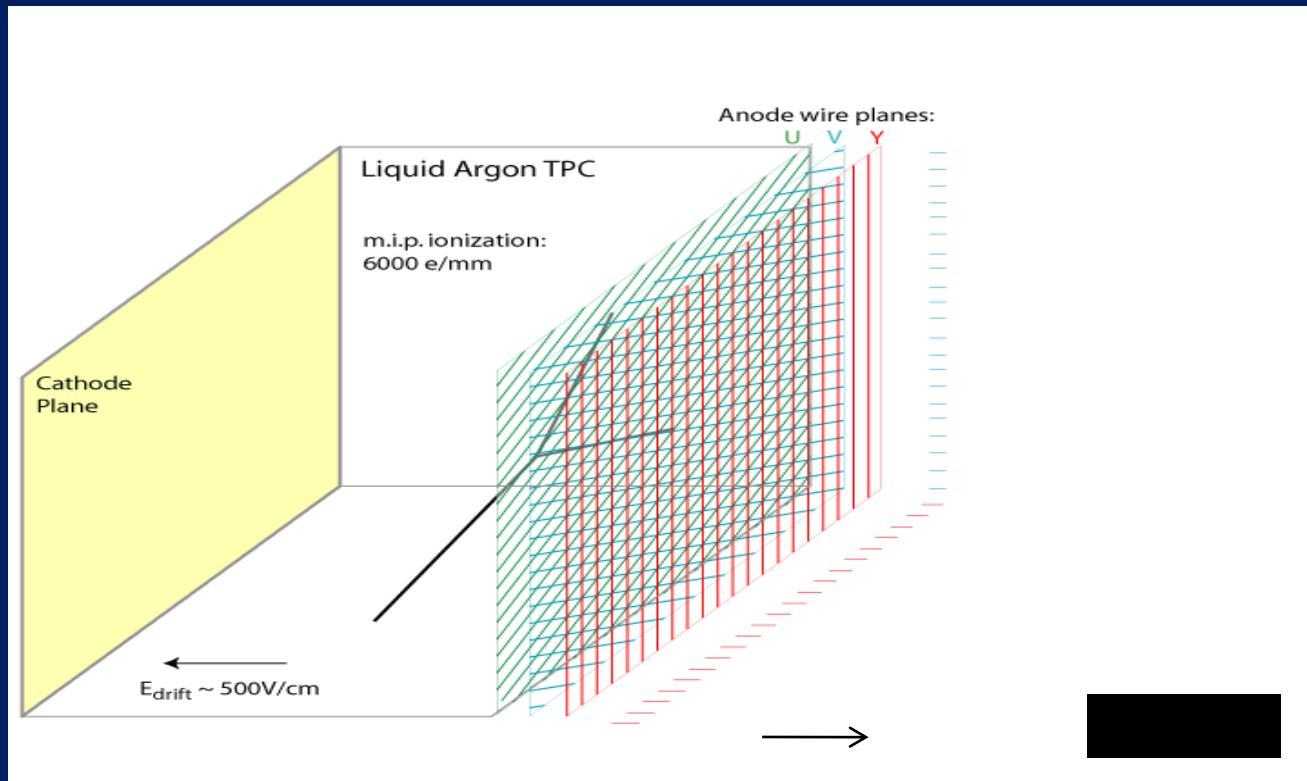
- The reconstruction plot is sensitive to the low frequency spectrum bump
- But the ENC is less sensitive to the low frequency (10kHz – 30 kHz) noise
- This is because the ENC is accounted for the integral of the noise spectrum over the bandwidth of the front end electronics (~350kHz with 1 μ s peaking time)

Test of MicroBooNE Mother Board with Twelve v4* ASICs Populated



5. “drift HV noise” → HV supply ripple

“We noticed TPC noise from the cathode coming along with a “blip storm” (lots of activity in the HV monitoring tools), but nothing in the PMTs ...”



Induced charge into anode wire plane by cathode potential variations:

Wire capacitance to cathode (2.5 m drift, 3 mm pitch $\sim 40\text{ fF/m}$.)

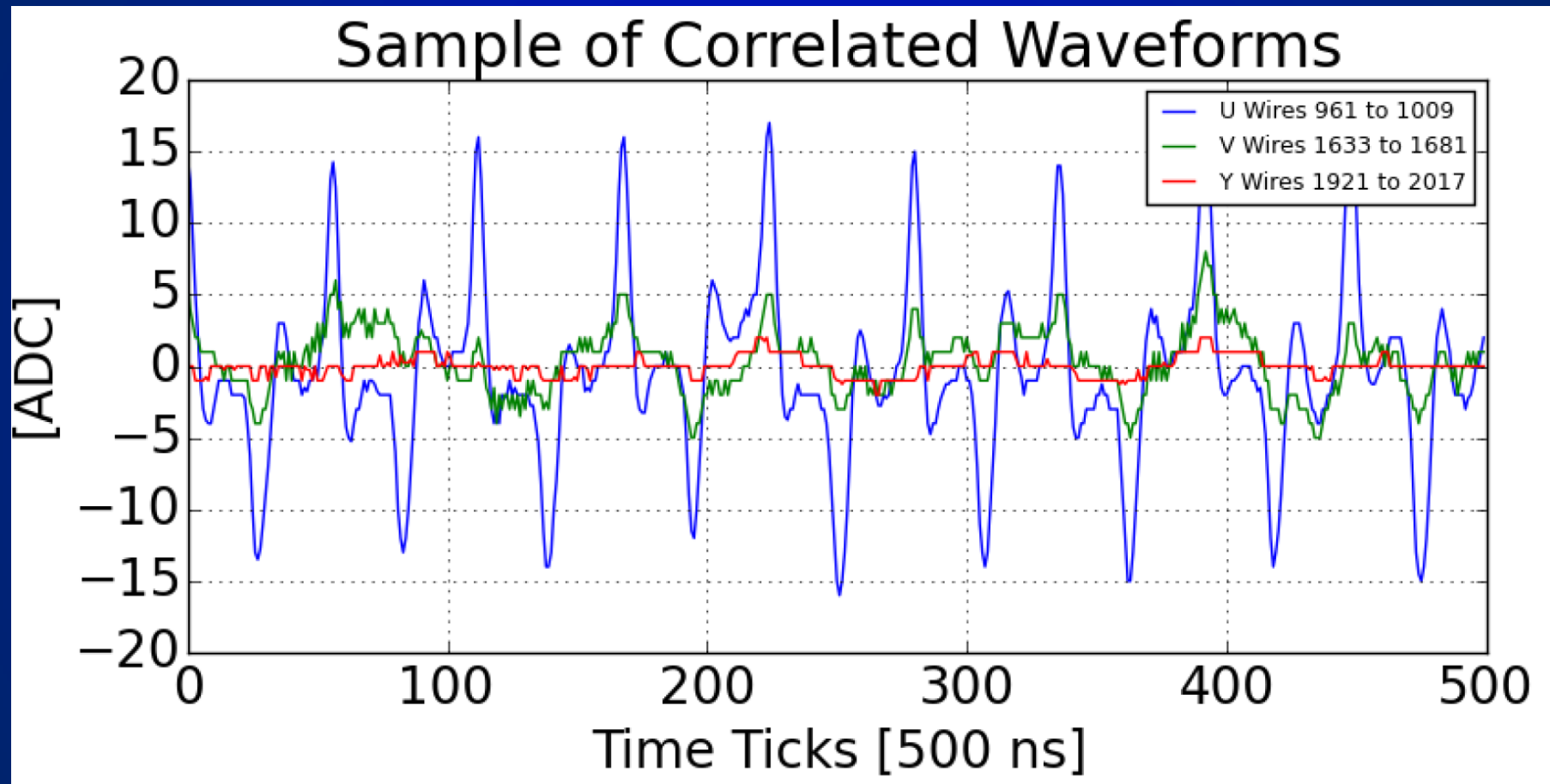
Assuming 2.5 m wire length, induced charge

$\sim 0.1\text{ fC/mV}$

$\sim 600\text{ e/mV}$

Needs detailed study for each TPC geometry!

HV ripple (36 kHz fundamental) induced on sense wires



Noise induced by the cathode is progressively attenuated by the shielding effect of the wire planes

HV supply ripple ~ 1 V p-p, 36 kHz



Summary of Excess Noise

1. “noisy wires after applying the wire bias” - wires in contact:
50-70 wires (mostly u), exact number unknown and varies in time as the contact is intermittent.
2. “chirping noise” - FE ASIC saturation due to wire motion:
Virtually eliminated (<20 wires) by proper ASIC bias setting (500 pA)
3. “zig-zag noise” - “pickup” burst noise:
The only unexplained source, likely from switching noise outside.
Negligible effect on signal/track reconstruction.
4. “10-30 kHz noise” - low voltage regulator noise:
Affects all wires.
5. “drift HV noise” - cathode→anode HV supply ripple:
Affects all u -wires, 1/3 amplitude on all v -wires; negligible on y -wires.
Both 4. and 5. easily removed by software, with an effect on signals from tracks in orientations producing long signals.
Both 4. and 5. will be removed by hardware steps which are under way (inserting better although quite different filters).