DUNE Cold Electronics Review Report
October 12-14, 2016
BNL

Sandro Centro, David Christian (Chair), Mauro Citterio, Philippe Farthouat, Carl Grace, Ted Liu, Abderrezak Mekkaoui, and Christophe de la Taille

1. Elements inside the Cryostat
    a. ASICs
    b. PCBs
    c. Cables
2. Signal Feed-Through
3. Warm Electronics
4. General Recommendation
5. Answers to the charge questions

1. Elements inside the Cryostat

1.a ASICs

Front End (FE) ASIC

Findings

1. The MicroBooNE cold FE ASIC has achieved good noise performance after proper filtering of power supply voltage.
2. MicroBooNE has observed a problem they call "chirping" which is understood to be caused by movement of some of the TPC anode wires. The number of affected channels was greatly reduced with 500 pA FE "input bias" (as opposed to 100 pA).
3. The P1 revision of the FE ASIC includes options for 1 nA and 5 nA input bias.
4. MicroBooNE has also had problems with FE ASICs failing to start up properly when power is applied.
5. The P1 revision of the FE ASIC includes a modified bandgap reference circuit designed to fix the start up problem.
6. A problem was discovered in the P1 revision due to mismatch between the biasing of the first and second stage (especially in cold operation). This problem was mitigated with the addition of an external 1 GΩ resistor. The P2 revision includes a modification to the biasing so that an external resistor should not be required.
7. Tests of the P1 revision at liquid argon temperature revealed that, for some channels, the output pulse shape is not as desired.
8. The P2 revision also includes a modification to the pole zero shaping network designed to eliminate this problem.
9. P1 packaged parts exhibit a large baseline shift in cold operation. This effect was not observed in MicroBooNE. The MicroBooNE package had a smaller CTE (Coefficient of Thermal Expansion) mismatch than the recently received package. The MicroBooNE package is no longer available.

Comments

1. The information provided by MicroBooNE has been extremely valuable for DUNE cold electronics development. The "chirping" problem, caused by extremely small and slow wire motion, was not anticipated.
2. The preamp noise performance is excellent given the large input capacitance, and this low noise will be crucial for DUNE. This performance would have not been possible without careful attention to proper grounding and shielding.
3. However, the circuit is very sensitive to input bias variations, both from power supply ripple and from input "leakage current." The "chirping" problem associated with this leakage current appears to have been solved by allowing for a larger bias current.
4. The modified bandgap circuit operates reliably at cryogenic temperature. This appears to have solved the cold startup problem.
5. Whereas the qualitative explanation on package stress is plausible, it would be good to also have a quantitative study. Package stress is known to induce offsets, but usually in the mV range and they follow the stress distribution, worse on the edges. In the preamp design, it is not clear what transistors would induce such large offset at the output. The proposition to use an open cavity or ceramic package would most likely solve the issue.
6. For each experiment, the acceptance criteria for the FE ASIC should be defined and documented.

No Recommendations

Analog to Digital Converter (ADC)

Findings

1. While pre-tape out simulations suggested the stuck bit problem would be solved in the latest ADC ASIC submission, testing clearly indicates it has not been completely fixed. Therefore the core problem with the architecture has not been completely understood.
2. The performance of the P1 ADC is about 1% linear but with significant nonlinearity at low input voltages. It also has missing codes (at intervals of 64 bits) and still has significant nonlinearity peaks (but it is improved from the V* prototype).
3. The average Least Significant Bit (LSB) of each ADC channel in the ADC ASIC shows significant variance at cold, indicating large mismatch.

Comments

1. The "domino" ADC architecture used in this ASIC fundamentally depends on matching between active devices. Moreover, current source mismatch is expected to be roughly four times worse at LAr temperature than at room temperature. This is reflected by worse cold performance, and in particular, stuck bits.
2. The ADC nonlinearity at low input voltages means that several hundred codes on the low end will need to be thrown away, reducing the effective dynamic range.
3. A 12-bit ADC operating at 2 MSPS at cryogenic temperature is extremely challenging given the power and area constraints.
4. The committee is not convinced that the requirement for a linear 12-bit ADC is fully justified.
5. For SBND it may be worthwhile to consider if a comprehensive analysis of the ADC issues could lead to a simple fix that would improve the performance of the ADC in time to be included in SBND. Converting the present design to an 11-bit ADC might

overcome the limitations of the current 12-bit version. It is likely that the area and power saved by eliminating one bit could be reused to make the design more robust to device mismatch.

6. For each experiment, the acceptance criteria for the ADC ASIC should be defined and documented.

Recommendations

1. Use the current ADC for ProtoDUNE-SP after a study of how to best use the data it provides. If the results of the first tests on a P1 ADC are a true indication of the performance of this version, it might be used as a 10-bit equivalent ADC by either truncating the two least significant bits or by rounding to the nearest multiple of 4. Tests of a single unpackaged die indicate this should eliminate the missing codes and reduce the impact of the nonlinearity peaks by a factor of 4. This will, however, increase the noise and lower the resolution, so it is necessary to determine the impacts of this on physics data.
2. Going forward, the ADC specifications for DUNE should be revisited. If 12-bit dynamic range is needed, can it be done with a 10-bit ADC with a programmable gain in front instead of with a single 12-bit ADC? Implementing a 10-bit ADC will significantly reduce risk compared to a 12-bit ADC.
3. For DUNE, it may be prudent to re-evaluate the cold electronics system partitioning. Significant risk is incurred by placing ASICs in the cryostat as any in-cryostat ASICs cannot be replaced for the duration of DUNE. It may be possible to balance this risk with other requirements by moving some of the cold electronics out of the cryostat. For example, if an analog multiplexer and differential line driver were added to the cold FE ASIC, it might be possible to move the ADC to warm and use a commercial ADC. While this would require more wires leaving the cryostat, it would have the benefit of reducing the number of ASICs that need a 30-year

lifetime in cold. This may or may not reduce overall system risk, and this should be evaluated.

4. For DUNE, if an in-cryostat ADC is preferred and if the reduced resolution of the current Cold ADC ASIC as-is does not meet experiment requirements, the group should explore replacing the ADC in a future submission with an ADC using a standard architecture, such as a Successive Approximation Register (SAR) ADC or a Pipelined ADC. Both of these architectures depend for precision on the matching of passive components rather than active components and will likely have better performance at liquid argon temperature.
5. We recommend (for DUNE) that for a modest number of lines, the output of the analog FE be made available for diagnostic purposes outside the cryostat.

1.b Printed Circuit Boards

Findings

1. ProtoDUNE-SP and SBND have different APA configurations and different wire pitches. Nonetheless, the cold electronics printed circuit boards for the two experiments are very similar. In both cases, 128 APA wires are input to a "Front End Mother Board (FEMB)" assembly consisting of an analog mother board and an FPGA mezzanine card.
2. The analog mother boards contain 8 FE ASICs and 8 ADC ASICs. The required low voltages are derived from 12 VDC by TI TPS74201 regulators that have been demonstrated to perform well at liquid argon temperature.
3. The FPGA mezzanine cards contain a single Altera Cyclone IV FPGA. Once again, TPS74201 regulators provide the required voltages.
4. SBND will use FEMBs mounted on the top and on the sides of APAs, so two types of analog mother boards are required (with input connectors configured for vertical and horizontal mounting).

5. All ProtoDUNE-SP FEMBs will be mounted on top of the APAs, so only one input connector configuration is required. The ProtoDUNE-SP analog mother boards will be identical to SBND analog mother boards with the horizontal input configuration.
6. The ProtoDUNE-SP and SBND FPGA mezzanine cards will differ only in the type of data I/O connector used.
7. A number of prototype FEMB printed circuit boards have been fabricated and tested, both at room temperature and at liquid argon temperature.

Comments

1. Both ProtoDUNE-SP and SBND benefit from the development of a single cold electronics solution, with minor PCB differences.
2. The committee recognizes the effort undertaken in selecting reliable PCB manufacturers and assembly houses for the production of the front-end boards operating at cryogenic temperature.
3. The practice of adding "via coupons," i.e. chains of interconnected vias, to the design to evaluate the quality of the manufacturer plating process, followed during the PCB manufacturer selection phase, should be pursued in the production phase also. It is indeed extremely important that the quality of the boards to be installed in the experiment, could be verified not only by a careful optical inspection but also with dedicated measurements. Being the vias, a possible weak point in a PCB production, the measurements of via resistance on each board is considered a standard QA/QC procedure. Moreover, having a dedicated "via coupon" per each PCB panel produced, will allow via-resistance measurements after multiple cooling cycles before board assembly, enhancing the confidence in the board reliability.
4. The QC procedure should include a description of what type and quantity of reworking is allowed on the cryogenic front-end board. A log of the reworking for each board should be kept in the QC database. The reworking protocol and log should also be agreed with the assembly house.
5. The group has recently developed a plan to test all ASICs at cryogenic temperature in a simple dewar before assembling FEMBs. While this is an attractive idea, it is not clear that sockets will survive a large number of temperature cycles. If sockets can

be found that do survive, it may be especially valuable to qualify and select ADC ASICs for cold operation before FEMB fabrication.

No Recommendations

1.c Cables

Findings

1. SBND will use 3M mini SAS (twinax with 30 AWG conductors) data cables. ProtoDUNE-SP will use Samtec twinax cable (26 AWG).
2. In the 35T test, Gore twinax data cables (with 24 AWG conductors) were used.
3. Both SBND and ProtoDUNE-SP plan to use unshielded twisted pair cables for power; 22 AWG conductors for SBND and 20 AWG conductors for ProtoDUNE-SP.
4. Both experiments will use RG316 cables terminated with SHV connectors to carry the anode plane bias voltages.
5. A cable strain relief scheme that uses custom clamps together with lock wires and hose clamps has been developed.
6. The designs for ProtoDUNE-SP, SBND, and DUNE call for power cables running from the cryostat feed through to the FEMB in close proximity to the TPC readout cables and to the photodetector cables.

Comments

1. Data cables chosen for ProtoDUNE-SP are sized for DUNE and use heavier gauge wire than necessary, given the length required for ProtoDUNE-SP. This is a good idea and will allow the group to gain experience with cabling infrastructure that can be used without modification in DUNE.
2. Eye measurements made using the Gore cable used in the 35T test and the Samtec cable chosen for ProtoDUNE-SP demonstrate that the Gore cable is superior to the Samtec cable, but that the Samtec cable is acceptable.

3. The cables selected have PTFE insulation, which will require authorization from CERN for use in ProtoDUNE-SP. This should be sought as soon as possible.

Recommendations

1. Given the sensitivity of the FE ASIC, we recommend the use of shielded power cables.

2. Signal Feedthrough

Findings

1. The feedthroughs designed for ProtoDUNE-SP and for SBND differ in detail, but share all important design elements.
2. In both cases, positive pressure ensures that gaseous argon contaminated by cable outgassing is not liquefied.
3. Both feedthroughs avoid condensation by providing a gradual temperature gradient from cold to warm so that the feedthrough boards are at or near room temperature on both sides of the boards.
4. The two designs use a common compression plate and indium wire to seal the flange printed circuit board against the flange. Signals pass through the flange printed circuit board on blind vias and no through-hole parts are used.
5. Finite element analysis has been used to compute the maximum deflection of the feedthrough boards in the expected range of cryostat pressures. The maximum deflection is very small.
6. The leak rate with an indium wire seal has been measured to be 1.6×10^{-9} mbar·liter/sec. The SBND specification is less than 10^{-9} mbar·liter/sec.

Comments

1. The feedthrough design is well advanced and meets specification in almost every regard. The ProtoDUNE-SP and SBND flange printed circuit boards differ only in the type and number of connectors used. We agree that it is likely that the leak rate specification will be met using an indium wire seal if hard gold is

used on the gold plated surfaces of the flange printed circuit board.
2. If shielded power cables are used, the flange printed circuit board designs will need to be modified.

No Recommendations

3. Warm Electronics

Findings

1. For both ProtoDUNE-SP and SBND, the warm electronics that interfaces with the cold electronics is located in a closed (air cooled) crate mounted on the feedthrough port.
2. In both cases, these warm electronics consist of a single Power and Timing Card (PTC) and one Warm Interface Board (WIB) per TPC Analog Plane Assembly (APA) serviced. Power, timing, and control signals are distributed on a custom Power and Timing Backplane (PTB).
3. The PTC, WIB, & PTB used for the two experiments differ in detail because the experiments use different data acquisition systems and different timing and control protocols, but they are very similar in design philosophy and share most components.
4. The current PTC designs use 12 VDC as input power. The experiments are considering using 48 VDC instead.
5. The WIBs are designed to monitor and control the cold electronics voltages and currents as well to control the cold electronics configuration and receive digital data.
6. Individual warm electronics components (WIBs) can be used in standalone test stands. A SBND test stand on a cart was demonstrated during the review.
7. Crate fans are not monitored. Crate temperature is measured, but the measurements are available only through functioning warm electronics.
8. The SBND data format includes an overall time stamp, but not a time stamp on each data packet.

Comments

1. The warm electronics that will interface directly with cold electronics is at an advanced stage of design.
2. We support a modification to the PTCs to allow the use of 48 VDC at the input rather than 12 VDC, especially as it appears likely that one of the problems in the 35T test was related to ripple on the 12 VDC caused by a long control feedback loop. If the 12 VDC required by the cold electronics is created at each PTC, this potential problem will be eliminated.
3. The temperature sensors distributed in various part of the cold/warm electronics were not discussed in detail during the review. We understand that the sensors have been carefully distributed to monitor possible unexpected temperatures of the electronics/flanges during the experiment. Presently, these temperatures can be read only through the slow control and DAQ systems. In consideration of the fact that these systems will not be always fully operational during the lifetime of the experiment, we recommend to include in the design the possibility of reading the sensor temperatures directly. It is important that these sensors follow the grounding and shielding rules.
4. SBND should seriously consider adding a time stamp to each data packet to ensure data integrity.
5. The ProtoDUNE DAQ system design is still at a conceptual level, so it is hard to judge how complete the PTC and WIB designs are now. The upcoming DAQ review will be important.

<u>Recommendations</u>

1. We recommend that the warm electronics system be modified to include the possibility of reading the temperature sensors directly. It is important that implementation of these sensors follows the grounding and shielding rules.

4. General Recommendation

1. Documentation is especially important for a program such as DUNE, which spans many years and will include generations of participants. The group will benefit (especially in debugging problems that may appear in the future) from detailed documentation of all electronics, especially the ASIC designs. Management should make documentation a high priority.

5. Answers to the charge questions

Q1) Are the requirements for the proposed ProtoDUNE-SP and SBND CE systems sufficiently complete and clear?

Mostly yes. For instance, the FE noise requirement follows from the minimum expected signal for a MIP parallel to and close to the cathode plane, and the 12-bit dynamic range required is justified by this minimum signal and by the expected signal from a proton stopping close to the anode planes. However, it is not clear that a 12-bit linear ADC is required.

Q2) Does the conceptual design for the CE system meet the requirements?

Mostly yes. MicroBooNE results show that this type of FE amplifier can achieve the required low noise. It is unlikely that the "domino" ADC can achieve 12-bit performance, but it is not clear that this should really be a requirement.

Q3) Are justifications for each of the specific technical design choices sufficiently documented?

Yes and no. The need for cold electronics in a large LAr TPC (to minimize capacitance at the input to the amplifier) is well established. It would not be possible to meet the noise specification in DUNE without cold front-end amplifiers. However, we did not review the justification of the specific technical design choices made so far for DUNE.

Q4) Does the design as presented represent a good development path toward DUNE and are there opportunities for incorporating potential advances in the CMOS technology over the DUNE time scale?

Yes, but… ProtoDUNE-SP and SBND are very important steps on the development path toward DUNE, as was MicroBooNE. However, it is clear that the ADC developed for ProtoDUNE-SP and SBND will not achieve the hoped-for combination of dynamic range and precision over that entire range. Alternatives should be explored, starting as soon as possible, for DUNE.

Q5) Are the CE interfaces to other detector subsystems including TPC, DAQ, and cryostat well defined and documented?

Yes. The interfaces to the TPC and the cryostat appear to be well defined and documented. The interface to the DAQ is not completely well defined, but is not impeding the development of system components.

Q6) Is the grounding and shielding plan for the detectors and its impact on the CE systems understood and adequate?

Yes, but… The grounding and shielding plan is simple and elegant. It is important that the plan be followed not only in the implementation of the TPC and photodetector electronics, but also by everything else inside the cryostat (such as cryogenic services). We believe that the possibility of including a shield around the power cables should be reconsidered. Finally, we note that there might be tension between the grounding plan and CERN safety requirements, and that ATLAS faced a similar issue.

Q7) Does the proposed CE design adequately address potential catastrophic failure modes, such as large HV discharges?

Yes, but… The TPC design, especially the protoDUNE-SP design including a resistive cathode, addresses most of the danger posed to the cold electronics by a HV discharge. Diode protection of the FE ASIC is also important. No other catastrophic failure mode was presented.

Q8) Are the proposed integrated system tests sufficient to assure that the systems will meet the performance requirements for ProtoDUNE-SP and SBND? Have applicable lessons-learned from previous LArTPC detectors been documented and implemented into the QA plan?

Yes, but… The timeline is very tight and some QA/QC procedures are still being developed.

Q9) Is the CE design robust enough and the quality control plan and testing program sufficiently comprehensive to assure the dead/bad channel requirements for ProtoDUNE-SP and SBND are achieved?

Yes, but... The QA/QC plan is still being developed. For instance, the decision was recently made to test all FE ASICs at cryogenic temperature as well as at room temperature, based on the MicroBooNE experience of problems that appeared only after cool down.

Q10) Is the proposed joint ProtoDUNE-SP/SBND production, installation, and commissioning plan reasonable?

Yes, but the schedule is very tight.

Q11) Are sufficient technical resources assigned to complete the design and production of the CE systems for ProtoDUNE-SP and SBND?

No. The team is aware of the need for additional resources given the tight schedule. The plan calls for a significant amount of the QC work to be done by students. It is important that the QC procedures be well thought out and well documented, and that sufficient student oversight be provided.

Q12) Are the technical risks associated with the development and implementation of the CE systems recognized and understood and is there a plan for managing and mitigating these risks?

Yes. The risks are recognized and understood. Some risks, most obviously those presented by a very tight schedule, cannot easily be mitigated.