The Correlator for the Tianlai Experiment

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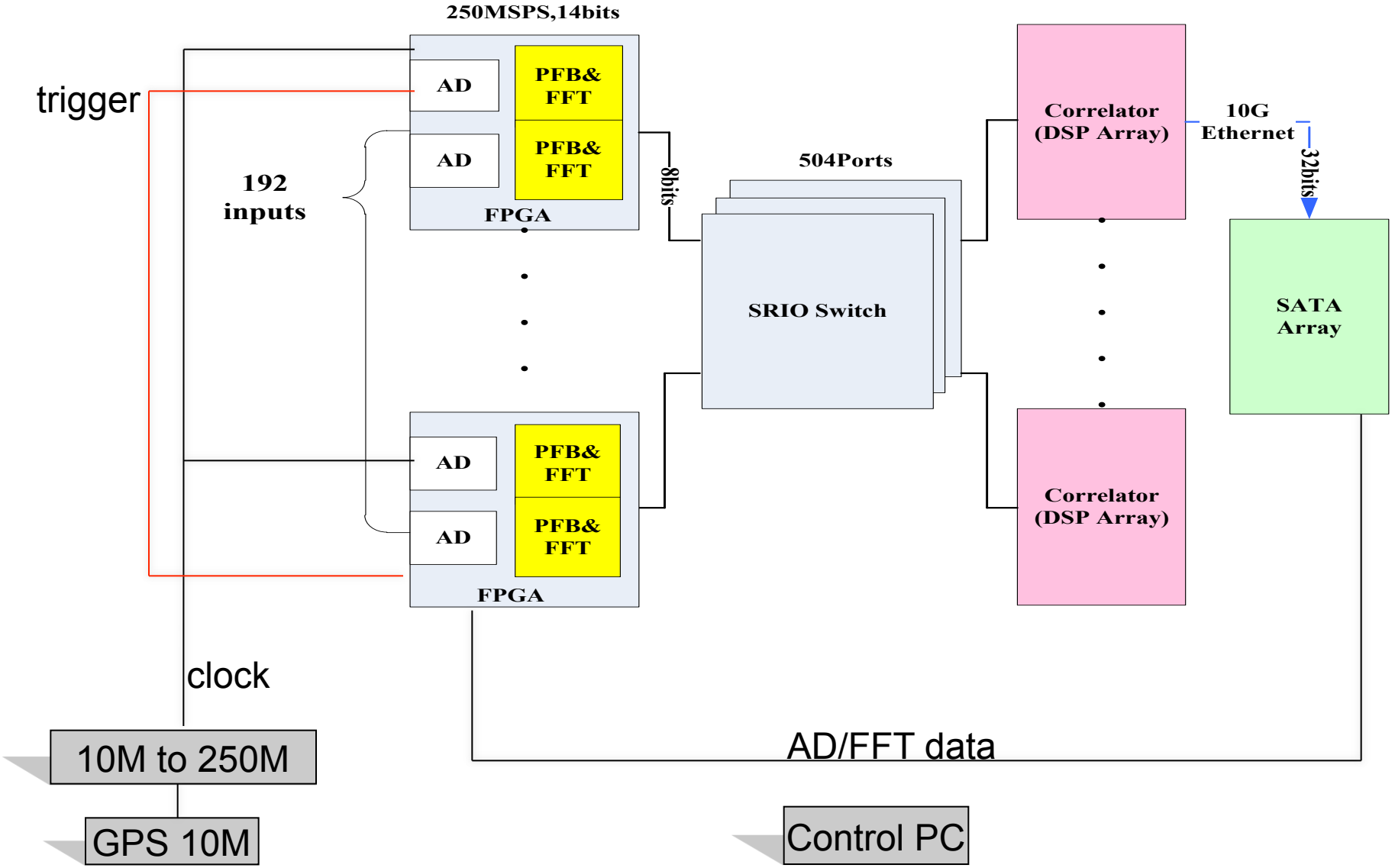
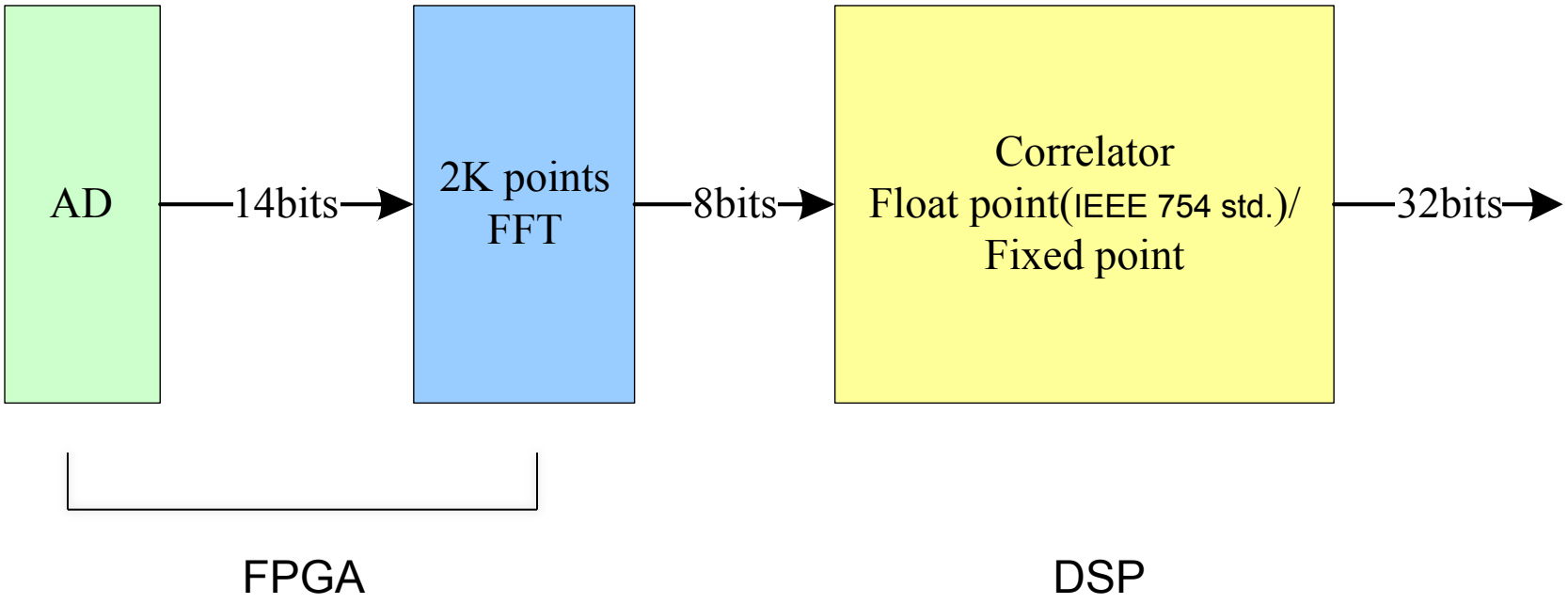
Outline

- System Design
- Hardware Design
- Algorithm Design
- Control Software Design
- Questions and Solutions

System Design



Data Flow

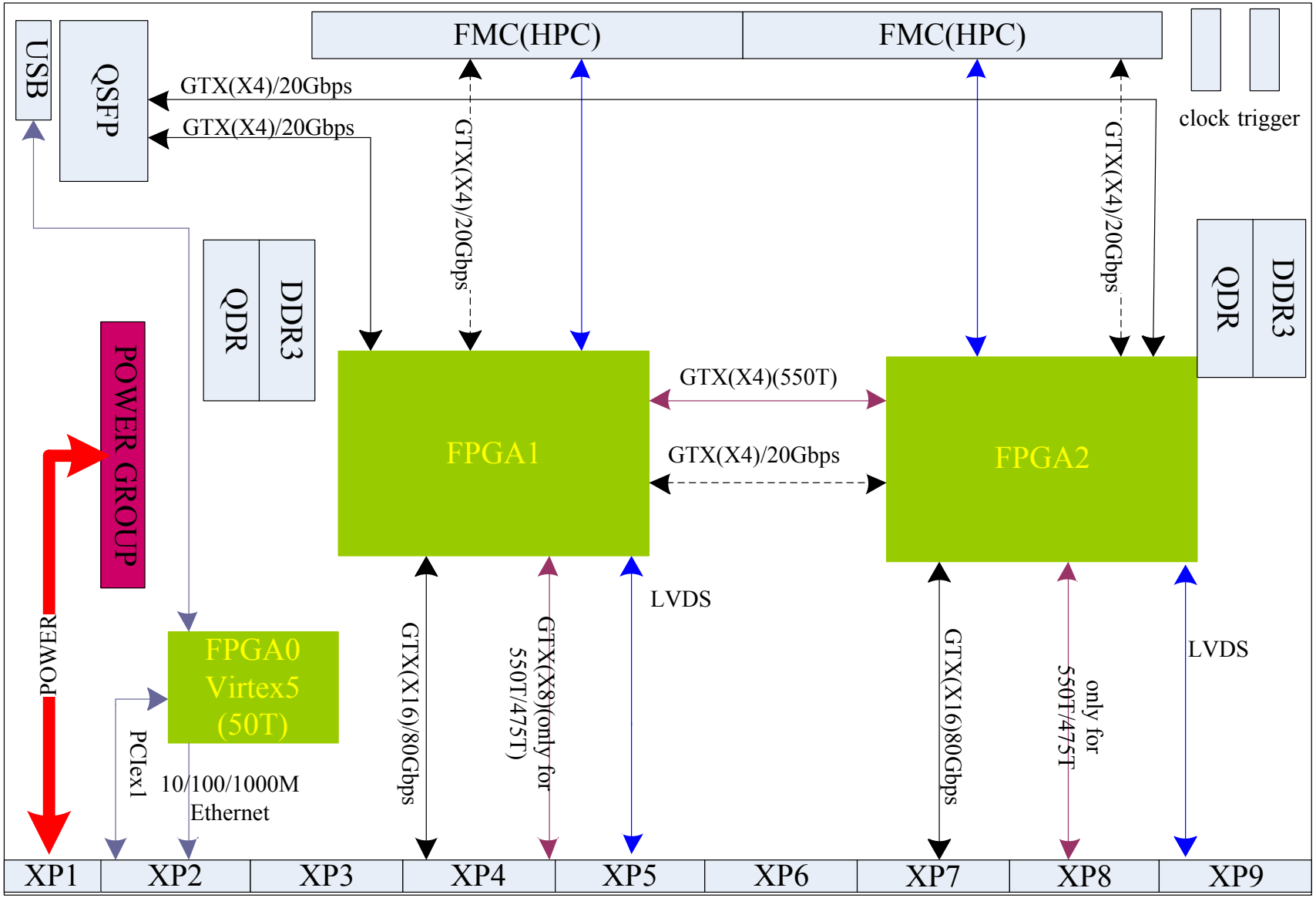

AD
14bits
2K points
FFT
8bits
Correlator
Float point(IEEE 754 std.)/
Fixed point
32bits
FPGA
DSP

Tianlai Digital Backend

Hardware Design

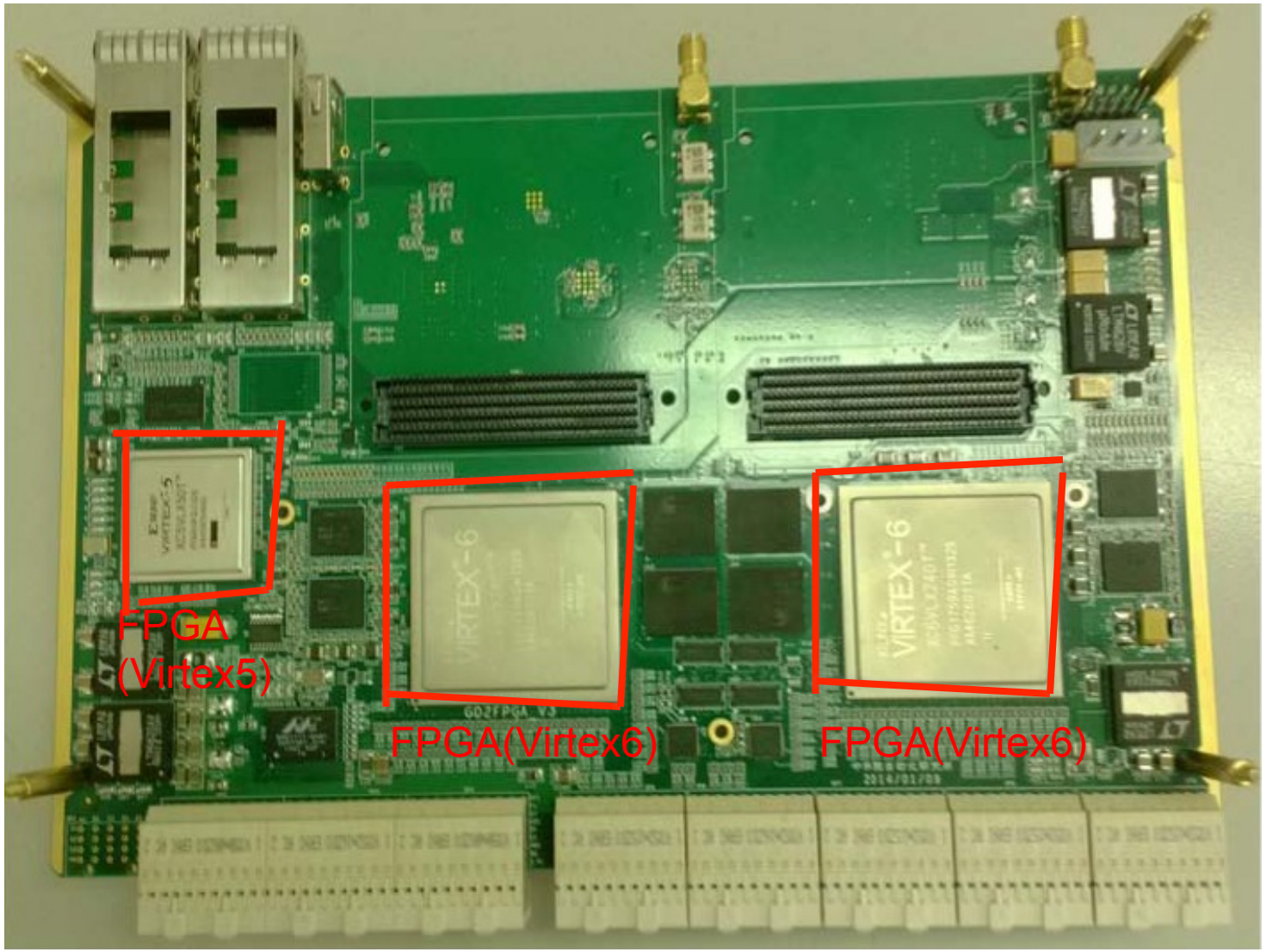
- Data Sampling(ADC+FFT)
  - -ADC based on FMC(FPGA Mezzanine Card) carrier board
  - -FFT based on FPGA(Virtex-6) board
  - -Rear board
- Data processing (Correlator)
  - -based on DSP(TMS320C6678)
- Data switch
  - -RapidIO switch
- Data storage
  - -10G Ethernet
  - -SATA Array

GD2FPGA Data Flow

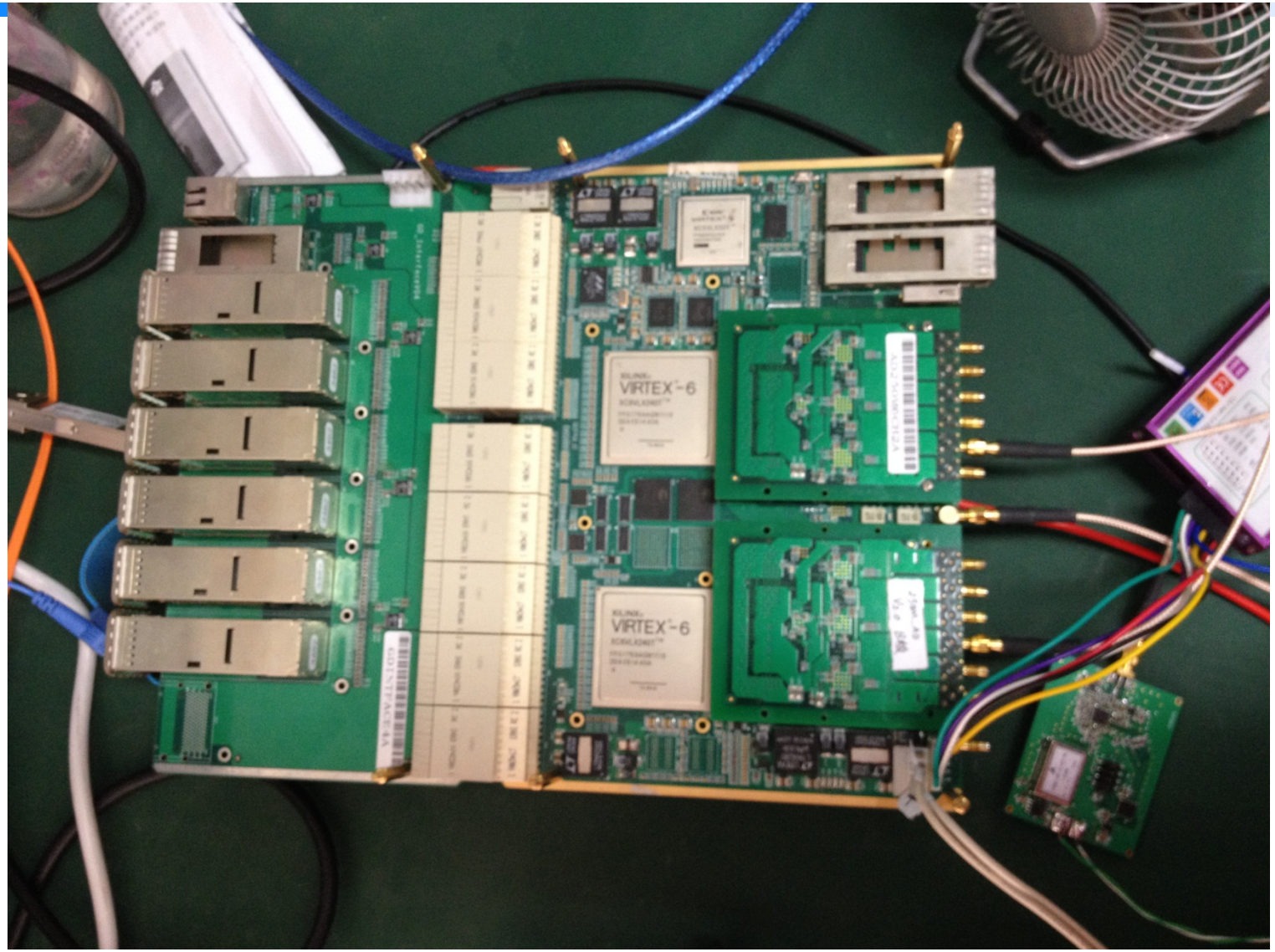


GD2FPGA board

Data Sampling(ADC+FFT)



Reconfigurable mother board



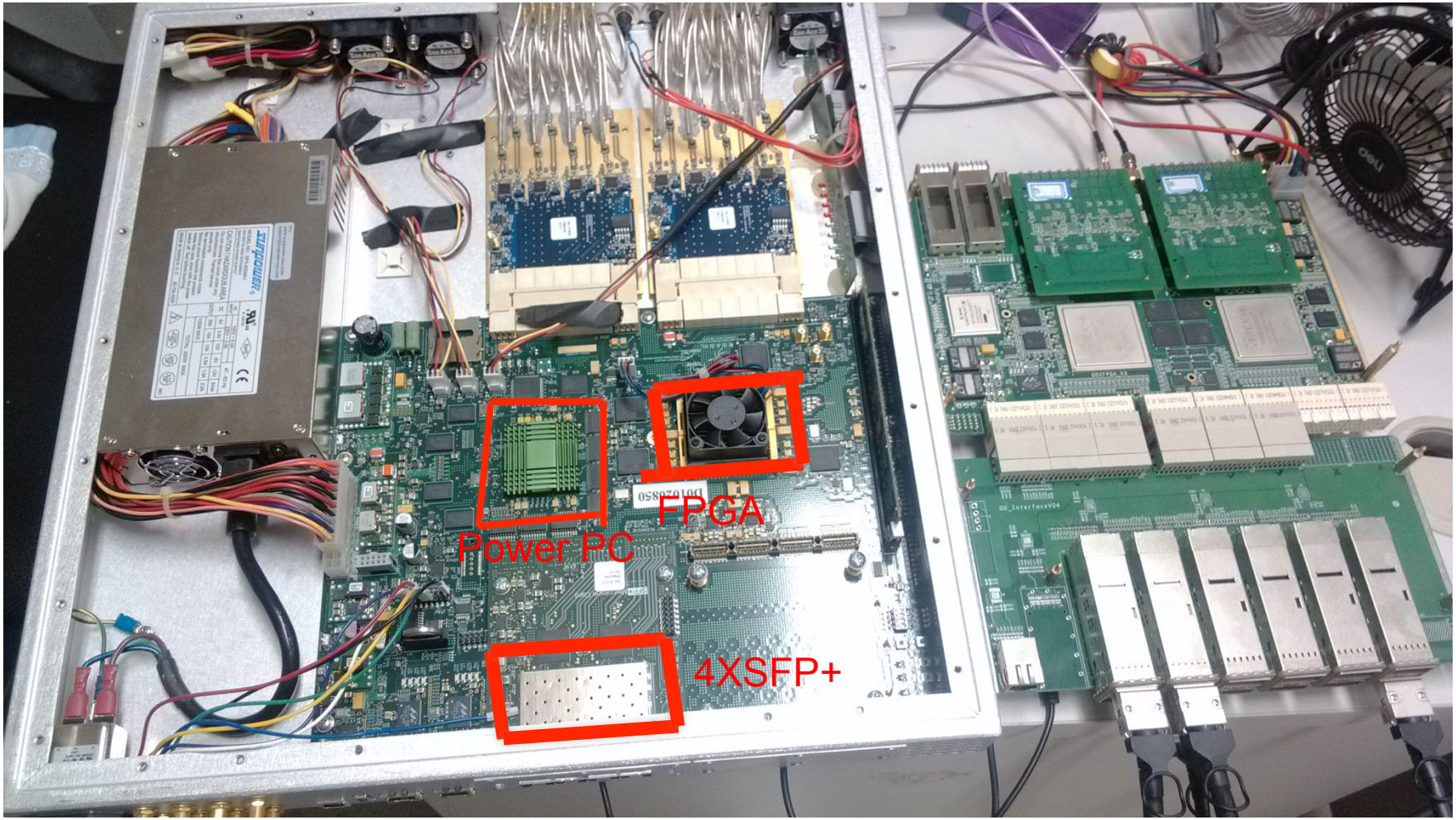
GD2FPGA Board

Data processing board+ FMC carrier board

Features

- 6U standard size
- 2xVirtex-6 FPGA (XC6VLX240T-2FFG1759/XC6VLX315T-2FFG1759 XC6VLX550T-2FFG1759/XC6VLX475T-2FFG1759)
- 16G DDR3-SDRAM
- 288M QDR
- 2xFMC (HPC) Expansion Slots
- 1xUSB2.0
- 2xPCIe
- 10/100/1000M Ethernet
- 2xGTX—40Gbps(RapidIO) through frontplane(QSFP connector)
- 8x GTX(X4) through backplane(ZD connector)—160Gbps(XC6VLX240T-2FFG1759/XC6VLX315T-2FFG1759)
- or 12xGTX(X4) through backplane(ZD connector)—240Gbps(XC6VLX550T-2FFG1759/XC6VLX475T-2FFG1759)
- Soft IP(high speed interface)
  -Rapid IO
  -10G Ethernet

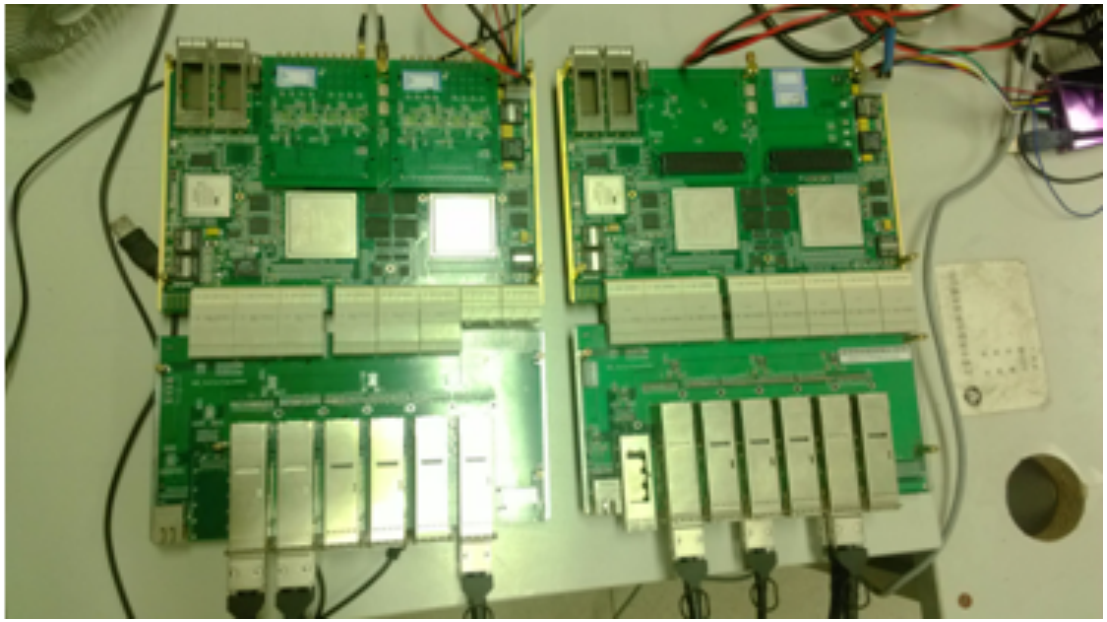
Roach2



Roach2

GD2FPGA

Rear board



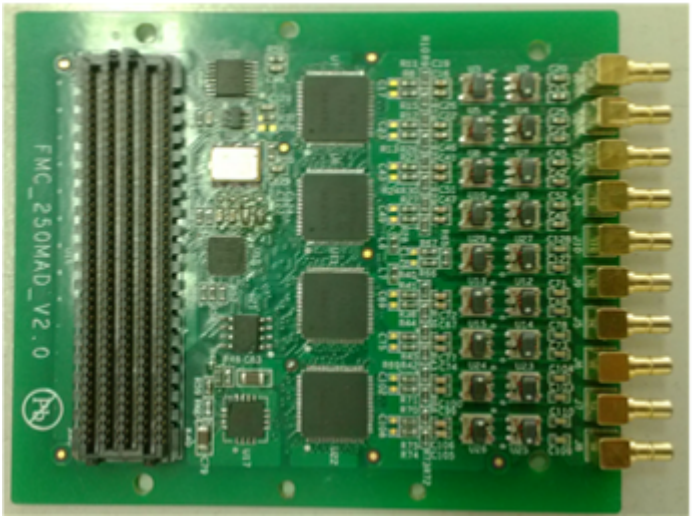
- Connecting boards through cable(Molex)
- Signal testing

10Gb Ethernet rear board

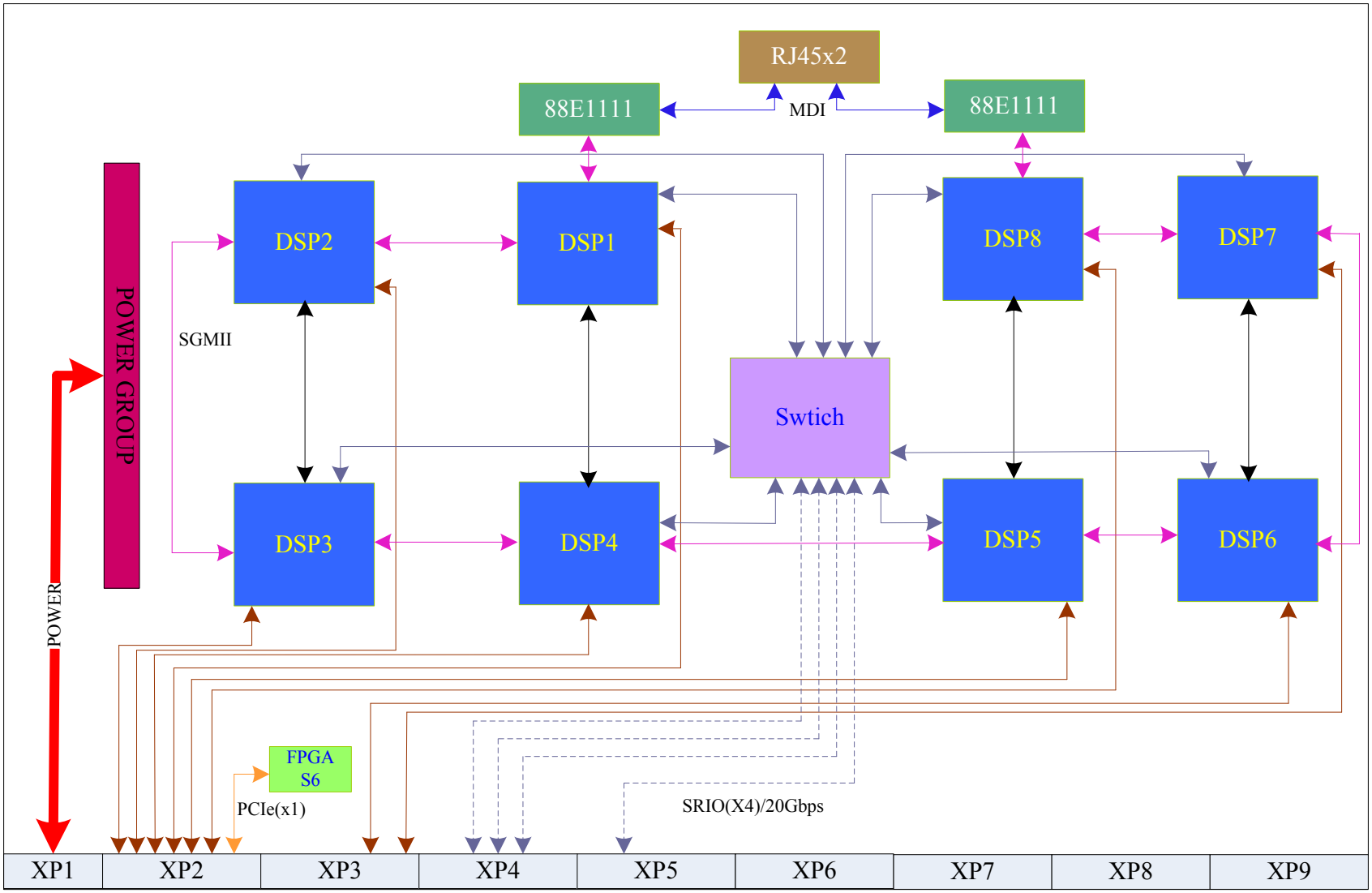
- 4xBCM8747
- 12xSfp+

FMC card (ADC)

- 8 channels
- 4xADS62P49
- External trigger&clock
- 250 MSPS, 14-bits A/D
- Supports multiple clock
- Versatile and industry-standard VITA 57.1 FMC

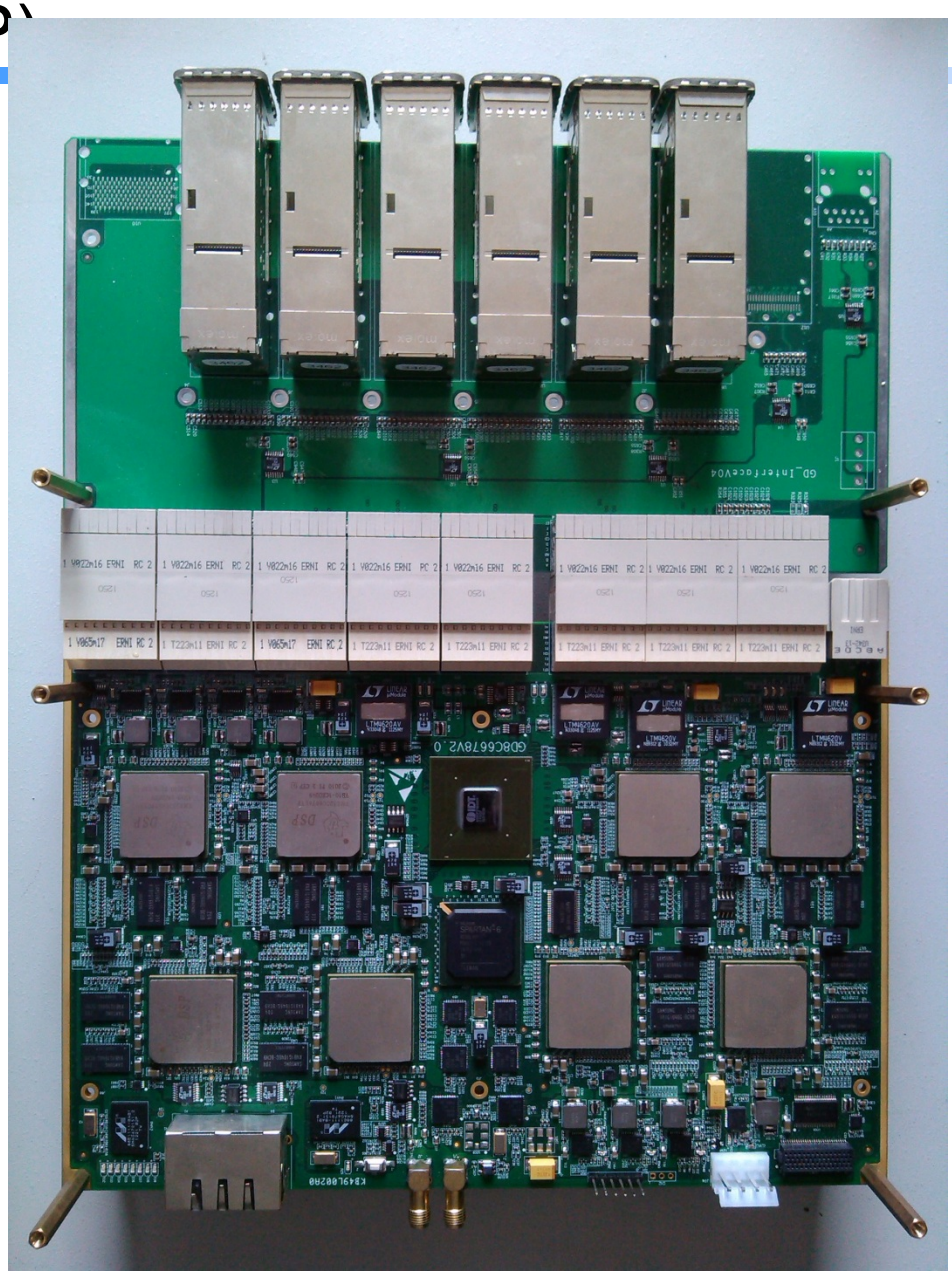


Data processing (correlator)



GD8DSP (based on DSP)

Data processing board



GD8DSP Board

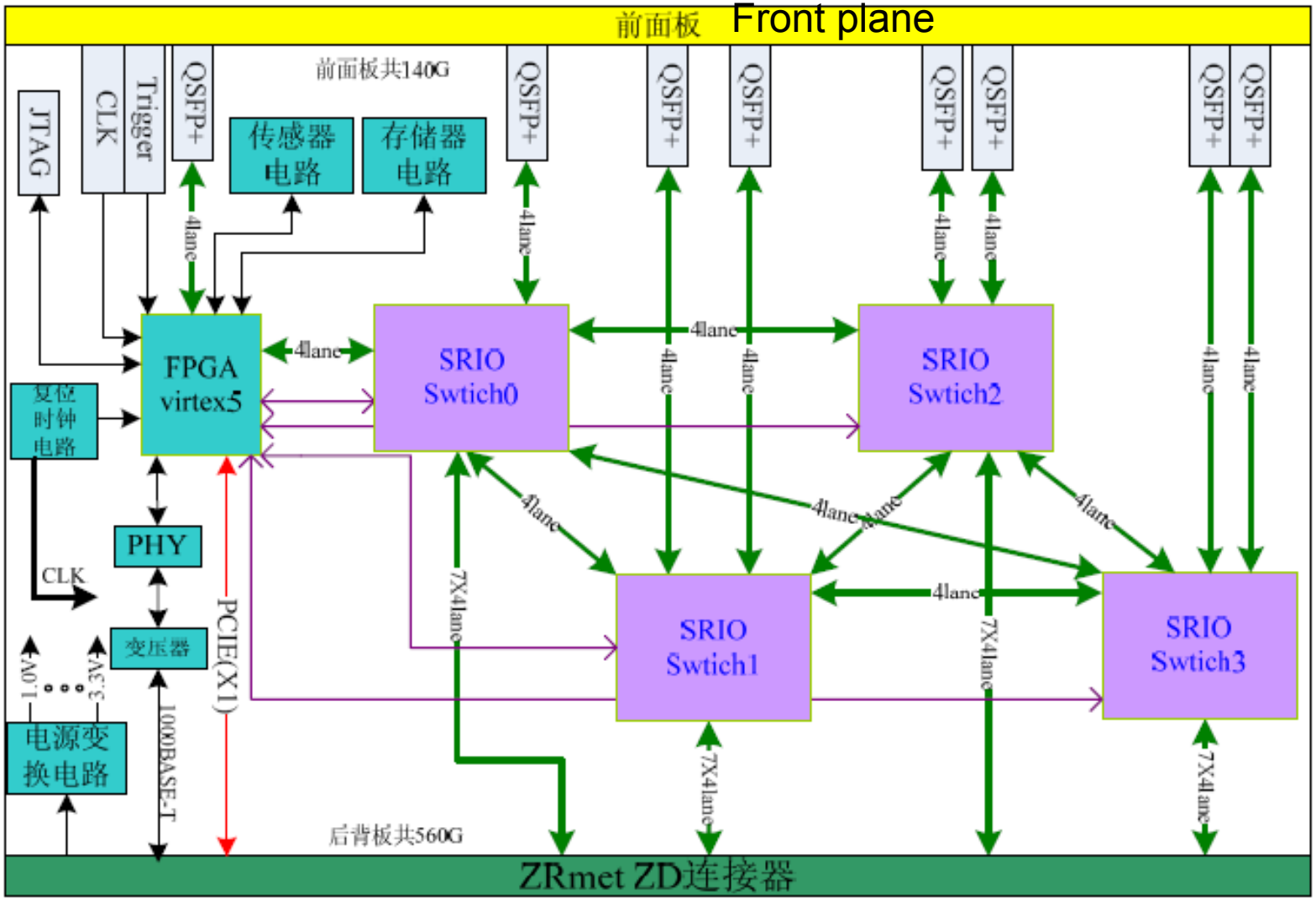
Data processing board

Features

- 6U standard size
- 8xTMS320C6678
- 16G DDR3-SDRAM
- 4xRapidIO(X4) through backplane(ZD connector)—80Gbps
- 8xPCIe(X2) through backplane(ZD connector)—80Gbps
- 2560GMAC(Multiply and Accumulate)

GDSRIOSW board

Data switch board



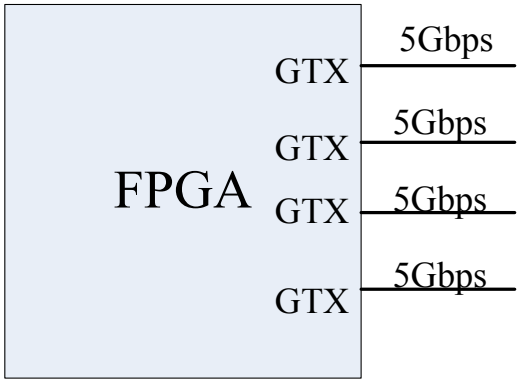
GDSRIOSW board

Features

- 6U standard size
- 4xIDT CPS1848(5~6.25Gbps/lane) serial RapidIO switches
- Supports Rapid IO 1.0,2.0,2.1
- 8xQSFP—160Gbps
- 28xRapidIO(X4) through backplane(ZD connector)— 560Gbps
- Supports backplane star topology

RapidIO vs. 10G Ethernet

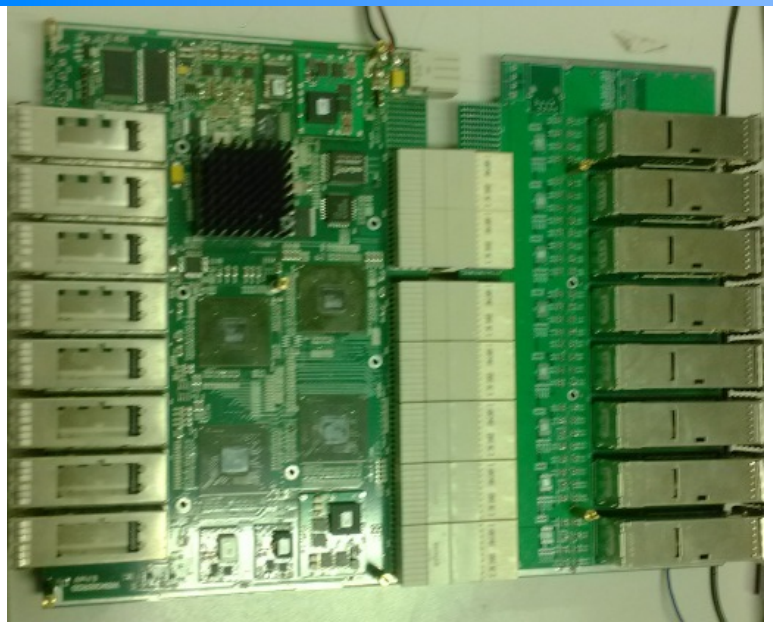
Virtex6's GTX transceivers: up to 6.6 Gb/s



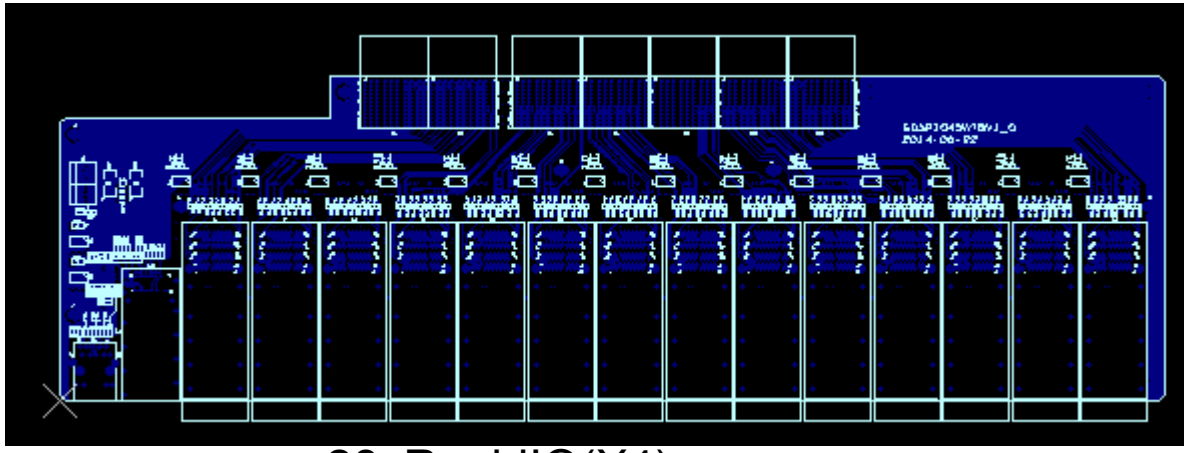
RapidIO

10 GE

The rear board of GDSRIOSW board

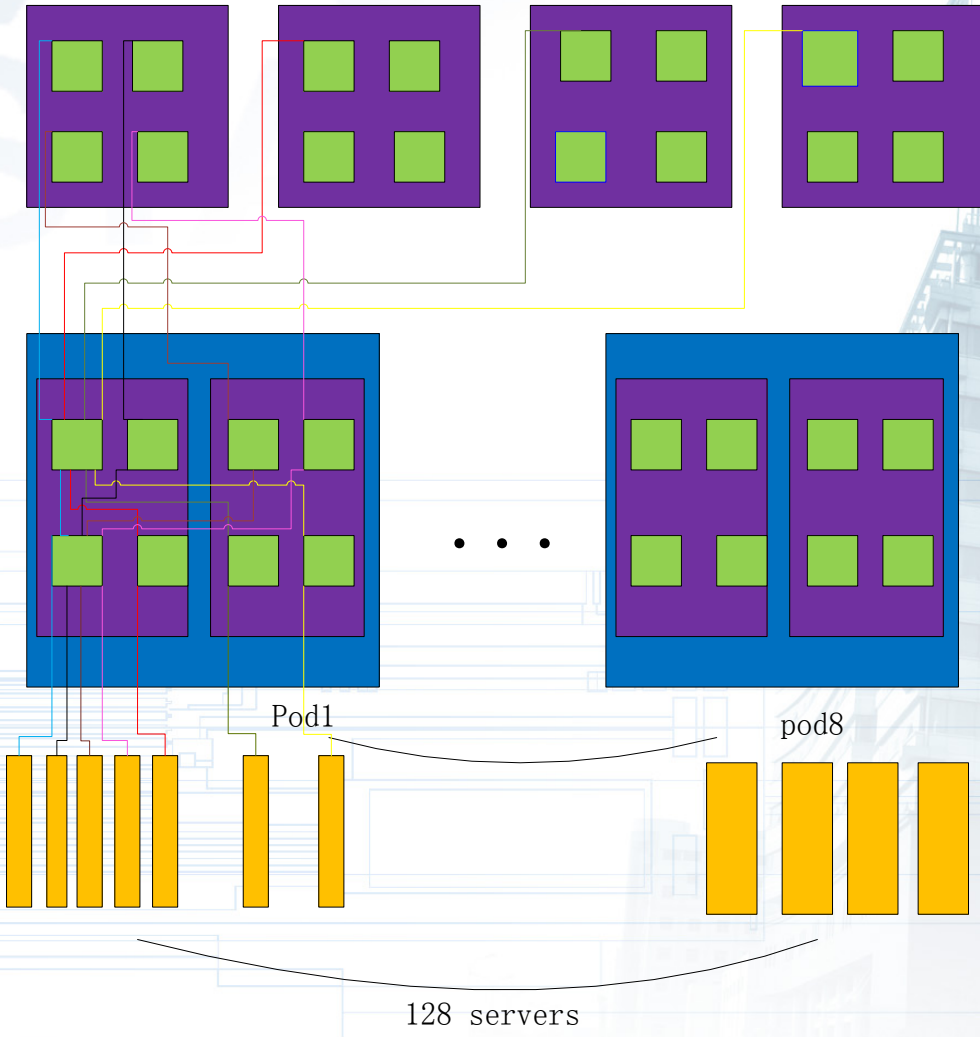


GDSRIOSW board & rear board

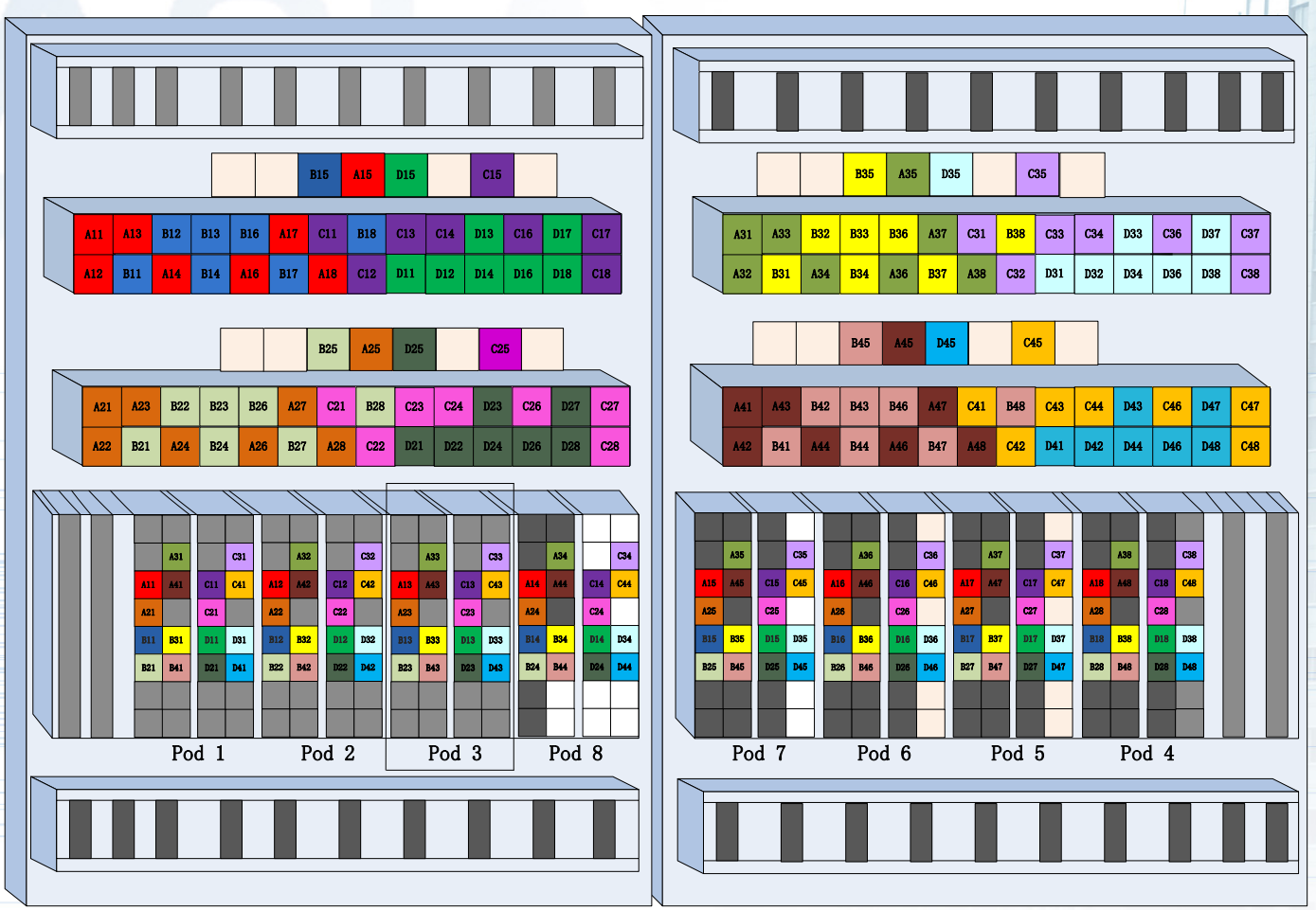


28xRapidIO(X4)

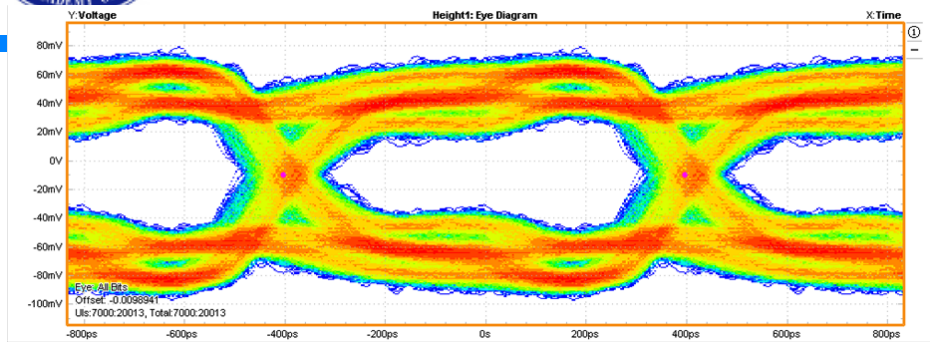
Switching System(fat tree)



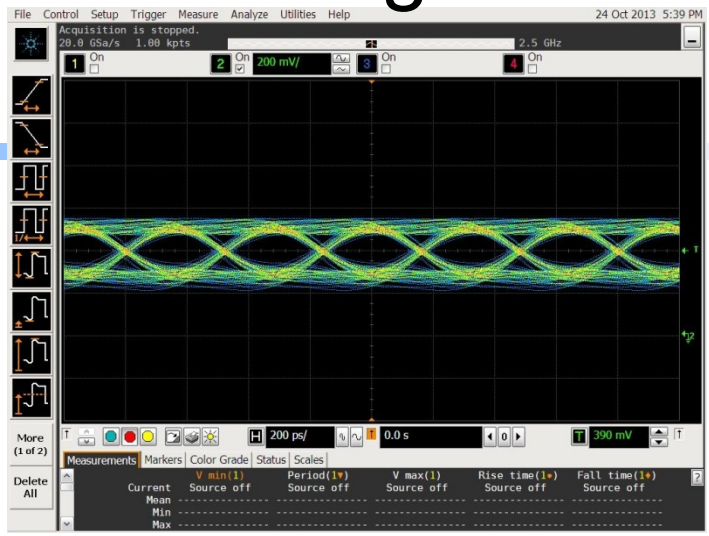
Switching System



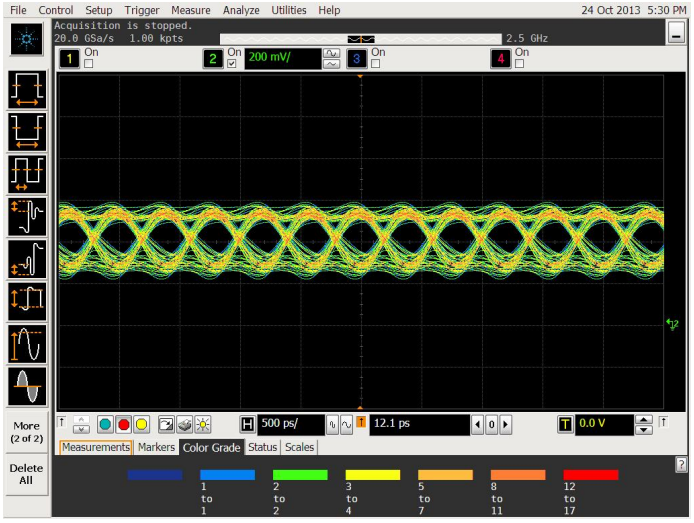
High Speed Interface Testing



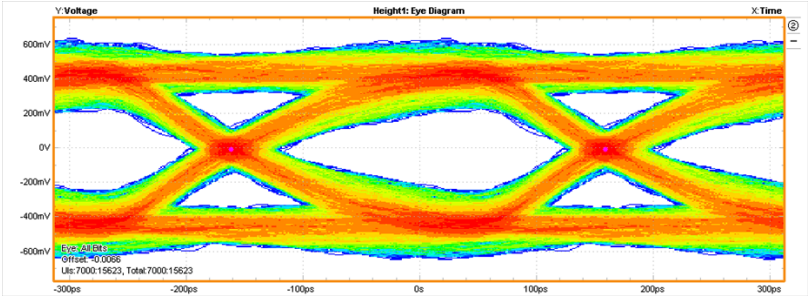
1.25Gbps



3.125Gbps



2.5Gbps



5Gbps

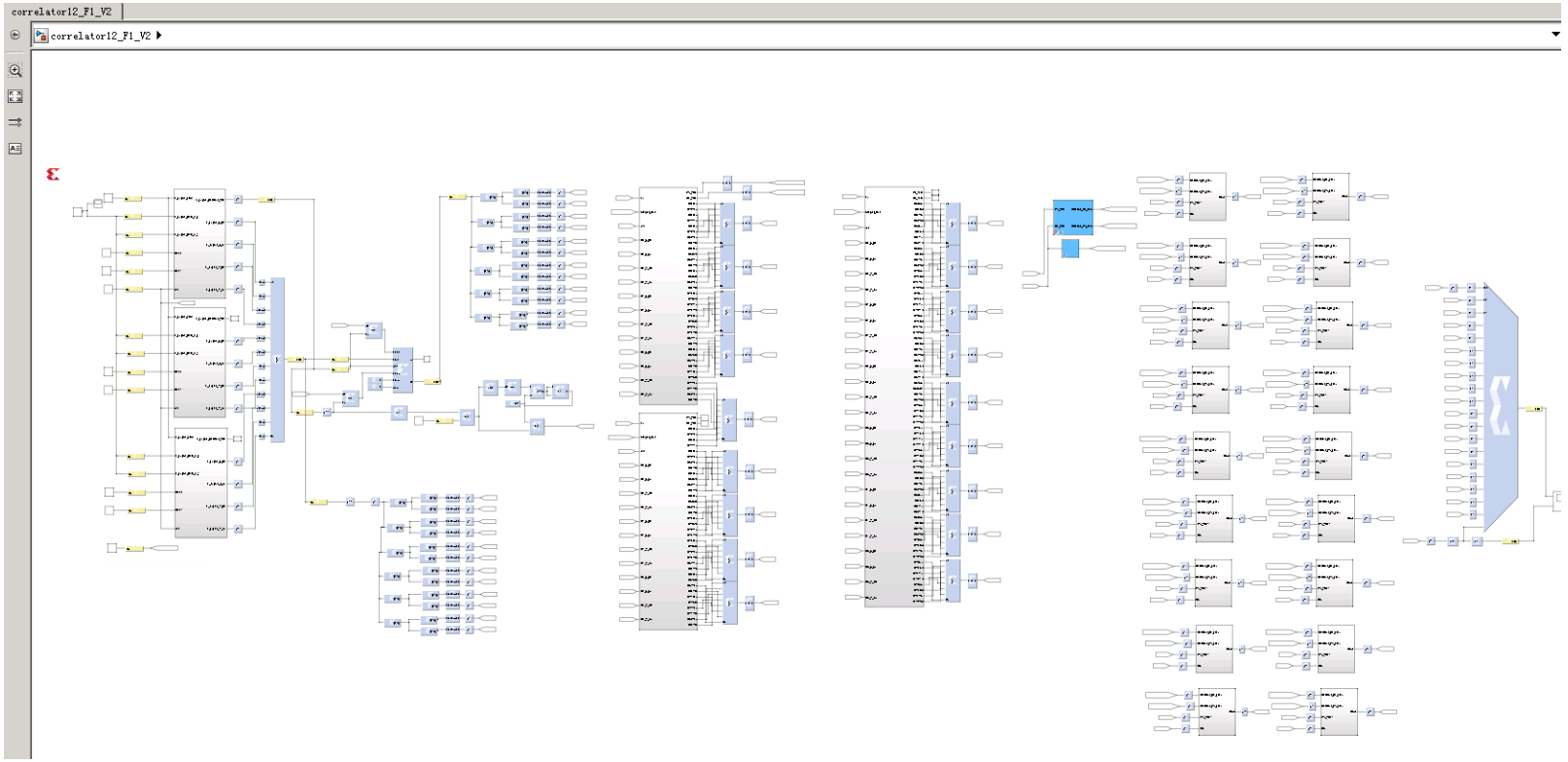
Data storage

- SATA Array+10G Ethernet card
- parallel processing
- >3.2Gbps

Algorithm Design

- Algorithm on FPGA
- Algorithm on DSP
- Interface program
- Switch schedule

Based on Simulink Development Environment



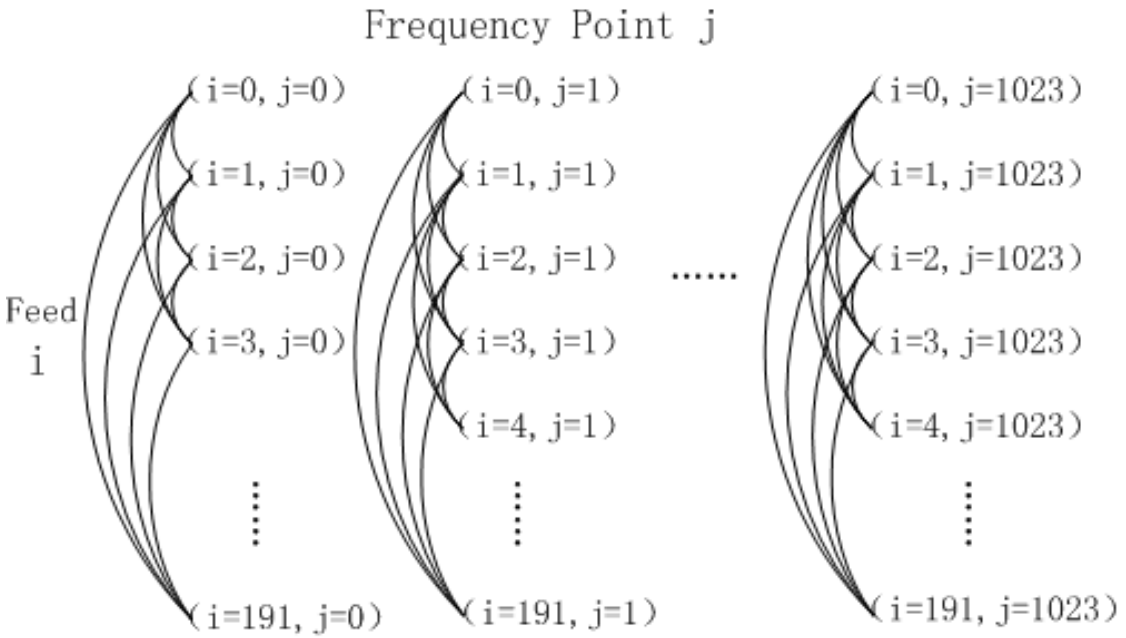
ADC PFB FFT Correlator

Correlation

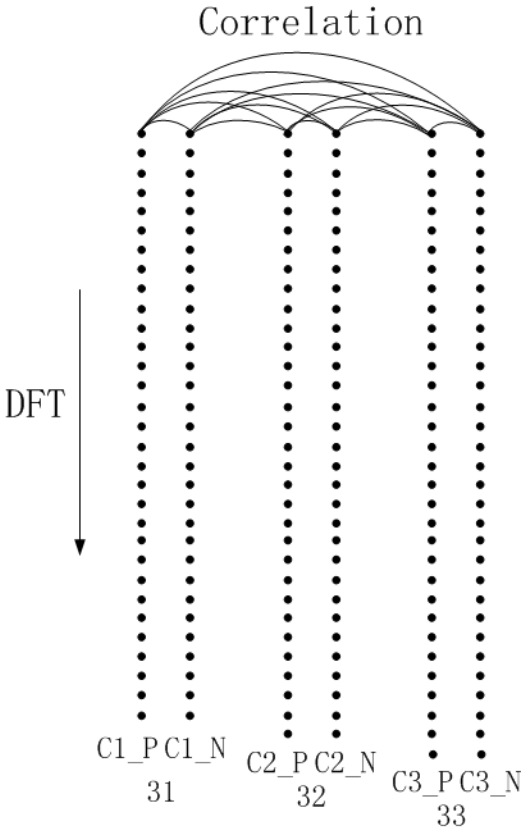
The Fourier domain cross-correlation is：

$$\widetilde{V}(k,k') = \langle \widetilde{f}(k)\widetilde{f}^{*}(k') \rangle$$

Plan A:Full Correlation



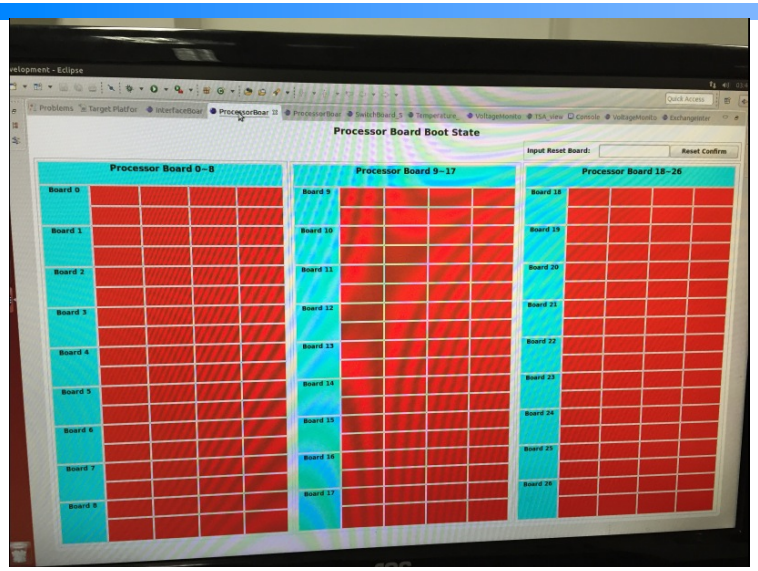
Plan B:1D DFT correlation

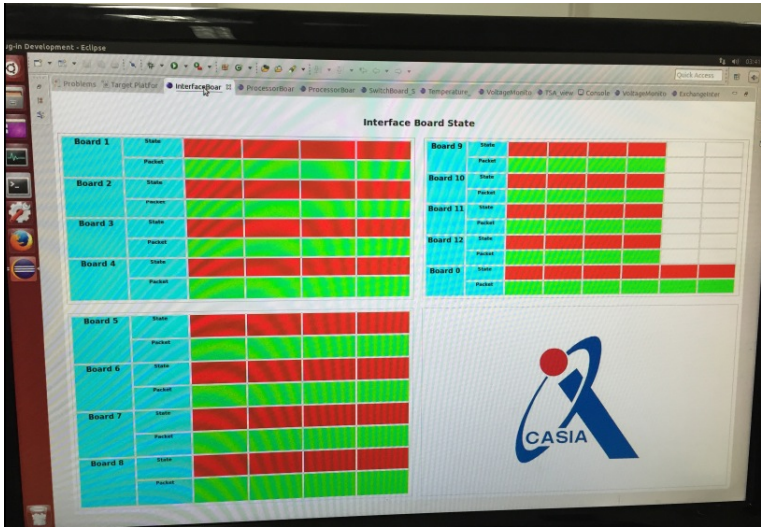


System Control software

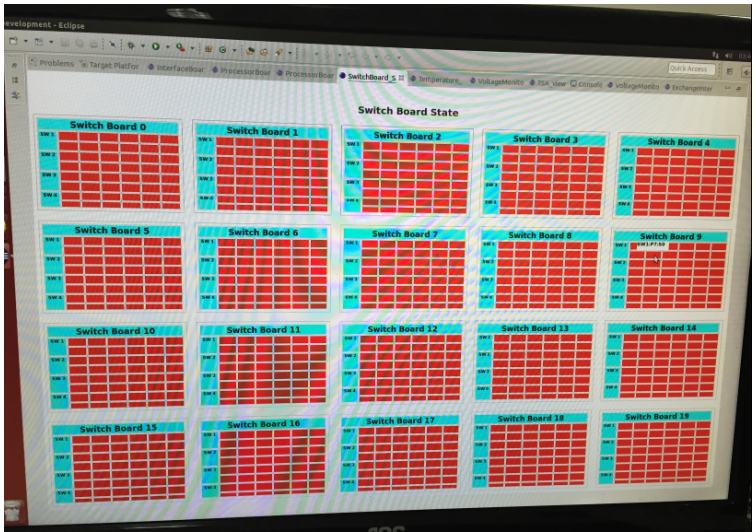
- System bootload
  - ✓ Flash
  - ✓ Ethernet
- Control instruction
  - ✓ System/Algorithm parameter
  - ✓ Control word format
- Information Display(Eclipse)
  - ✓ Original AD data display
  - ✓ Board information collection
  - ✓ High speed interface information display
  - ✓ Board temperature information display
  - ✓ Power voltage and Current information display
- Remote Control

Control and Display Interface



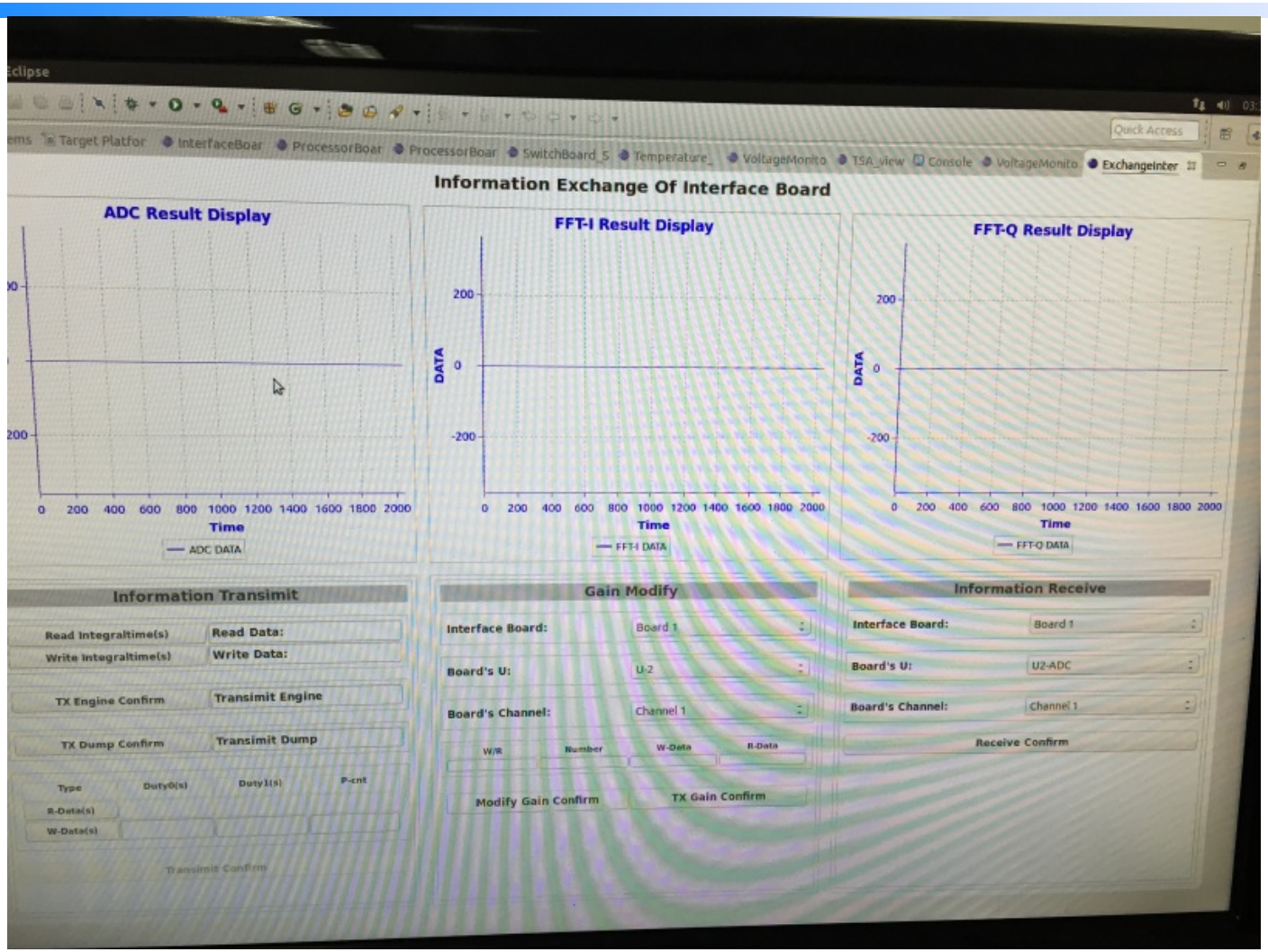


System bootload control



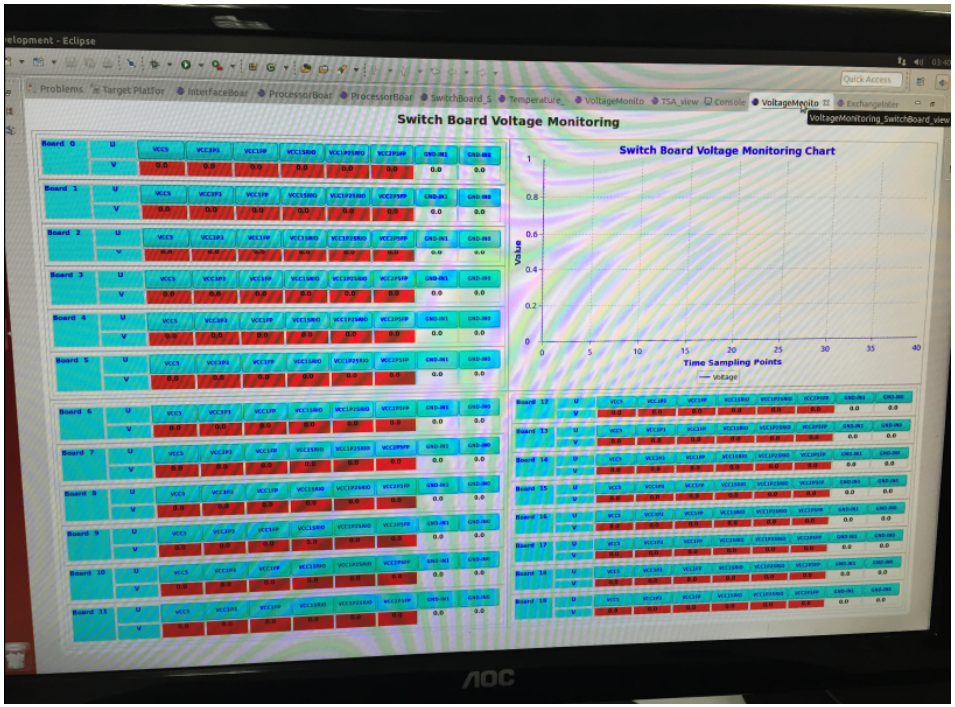
High speed Interface Information

Control and Display Interface

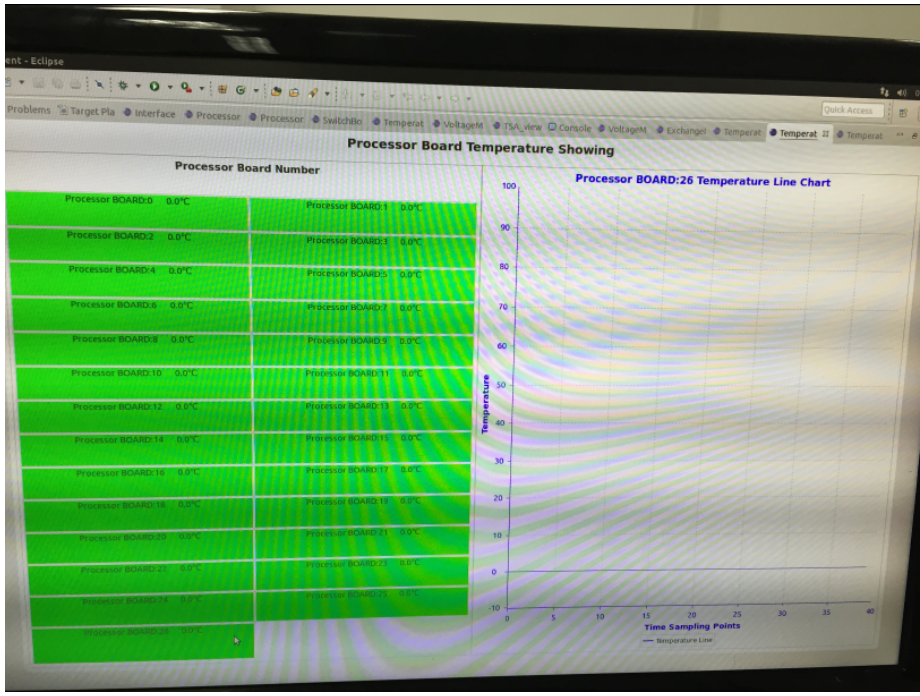


Original AD data display

Control and Display Interface



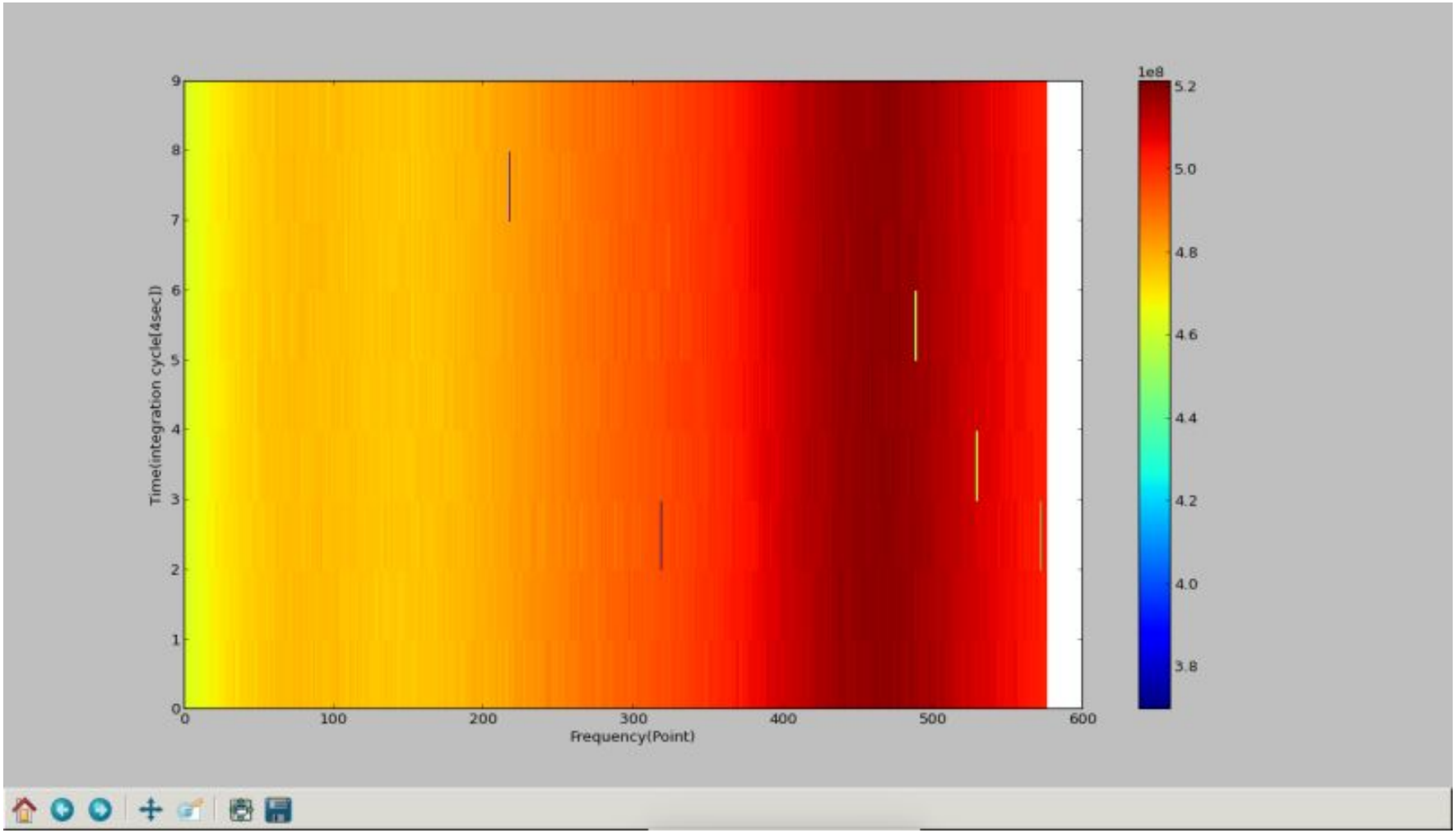
Power voltage and Current information



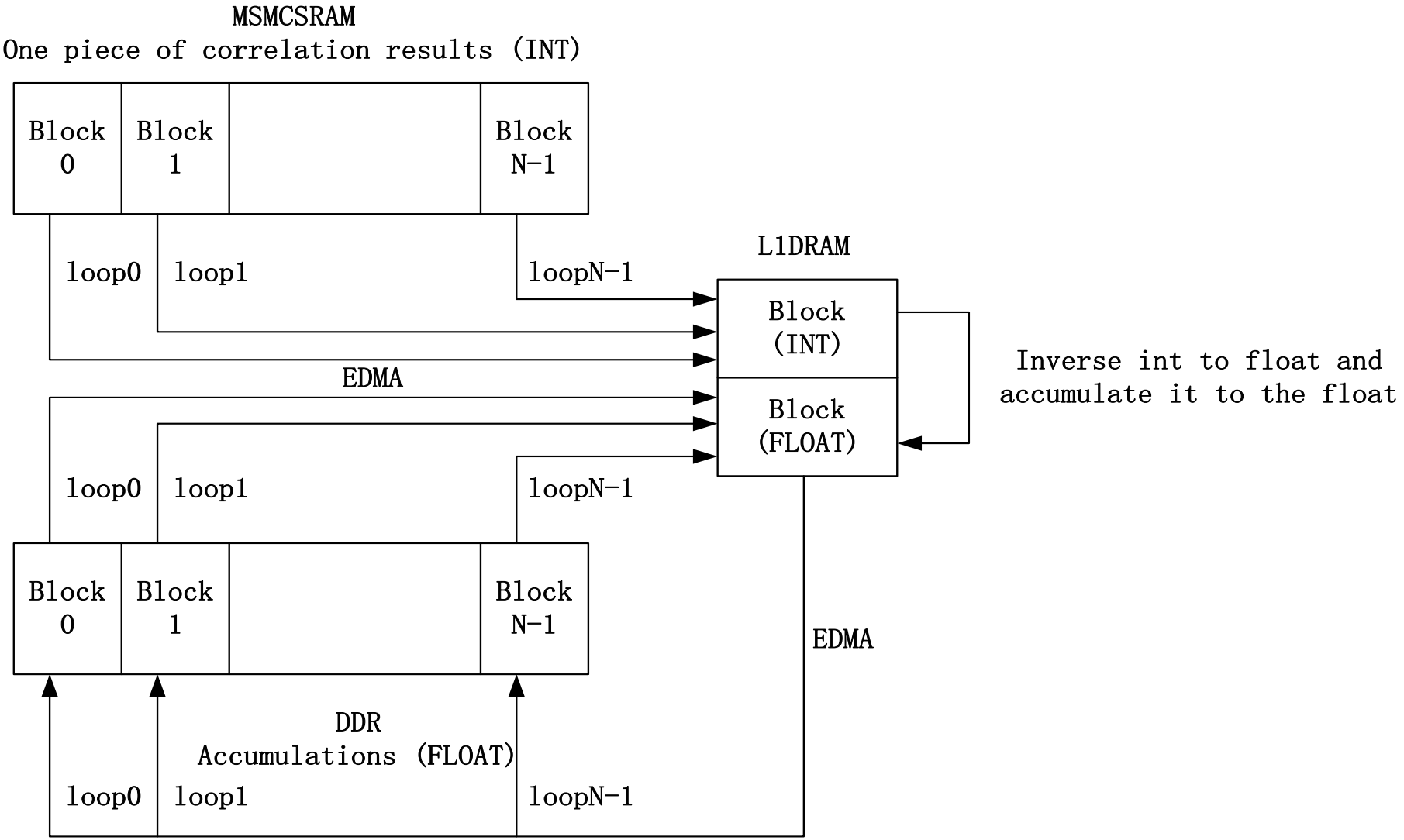
Board temperature information

Questions and Solutions

"Noise"



How does it work?



accumulation

How did that happen

Since we use the EDMA for the data transfer, it's not controlled by the cores. If the data in loop n flushed in before the results moved out in loop n-1, the final results in loop n-1 could be covered by the data in loop n, resulting in the “Noises”.

Solution

In order to avoid this, we control the time gaps between the loops next to each other by inserting a proper time delay.

Thank You!