Central Trigger Board
Design Report

Draft 0.1

Nuno Barros, Shannon Glavin, Joshua Klein, David Rivera, Rick van Berg
University of Pennsylvania

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Abstract

The Central Trigger Board (CTB) was originally designed to serve as the master trigger and for readout of the muon counters for the DUNE 35 t prototype, where it was also known as Penn Trigger Board (PTB). While some of its characteristics were driven by the specific design of the prototype, most of the features were designed in order to make the board sufficiently generic so that it could be used in other applications. In this document a description of the board, its capabilities and plans for integration into the ProtoDUNE DAQ are presented.

Chapter 1

Conceptual Design

1.1 Introduction

The current CTB design implements both the readout of the CRT and the master trigger of DUNE 35 t prototype. In this chapter the current design of the board is presented. At the end of the chapter a short discussion is done about possible modifications for its application to ProtoDUNE.

The included schematics are a top-down view of the PTB which is subdivided into two main parts, (1) the FPGA including all I/Os and (2) everything else including the power and all peripherals.

The MicroZed plugs in at the top of the board on the two MicroHeader connectors as seen on Figure 1.1. Each MicroHeader connector has 100 connection pins, but not all of them are routed. These pins provide connection to 115 single-ended PL I/Os, 8 PS GPIO, six dedicated analog inputs and four dedicated analog signals. The JTAG and the PS-GPIO are used in exclusivity mode between the MicroZed and the PTB mainboard. The PS-GPIOs are used to configure and run the self-test module. The routed inputs and outputs are shown in page 5 of the schematics[1].

1.2 Inputs and Outputs

The MicroZed FPGA is configured to use LVCMOS3v3 for the internal logic; therefore, to interface between the different inputs and outputs the PTB houses the following logic conversions:

- ECL → TTL (see page 28 in the schematics)
- TTL → LVCMOS3V3 (see page 28 in the schematics)
- NIM ⟷ LVCMOS3V3 (see pages 10 and 14 in the schematics)

The cosmic ray tracker (CRT) for the DUNE 35 t prototype consists of scintillator paddles located on all sides of the cryostat and were used primarily to detect cosmics. The counters were divided into two groups: TSUs consisted of panels located on the sides of the cryostat and were noisier, and therefore an initial coicidence of two superimposing counters was performed to validate a signal. BSUs were counters located on top of the cryostat and, being less noisy,each counter was independently router to the FPGA. The counters (both BSUs and TSUs) are connected via 50 pin connectors in the back of the PTB. Signals from the counters enter the PTB as differential ECL pulses and are converted to LVCMOS3V3 in two stages (ECL → TTL and then TTL → LVCMOS3V3). For the TSU counters only, the TTL signals are ANDed in pairs to reduce triggers from noise[2] prior to being converted to LVCMOS3V3 (see page 19 in the schematics).

[1] Note: In the schematics, connector JX1 corresponds to the white MicroZed connector on the right while JX2 is the connector on the left.

[2] Note: this noise was an artifact of the 35 t counters that were salvaged from the CDF detector and not of the electronics

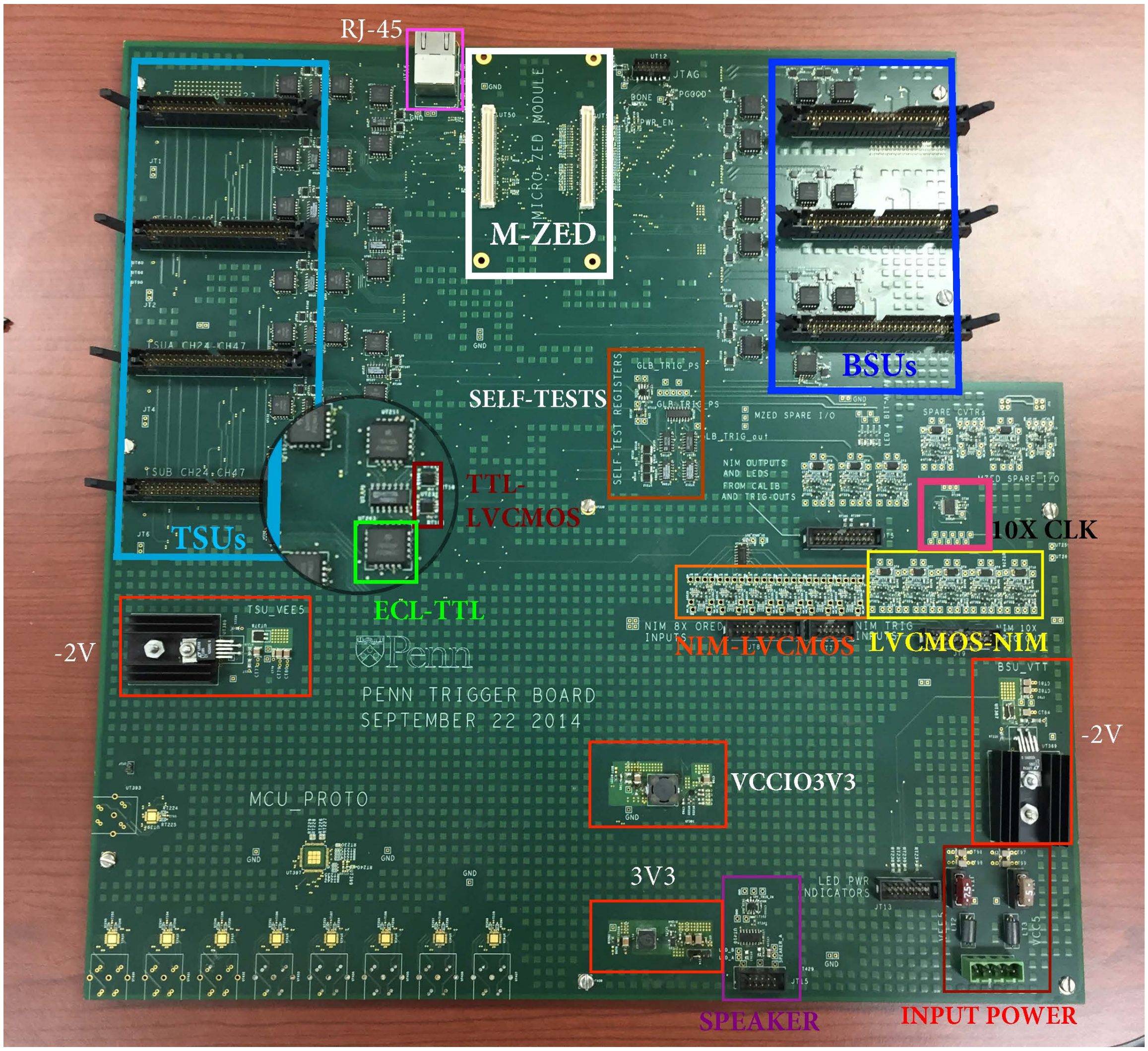


Figure 1.1: Top view of the Penn Trigger Board (PTB).

Figure 1.2: Back view of the PTB box. The white connectors are the BSU and TSU inputs.

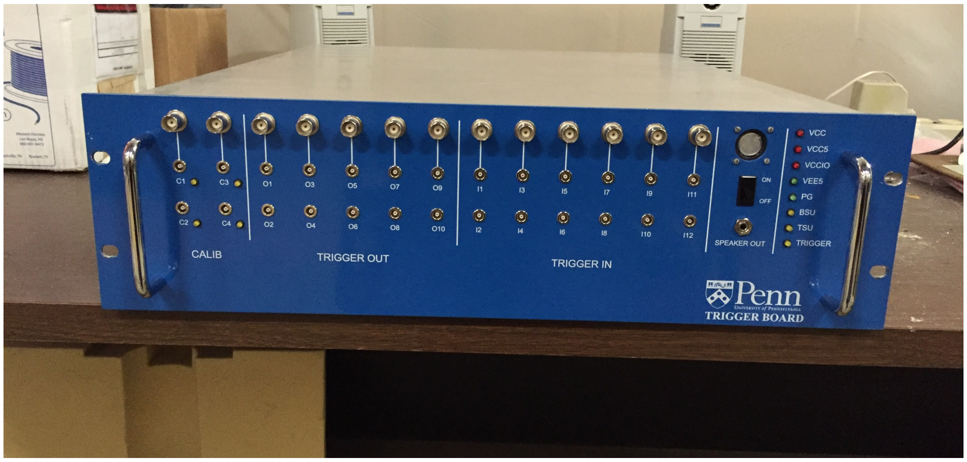


Figure 1.3: Front view of the PTB box. From left to right: Calibration inputs, trigger outputs, trigger inputs, speaker and speaker jack, LED power/signal indicators. Half of the LEMO connectors are also wired to a BNC connector, for ease of use with a scope.

The DATA OUT jack connects to the MicroZed Ethernet port, and the TIMING input connects to an onboard RJ-45 connector. The 35-ton prototype utilizes a NOvA Timing Distribution Module (TDM) to synchronize the different systems in time. The PTB connects directly to the TDM via the RJ-45 connector visible at the top of figure 1.1. A transceiver is used to convert the Low-Voltage Differential Signals (LVDS) from the RJ-45 to single ended LVCMOS3V3 signals into the MicroZed. The timing input (see page 6 of the schematics) includes a 32 MHz clock (TIMINGCLOCKIN), a command line (TIMINGCOMMANDIN), and a sync pulse (TIMINGSYNCIN). The fourth differential signal on the ethernet connection to the timing module is the TIMINGSYNCECHOOUT output of the PTB that echoes the sync pulse back to the TDM and is used to perform propagation delay correction.

There are a total of 50 signal inputs through the BSU ribbon cable connectors on the back plate of the PTB box, all differential ECL signals. Each is routed independently to a MicroZed I/O after the logic conversion to LVCMOS3V3. There are a total of 96 signal inputs through the TSU ribbon cable connectors. However, as mentioned above, these are anded in pairs which means that, effectively, there is a total of 98 independent signals (BSUs and TSUs combined) being routed to the MicroZed.

Local triggers from the external subsystems (RCEs and the SSPs) enter the PTB via the LEMO connectors in the TRIGGER IN section on the front panel and the triggers from the PTB to all the other systems leave via the connectors in the TRIGGER OUT section. These connectors use NIM logic. Additionally, the PTB implements 4 independent calibration channels which were used to drive different calibration systems (LED pulser, charge injection). Each of these channels uses NIM logic.

Trigger inputs I1-I8 are ORed into a single line (see page 13 of the schematics). The remaining NIM inputs are converted directly to LVCMOS3V3 and are inputs to the MicroZed.

The 10X Clock is used to produce 10 copies of a trigger signal generated in the MicroZed (see page 12 in the schematics). The 10 signals are then converted to NIM logic and used to trigger the other subsystems via the Trigger Outs (O1-O10 in figure 1.3).

1.3 Power and Other

The PTB utilizes +5V and -5V to produce all additional needed voltages which include 3.3V for use with LVCMOS and -2V for use with ECL. The two power supplies used are secured to the bottom of the PTB box. Following Fermilab regulations, the input power lines each include fuses

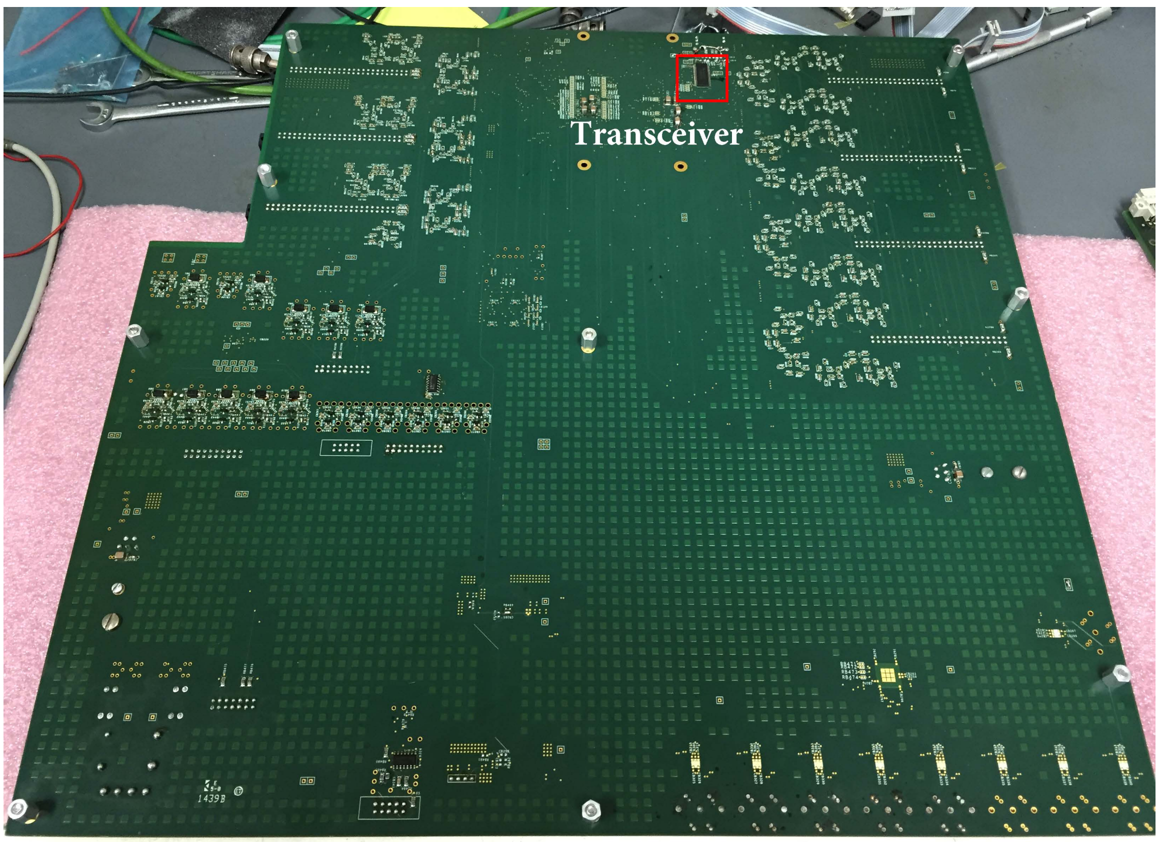


Figure 1.4: Bottom of PTB.

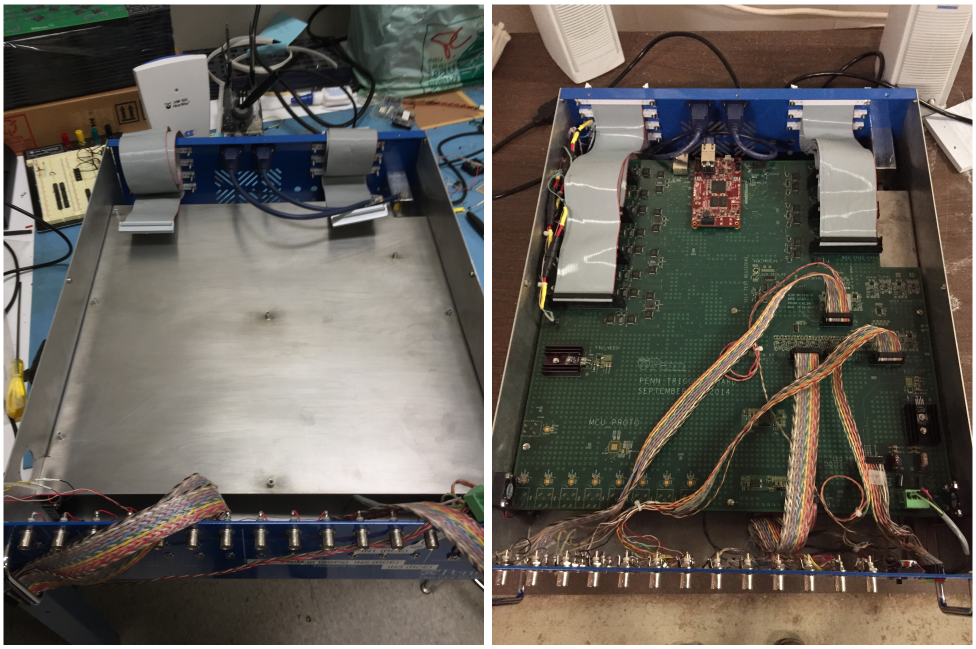


Figure 1.5: The Penn Trigger Board inside its box.

to protect against current overdraw. The board itself is screwed onto a thick metal platform that is bolted to the box supplies and serves as the local ground (see figure 1.5).

The board produces two independent 3.3V lines i.e. VCC3V3 and VCCIO3V3 (see figure 1.1 and page 2 of the schematics). The latter is used for the bank voltages of the MicroZed and has to be turned on after the MicroZed is fully powered. This is achieved by controlling the enable line of the voltage regulator(VCCIO_EN) (see pages 21 and 23 in the schematics) with the MicroZed. The MicroZed itself powers on from the +5V rail.

The portion of the board labeled MCU_Proto is for a different project that makes use of the MicroZed and is independent of the PTB. The PTB is made considerably smaller with the exclusion of the second project.

Four fans are located near the front of the PTB box, close to the power circuits (two on each end side: one sitting above the board platform and one below, see figure 1.5). The slits in the back plate of the box allow for air circulation.

The speaker located on the front plate of the PTB box produces a click when there is a trigger. Sound can be transmitted via an audio cable as well.

1.4 Data Format

In the present implementation of the firmware, the CTB constructs two types of data units that are passed down to the DAQ software.

1.4.1 Counter Words

The counter words are a snapshot of the CRT state. These words have a 32 bit *header* with a 3 bit word type ID, followed by a 27 bit timestamp rollover, composed of the 27 least significant bits of the timestamp. The *body* of the word is composed by 98 status bits, each representing the state of each muon counter. These words are produced every time a counter becomes asserted and represent the vast majority of the data produced by CTB. In DUNE 35 t, these represented an event rate of about 15 kHz.

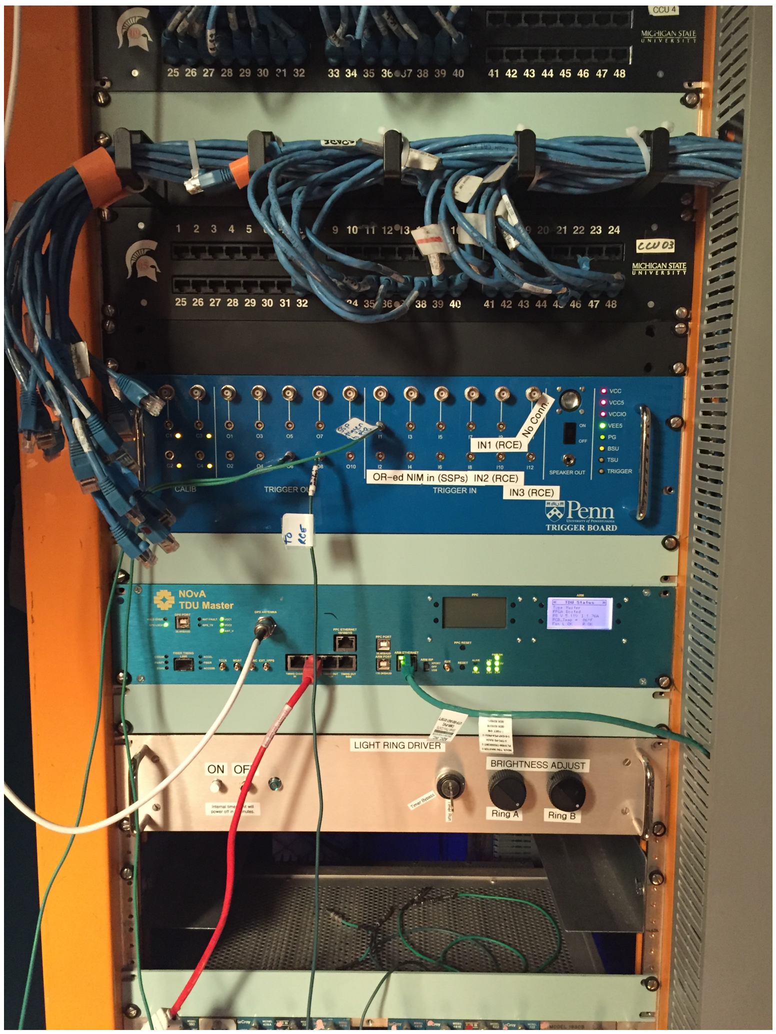


Figure 1.6: PTB in the 35 ton rack at PC4.

1.4.2 Event Words

The event words were smaller in size but more complex in structure. These contained the same 32 bit header but the body composed of a single 32 bit word, where the meaning of each bit depended on the type of word. The different types of event words were distinguished by the 3 most significant bits of the header.

Examples of event words are:

- Trigger words. Produced every time a global trigger was obtained (internal - CRT - or external).
- Calibration words. Produced every time one of the calibration channels was fired.
- Self test words. Produced every time a self test signal was generated.

1.4.3 Timestamp words

Timestamp words were generated periodically and sent downstream to the DAQ regardless of the existence of other data. These words were composed by a 32 bit header like all other words, followed by the full 64-bit timestamp.

The period these words were generated was configurable and dictated the frequency ethernet packets were generated. Each ethernet packet had only one of these words and the word itself marked the end of the packet. Since the headers contained only a 27 bit rollover of the full timestamp, the largest time between timestamp words was $(2^{28} - 1)$ clock ticks (in the case of the NOvA clock this meant about 8 s), but the time interval was usually kept in the order of 1 millisecond.

A simplified diagram of an ethernet packet sent downstream to the DAQ software is shown in figure 1.7.

1.5 Software

The CTB runs a stripped down linux distribution (Arch linux) on its dual-core ARM processor. This means that simple tasks can be performed at the software level, and multiple ethernet sockets can be created to have multiple clients to connect into it. This is particularly useful if, for instance, one would have a separate machine responsible for collecting data and/or trigger statistics for monitoring purposes.

However, the board only contains one physical ethernet interface, which means that despite being able to establish multiple dedicated connections, all these connections have to be inside the same subnet.

Another advantage of running a linux distribution is that the FPGA can be reprogrammed without physical presence. For this purpose, the board also runs a SSH server.

In its present configuration, the CTB software is composed of two parts: a server application that runs in the board and communicates with the hardware; and a client *BoardReader* process, which provides the link between the CTB and the DAQ software. The CTB is already integrated with artdaq, requiring only minimal changes to accommodate any differences in the data format.

The server application makes use of the dual core ARM processor in the MicroZed and implements different working threads that are responsible for the command parsing and execution, data collection and subsequent construction and shipping of the ethernet packet, and also collection of data statistics for monitoring purposes.

The *BoardReader* was originally implemented for the DUNE 35 t prototype and is responsible to read in a fhicl fragment which configures the board, including trigger patterns, trigger gates, prescales, client IPs (where to send the data and where to send monitoring statistics), calibration pulses, channel masks, amongst other information. Internally this configuration is converted into an XML string which is then transmitted to the server application through the control ethernet socket which then configures the hardware and opens the necessary ethernet connections. The

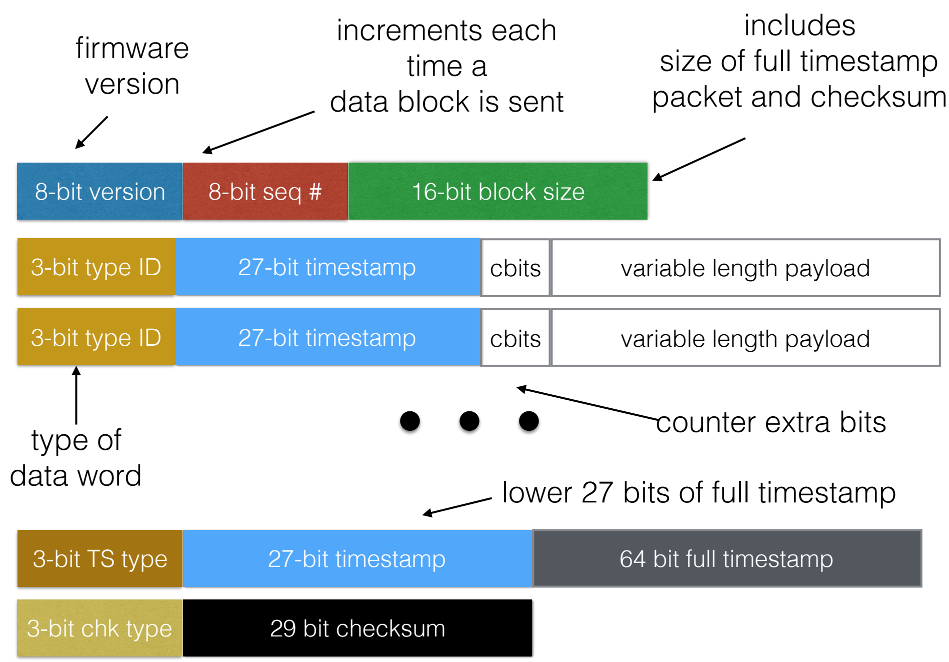


Figure 1.7: Ethernet packet structure in the CTB.

choice of an XML fragment was to minimize the performance penalty and reduce the amount of software dependencies.

The communication between the CTB server and the BoardReader (and any other clients, such as the monitoring client) is performed through TCP socket connections, which has the advantage of ensuring the order of the packets and has already embedded error checking. Currently the CTB has three socket connections in place:

- a control connection, where configuration and artdaq commands are passed, such as start and stop run, and soft and hard resets;
- a data connection where the CTB data is pushed downstream.
- a monitoring connection, where data statistics are pushed downstream. These data statistics included trigger and clock counters, individual muon counters and number of ethernet packets sent.

A schematic of the current software interface is shown in figure 1.8.

1.6 Modifications

All the trigger decisions are encoded in the FPGA, in which case the mainboard is responsible mostly for the logic conversion. This implies that several hardware changes might become necessary to accommodate the new interface requirements. In the present implementation of the board, most of the I/O is performed with differential ECL through a series of 50-pin ribbon cables. However, this is not a signal logic that is very commonly used and there isn't any system at the moment in ProtoDUNE that is planning to have this I/O.

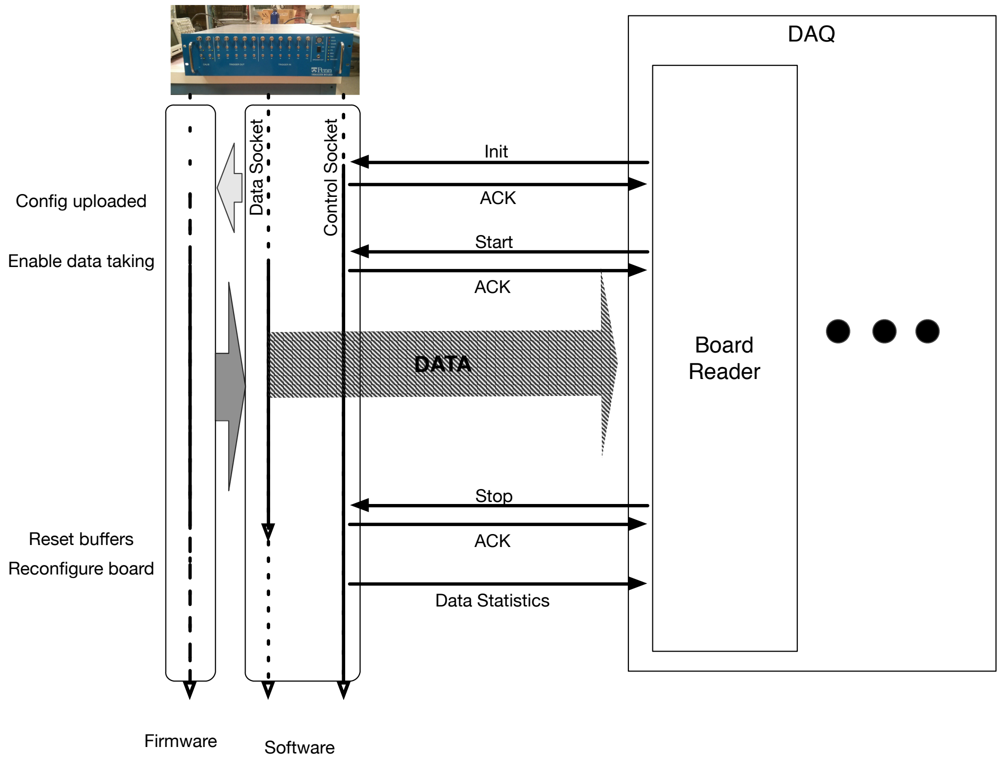


Figure 1.8: Software infrastructure of the CTB.

Internally the ECL I/O is converted to TTL, and later on to LVCMOS 3.3V. While these two are more common, it is unlikely that they will be used as inter-system communication logic.

A call for collecting the details of each interface will be initiated, after which a full assessment of the modifications will be performed. One major modification is that now the board will likely deal with two grounding domains. Although most of the inputs are on building ground, a possible connection to the PDS would be on detector ground.

Several options for ground isolation have been considered with the best candidates being discussed below.

1.6.1 Optical I/O

One of the favored options is to convert all (or most) of the I/O to optical fibers. This option has the advantage of automatically solving the grounding separation problem. However it is a more costly implementation, and requires a clear decision of the directionality of each port, since optical connectors are unidirectional. Since it is not foreseen that the trigger board will use all its I/O's, one can add contingency to the number of input (the vast majority) and output ports.

An additional point to take into account when considering the optical solution is that a standard for optical connections will have to be agreed between all the connecting subsystems. This discussion has not yet taken place, but it seems that 850 nm fibers are the favored solution.

1.6.2 Optical isolators

Another solution is to use optical isolators at all the I/O ports. These are usually a DIP consisting of a diode coupled with a photodiode, each one connecting to a different grounding domain. This option is significantly cheaper than the solution using optical fibers, but retains the same requirements since these isolators are also unidirectional.

Another disadvantage of this solution is that these optical couplers introduce a signal delay. Solutions have been found that introduced a delay of $\tilde{1}$ ns, which would most likely be acceptable.

1.7 Requirements for the DAQ software system

Given that the board is already integrated into artdaq through a *BoardReader*, there aren't any particular requirements on that front. Or rather, the requirements are that the software infrastructure is well defined beforehand to evaluate the extent of modifications that will be necessary to add to the BoardReader.

However, as most of the board is configurable through software by using configuration memory mapped registers, it is necessary to define these configurable parameters well in advance. Of these, the most relevant are the trigger conditions, since these are usually very specific of the use of the board. In the same way that the definition of the trigger conditions represents the majority of the changes to the firmware, so it will also represent the majority on the software side.

Chapter 2

Interfaces

The CTB requires interfaces to all the subsystems in order to construct the trigger decision. Additionally an interface to the DAQ software is necessary. As described in section 1.5, the CTB is already fully integrated into artdaq, which means that this part of the interface is virtually done, except for a couple of small changes tweaks that are specific to ProtoDUNE.

2.1 Interface to detector subsystems

The interfaces and its properties are currently still being collected, however there already a fair idea of the sources and number of channels that will be necessary. These interfaces are discussed below in more detail.

2.1.1 Timing System

Unlike in DUNE 35 t prototype, the CTB won't be connecting directly to each subsystem where triggers are needed. Instead, the CTB will pass a trigger primitive to the timing system, which will then be responsible for distributing the trigger command to the relevant subsystems.

The connection to the timing system will most likely consist of 3 or 4 channels using differential LVDS I/O. Two of these channels will implement a clock and a sync line, and the remaining 1 or 2 will implement a return which will carry the feedback from the CTB and the trigger primitives. A specific solution for the medium of this connection is still under consideration but one possible solution is to re-use the RJ-45 socket that was previously used for the NOvA timing system. This socket is already designed to carry 4 differential LVDS signals and is fully bidirectional.

2.1.2 Cosmic Ray Tracker

This subsystem will in principle pass onto the CTB the trigger status of its electronics. For this interface the CTB will most likely act both as a readout system (recording the status of each channel) and trigger system, constructing trigger primitives according the configured trigger conditions.

Although the logic and the details of such a system are not totally known, it is expected that 40 inputs will be required in the CTB to interface with the CRT system.

Since the CTB will also act as readout for this system, it is expected that recording of the channel status will take up most of the modest data volume produced by the CTB.

2.1.3 Beam Instrumentation

The details of the interface to this subsystem are still largely unknown. This will represent the primary source of triggers, since will provide information concerning the beam and therefore most of the beam induced events will be triggered by the information provided by this systems.

At the moment, it is expected that this subsystem will require about 10 input ports, which will then be used to generate triggers. Most likely, the CTB will record status changes from the inputs of this subsystem, but this has not yet been fully decided.

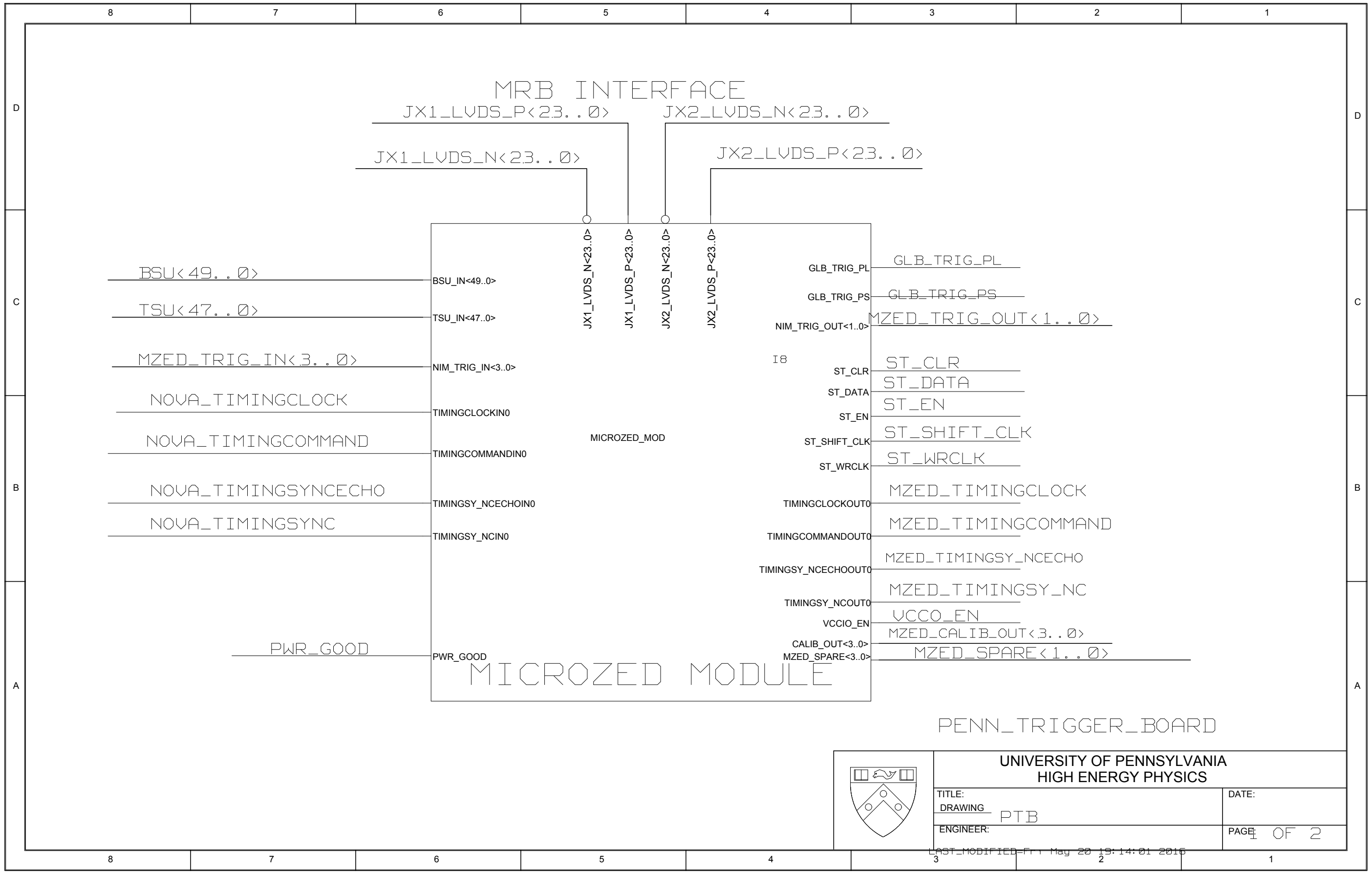
2.1.4 Photon Detection System

It is not yet clear whether the CTB will receive inputs from this interface, and so, how many. In DUNE 35 t, there were 8 inputs from the PDS (SSPs) through a coaxial cable with NIM logic. These inputs were logically OR-ed together to form a single PDS input that was then used to form a trigger. However, due to the large s.p.e. rate of the system, it's input was never used to form triggers during production data taking.

In ProtoDUNE it is still being considered whether this system will be providing inputs to the CTB, and how many. In any case the details of the inputs will most likely be different, as there seems to be a consensus to no longer use NIM logic.

Appendix A

CTB schematic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JX2_LVDS_P<23..0>
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TIMINGSY_NCECHOIN0
NOVA_TIMINGSYNC
TIMINGSY_NCIN0
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PWR_GOOD
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GLB_TRIG_PL
GLB_TRIG_PS
GLB_TRIG_PS
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ST_CLR
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ST_DATA
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ST_EN
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ST_SHIFT_CLK
ST_WRCLK
ST_WRCLK
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MZED_TIMINGCLOCK
TIMINGCOMMANDOUT0
MZED_TIMINGCOMMAND
TIMINGSY_NCECHOOUT0
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UNIVERSITY OF PENNSYLVANIA
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DRAWING
PTB
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ENGINEER:
PAGE 1 OF 2
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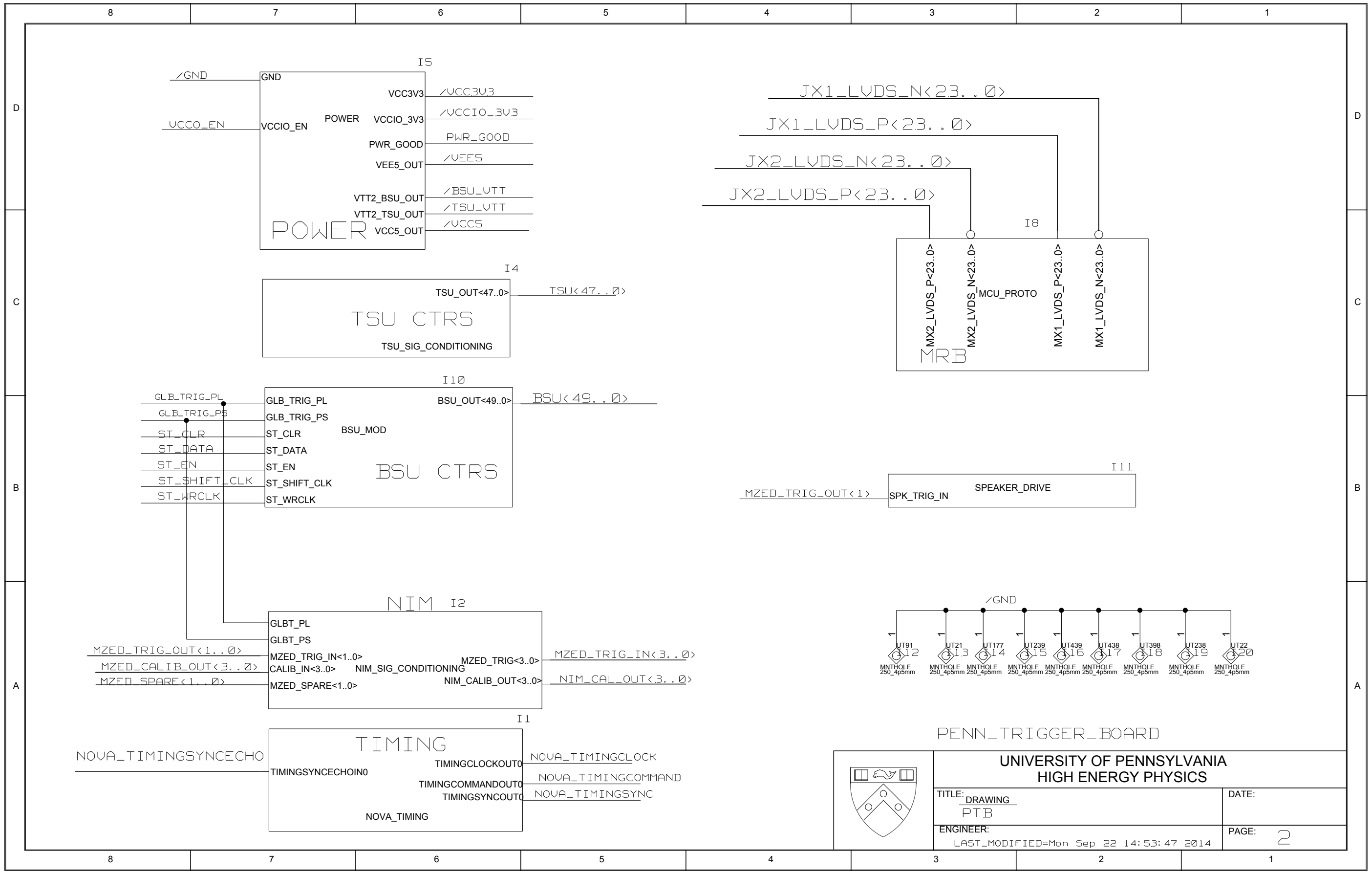

I5
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GND
VCCO_EN
VCCIO_EN
POWER
VCC3V3
/VCC3V3
VCCIO_3V3
/VCCIO_3V3
PWR_GOOD
PWR_GOOD
VEE5_OUT
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VTT2_BSU_OUT
/BSU_VTT
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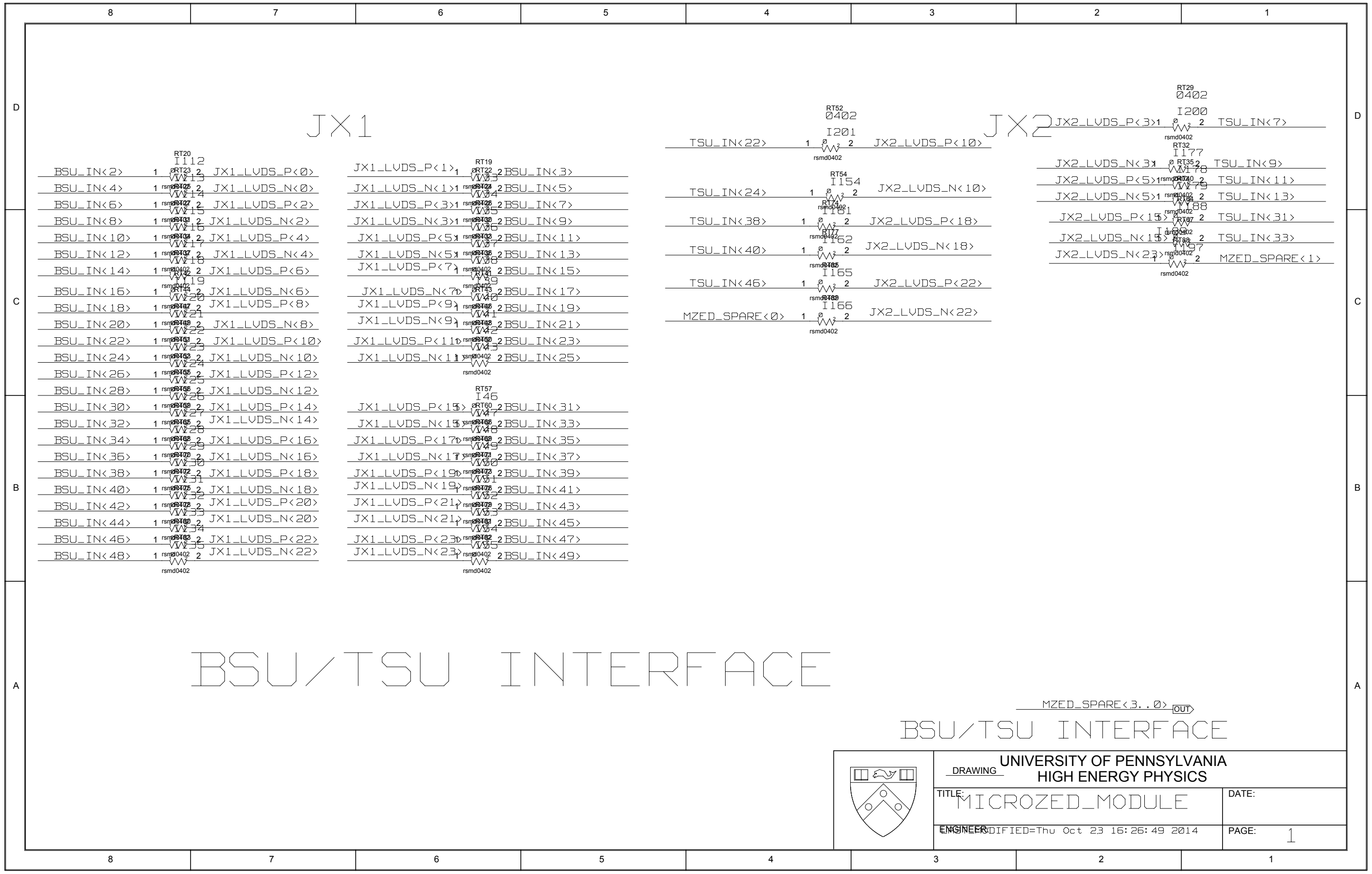
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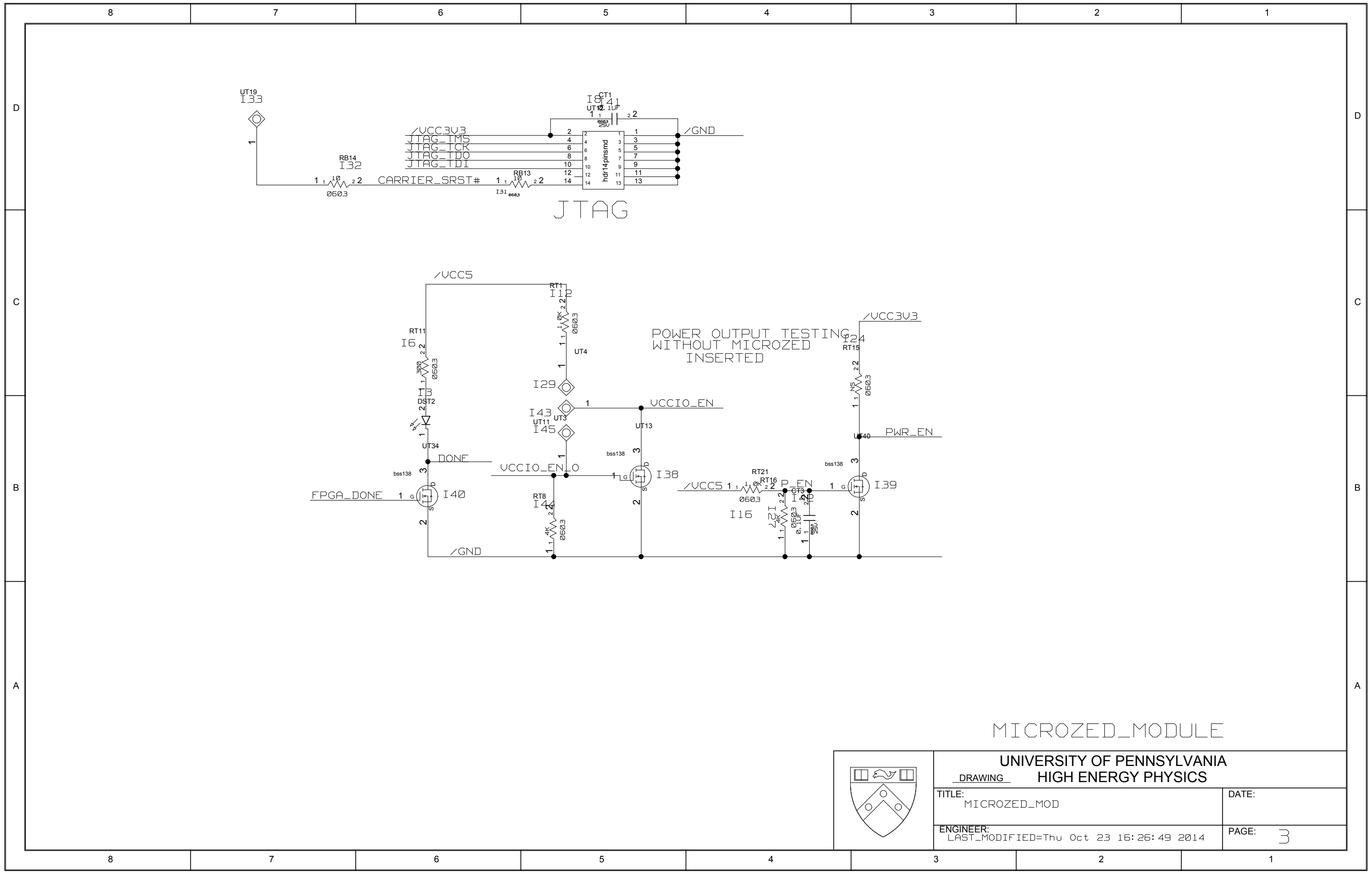
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WITHOUT MICROZED
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PWR_EN
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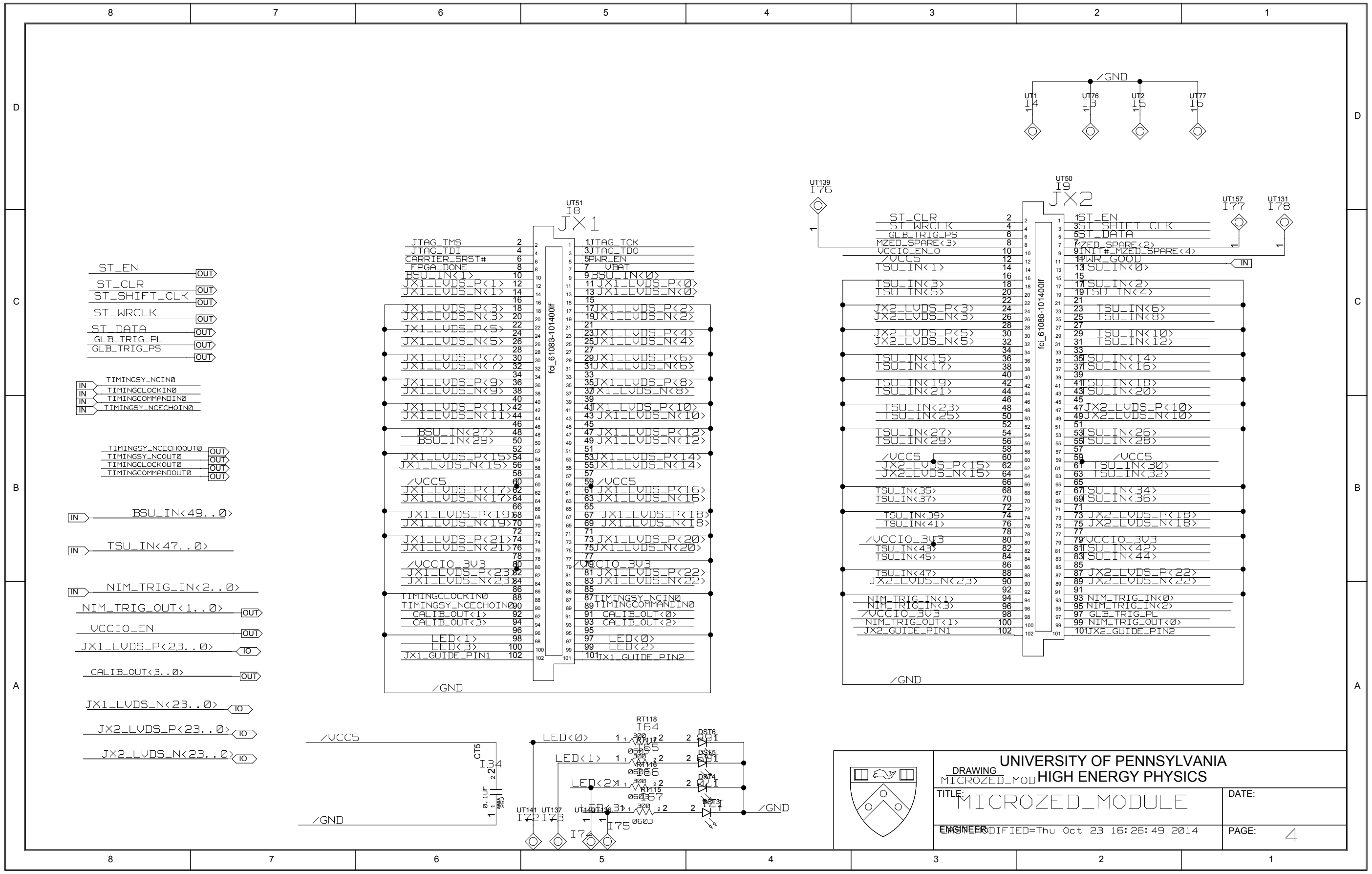
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ST_DATA
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GLB_TRIG_PS
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TIMINGCLOCKIN0
TIMINGCOMMANDIN0
TIMINGSY_NCECHOIN0
TIMINGSY_NCECHOOUT0
TIMINGSY_NCOUT0
TIMINGCLOCKOUT0
TIMINGCOMMANDOUT0
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TSU_IN<47..0>
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NIM_TRIG_OUT<1..0>
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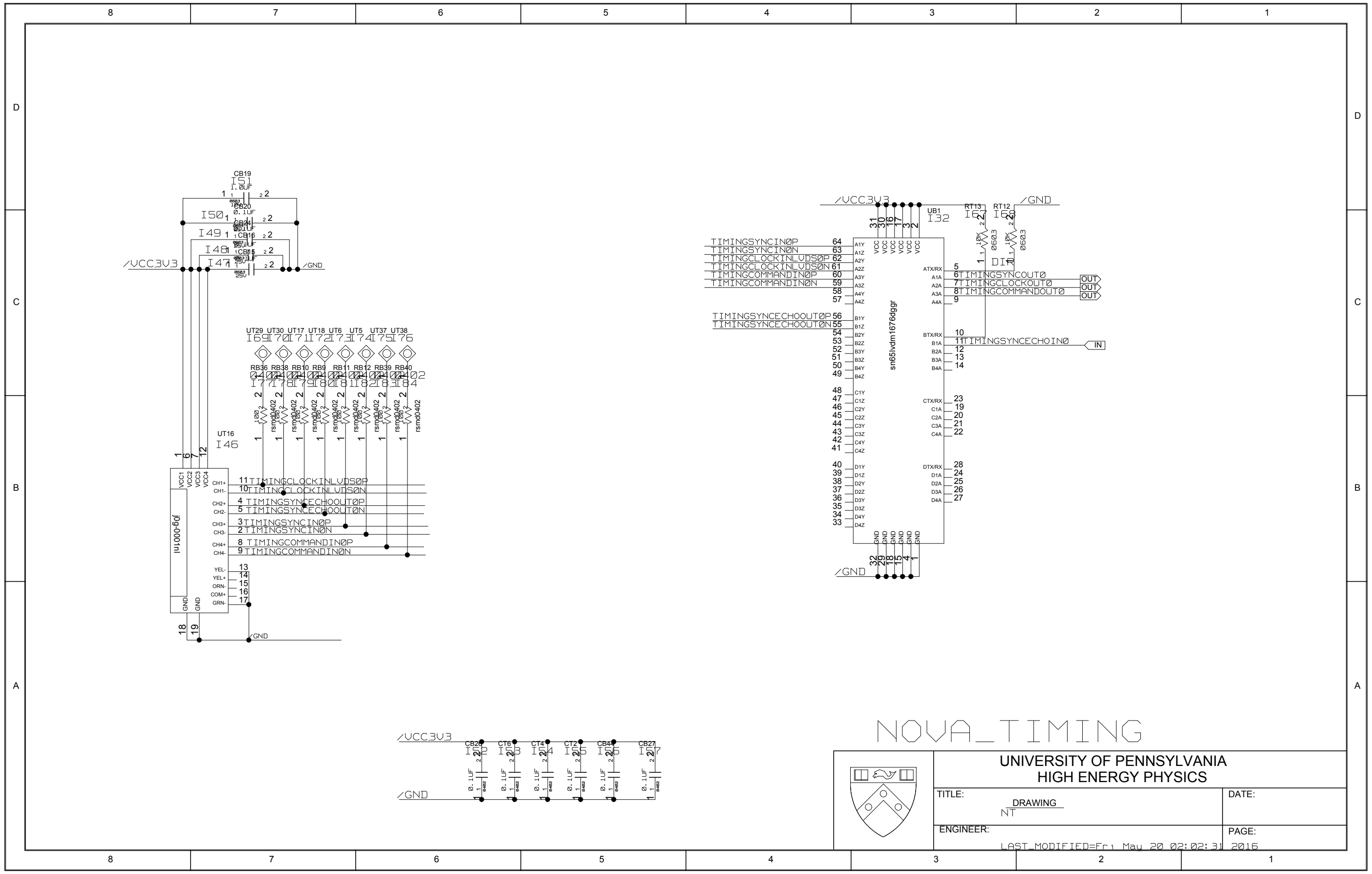
LED<3>



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TIMINGCLOCKINLVDS0N
TIMINGSYNCECHOOUT0P
TIMINGSYNCECHOOUT0N
TIMINGSYNCIN0P
TIMINGSYNCIN0N
TIMINGCOMMANDIN0P
TIMINGCOMMANDIN0N
UB1
I32
sn65lvdm1676dggr
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OUT
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NOVA_TIMING
UNIVERSITY OF PENNSYLVANIA
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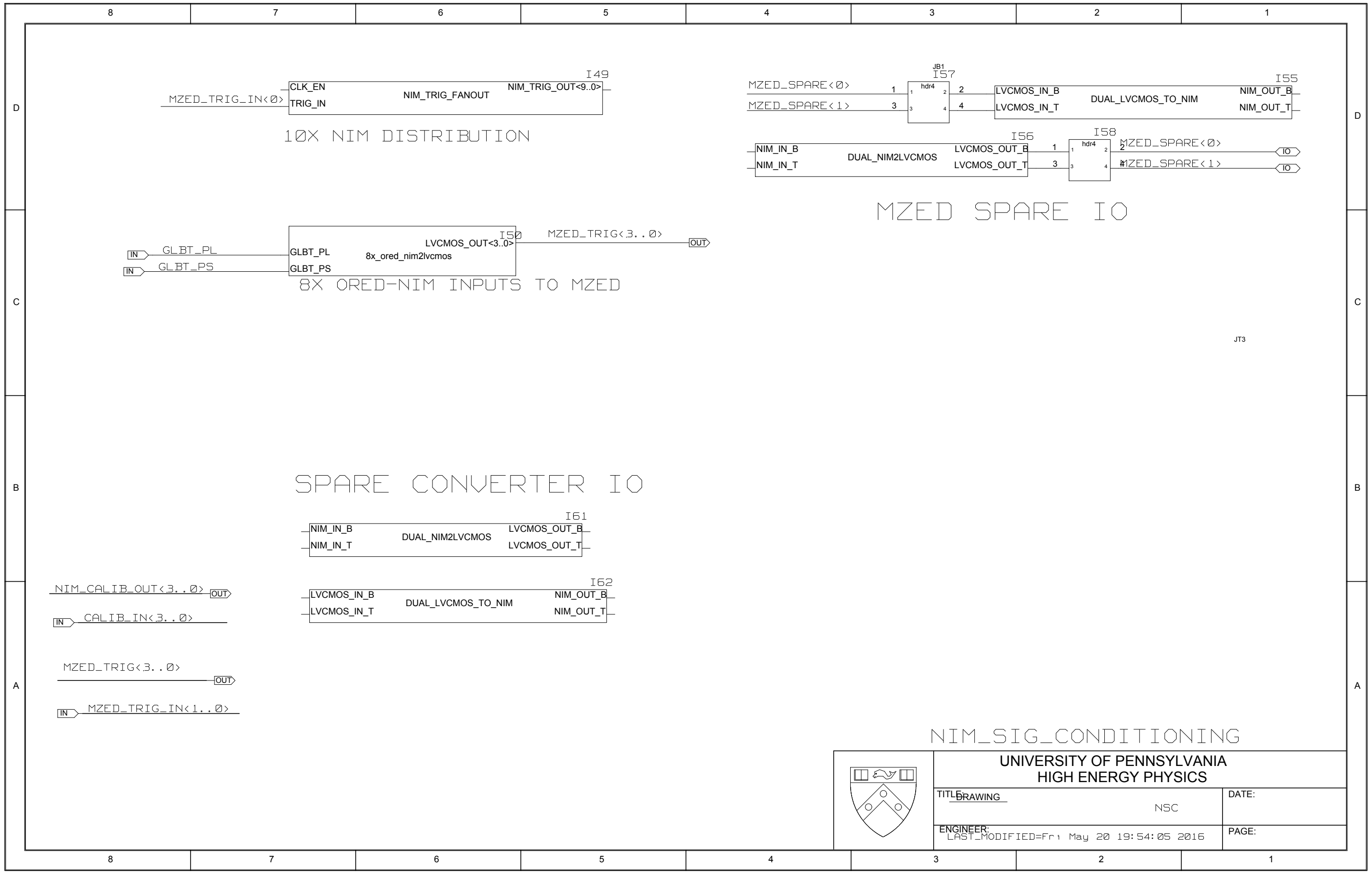
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GLBT_PL
GLBT_PS
LVCMOS_OUT<3..0>
8x_ored_nim2lvcmos
I50
MZED_TRIG<3..0>
OUT
8X ORED-NIM INPUTS TO MZED
MZED_SPARE<0>
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I57
hdr4
LVCMOS_IN_B
LVCMOS_IN_T
DUAL_LVCMOS_TO_NIM
NIM_OUT_B
NIM_OUT_T
I55
NIM_IN_B
NIM_IN_T
DUAL_NIM2LVCMOS
LVCMOS_OUT_B
LVCMOS_OUT_T
I56
I58
IO
MZED SPARE IO
JT3
SPARE CONVERTER IO
I61
I62
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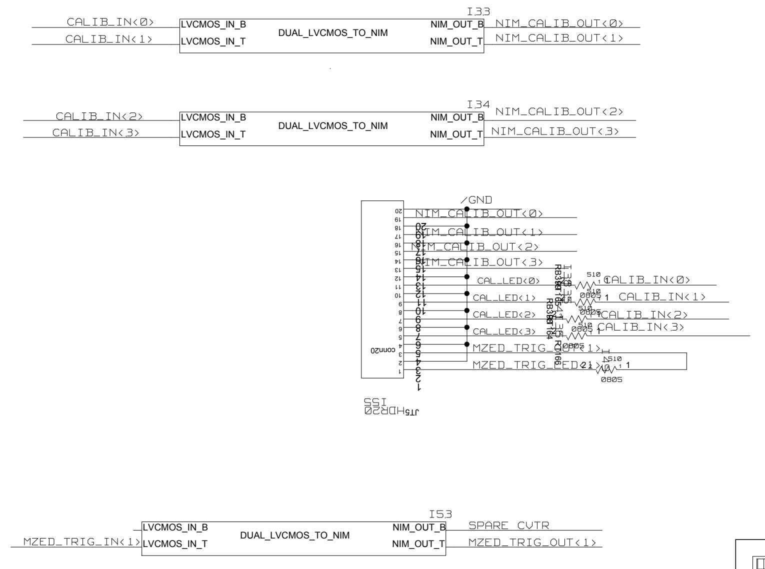
MZED CALIBRATION AND TRIG_OUT



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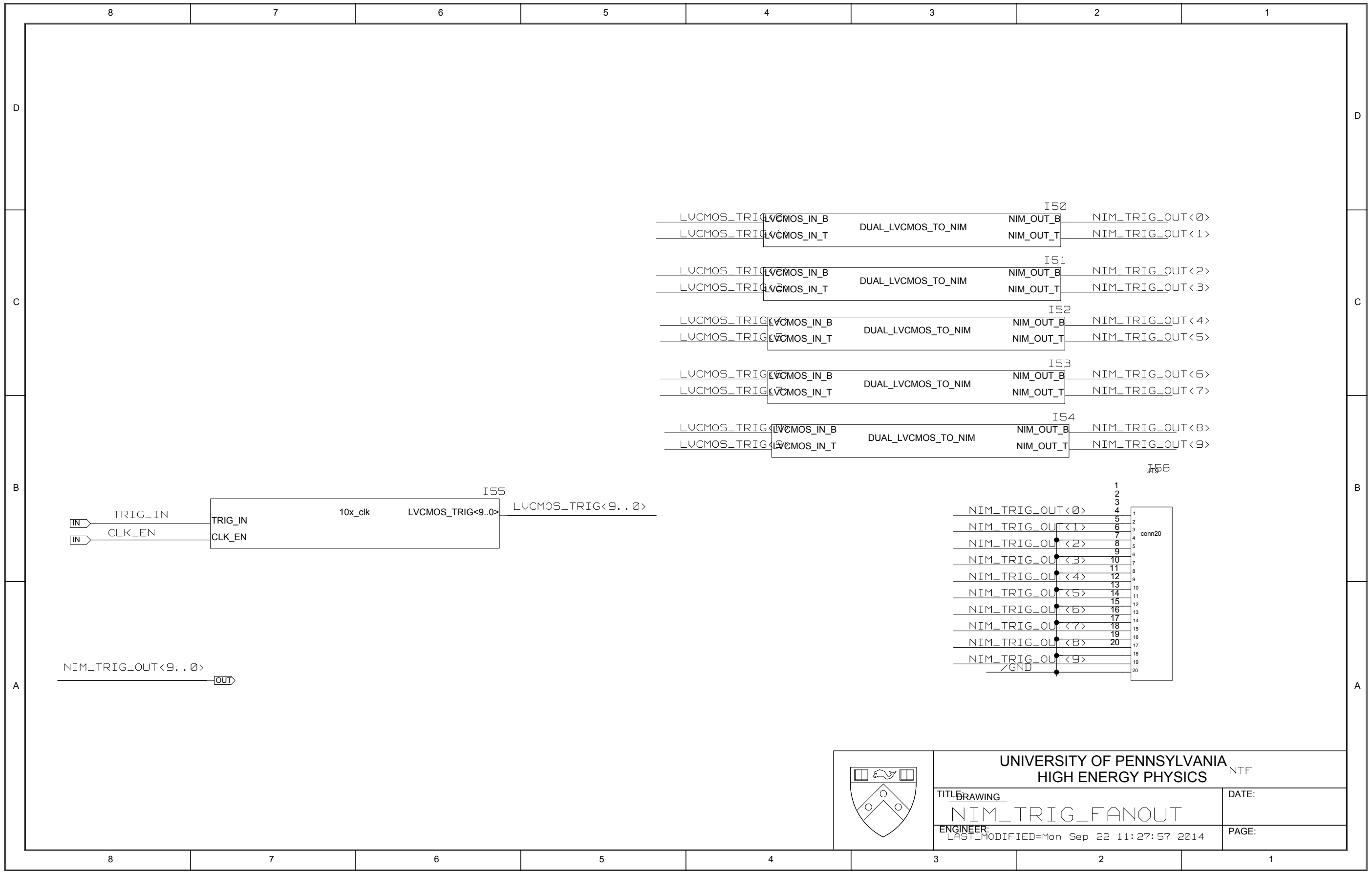
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LVCMOS_IN_B
LVCMOS_IN_T
NIM_OUT_B
NIM_OUT_T
I50
I51
I52
I53
I54
I55
I56
10x_clk
TRIG_IN
CLK_EN
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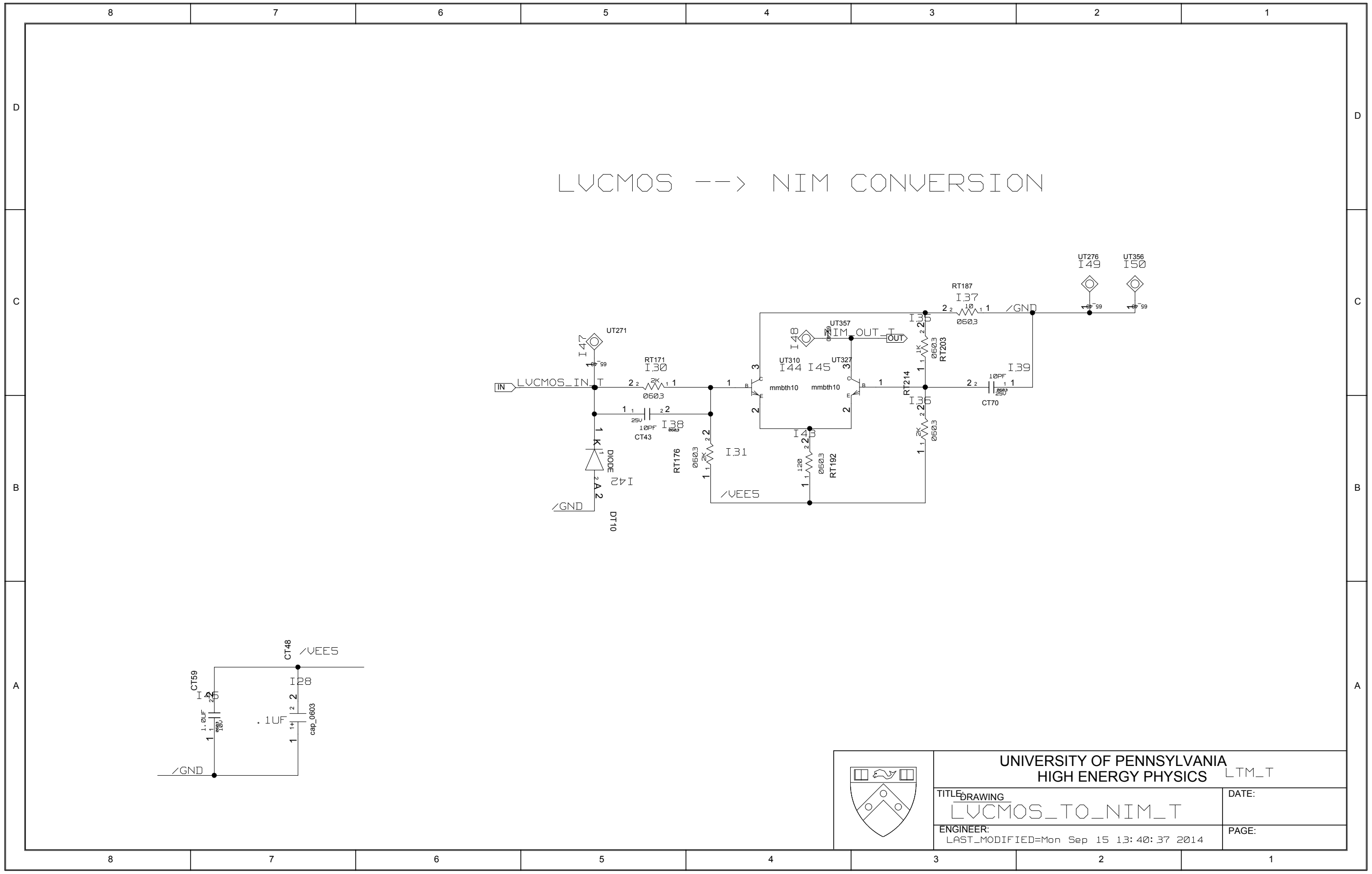
conn20
IN
OUT



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NIM_OUT_T
OUT
/GND
/VEE5
mmbth10
DIODE
RT171
RT176
RT187
RT192
RT203
RT214
CT43
CT48
CT59
CT70
DT10
UT271
UT276
UT310
UT327
UT356
UT357
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10PF
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cap_0603
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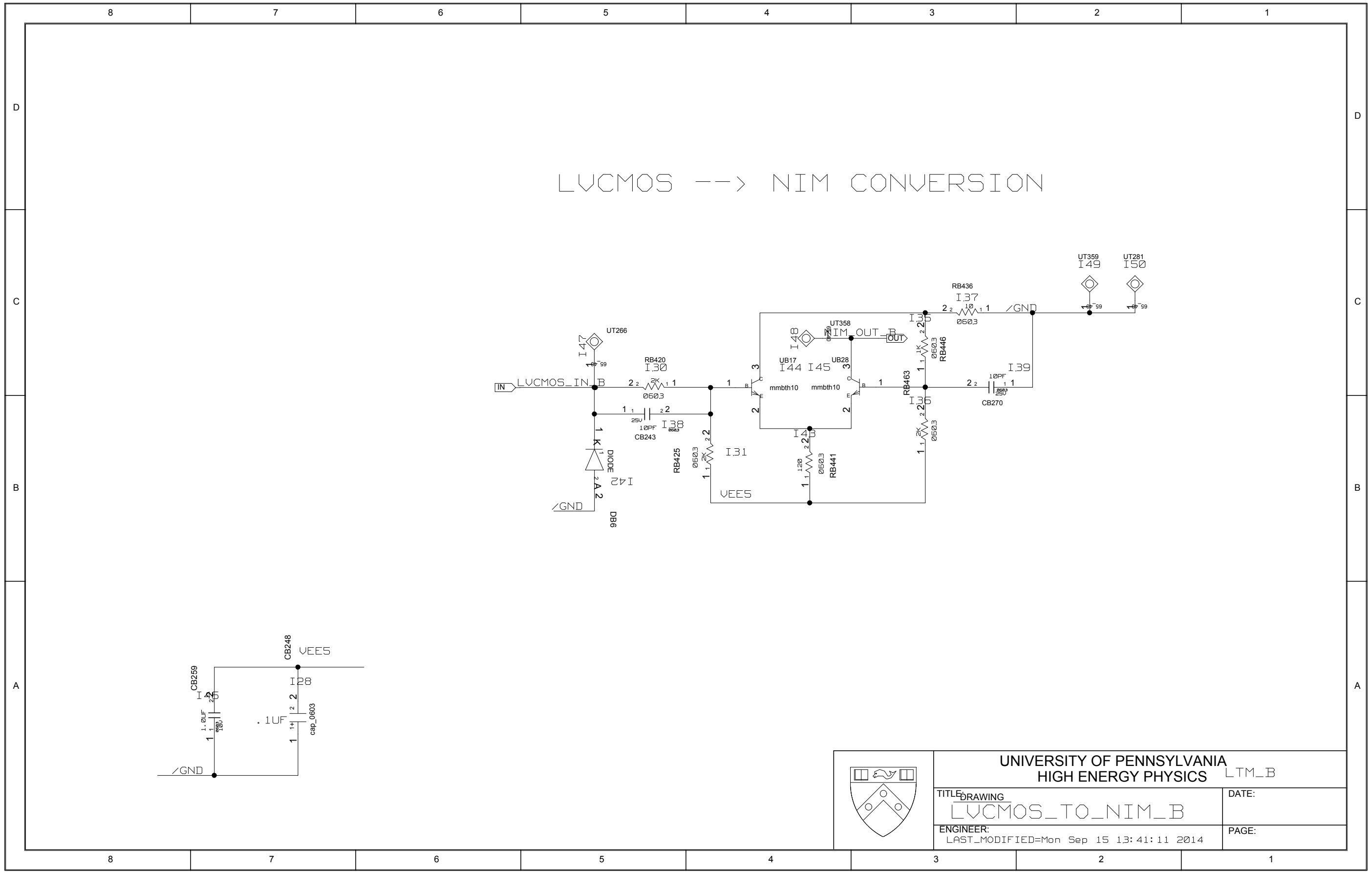
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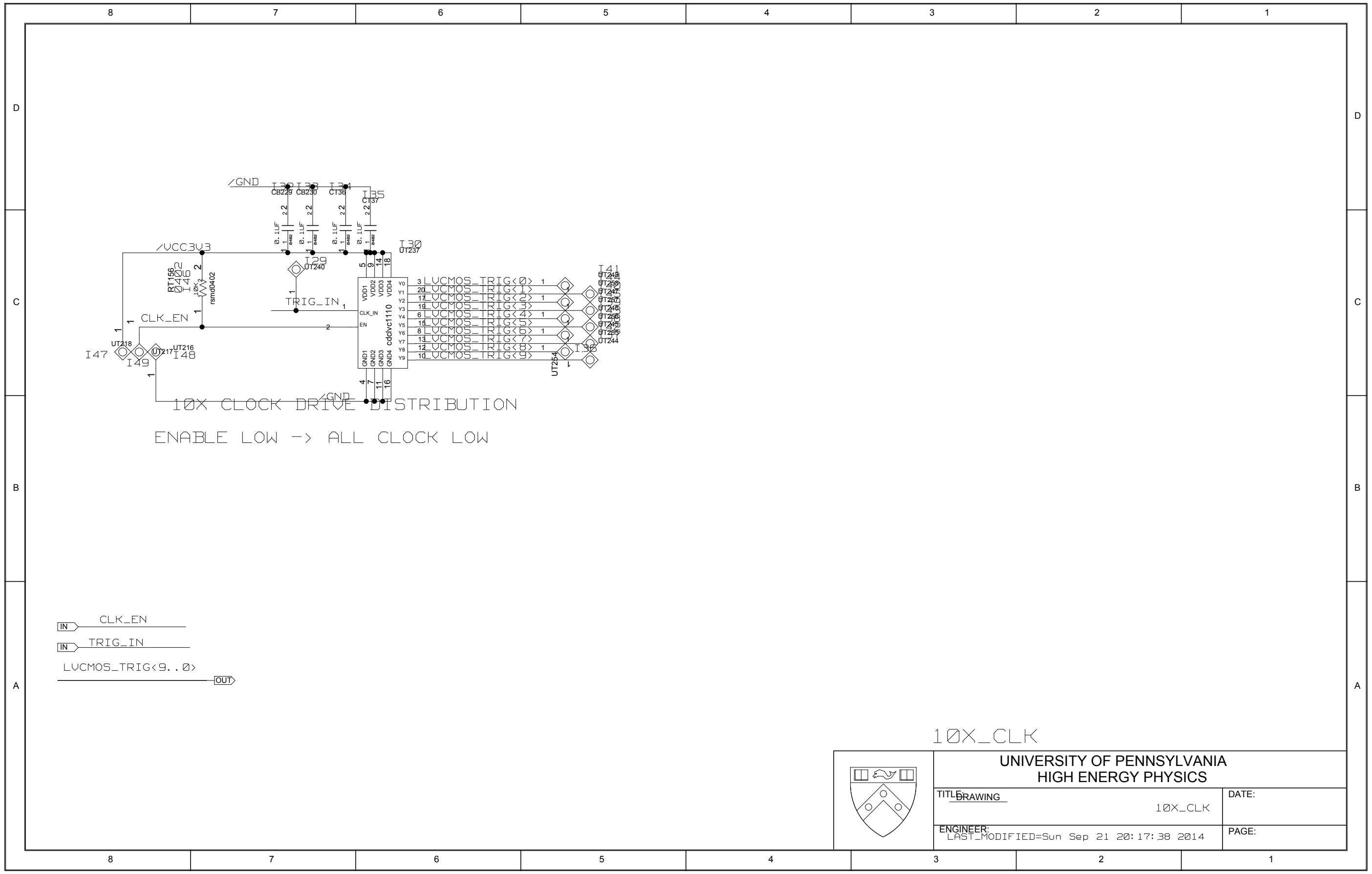
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LVCMOS_TRIG<3>
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LVCMOS_TRIG<9>
10X CLOCK DRIVE DISTRIBUTION
ENABLE LOW -> ALL CLOCK LOW
IN CLK_EN
IN TRIG_IN
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UNIVERSITY OF PENNSYLVANIA
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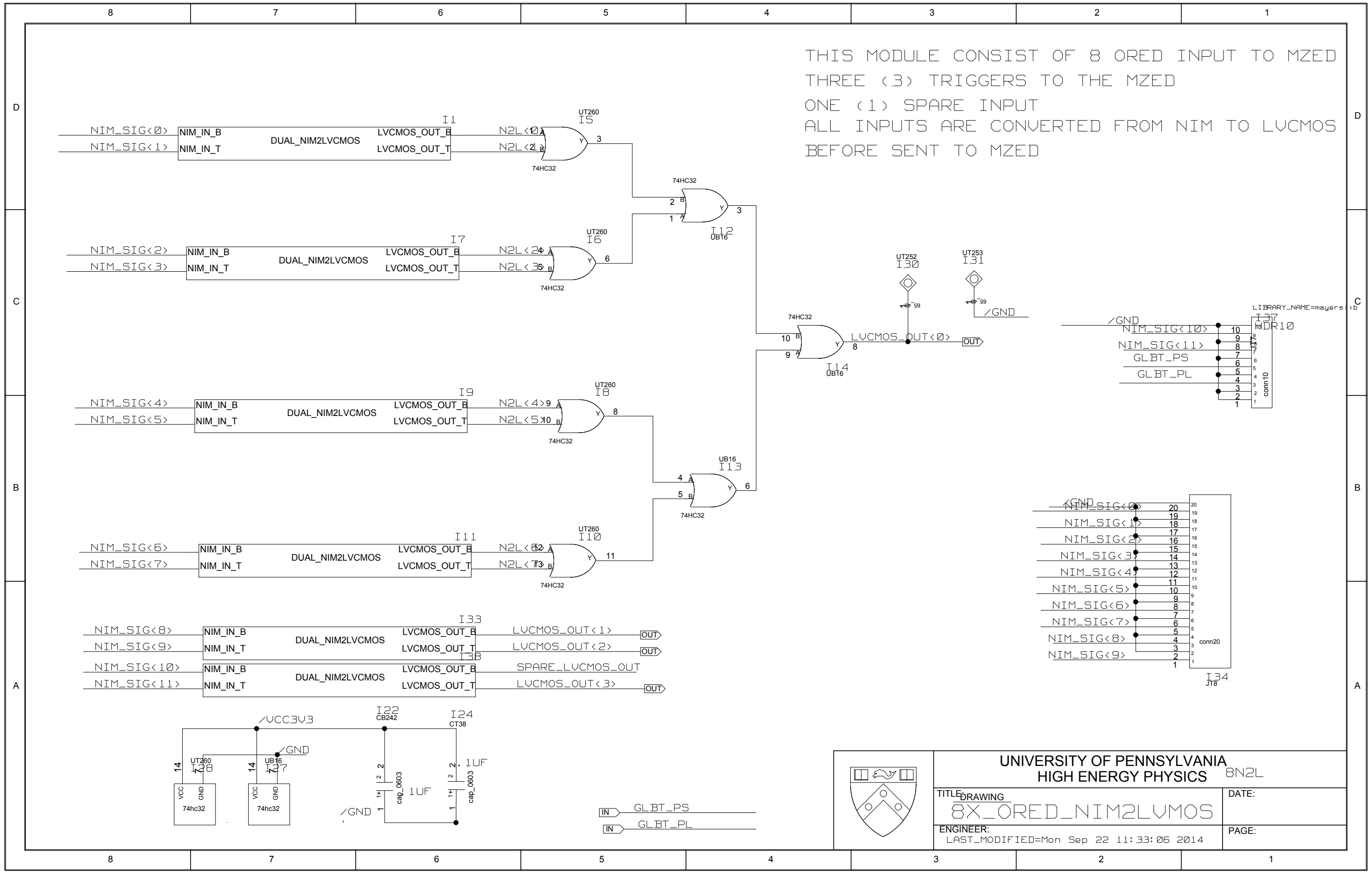
THIS MODULE CONSIST OF 8 ORED INPUT TO MZED
THREE (3) TRIGGERS TO THE MZED
ONE (1) SPARE INPUT
ALL INPUTS ARE CONVERTED FROM NIM TO LVCMOS
BEFORE SENT TO MZED
DUAL_NIM2LVCMOS
74HC32
LVCMOS_OUT<0>
LVCMOS_OUT<1>
LVCMOS_OUT<2>
SPARE_LVCMOS_OUT
LVCMOS_OUT<3>
GLBT_PS
GLBT_PL
/VCC3V3
/GND
.1UF
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8N2L
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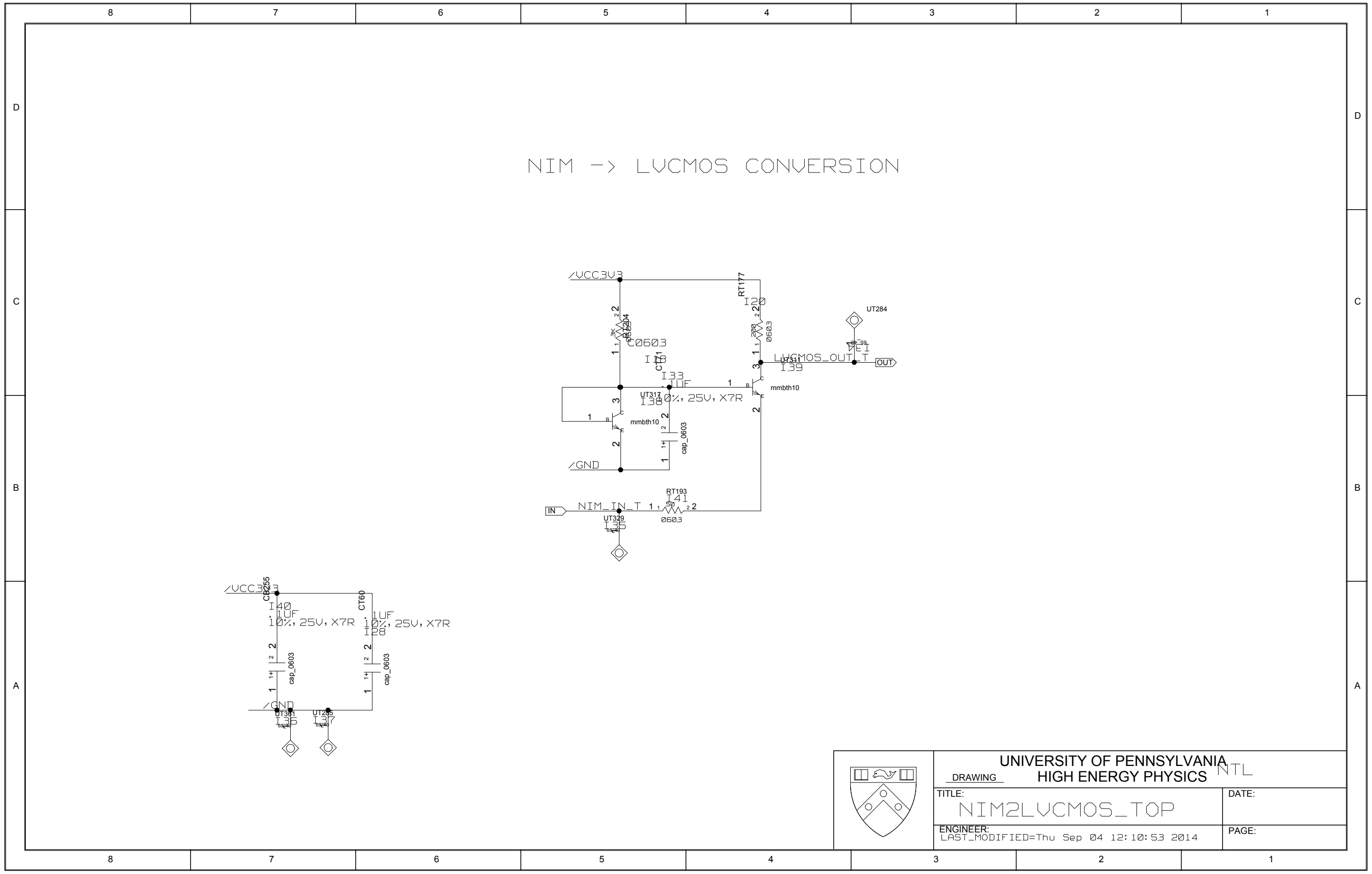

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UNIVERSITY OF PENNSYLVANIA
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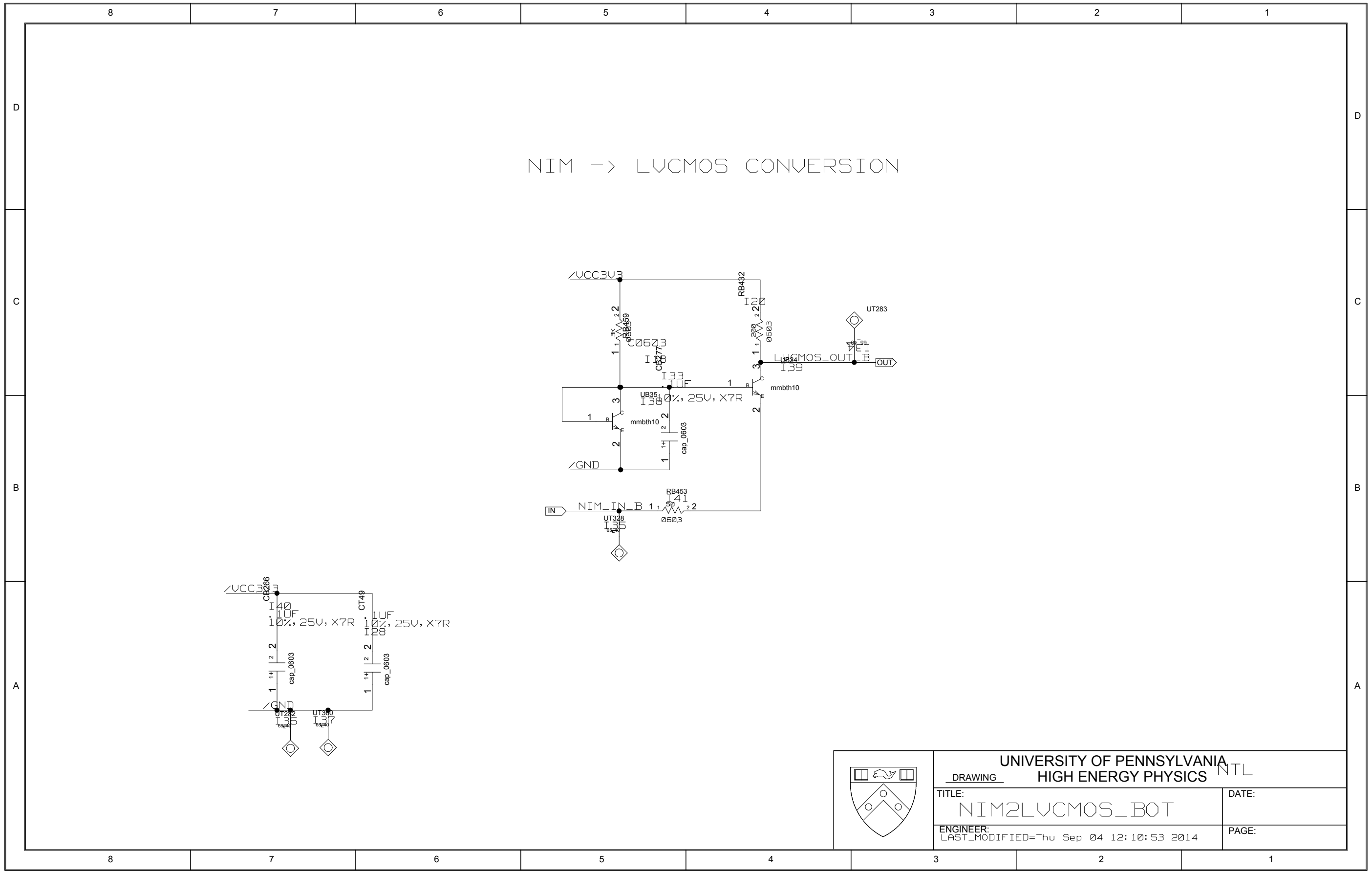
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cap_0603
IN
OUT
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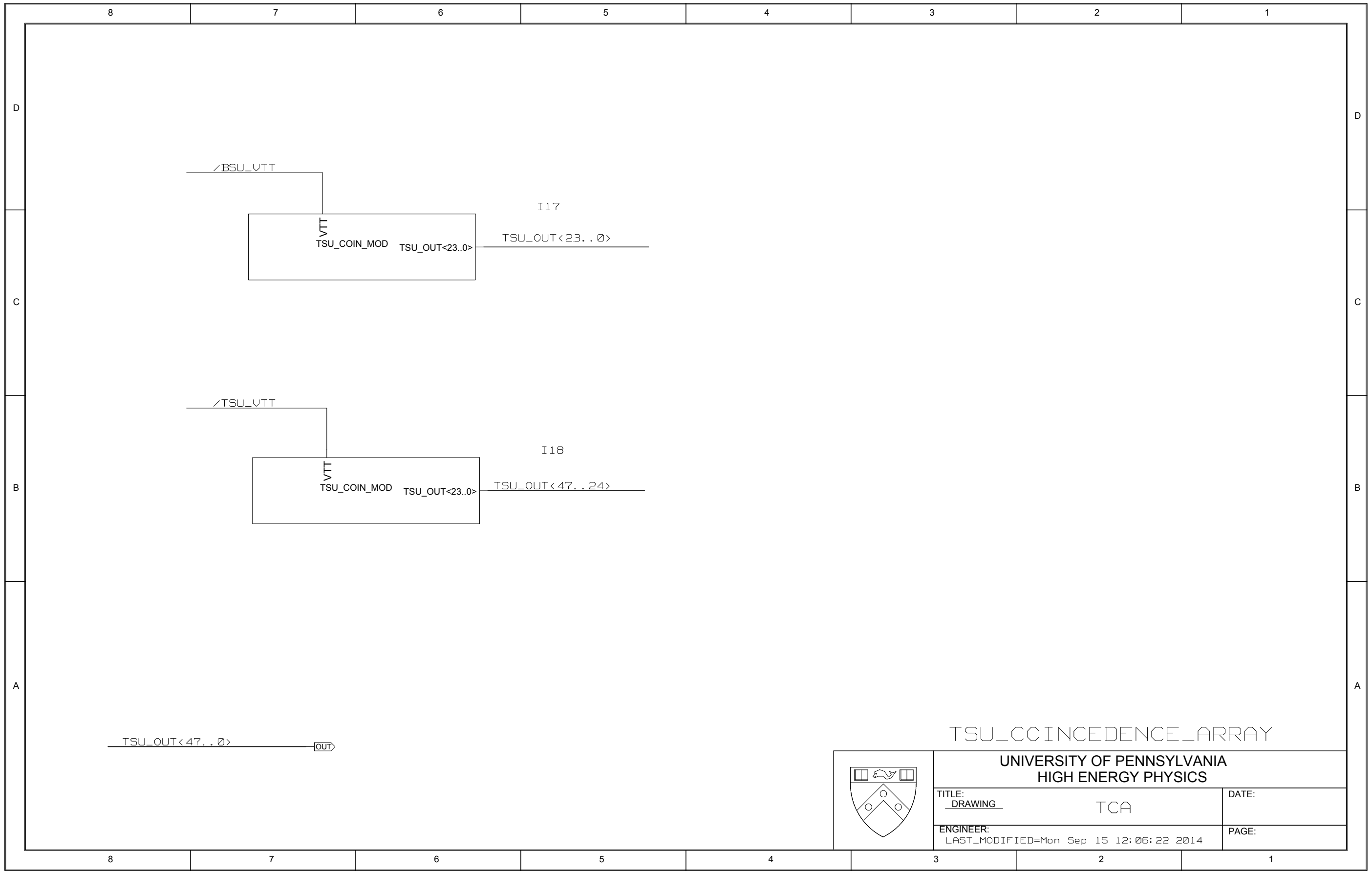
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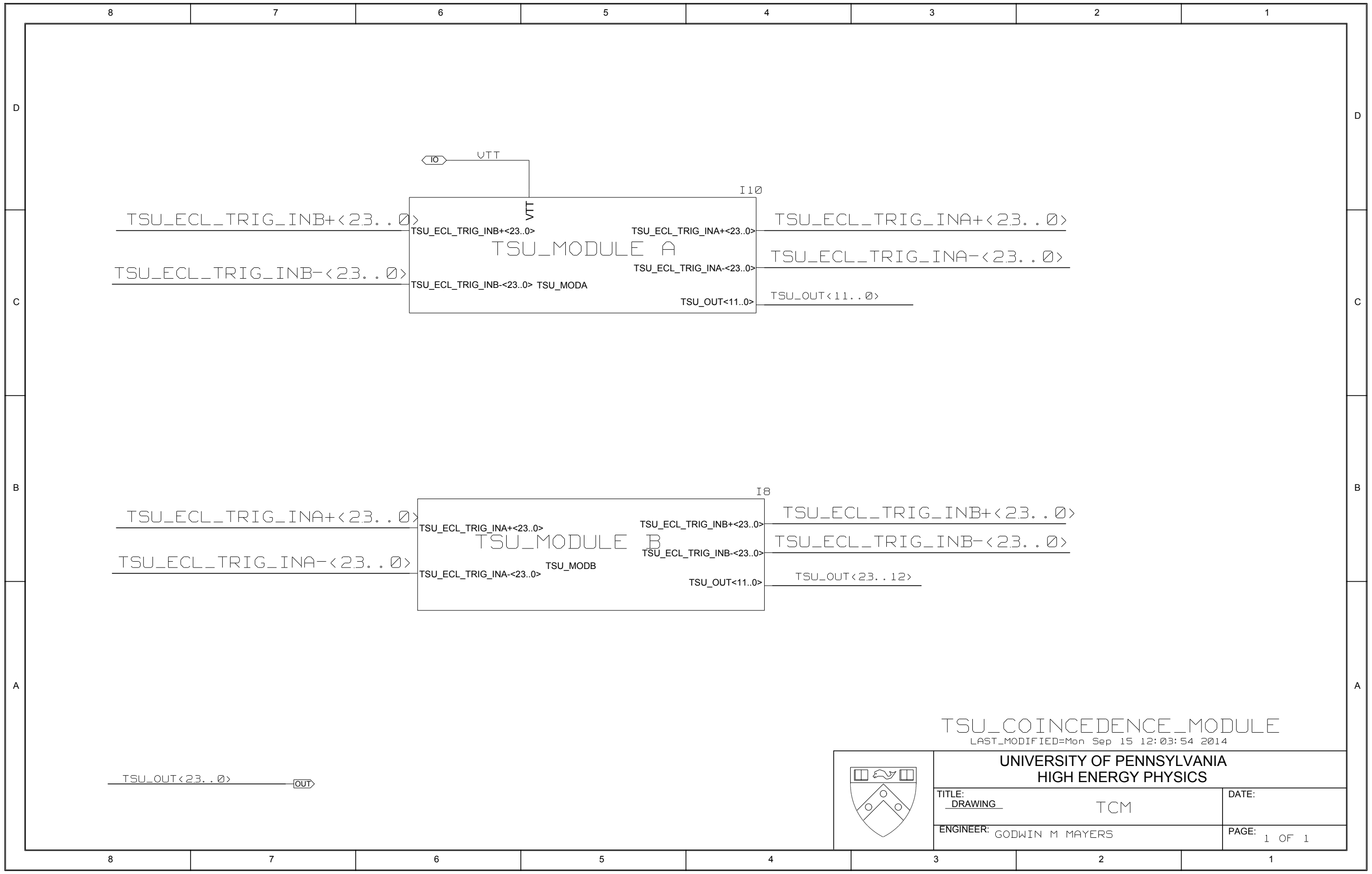
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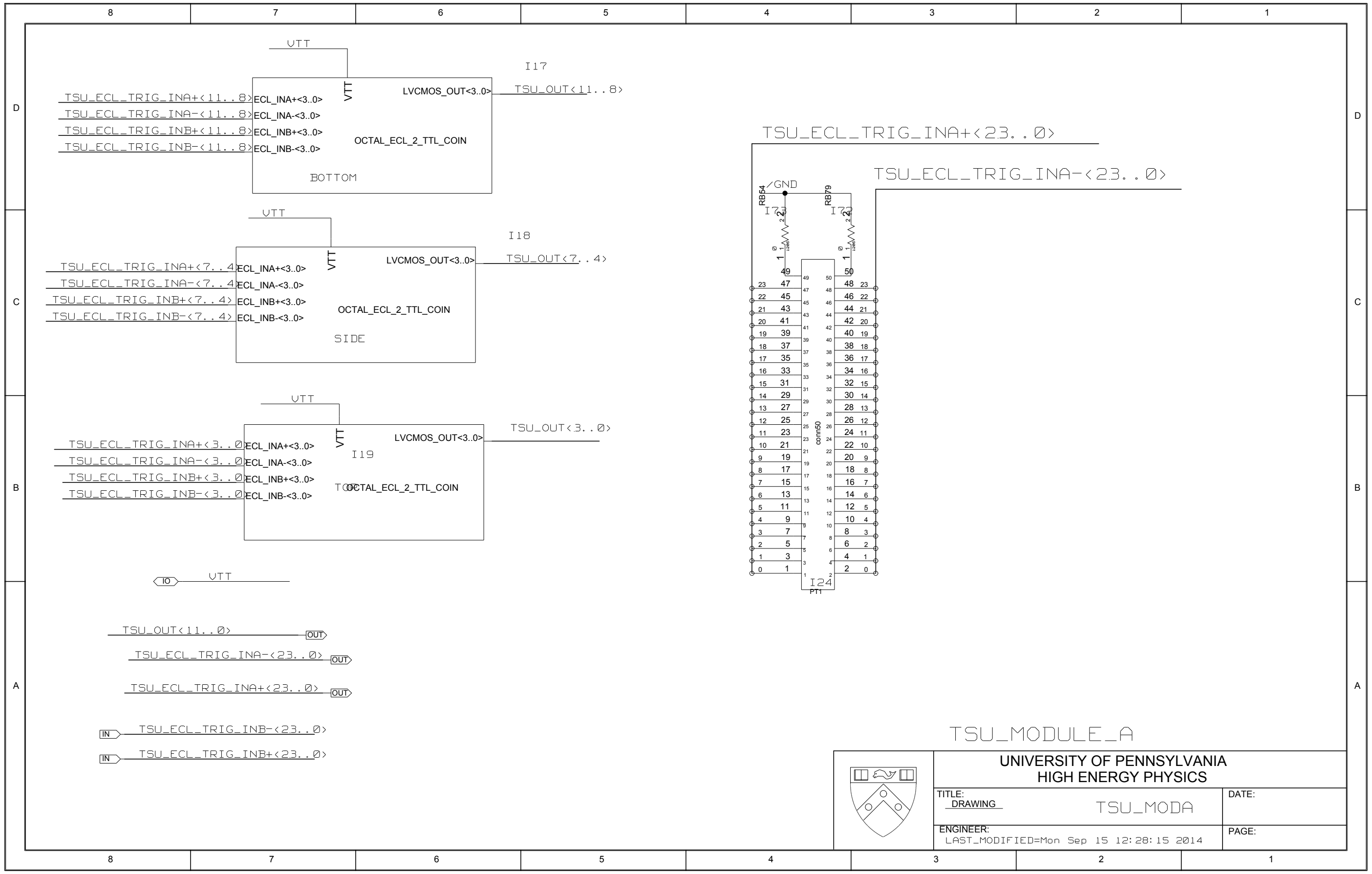
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IO
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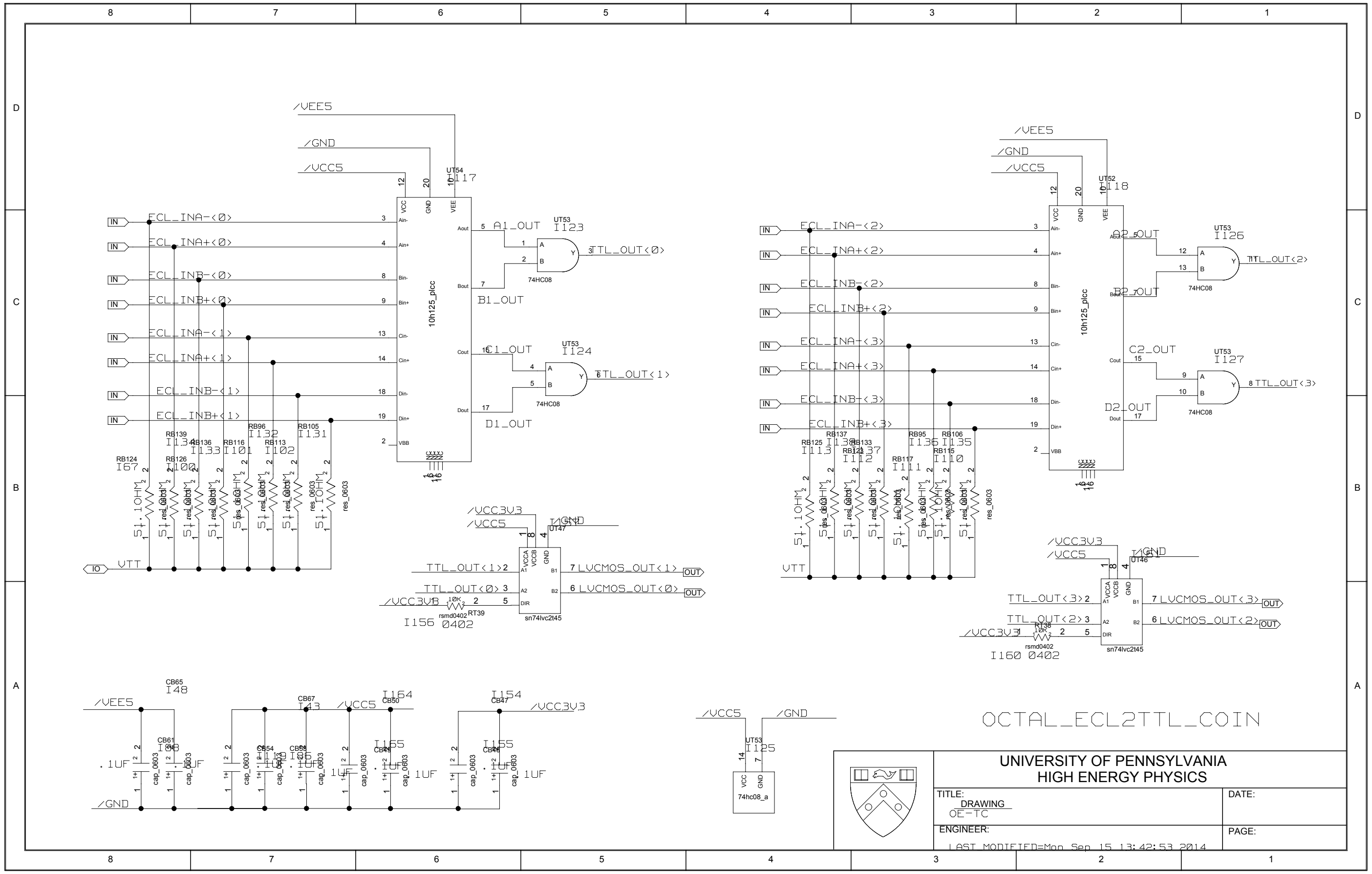
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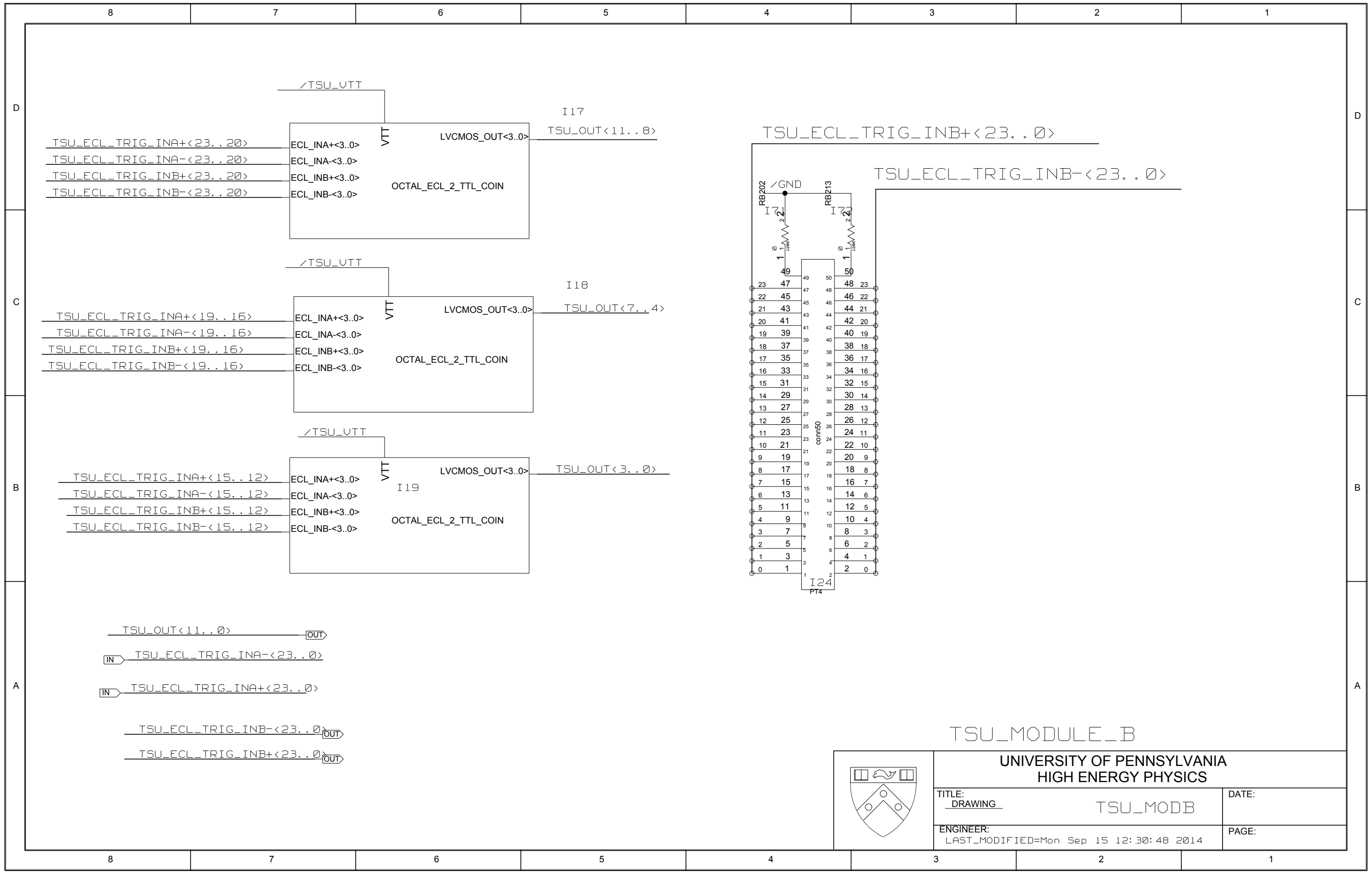
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UNIVERSITY OF PENNSYLVANIA
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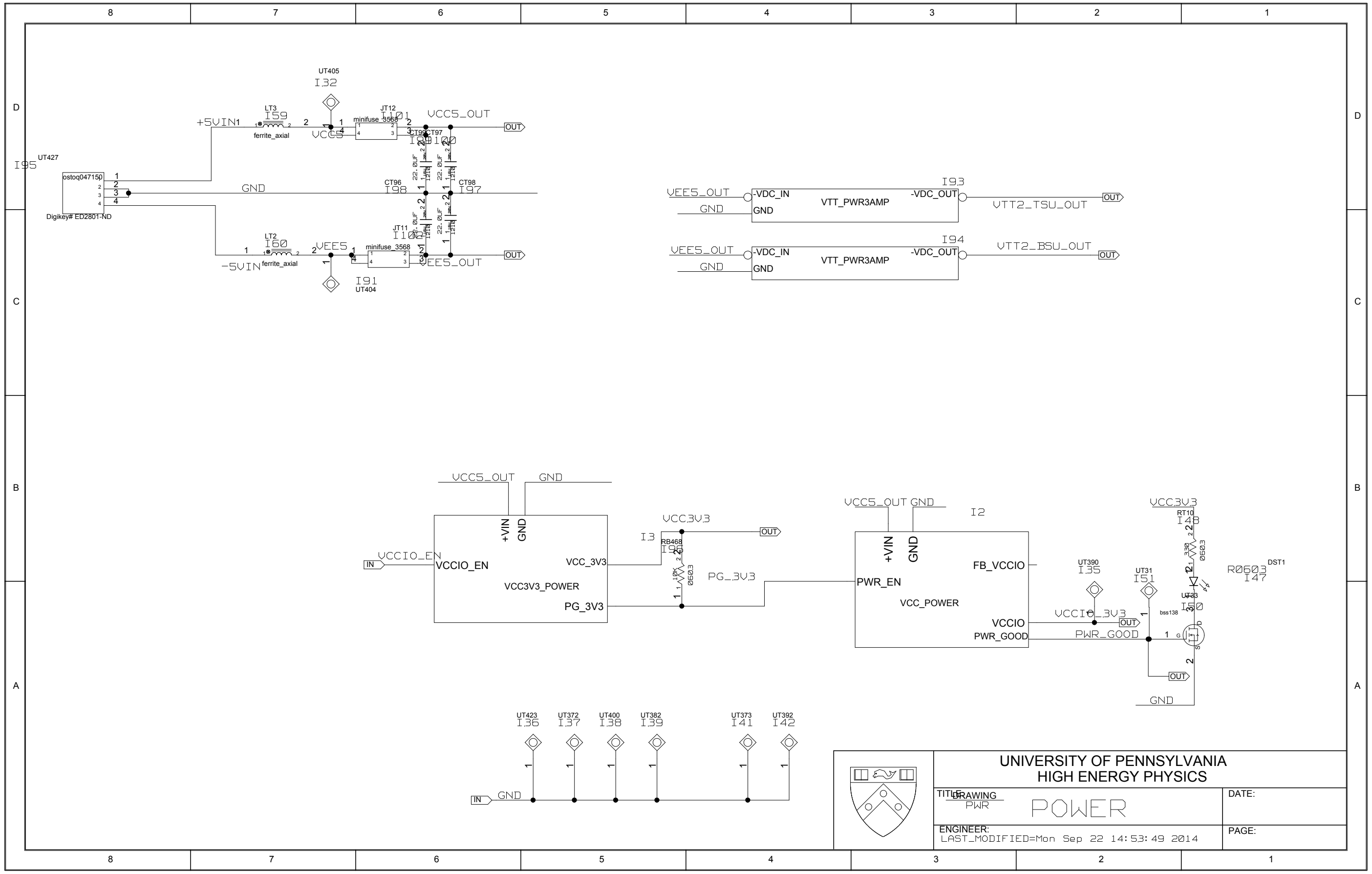
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VEE5
VCC5_OUT
VEE5_OUT
GND
ferrite_axial
minifuse_3568
Digikey# ED2801-ND
VTT_PWR3AMP
-VDC_IN
-VDC_OUT
VTT2_TSU_OUT
VTT2_BSU_OUT
VCC3V3_POWER
VCCIO_EN
VCC_3V3
PG_3V3
+VIN
VCC3V3
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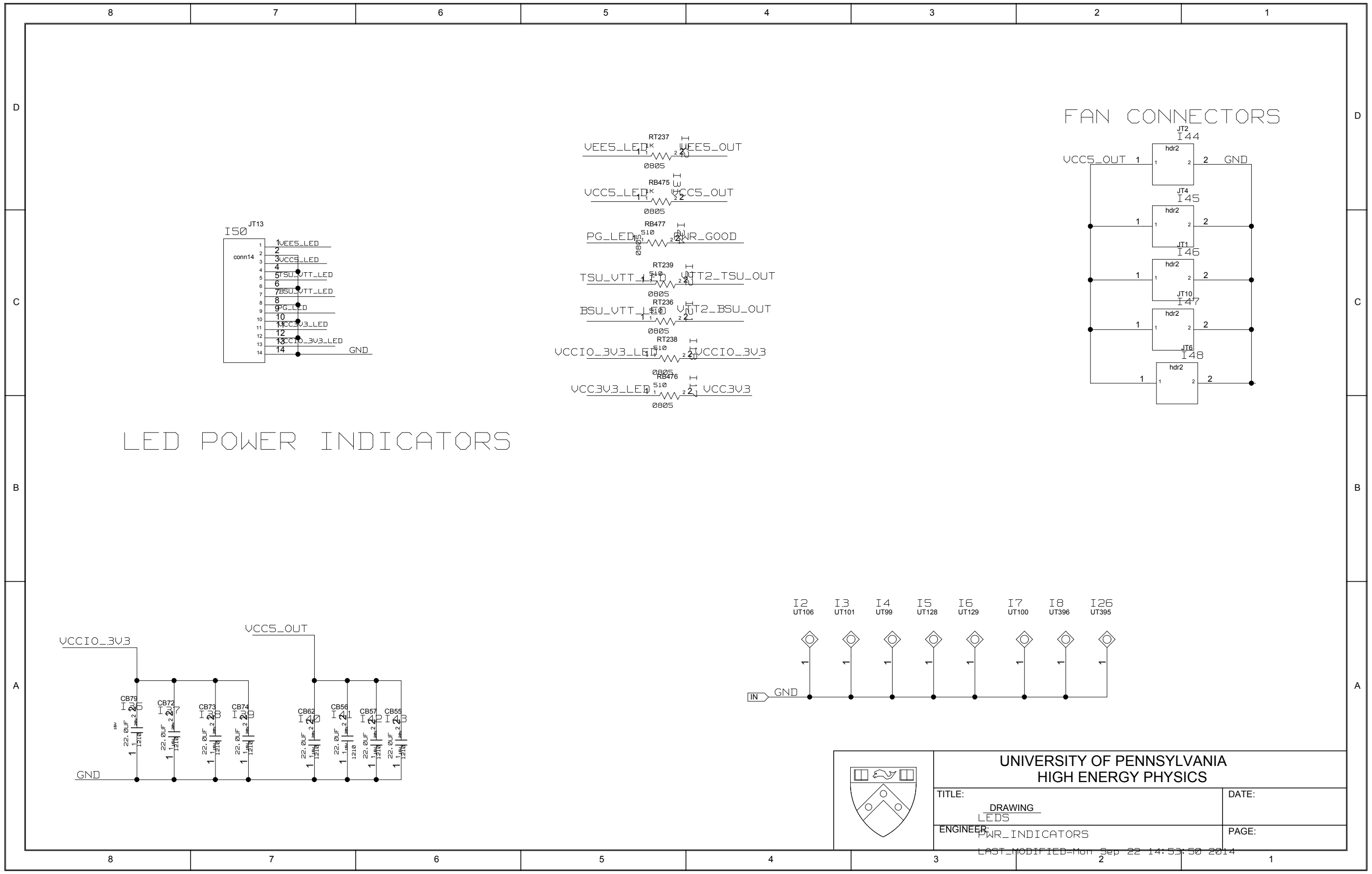

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LED POWER INDICATORS
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VCC5_OUT
PG_LED
PWR_GOOD
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VTT2_TSU_OUT
BSU_VTT_LED
VTT2_BSU_OUT
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VCCIO_3V3
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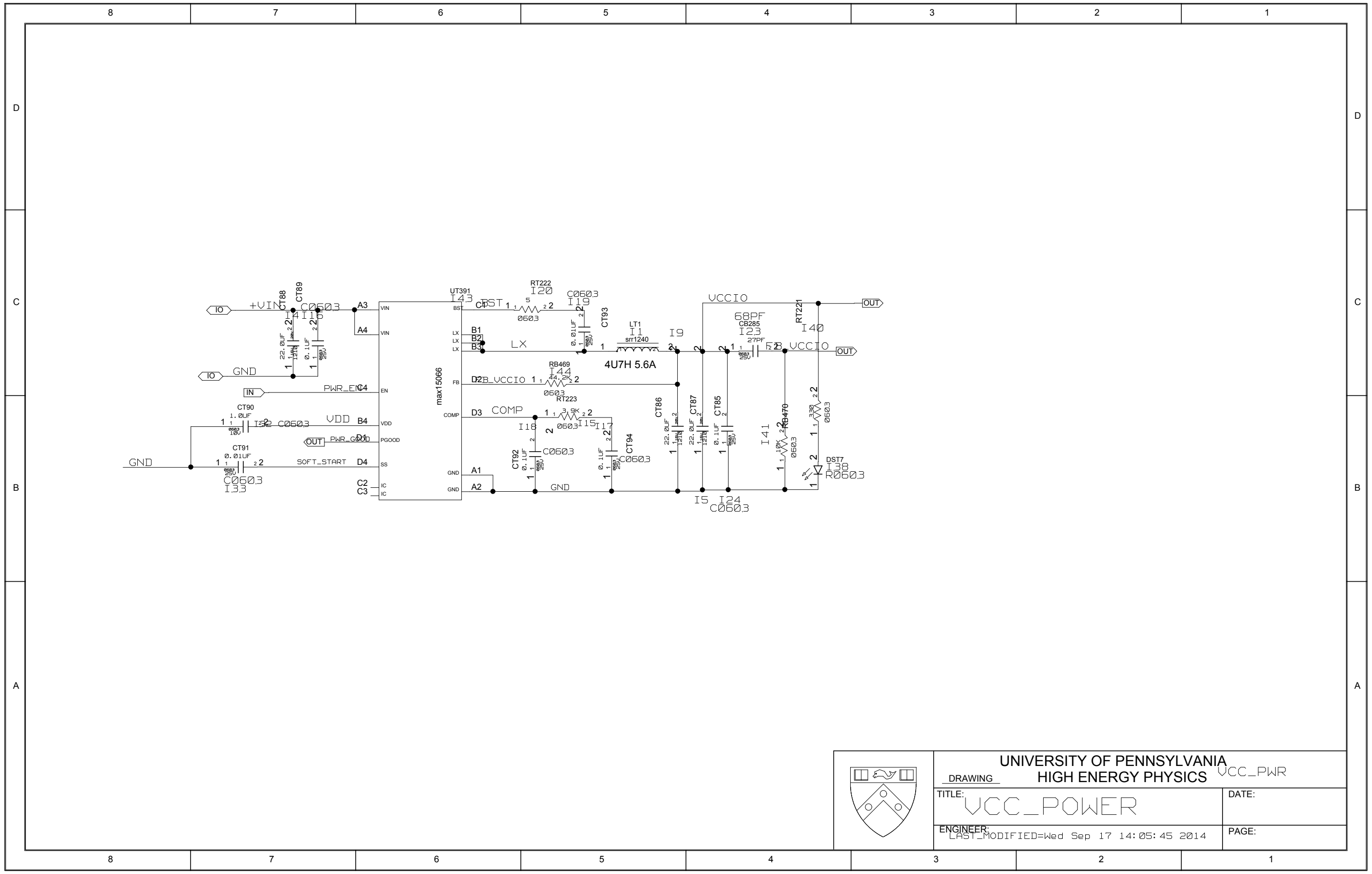
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LX
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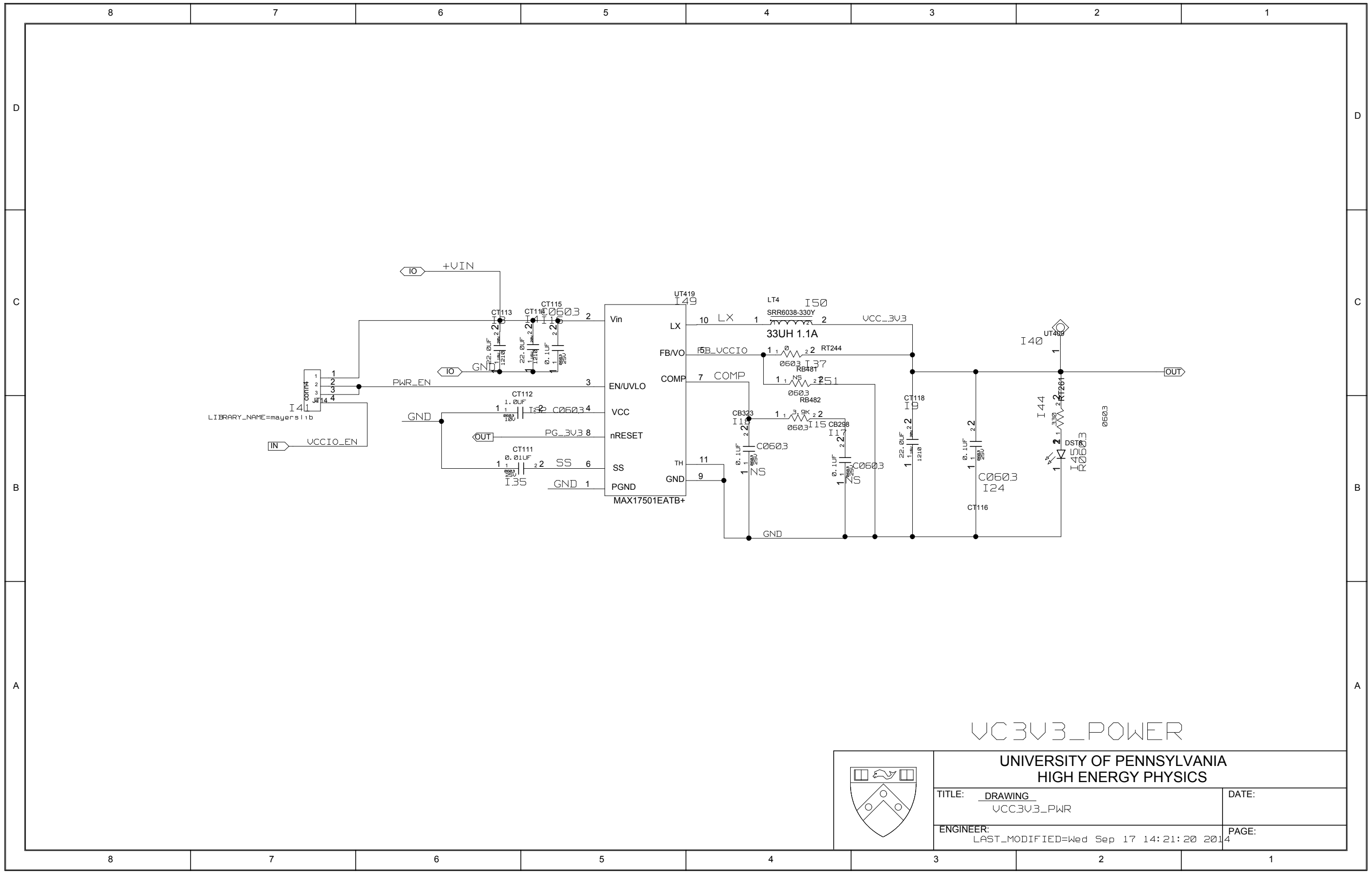
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OUT
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33UH 1.1A
SRR6038-330Y
Vin
LX
FB/VO
COMP
EN/UVLO
VCC
nRESET
SS
PGND
TH
GND
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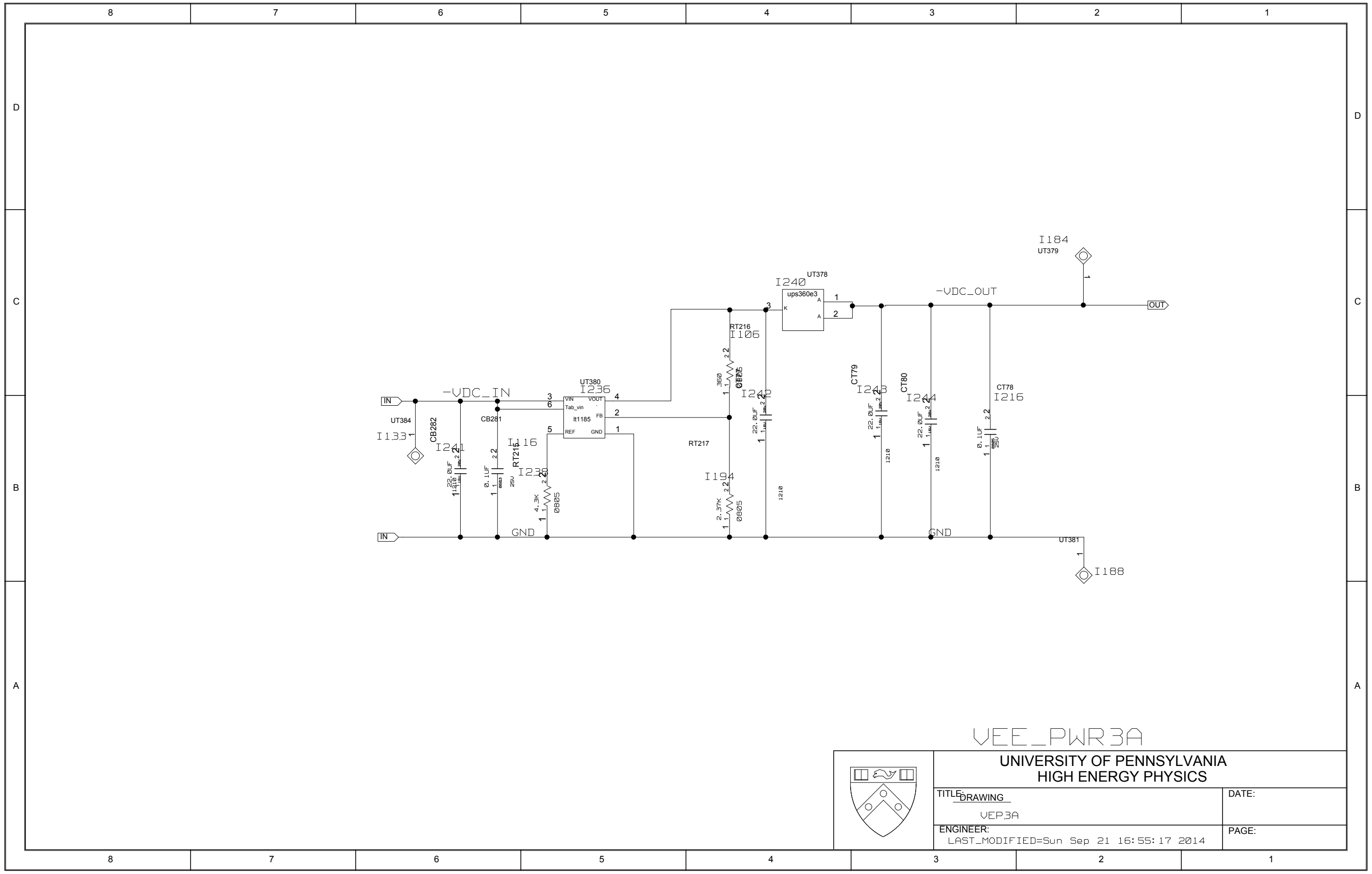

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-VDC_OUT
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OUT
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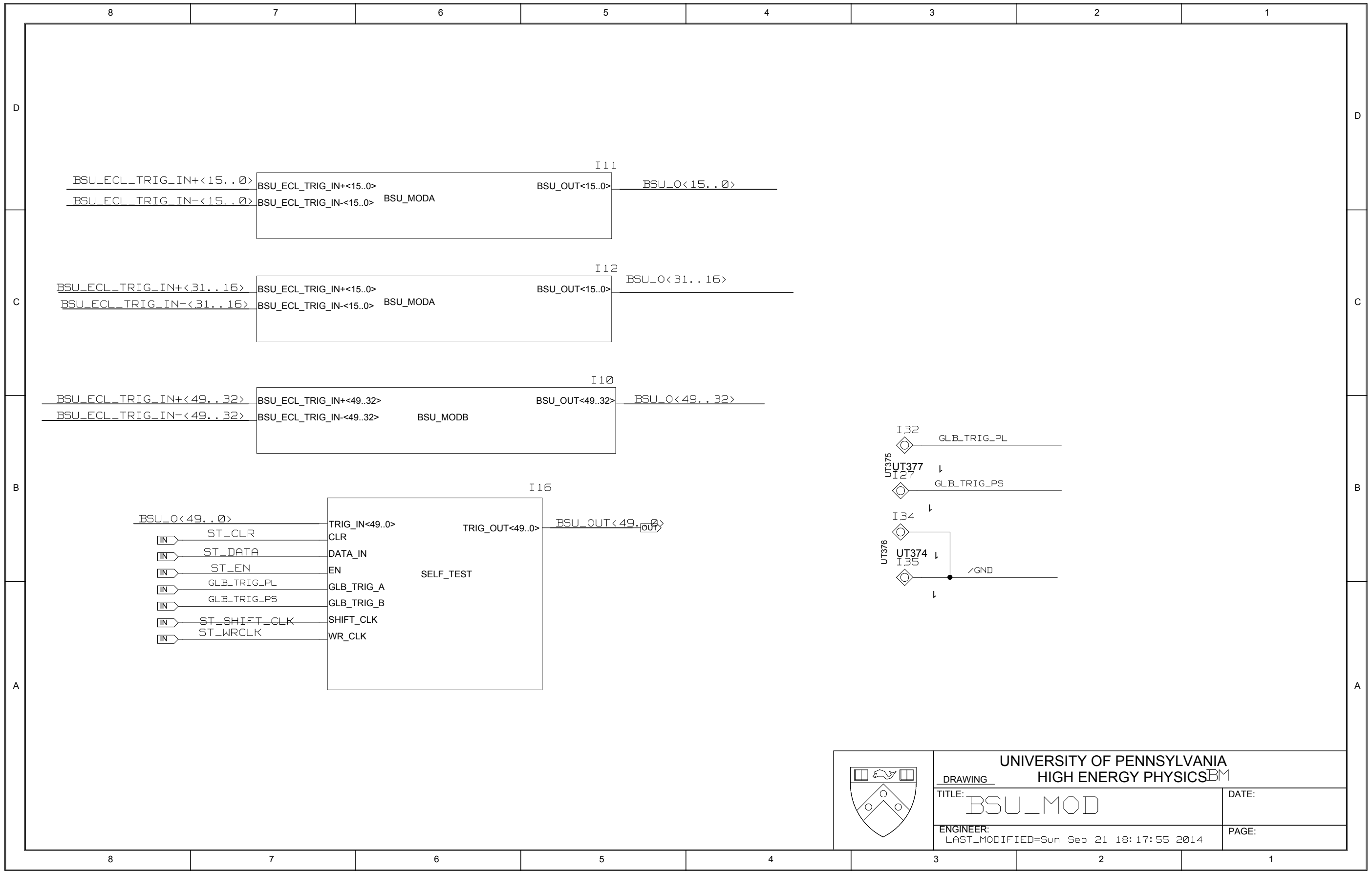

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DATA_IN
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GLB_TRIG_A
GLB_TRIG_PS
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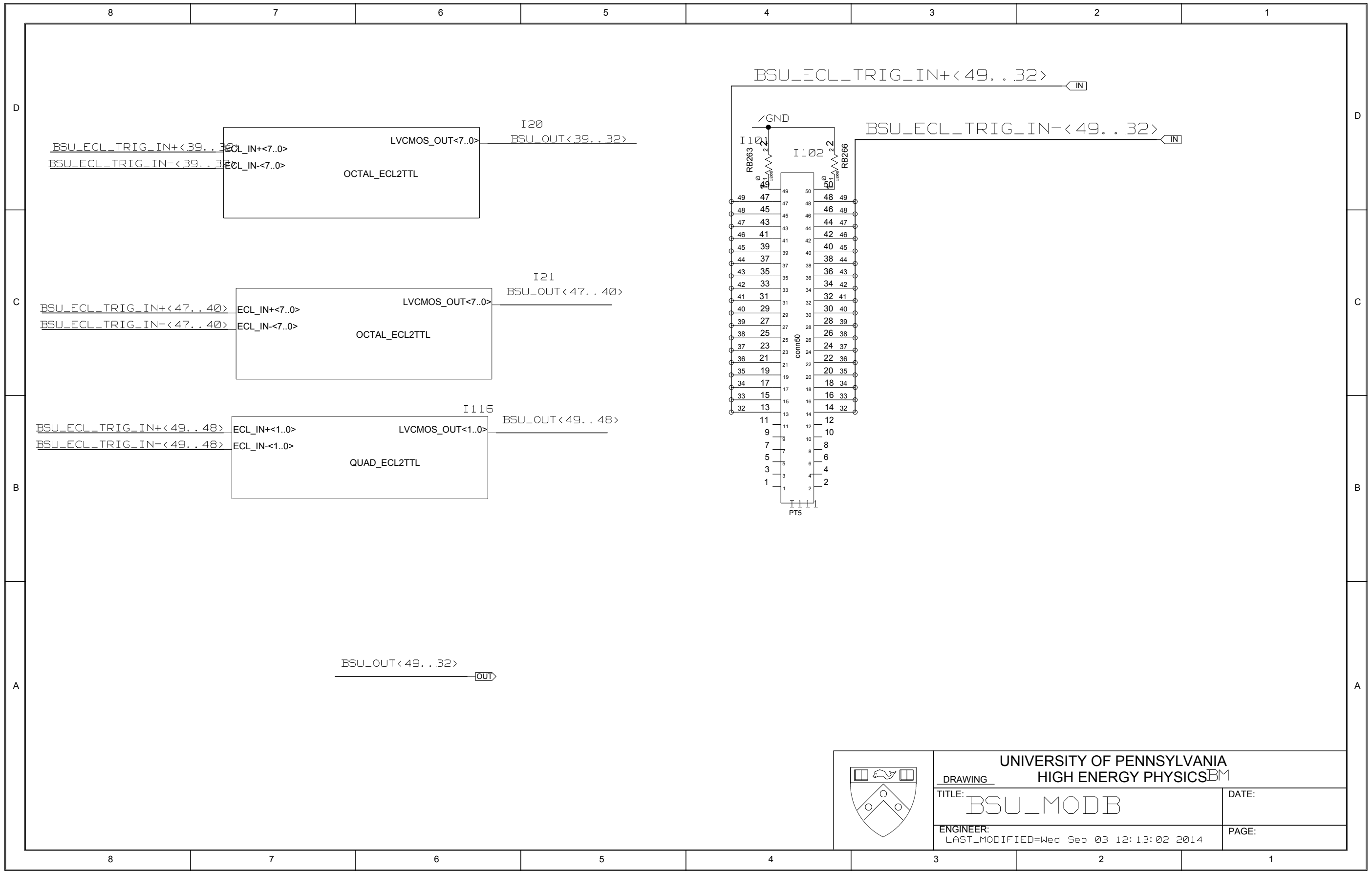
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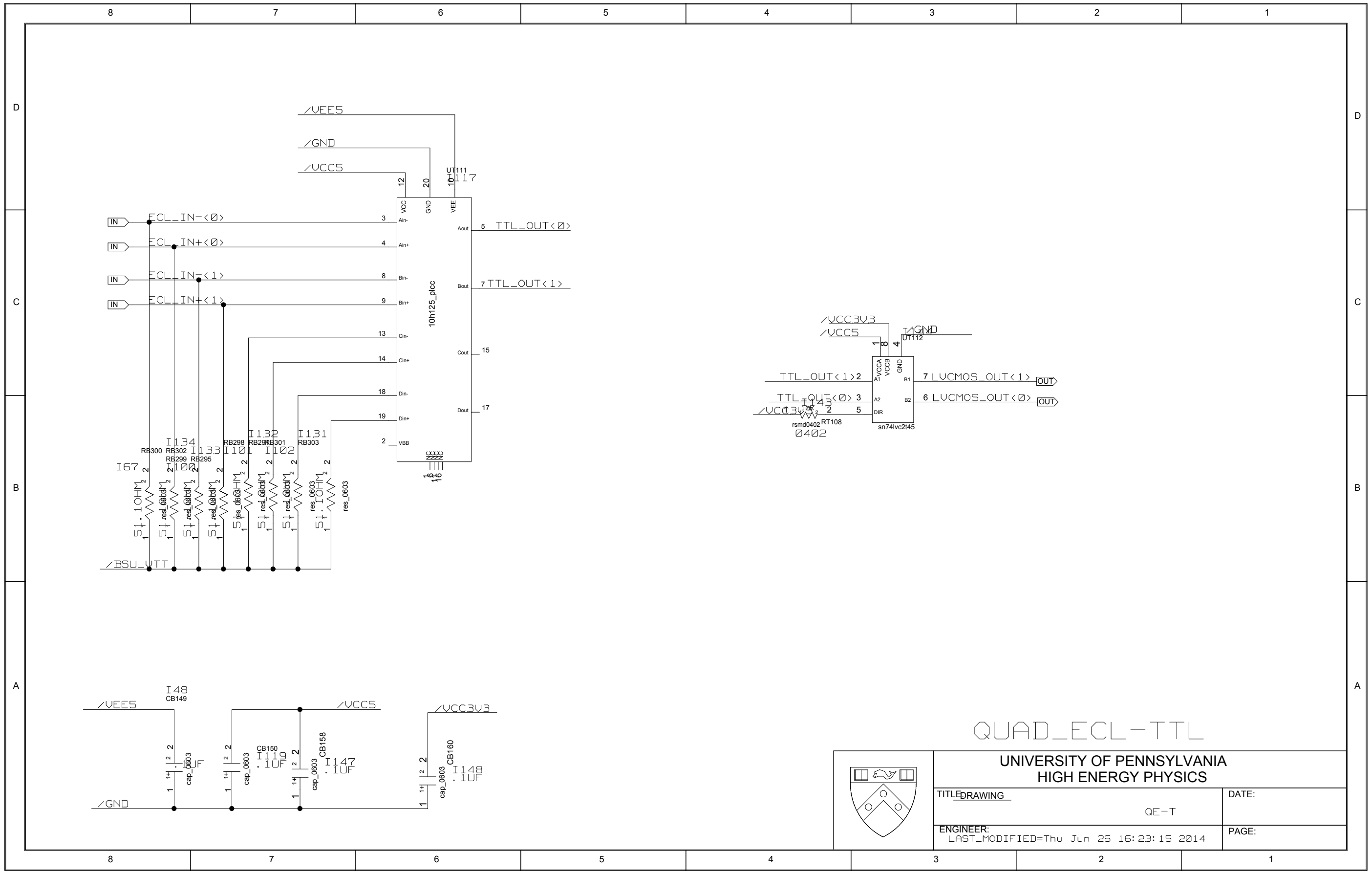
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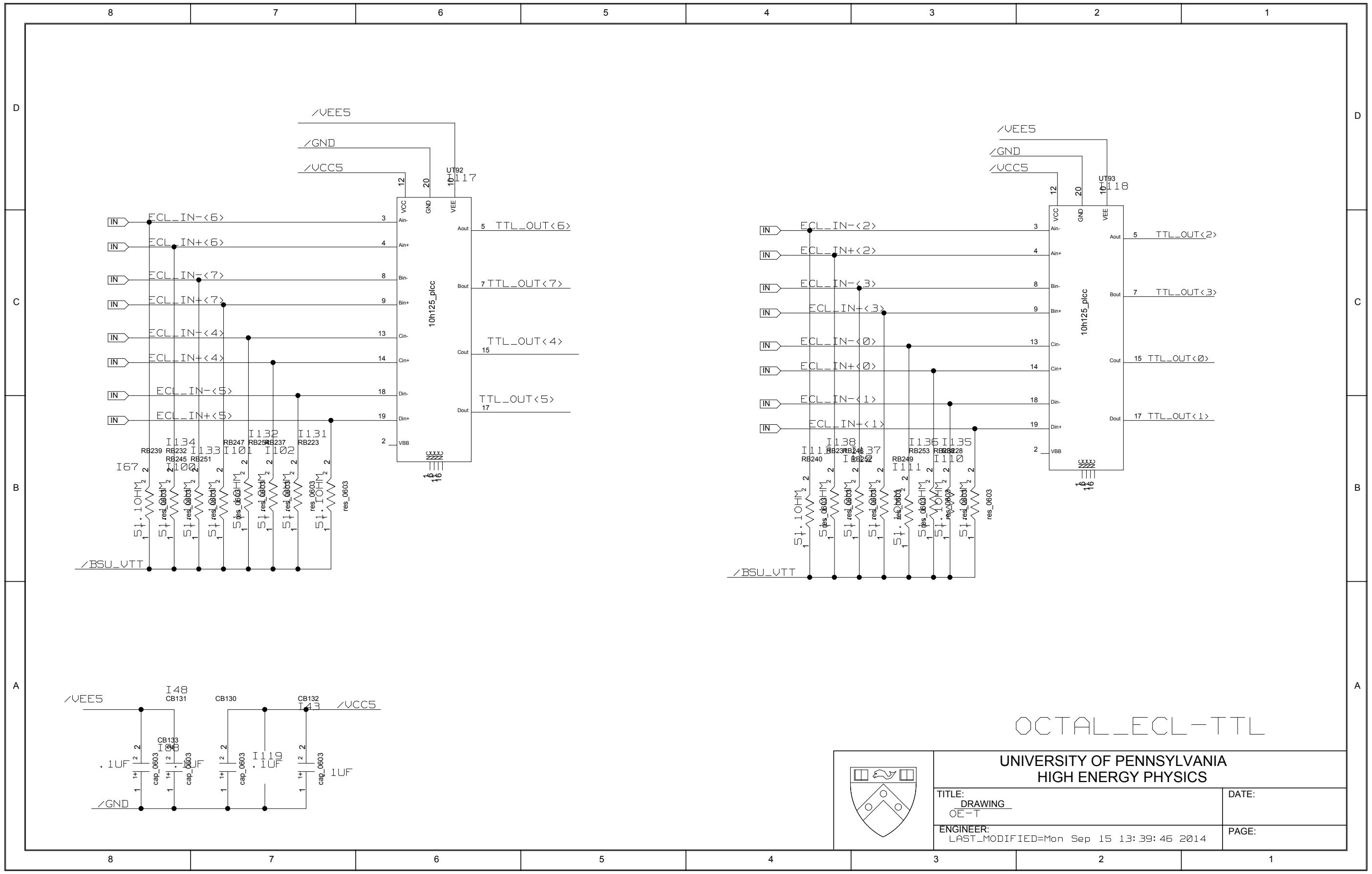
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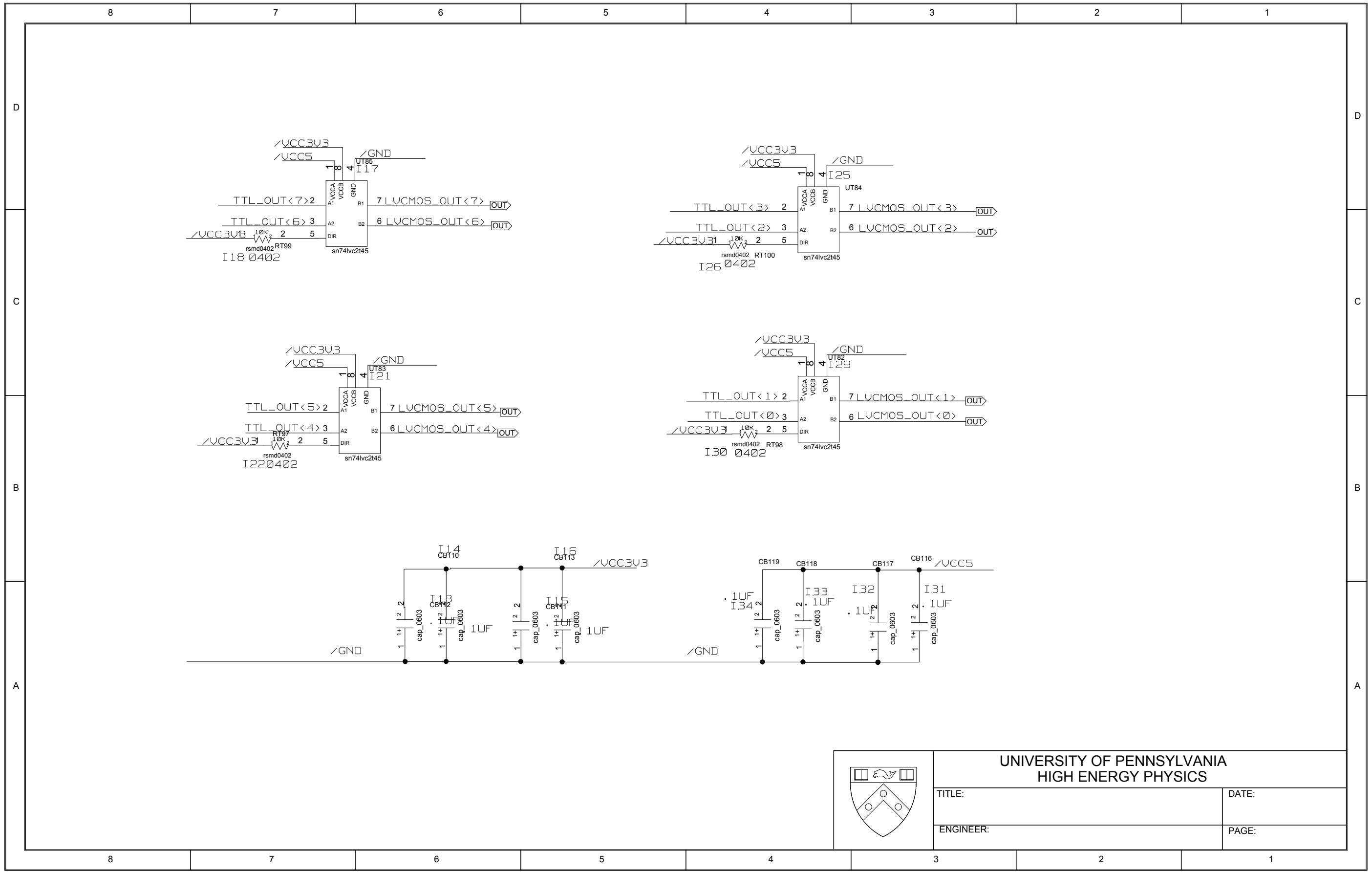

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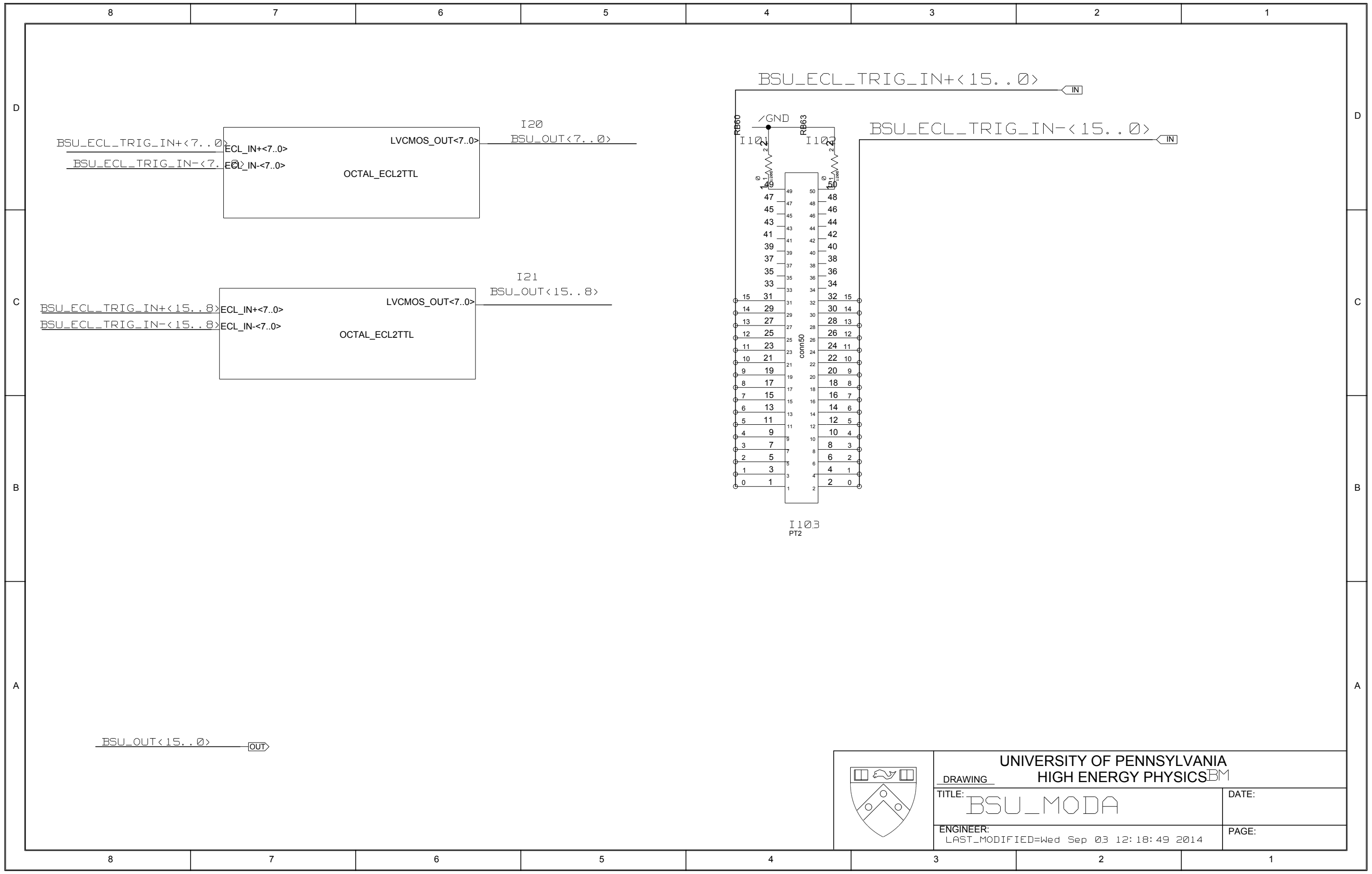

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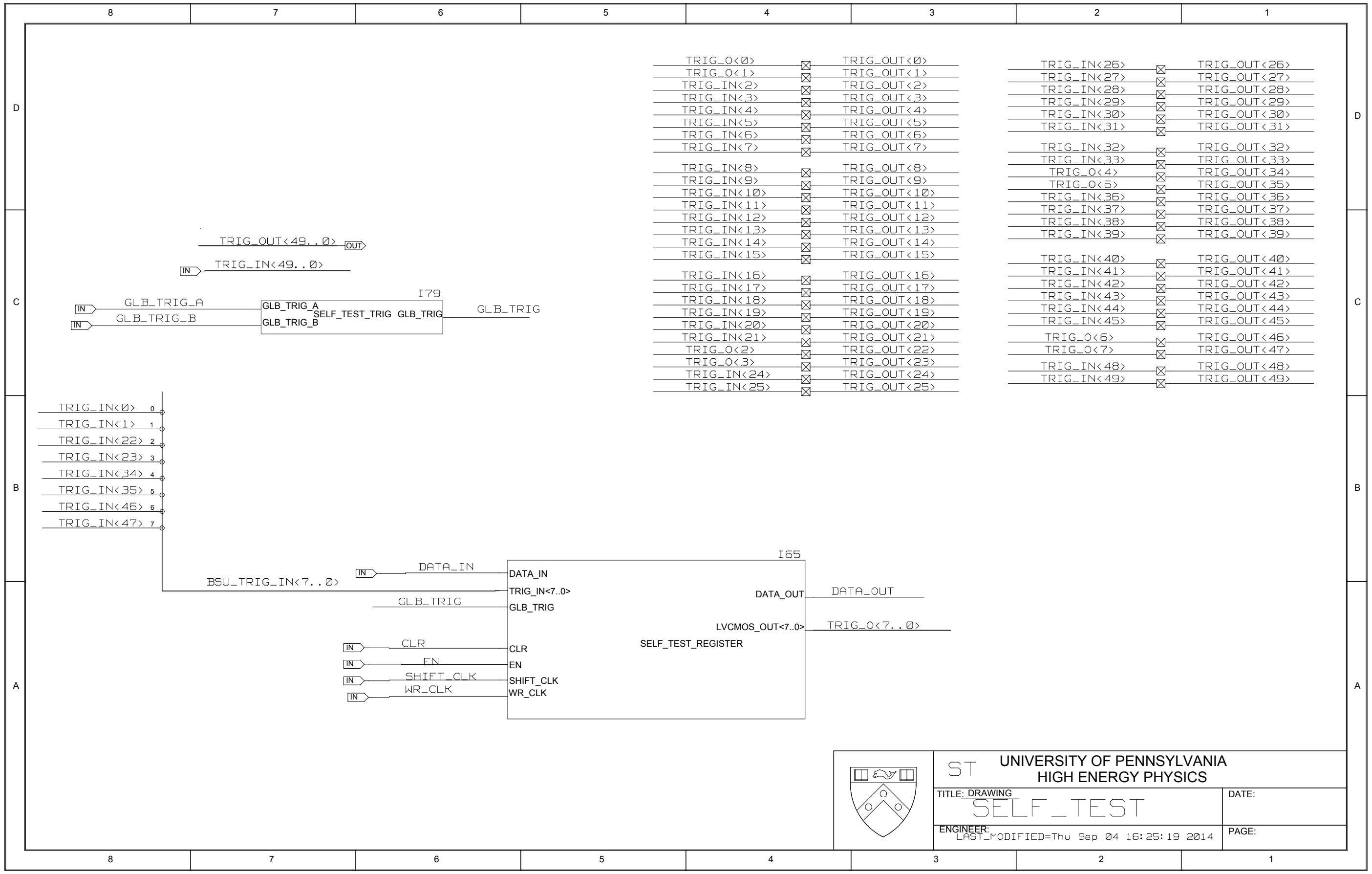

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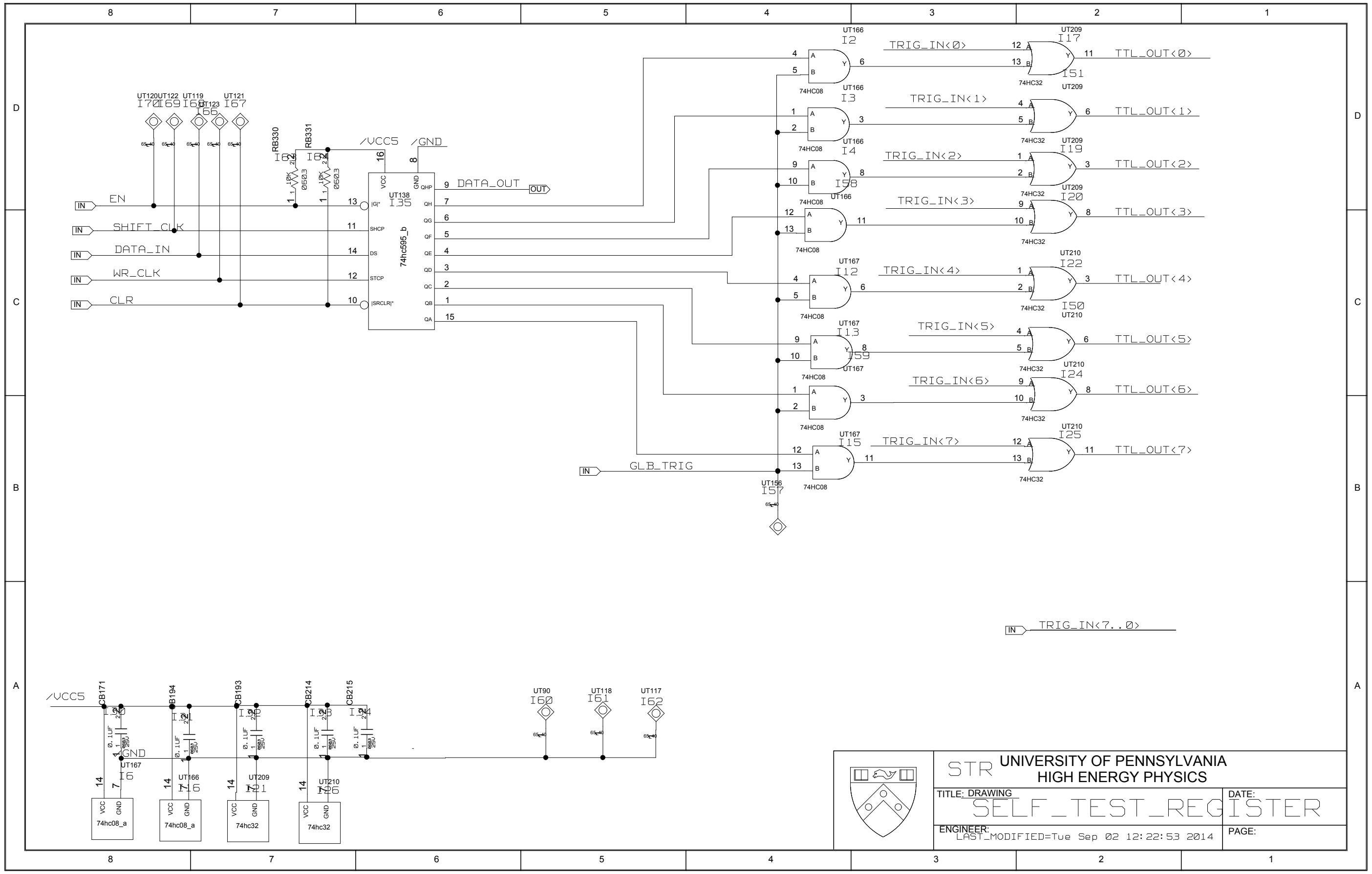

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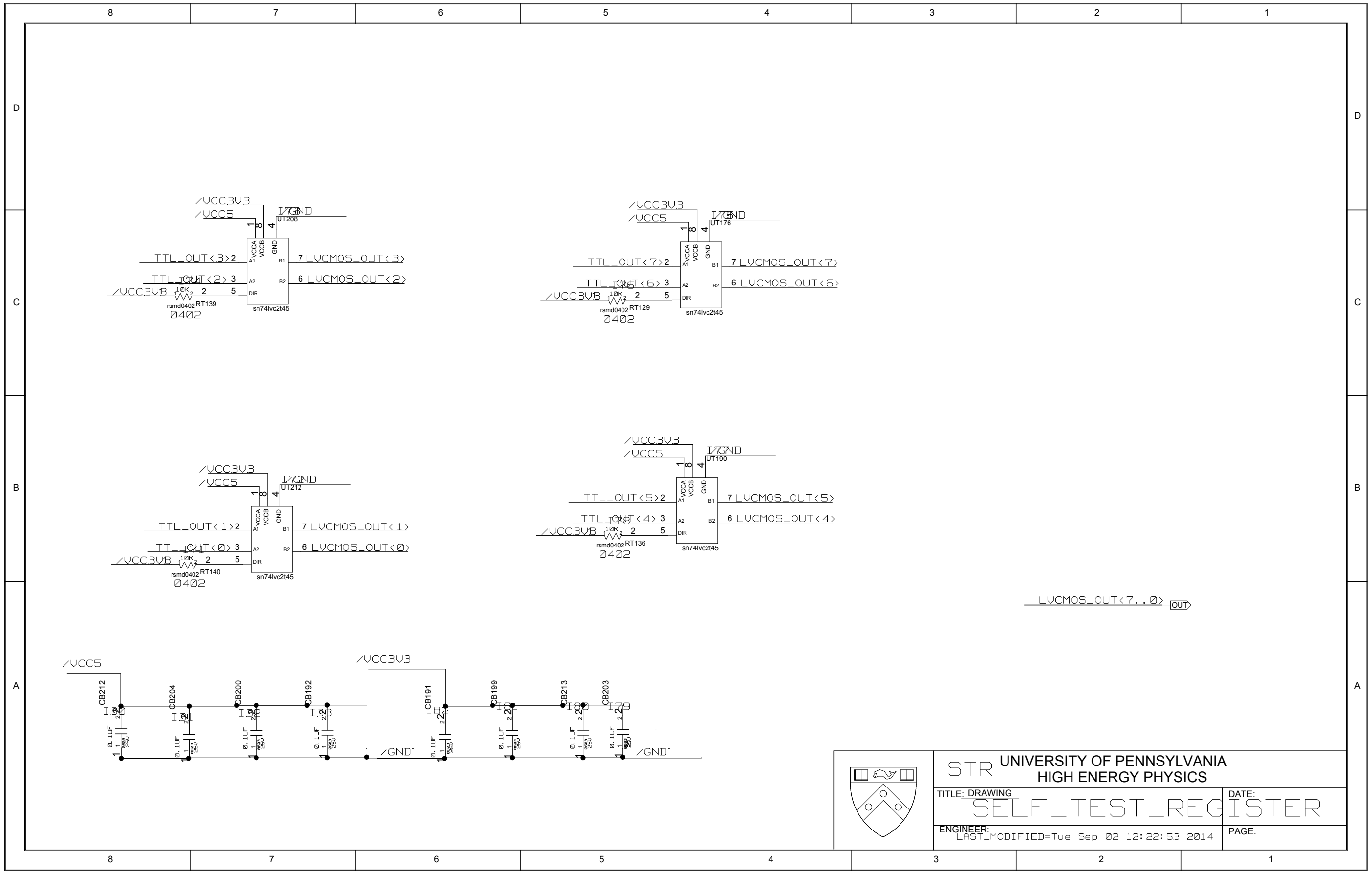
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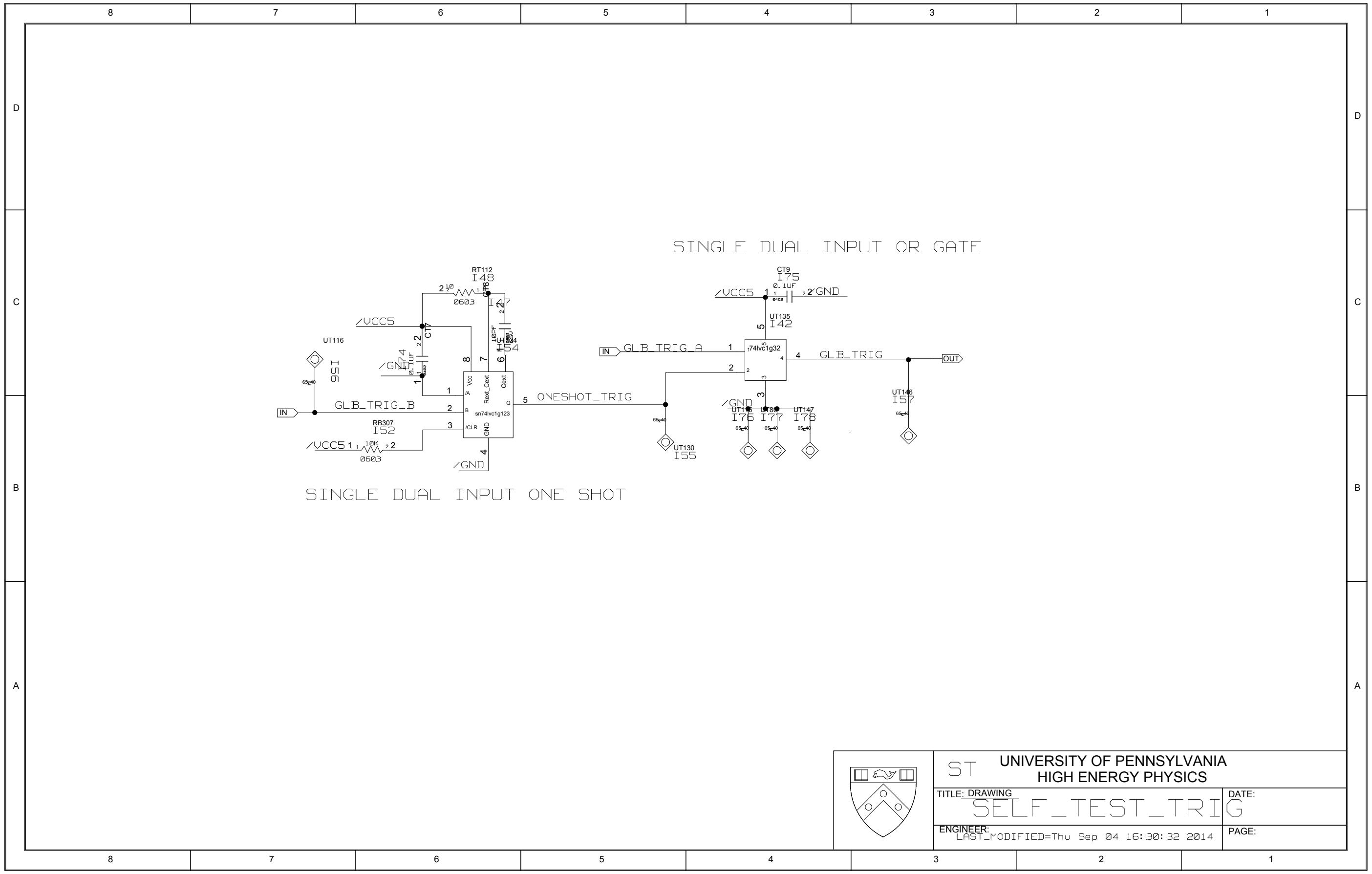
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OUT
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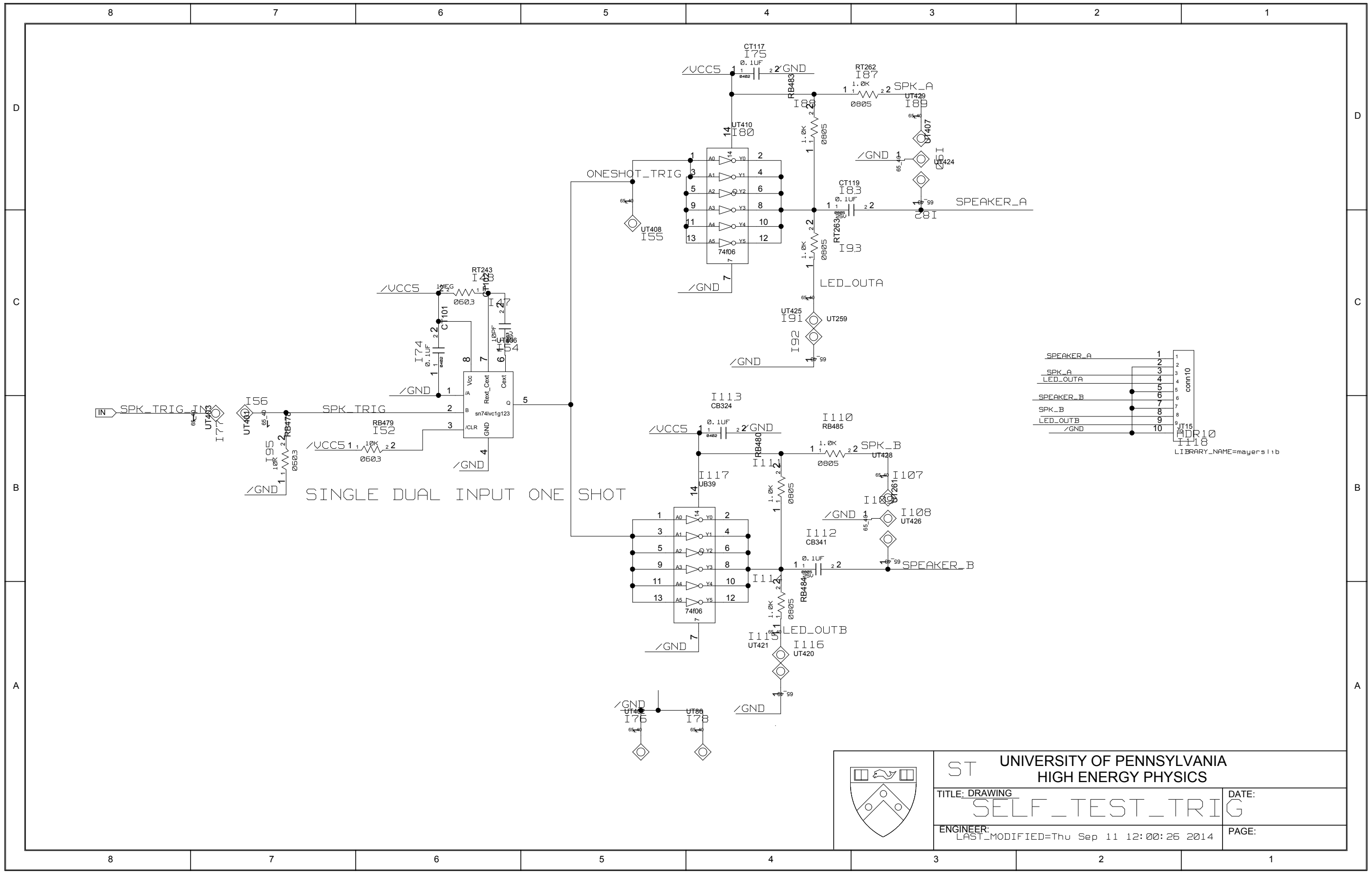
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