ProtoDUNE-SP Trigger and Timing System

Dave Newbold, for Bristol, Oxford, UPenn, W&M groups

ProtoDUNE DAQ Review

3rd November 2016

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Contents

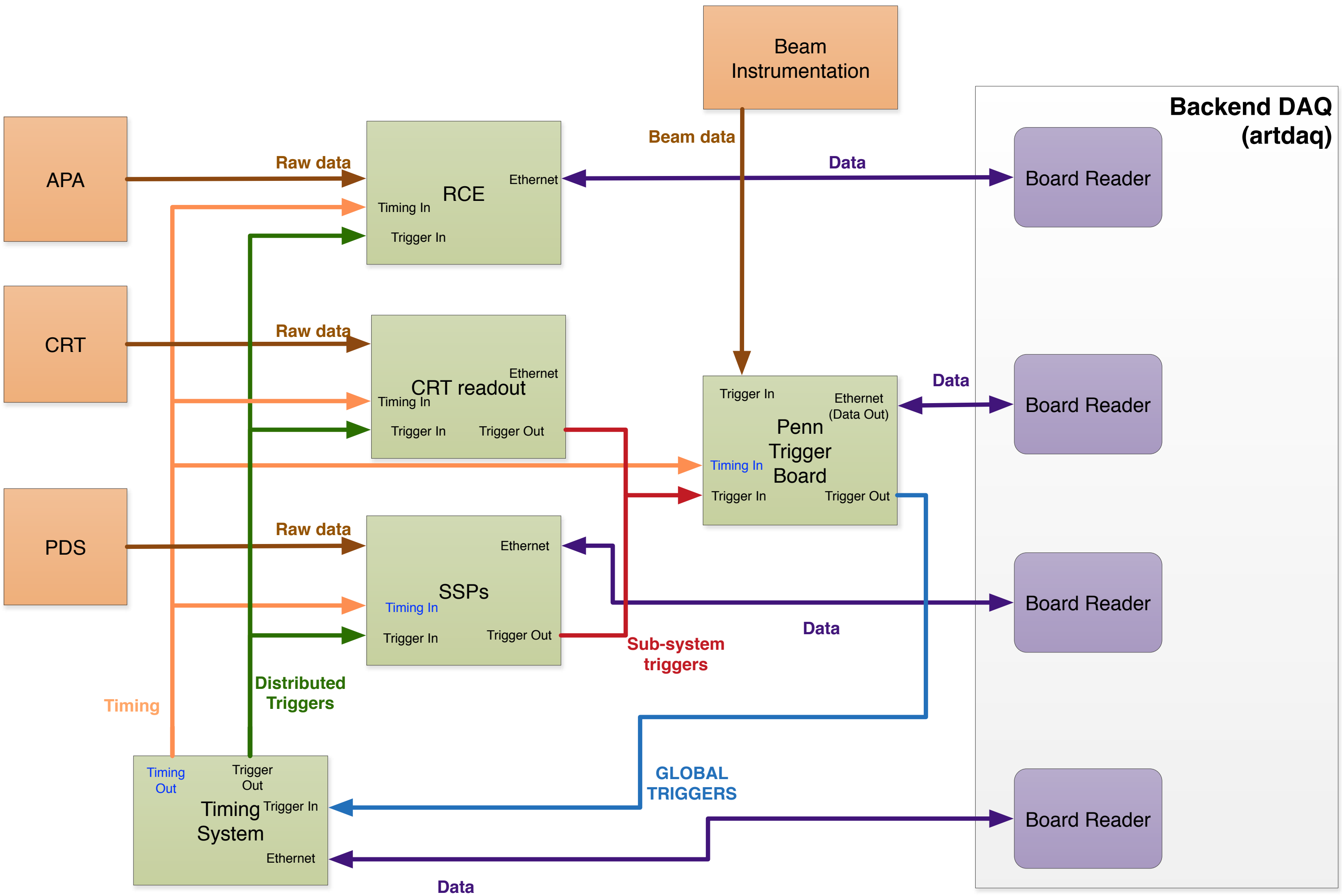
- Introduction & specification
- Summary of status
- For {trigger, timing system}
  - Interfaces
  - Design
  - Implementation
  - Testing
- Risks

- Trigger documentation: DUNE-doc-1583-v1
- Timing protocol and interface specification: DUNE-doc-1651-v3

Introduction

- ProtoDUNE-SP runs in externally triggered, synchronous mode
  - Physics and performance criteria require a beam trigger
  - Readout systems must be closely synchronised in time
  - For simplicity, operate with single common phase-aligned clock
- Two closely-coupled systems
  - Trigger system (CTB) interfaces to beam instrumentation and other fast signals, produces trigger primitives (Penn)
  - Timing system distributes common 50MHz detector clock, along with synchronisation and trigger commands (Bristol)
- The trigger and timing are the ‘heart of the system’
  - Emphasise simplicity; robustness; flexibility; early availability

System Overview



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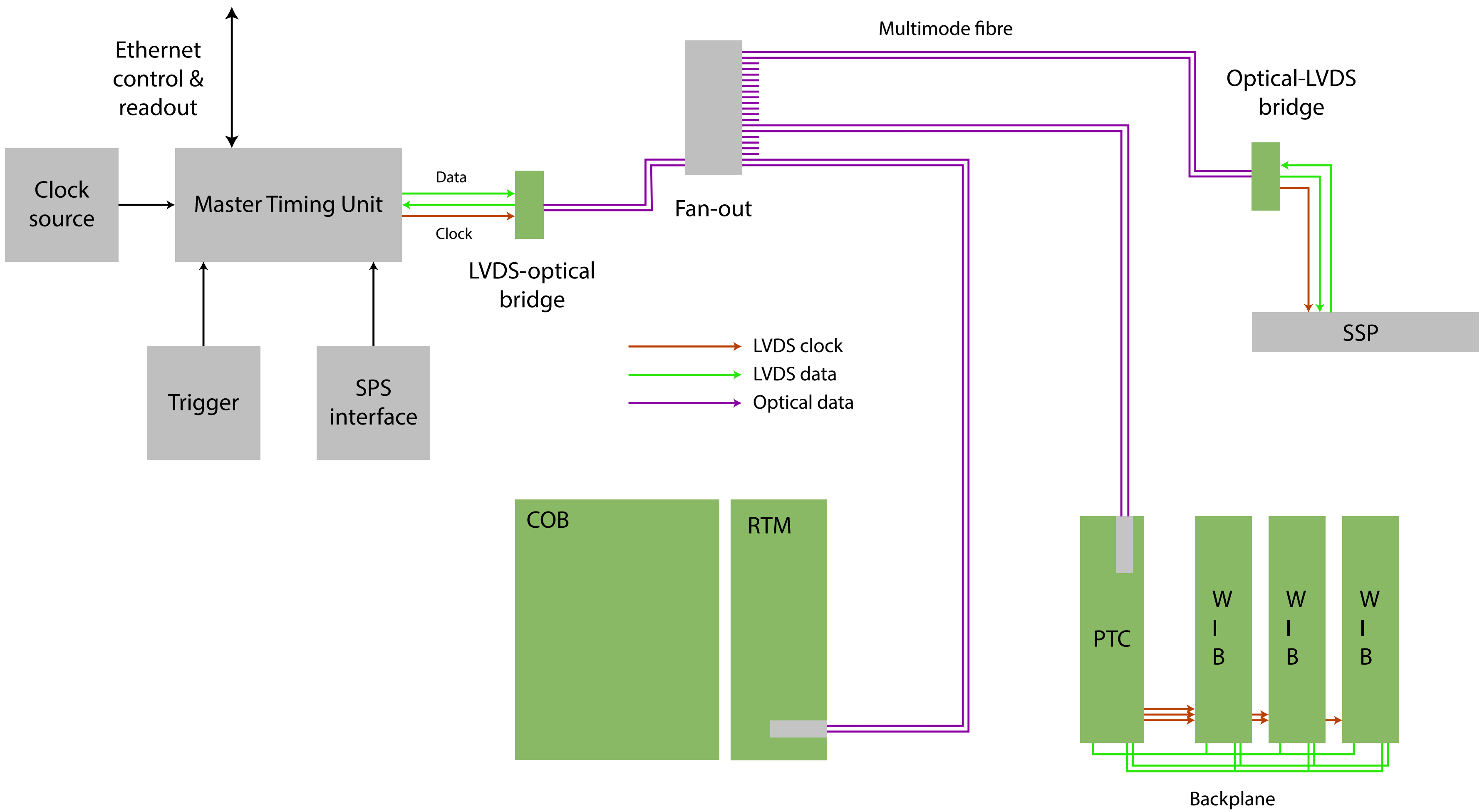
Timing System View



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Summary of Status and Schedule

- Trigger
  - Existing hardware, firmware, software successfully used in 35t
  - Modest firmware and timing changes for ProtoDUNE-SP
  - Work well under way to finalise hardware interfaces
- Timing system
  - New system, re-using proven hardware and firmware components
    - Interfaces to ‘endpoints’ (readout boards) necessarily vary
  - Integration of hardware and firmware components under way
    - Functional prototype: Dec 2016; extended functions Feb 2017
    - Final hardware: Apr 2017; Installation: June 2017
  - Software is at an earlier stage, but not expected to be critical path

Specification

- CTB
  - Receive {BI, CRT, PDS} input
  - Sample and re-sync to ProtoDUNE clock domain where necessary
  - Logic and coincidence finding to form global trigger
  - Time stamp input hits and triggers, keep event count, record trigger type, error conditions – and stream to DAQ
- Timing
  - Distribute high quality clock, and synchronisation signals
  - Issue trigger, calibration and state change signals
  - Monitor timing alignment of all system components
  - Throttle triggers under software or back-pressure control if needed
  - Time-stamp all received and issued signals – and stream to DAQ
- Operate with nominal 25Hz trigger rate (but can cope with far higher)

Trigger: Interfaces

- The interfaces are mostly the same as in DUNE 35t
- Changes needed:
  - Front-end interface (different I/O logic), including timing
  - Firmware (different trigger and readout logic)
- Details of interface to each sub-system currently being collected:
  - CRT provides 40 trigger signals
  - PDS provides 24 trigger signals
  - Beam provides < 12 input signals
  - Timing interface (bi-directional) via standard serial timing link
  - No trigger from TPC (too slow)

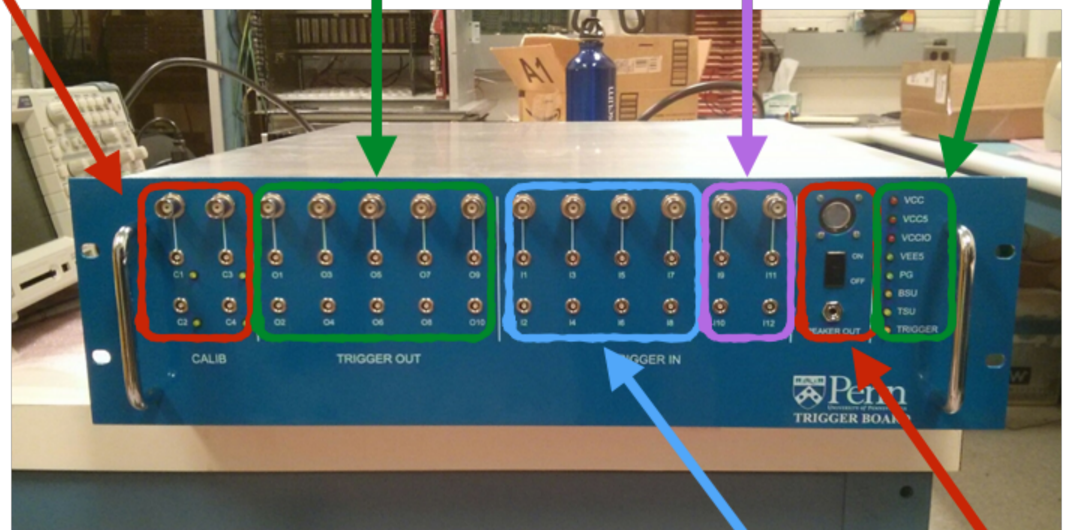
Trigger: Physical Interface (Front)

Calibration outputs (4 ind.)

Trigger output pulse (10 ORed)

Trigger inputs (4 ind.)

Info LED's



- calibration and trigger I/O uses LEMO connectors with **NIM logic**
  - Half the connectors are also wired to a BNC connector (just in case)

Trigger inputs (8 ORed)

Speaker

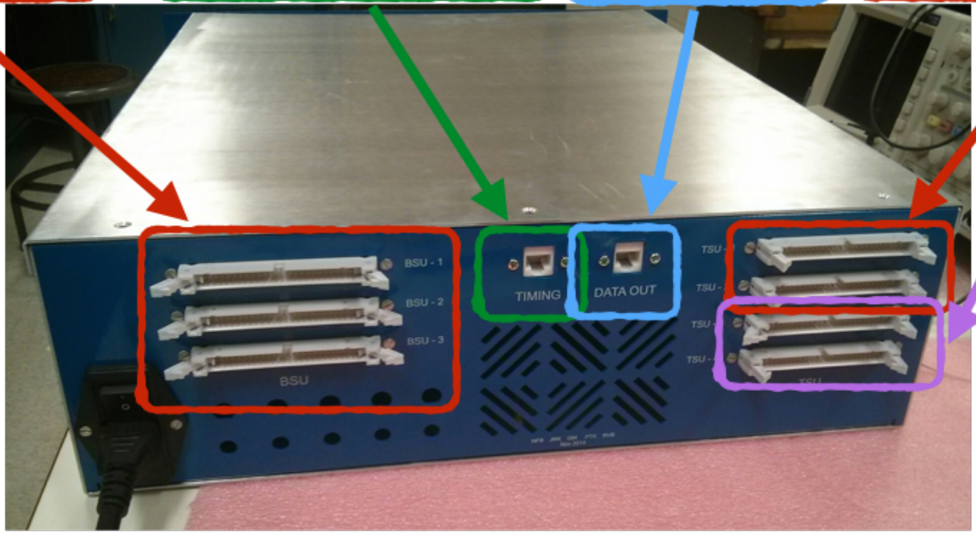
Trigger: Physical Interface (Back)

BSU input
(3x 50-pin - 50 ch.)

NOvA timing input
(RJ-45 - 4 diff. LVDS)

Ethernet Data
Out

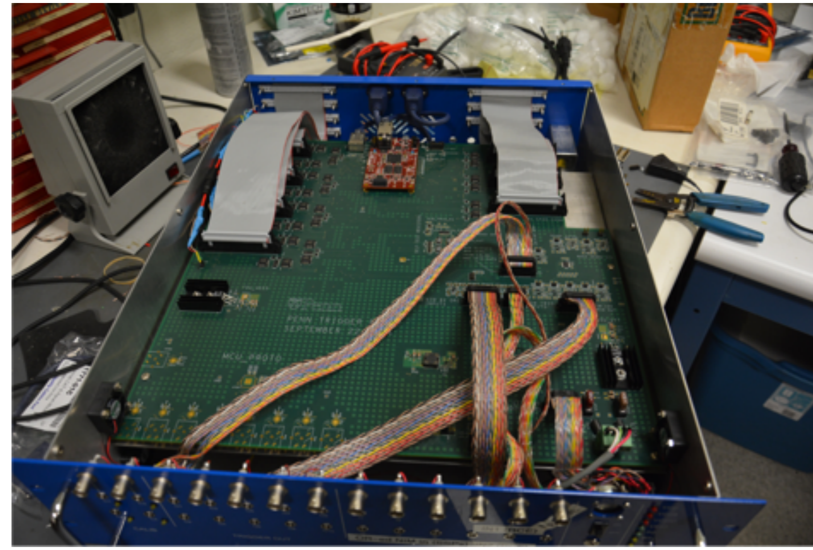
TSU input
(4x 50-pin - 48 ch.)

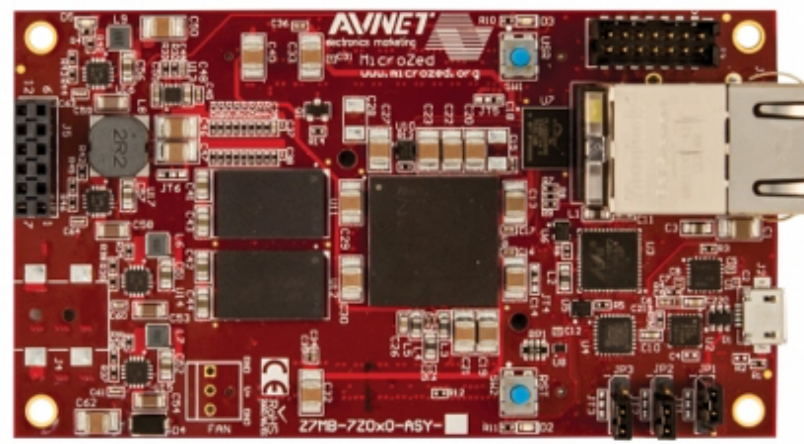


- Ribbon cable inputs in differential ECL
  - TSU's are AND-ed in pairs on the hardware

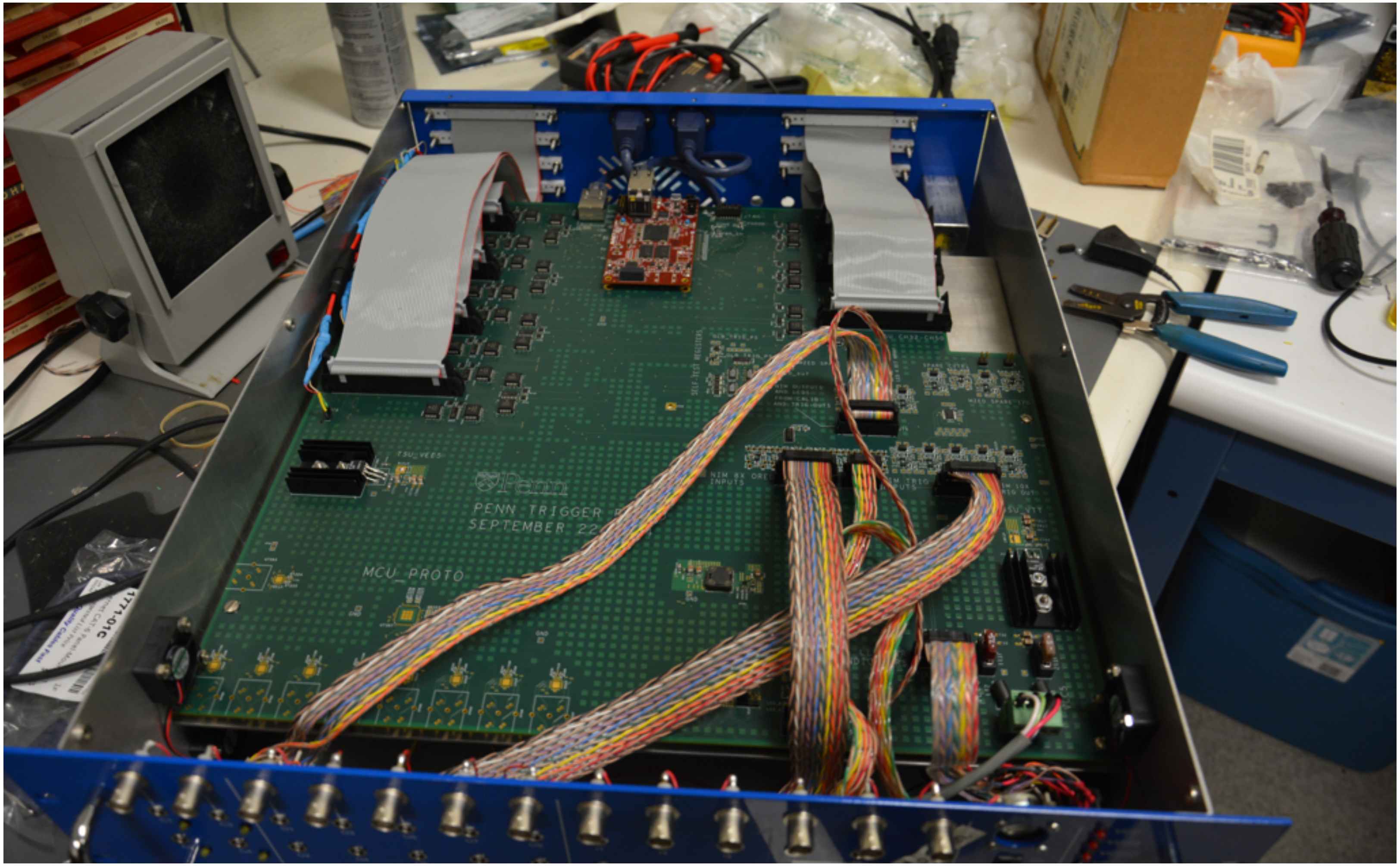
Trigger: Implementation (HW)

- Xilinx Zynq-7Z020 SoC
  - 1 GB DDR3 RAM
  - Gigabit Ethernet
  - 2 ARM Cortex-A9 cores
  - The CTB runs a linux distribution inside
  - Most of existing firmware and software will be re-used
- Rest of hardware is physical interface to FPGA module

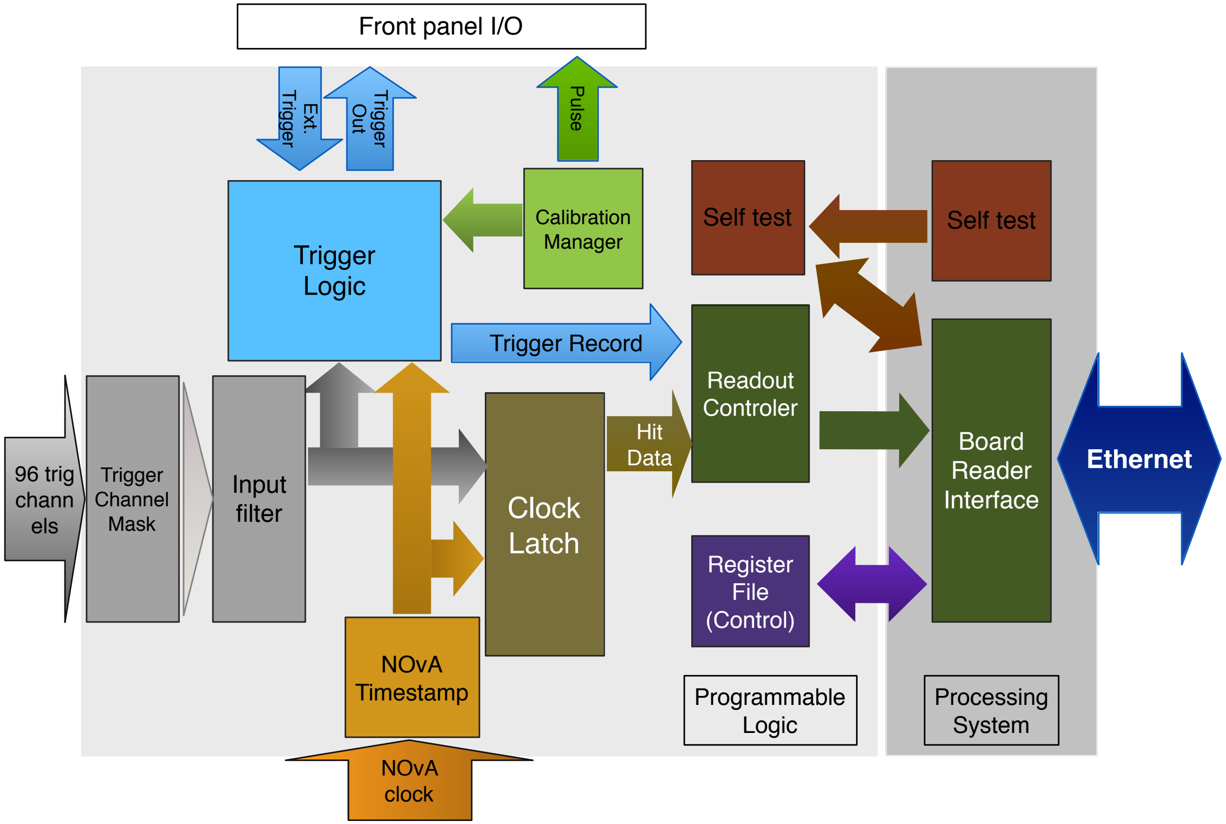




Trigger: Implementation (HW)

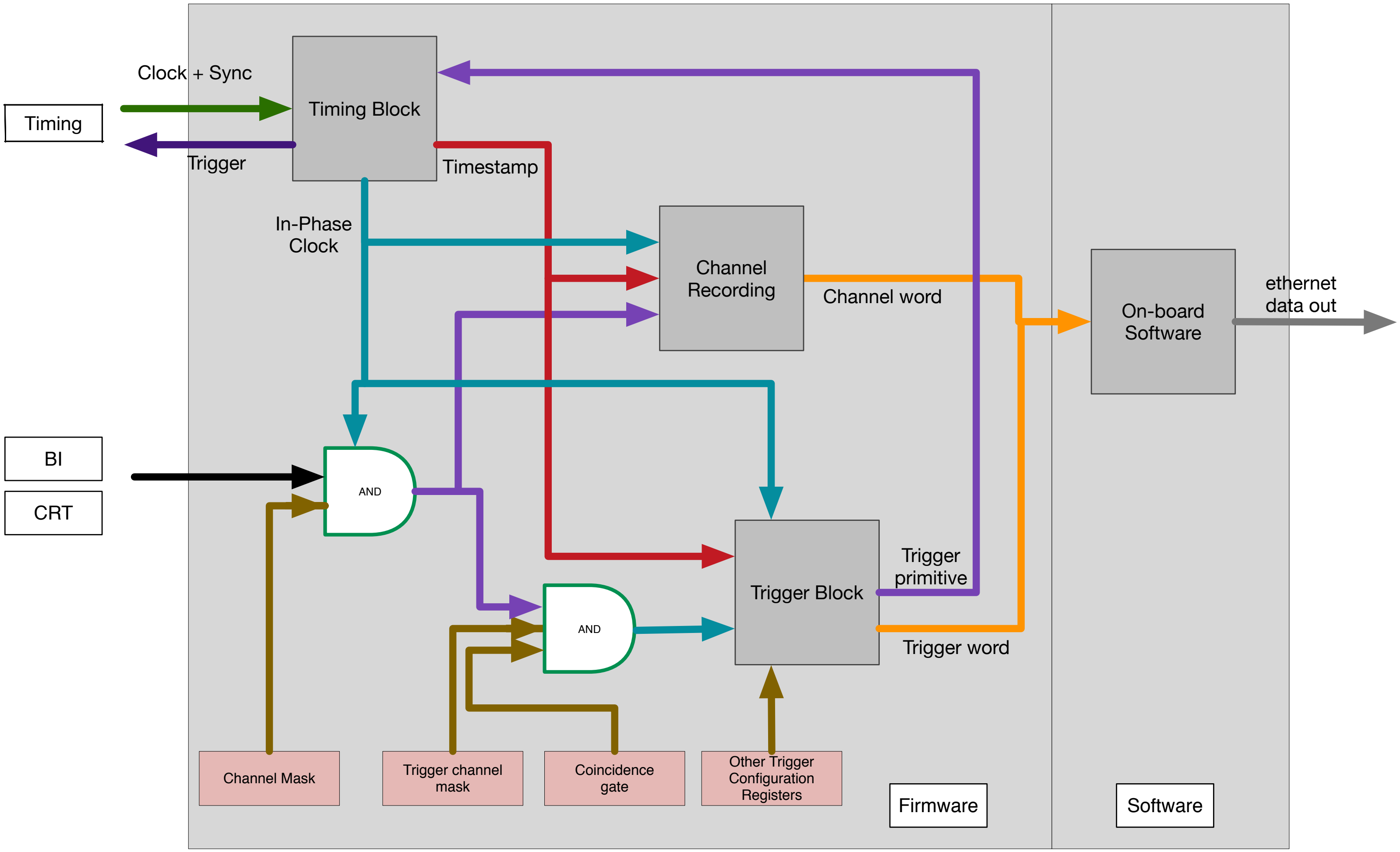


Trigger: Implementation (FW)



- Most of the firmware remains unchanged from 35t
  - Rewrite trigger / timing block / data structure

Trigger: Implementation (FW)



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Trigger: Testing

- Remaining steps for definition of final system:
  - Finalize definition of input counts and characteristics (Nov 2016)
  - HW (interface) and FW modifications for timing (Nov 2016)
  - Definition and implementation of trigger conditions (Mar 2017)
- Testing programme:
  - At UPenn (by Jan 2017)
    - “smoke tests” of hardware modifications
    - Logical tests; functional tests with pulser
  - At CERN:
    - Installation (June 2017)
    - Functional tests in test stand with artdaq (Oct 2017)
    - Integration tests with other systems, incl. timing (Dec 2017)

Timing: Master Interfaces

- Master clock source
  - 10MHz reference, time-of-day via fibre from SPS control room
  - This ensures synchronisation with beam instrumentation
- Trigger system
  - Interface via copper serial interface; boxes are adjacent
- Condition signals
  - e.g. SPS start-of-spill warning, NIM format
- Control and DAQ
  - Gigabit Ethernet
  - A rolling record of all received and issued timing signals is kept
- Downstream timing system
  - Multimode optical fibre, consistent with detector grounding scheme

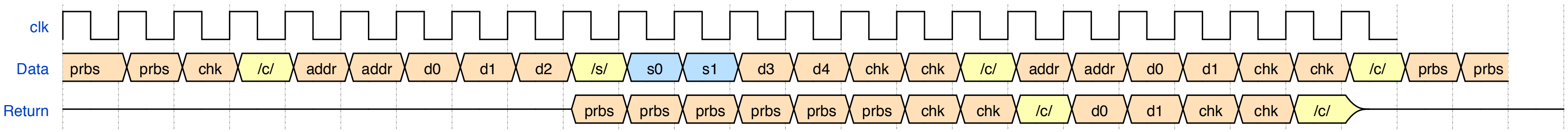
Timing: Endpoint Interfaces

- Timing protocol
    - Clock and data are carried as a single 8b10b encoded optical signal
    - 500Mb/s data rate
        - Allows use of COTS optics components (SFP modules)
    - Return path allows self-test, accurate phase alignment (<1ns)
- Endpoint interfaces
    - Style 1: direct optical connection (COB, WIB-PTC)
    - Style 2: LVDS connection, via converter card (SSP, muon veto)
        - Electrically backward-compatible with NOvA interface
        - Protocol is not compatible; firmware-level change

Timing: Design

- Protocol design
  - Uses concepts from CERN TTC, NOvA, SOLID
  - Higher performance design using modern COTS components
  - Suitable for optical (MM/SM) or galvanic transmission
  - ProtoDUNE will be a testbed for DUNE timing system
- Hardware design
  - COTS FPGA hardware; avoids substantial design effort
  - Timing system specific functions integrated onto single multi-purpose FMC module
  - AIDA TLU module re-used as general IO interface
- Firmware and control interface design
  - Based around well-tested IPbus control / SoC system
  - In use in ~15 experiments at CERN, FNAL, and elsewhere

Timing Protocol



- On the wire:
  - 500Mb/s 8b10b encoded signal, DC-balanced, optical (850nm) or galvanic
    - Compatible with COTS optics, connectors, clock recovery devices
  - Forward and return paths for two-way communication
  - “Intra-FPGA” firmware implementation has been thoroughly tested
- Two command types
  - Synchronous cmds pre-empt other traffic, propagate with *fixed latency* of <1us
    - Fundamental commands: ‘reset timestamp counter’, ‘trigger’
  - Asynchronous cmd for internal and endpoint control, system setup
  - Master FW receives cmds from SW, trigger, sync state machine; arbitrates

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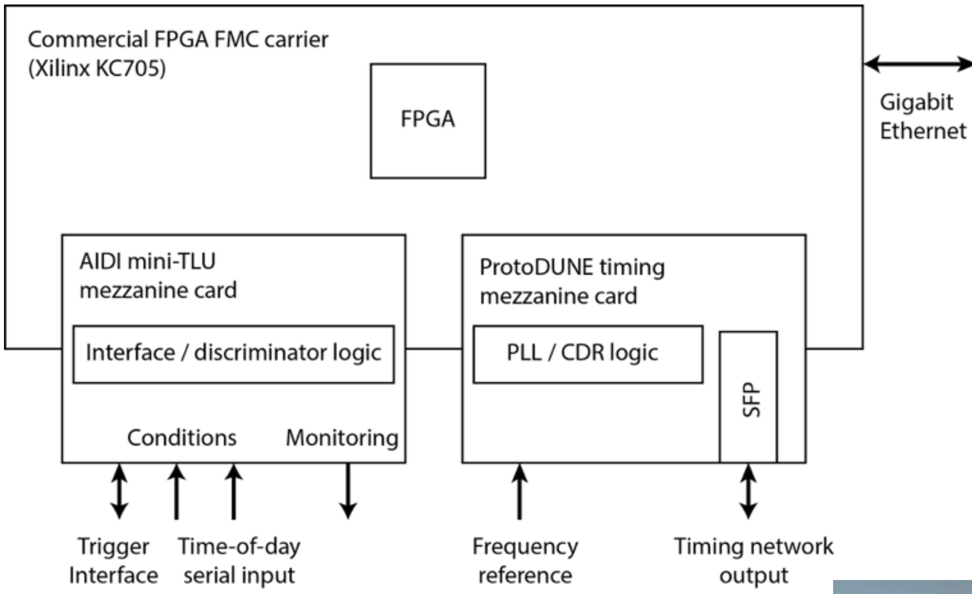
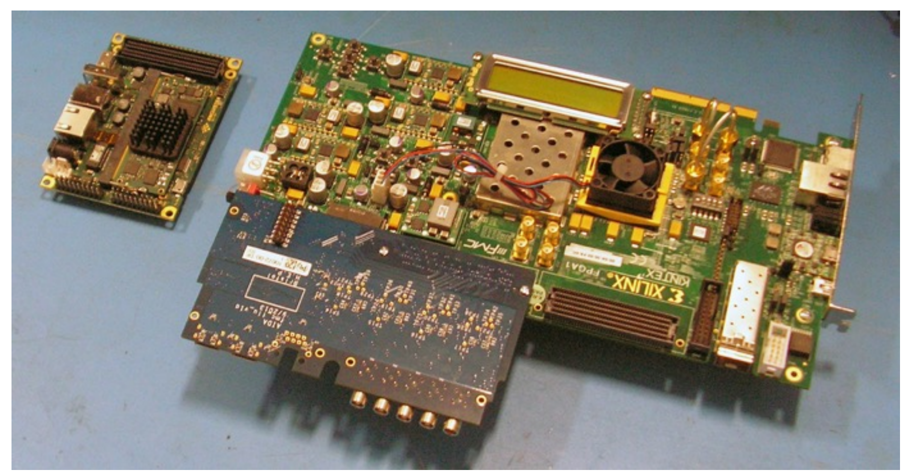
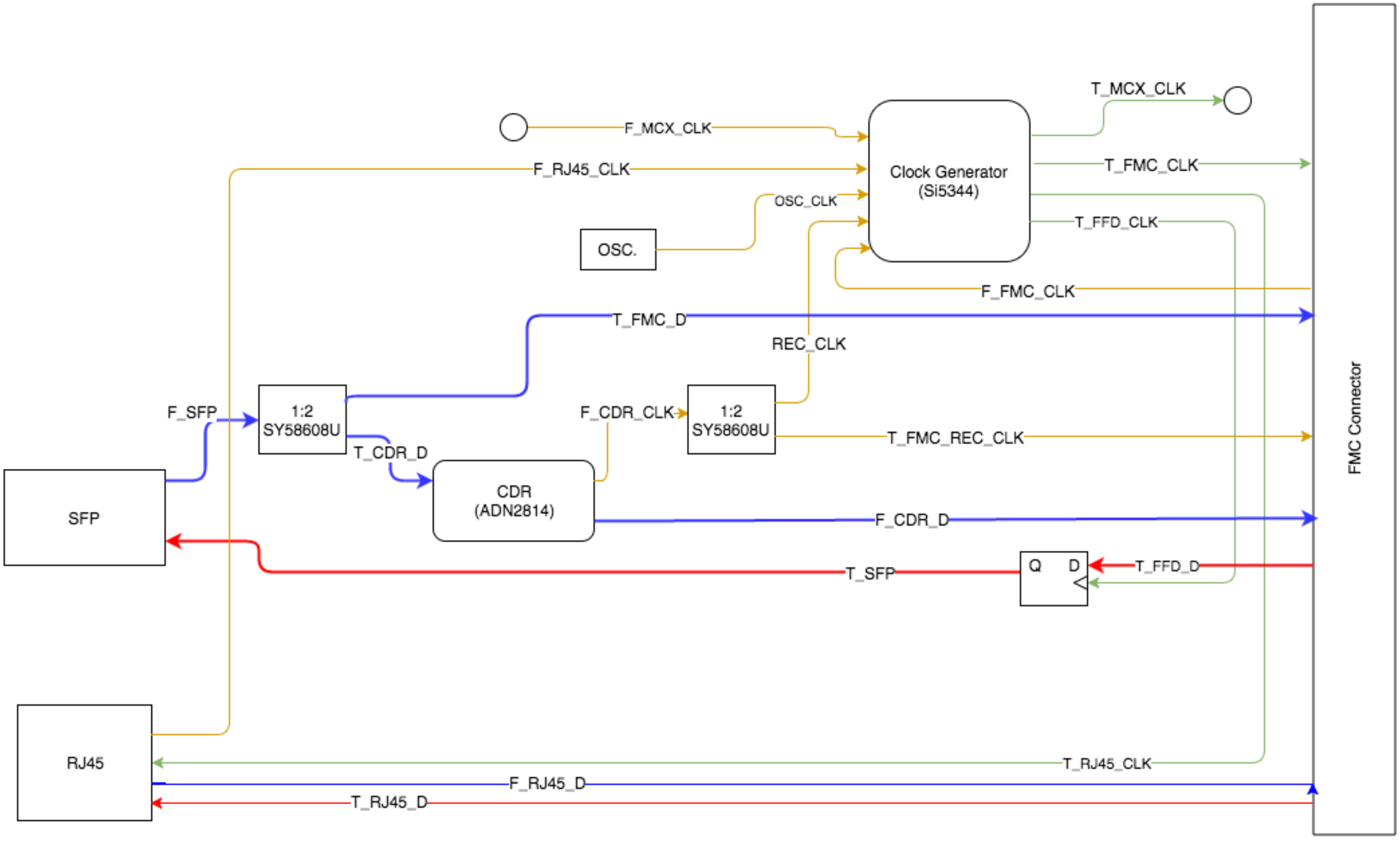
Timing: Master Implementation

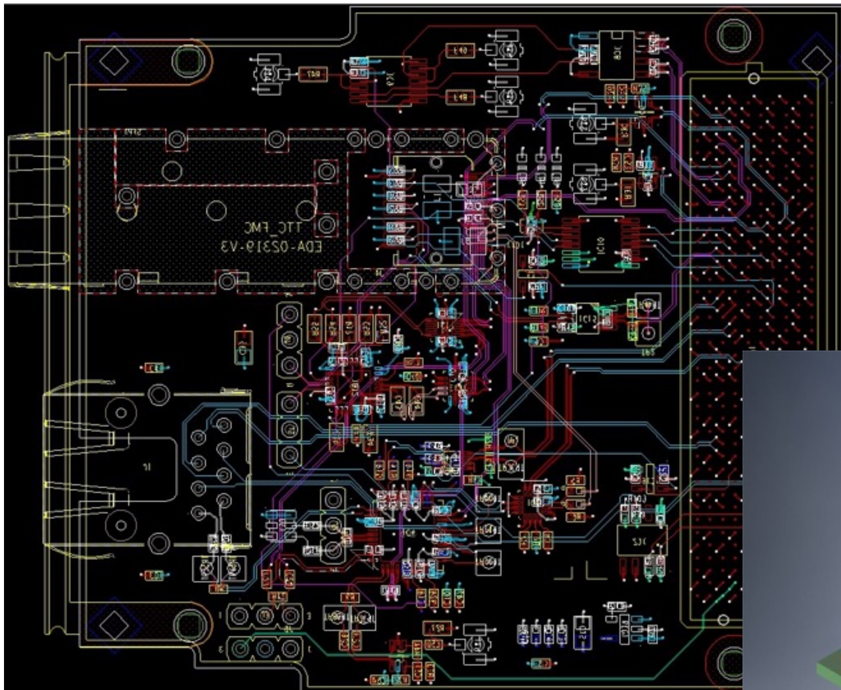


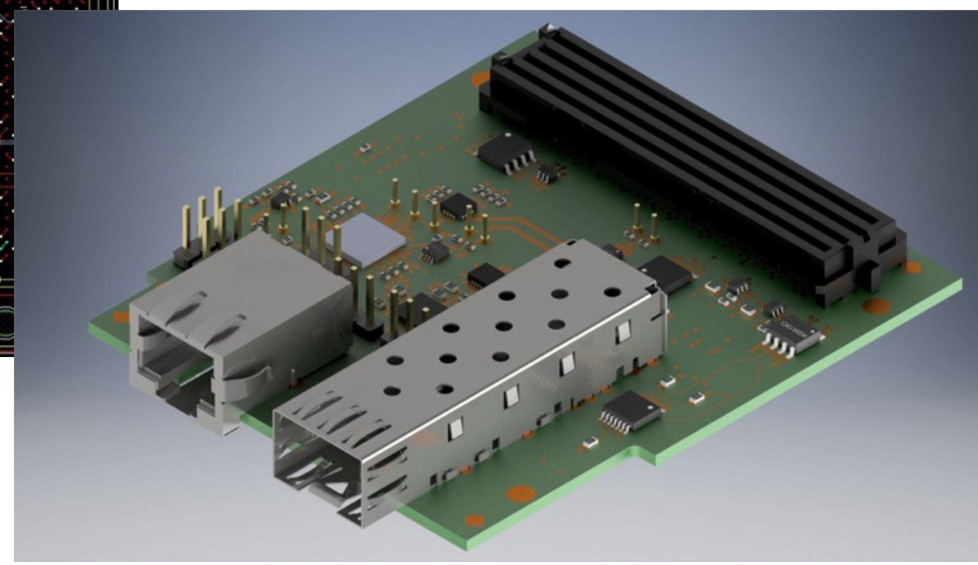


Timing: FMC Implementation



Timing: FMC Implementation



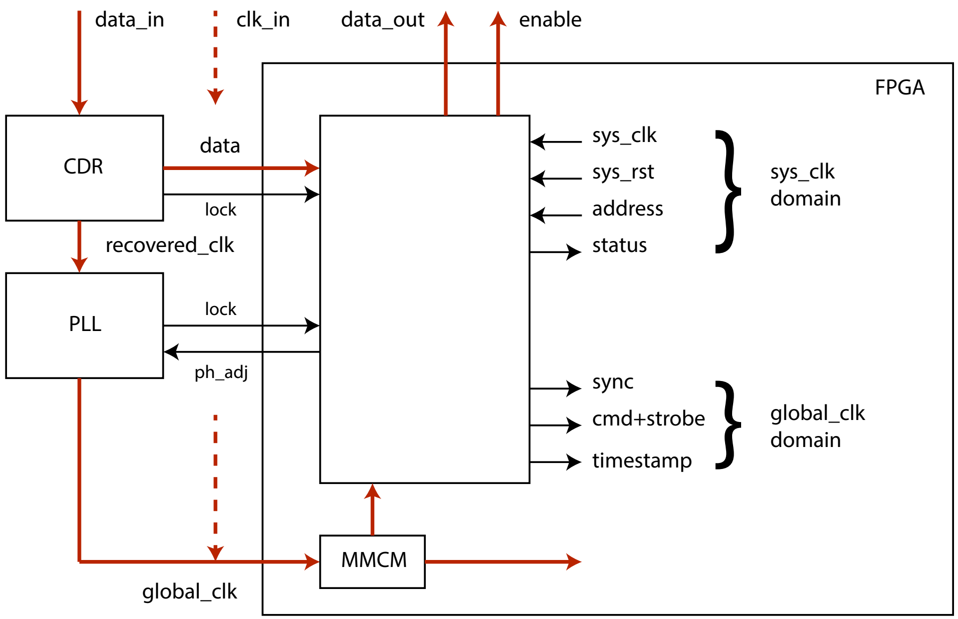


- Cards expected in Bristol this week

Timing: Distribution

- For test-stands
  - Passive COTS optical splitter / combiner will run up to 16 endpoints
  - Limit is from optical power budget of SFPs
- Final system has ~48 endpoints, plus spare capacity for safety
- Concept A: passive optical splitter / combiner
  - Simple, familiar technology
  - Commercial external laser head for power budget - safety implications
- Concept B: active fan-out / fan-in based on COTS FPGA board
  - Requires additional HW; slightly worse jitter performance
  - Laser safety no issue; allows flexible back-pressure system if needed
- We favour Concept B, as long as schedule can accommodate it
  - Final decision in Feb 2017

Timing: Endpoint Implementation



- Endpoints receive:
  - Phase-aligned clock from external or FPGA PLL
  - Synchronous trigger and timing signals, aligned to ~1ns across system
  - Setup and control data in packet format
- Endpoints transmit:
  - Status information; back pressure signals if required

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Timing: Endpoint Implementation

- WIB, COB
  - Timing interface (optical via SFP) built into PTC / RTM
  - WIB design includes jitter-reducing PLL; not required for RCE
    - System clock jitter expected to be <100ps
- SSP, other systems
  - Timing FMC used as ‘bridge’ to LVDS interface compatible at hardware level with NOvA – jitter-reducing PLL available if needed
  - Low-cost FPGA carrier + timing FMC used for this purpose
- Protocol decoder
  - Common firmware block provided by timing developers
  - Well-defined interface to readout board firmware agreed with all parties
  - Timing group system allows flexible partitioning

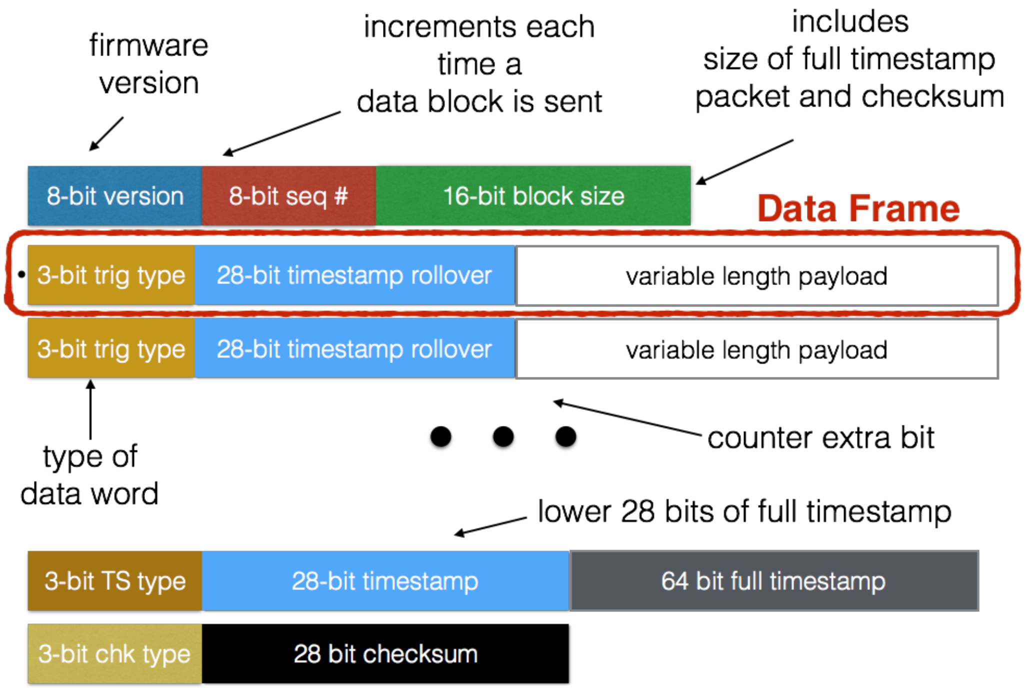
Timing: Testing

- Hardware
  - Timing system interfaces defined, agreed, documented
  - First prototype timing FMCs received in Bristol this week
  - Emphasis is on rapid HW testing in coming weeks, then distribution for test stands
- Firmware
  - Protocol, clock control, physical interfaces already implemented on existing hw
  - IPbus test harness implemented – sufficient functionality for integration / test stands
  - 'Upper layer' functions, trigger interface, phase alignment implemented by Feb 17
    - Rolling firmware updates to be applied in test stands as we progress
- QA
  - Correct operation of timing system is critical for operations and good data
  - System is designed for comprehensive and continuous self-test

Software

- CTB
  - Readout with artdaq exists from 35t, largely unchanged
  - Software runs on-board, on full linux OS
    - Allows development on any machine
- Timing
  - Software at an earlier stage of development
  - Experienced Oxford team working on this from Nov 2016
  - Control is via established IPbus protocol, software runs on PC
  - JCOP-IPbus bridge already exists
    - A 'thin layer' on top of this will need to be implemented
  - artdaq readout module needs to be implemented

Data Format



- CTB 35t format shown above - no major modifications
- Timing system format will be in same style
- Neither trigger nor timing will be major contributors to data volume
  - Expected to be <1MB/s, easily within capabilities of interfaces and SW

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Risks Summary

- Further interface or specification changes
  - Regime of formal documentation for interfaces
  - Specification is now fixed, controlled changes only
- Availability of expert personnel
  - Schedule is not dependent on any individual at this point
- Delays in hardware supply chain or production
  - Schedule has adequate contingency; if needed, testing can proceed with prototype hardware (already in our hands)
- Failure of electronic integration review (e.g. grounding issue)
  - We have taken a conservative approach
  - Schedule allows re-working of hardware after June 17 if needed
- Physical failure of installed system
  - Provide spares at CERN and on-site expert support throughout running period

Conclusion: Charge

- *Does the DAQ meet the science and engineering requirements?*
  - Confident that we have an appropriate design for T&T ✓
- *Does the design provide sufficient flexibility for alternates?*
  - Interfaces cannot change now, implementation more flexible ✓
  - Sufficient capacity for increase of rate and / or throttling ✓
- *Are the requirements sufficiently complete and clear?* ✓
- *Are risks captured and is there a plan for managing risks?*
  - Risks identified, risk register is being finalised and updated
- *Is production schedule reasonable?*
  - Prototypes of hardware available now ✓
  - Final versions available on an attainable schedule ✓

Conclusion: Charge

- *Does schedule allow sufficient time for testing of other components?*
  - Schedule planned around testing regime – target is June 2017 ✓
- *Is the documentation of the system comprehensive?*
  - Largely complete, a few details still to document
- *Are all interfaces to other systems understood?* ✓
- *Is grounding and shielding understood?* ✓
- *Is the software architecture suitable? Sufficient resources for software?*
  - Software for timing under definition, effort is more than adequate ✓
- *Are the specifications of hardware complete?* ✓
- *Are operation conditions understood?*
  - The nominal conditions are firm, but we reserve flexibility in T&T ✓

Conclusion: Charge

- *Are proposed triggering schemes sufficiently well understood?*
  - Detailed logical flow under definition
  - Flexible system can cope with any reasonable request ✓
- *Is the installation plan sufficiently well developed? Are the DAQ quality control test plans sufficient?*
  - Groups have stringent quality control plans in place for deliverables ✓
  - System is designed for self-test from the start ✓
  - Detailed installation planning under way

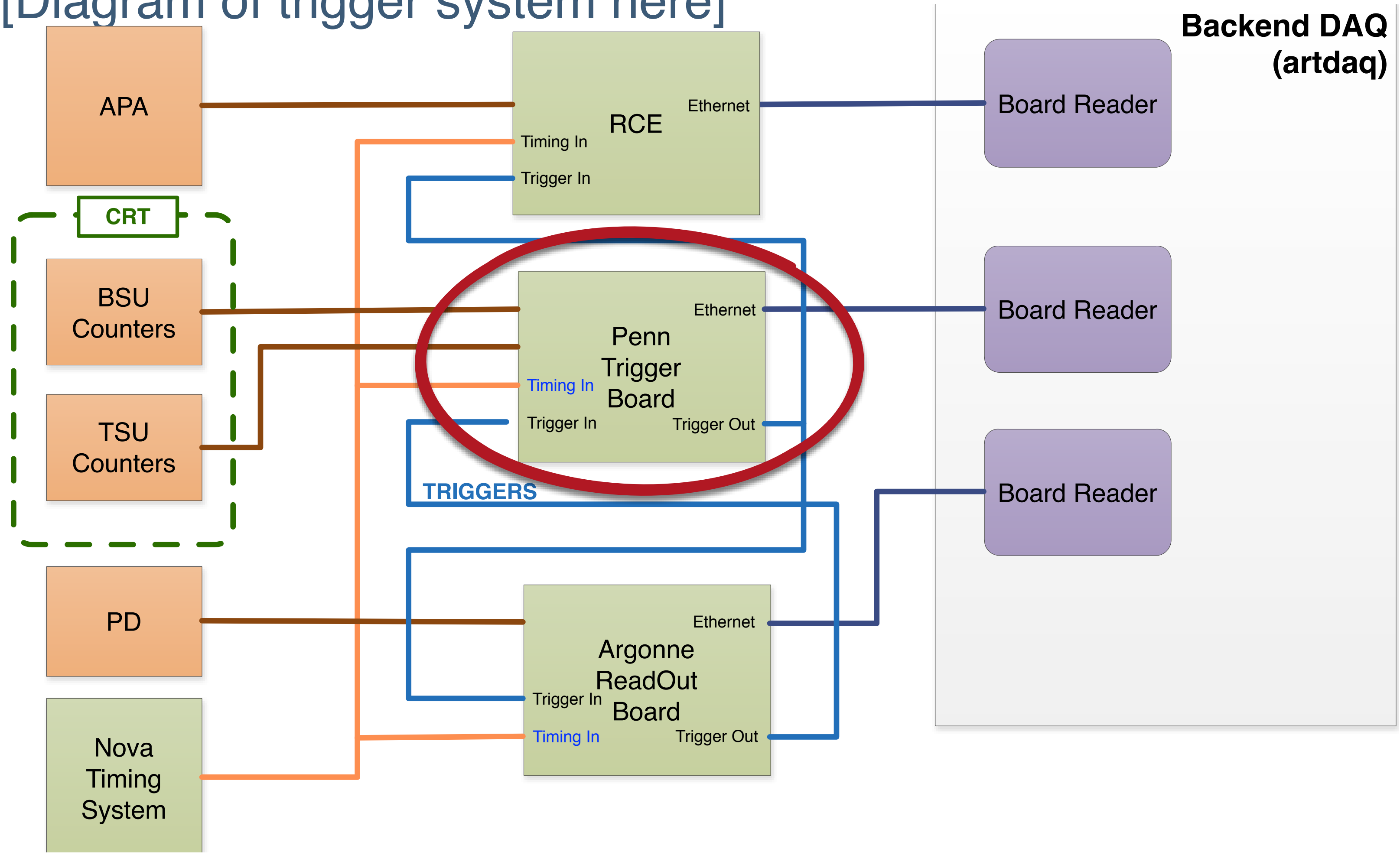
Conclusion: Schedule

- Scope and requirements for trigger and timing are well understood
  - Final technical details of HW, FW, SW interfaces being formally documented and agreed
- Development of systems is well advanced, with experienced teams
- CTB is a modest modification of 35t system
  - New system available in Jun 2017
- Timing is a new development, using well-known technologies
  - Prototypes for test stands Dec 2016; final system Jun 2017
- Trigger and timing need to be robust, flexible, available
  - Schedule therefore has large built-in contingency
  - Support for system testing will be the major task late 2017 onwards
    - Expect to adapt to new requirements, conditions, as they arise
    - FW and SW modifications will be made as needed

Backup

Trigger Overview (35t)

- [Diagram of trigger system here]



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CTB Software Flow

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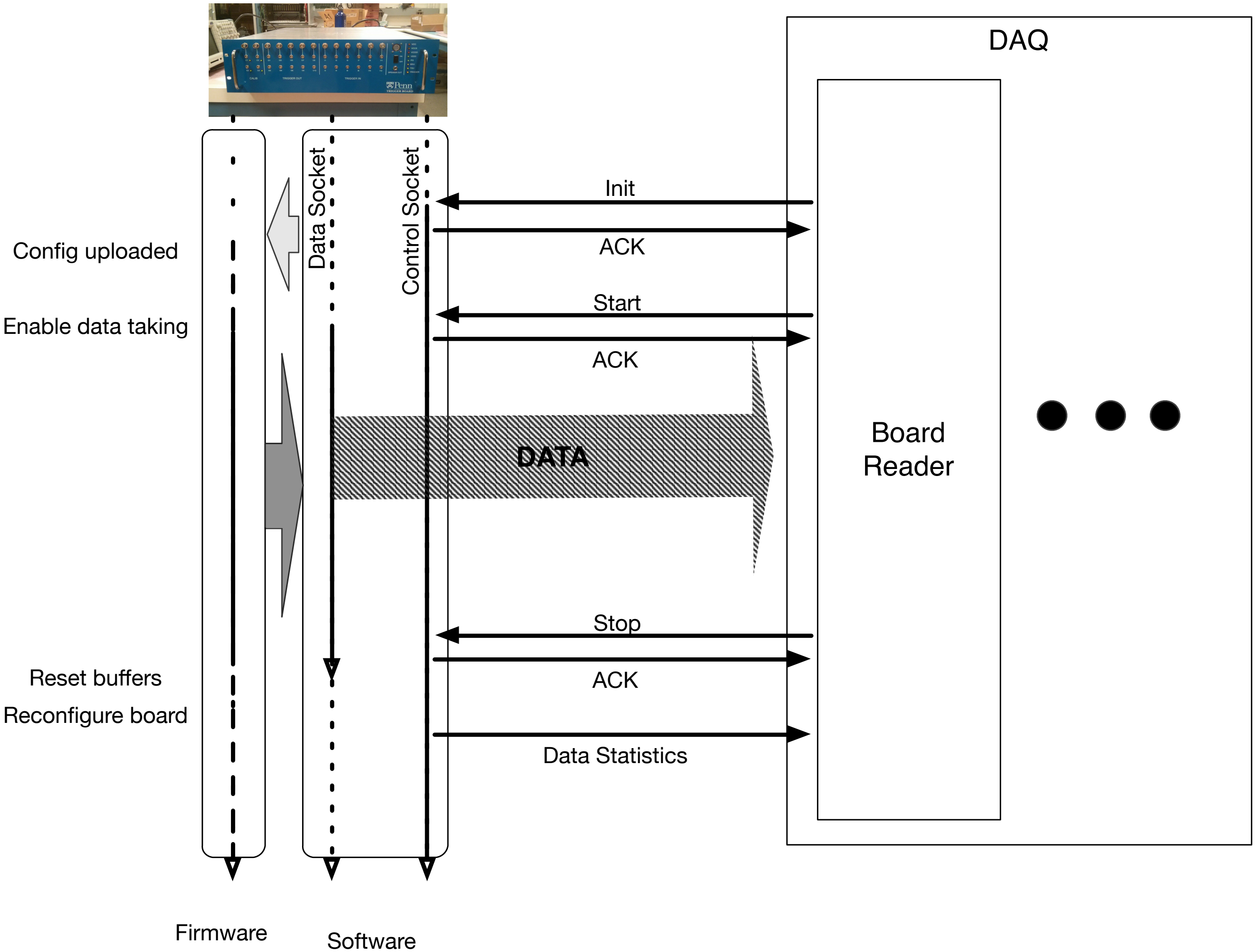

Endpoint Firmware