ProtoDUNE Muon Counter system

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I. NEED IN PROTODUNE FOR A MUON COUNTER SYSTEM

In the ProtoDUNE detector there is a need for a muon counter positioned in front and back of the TPC to better understand the muon coming in the beam and there is also a need for a cosmic muon veto on top of the TPC to deal with the fact that the detector is on the surface and a further reduction of cosmic rays in the beam spill can be needed. Tagging cosmic muon will also be useful during the commissioning of the detector for understanding the behavior of the TPC and monitor the purity of the liquid Ar and reconstruction efficiency.

II. MUON COUNTER - READOUT SYSTEM

The Muon Counter's (MC) readout system consists of a front-end electronics board (FEB) attached to each MAPMT (photomultiplier tubes with 64 individual channels) and a back-end USB module directly connected to a PC. The system can also be equipped with a trigger board to provide a second level trigger based on the info from multiple pmt board.

A. PMT Board

Each MC scintillator module is connected to a single PMT Board. All the PMT boards are then linked together with Cat5e cables and connected to a USB readout board. The USB board is then connected to a PC. A token passing scheme is used to readout serial data into the USB hub-module: in case a PMT-module has no data, the token is passed forward. If instead a PMT-module has data, it reads-out the next triggered event from the hit-pattern-fifo and the ADC-fifo, and then passes the token to the next PMT-module. Each PMT module also receives 2 analog signals (NIM signal -800 mV of amplitude): clock, gate/sync and provide a trigger output made of the OR of the 64 Maroc2 channels. The clock signal is a 62.5 MHz signal, that simply increments an internal counter. The other input discriminates between input signal based on the width of the signal received. If the width of the signal is less than 16 ns the signal is defined and treated internally as a sync signal. If instead the signal's width is more than 32 ns (two clock's cycles) the signal is interpreted as a gate. The sync signal is used to synchronized all the different PMT's boards that belong to the same or to a different daisy chain and simply reset the clock counter. The gate is used only in certain types of data acquisition modes and will be explained later on in this section.

An interlock-wire in the link checks that all modules are active and connected. The 62.5 MHz system clock and sync-pulse are fanned-out and individually connected to each PM-module with coax-cable.

The PMT boards also host an LV connector and needs a power of 6 V to correctly operate. A voltage regulator is installed on the power line and enables the board to able to accept a range of voltage between $5.8 - 6.2$ V and protects the board itself from overvoltages.

1. Maroc2

The Maroc2 chip discriminates the 64 outputs from the H7546 MAPMT. The Maroc2 chip also incorporates a slow-shaper with a track-and-hold for each input, and a multiplexed output for an external ADC. The slow-shaper peaking time provides a delay for holding the outputs for digitization. The 64 time-over-threshold outputs from the Maroc2 connect to an FPGA where they are latched and/or connected to form a trigger. The trigger-hit pattern, along with a 32 bit 16 ns/bit time-stamp are written to a fifo for readout. In addition, the trigger sends a hold level to the Maroc2 and writes the multiplexed ADC data, with time-stamp, to a second fifo. The trigger-hit pattern determines which of the 64 ADC outputs are written along with a pm-channel number. For reference see [1]. The second version of MAROC chip is a 64 channels input front end circuit based on AMS $Si - Ge$ 0.35mm technology and developed with a CQFP240 package. It has an area of $16mm^2$ ($4mm \times 4mm$) and operates with 3.5 V power supply. For each of the 64 channels, the PMT signal is first amplified thanks to a variable gain preamplifier which has low noise and low input impedance (super common base inputs) to minimize crosstalk. It allows compensating for the PM gain dispersion up to a factor 4 to an accuracy of 6% with 6 bits. The amplified current then feeds a slow shaper combined with two Sample and Hold buffers to store the charge in 2 pF and provide (5 MHz) an analog and digital multiplexed charge output up to 5 pC. The digital charge output is provided by a 12 bit ADC Wilkinson. In parallel, 64 trigger outputs are produced via fast channels made of a fast (15 ns) shaper followed by three discriminators. The discriminator thresholds are set by an internal 10 bit DAC, made of a 4 bit thermometer DAC for coarse tuning and a 6 bit mirror for fine tuning. They have respectively steps of 200 and 3 mV per bit. The trigger outputs correspond either to the response of a single discriminator (DAC1) or to an encoded response from the three DACs.

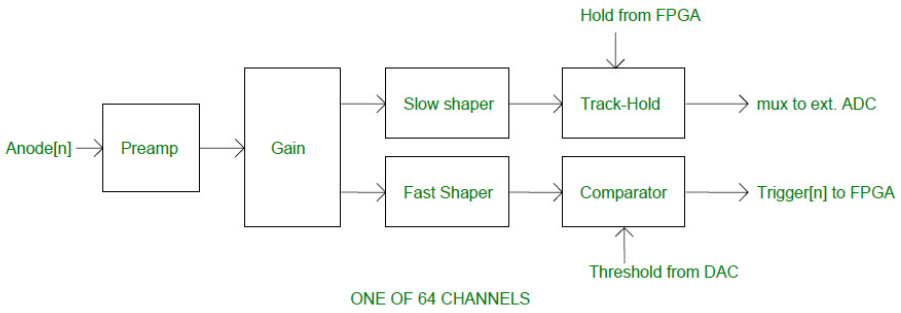

FIG. 1. Maroc2 diagram for one of the 64 channels

Figure 1 shows the Maroc2 diagram for one of the 64 available channels. The preamplifier input is 50 Ω in series with the pm-anode, offset from ground by 0.8 V. The preamplifier copies the input current to the gain-block where each pm channel gain can be corrected from 0 to x4 with a 6-bit parameter. The gain output is copied to the two shapers. The fast-shaper transforms current to voltage with a programmed resistance value. 25 k, 50 k, and 100 k resistors can be connected in parallel with 10 0k to provide gain scaling to the comparator. Switch programmable caps provide a small amount (1-2 ns) of Integration. Unlike the parameters for the gain-block, the shaper parameters are common to all 64 channels. The comparator input threshold from a DAC is common to all channels. The DAC has an 8 bit binary scale with a 16step thermometer scale, corresponding to a resolution of 12 bits from 0.8 V to 2.8 V. The outputs of the 64 comparators go to the FPGA to form a trigger. The slow shaper uses bipolar shaping to provide trigger delay and noise filtering for the Track-Hold. 3 programmable switches provide 8 possible shaping times. These parameters are common to all channels. The Maroc2 data sheet shows typical fast shaper peaking times of 10 ns and typical slow shaper peaking times of 100 ns. The time difference is enough to form a trigger in the FPGA and hold the peak value of the slow shaper. The time to form and release such trigger is about 120 ns. Two 3-wire serial ports, G and R, are provided for controlling the chip. Set-up parameters are written to the G port from the FPGA; 3 bytes for switch settings, 3 bytes for the DAC value, and 64 bytes for the gain values. These are stored

in internal registers and are lost after power-down. The multiplexer to the external ADC is incremented from the R port. The multiplexer requires a minimum settling time of $0.5\mu s$ corresponding to a readout time of $32\mu s$.

2. FPGA

The FPGA is an Altera EP1C6Q240. The FPGA is automatically configured on power-up from an EPROM. A JTAG connector is provided for loading code to the EPROM. Parameter data is written or read via the serial-link. A schematic of the FPGA is shown in Figure 2 while the internal logic scheme is shown in Figure 3.

The high-true edges from the Maroc2 comparators set discriminator flip-flops in the FPGA. The flip-flop outputs are individually synchronized to the 62.5 MHz system clock. The 64-fold-or of the synchronizer defines a trigger. The trigger writes the 64 synchronizer bits with a 32 bit time-stamp to a Fifo, sends a copy of the data to the ADC-Logic, generates a Hold to the Maroc2, and sets a dead-time interval for resetting the discriminator flip-flops.

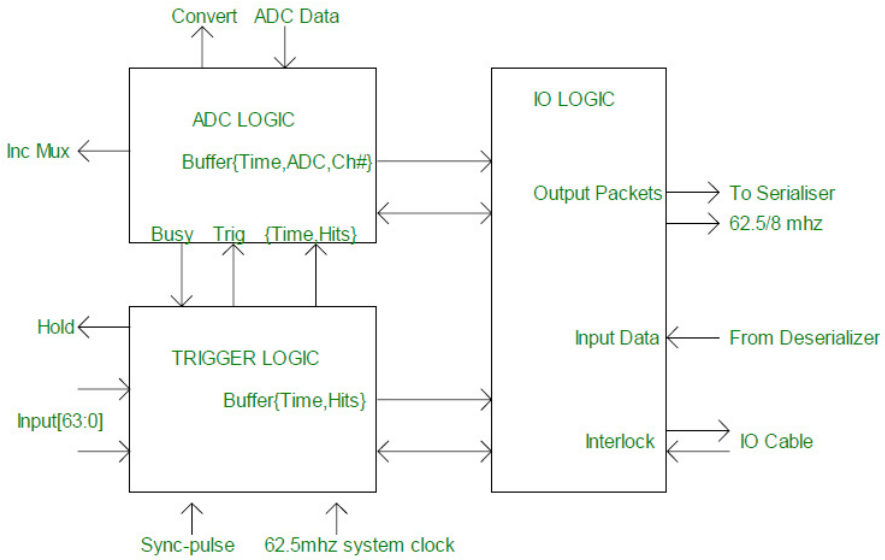

FIG. 2. FPGA schematic

The time−stamp corresponds to the earliest synchronized input. Any following inputs are recorded up to the trigger−time (4×16 ns clock-cycles in the current design). The 64 discriminators are then held reset for a dead-time, set at 80 ns in the current design, to avoid after pulsing. The FIFO does not create additional dead-time because the data is written as a single 96 bit word in 1 clock cycle. The Hold to the Maroc2 track-holds is synchronous to the system clock and therefore has a jitter with respect to the Maroc2 shaper peak. The peak is fairly soft, so for calibration data, the jitter should not a problem. The Hold-delay value is a software parameter to be determined by experiment. Because of the 32 μsec of the ADC process, the ADC will sometimes be busy, and no ADC data recorded, but with no affect on the trigger. The ADC-control logic reads-out the track-hold data to the external-ADC by sending 64 R_{clocks} to the Maroc2, and 64 convert−clocks to the ADC. The time-stamp is written to a Dual−port memory, followed by the 12 bit ADC output and channel number for each successive conversion. The registered sync-bits from the trigger-logic condition the write-enable of the memory to optionally suppress data below threshold. The memory-address and word-count are written to a separate Fifo for reading out the Dual-port memory, and insert a word-count in front of the event packet.

Data from the trigger-logic and ADC-logic buffers is read out via a token passing link. 24-bit data from the FPGA is connected to a DS90C241 serializer at 1/8 the 62.5 MHz Clock frequency. The serialized output is cabled to the upstream PMT-module with cat5 cable. Data from a downstream module is de-serialized with a DS90C124 and connected to the FPGA, where it is synchronized to the local clock.

The data[23:22] defines the word type:

- D[23:22] = 1 defines a control word
- D[23:22] = 2 defines a token

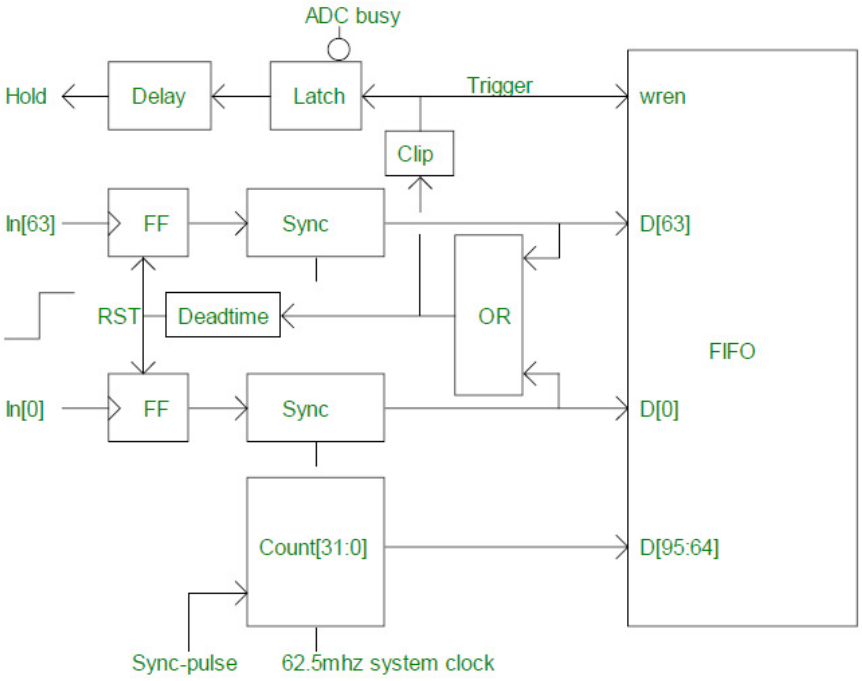

FIG. 3. FPGA internal logic

- D[23:22] = 3 defines a data word

A new token is sent to the input of the link after the previous token is recovered from the end of the link. If a module has data, the input token is held until data is sent. If a module has no data, the token is passed to the next module. If both trigger and ADC data are available, trigger-data is sent first followed by ADC-data.

3. PMT board Firmware

a. Requirements for Commissioning and Calibration During the installation of the MC detector, there may be special readout configurations we wish to run to debug or calibrate our system. During the commissioning phase, it will be important to know the absolute rates at a given threshold in order to verify that our system is working properly. To this end, the PMT board firmware should be able to read out latch-only data as well as provide a hardware level trigger-out signal that can be connected to a scaler. Comparing data rates collected via the USB link with data rates collected via the trigger-out signal and a scaler will be a powerful tool to debug our installation. Therefore, it will be important for our hardware level trigger-out signal not to be only a simple OR of the 64 PMT channels but instead to encode a more sophisticated trigger logic.

For calibration purposes we need to know the absolute light yield for muons for each channel. One method to obtain this information is to divide the muon peak by the single PE peak for a given channel. Therefore, it will be useful to be able to read out single-hit ADC data in order to measure the single PE peak from the ambient radiation. We can also acquire the single PE peak by looking at crosstalk into neighboring pixels, so it will also be useful to be able to read out the ADC data for all channels when any 1 channel is above threshold.

b. Data Taking We will not use an external trigger during the normal OV operation. The system can provide hit patters or ADC readout values through the data stream or a trigger signal per board made for example of the OR of all 64 channels of the MAPMT or a particular trigger can be formed via the use of NIM electronics.

The trigger configurations will be encoded in the firmware and will be able to switch between one trigger configurations to another using the DAQ.

c. XY Trigger The PMT board does not include the capability of knowing if and how many channels are triggered in another PMT board. To deal with that the system cna be equipped with a trigger box. The trigger box will be installed nonetheless and used as local fan-in modules for the hardware level trigger-out signals generated by each module. These modules will be part of the DAQ system and will have the capability of being remotely operated.

Each module can be operated as a fan in/out or trigger module just by sending the appropriate command through the DAQ. This leaves open the possibility of forming a higher level trigger based on the info collected from individual pmt board if it becomes necessary.

The pmt boards firmware will include this capability. An example of that would be a 3-layers coincidence trigger that would require that each PMT board perform local coincidence logic before sending its hardware level trigger-out signal. Then, the ADC value (or hit values) for this pmt board will be stored into a fifo and read-out only under particular conditions dictated by the trigger condition implemented in the trigger box.

B. USB Board

The USB board connects to the PMT board via ethernet cables (a.k.a. cat5e or cat6 cable). The USB board also requires the same 62.5 MHz clock that the PMT board requires, and it should be connected, via lemo cable, to the same NIM module providing the clock to the PMT board. Figure 4 shown the USB board.

The USB module transfers the data packets to the PC−processor and re−circulates the token. Control data is also passed over the serial-link, where each PM-module contains a 7bit switch-settable address.

FIG. 4. OV USB readout board

III. INTERFACE BETWEEN OV AND LEVEL-1 TRIGGER

TBD

The Trigger and Timing System of ProtoDUNE will send signals to the MC and receives triggers from it as in Fig. 5. The goal of the signal exchange is to join the independent data-sets already online, at the level of the Event Builder Process. There is redundancy involved, since the signals provided by the Level-1 Trigger System alone or the triggers from the Outer Veto would already allow the two data-sets to join.

The trigger master board (?) will provide the MC with a 62.5 MHz System Clock. However to minimize (and study) the effect of miscounting clock cycles, a Sync-Signal is issued by the TMB at a fixed frequency (O(0.1) Hz) and synchronous to the System Clock. Since the OV knows when to expect the Sync-Signal, it can be used to check errors in the data taking.

The third signal that the Level-1 Trigger System provides to the MC is the Inhibit-Signal.

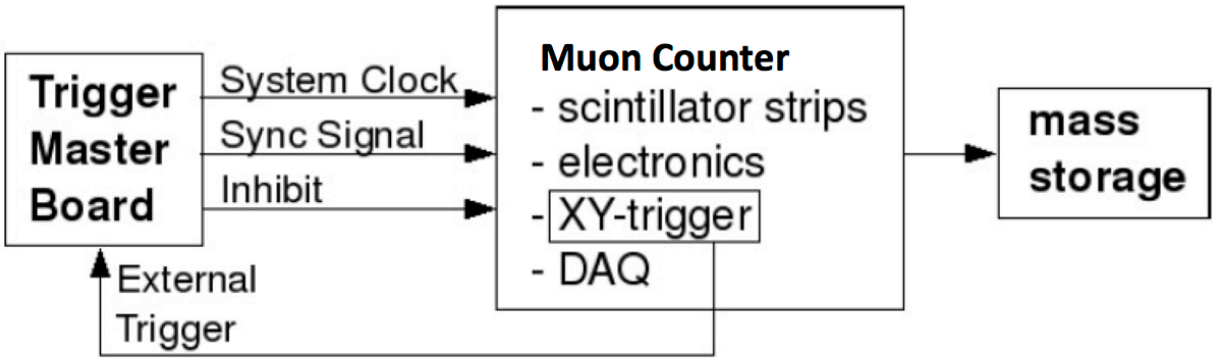

FIG. 5. Connection scheme between the MC trigger board/system and the ProtoDUNE TB

The PMT board will also generate a trigger signal that will be collected by the OV trigger box. Signals from the X and Y modules will be collected in the trigger box and two general trigger outputs will be generated. The first will be an OR of all the X modules and the second will be an OR of all the Y modules. The expected delay for the set of this signal into the protoDUNE trigger board will be <500 ns.

IV. THE DAQ

The MC DAQ will be separated from the one of the TPC and it will be a USB-based readout system. Each of the MC front end board are connected through a cat-5 cables and each of those daisy chains is readout by a separate USB board. The data stream coming out of the USB board will be combined offline to identify muons. The MC readout processes will launch indipendent threads (C++) to manage the data coming from each individual USB board. We will use libusb for that interface. Each of the thread will constantly be monitored by the MC run control that can connect to the TPC DAQ using TCP/IP interface. Each thread will write on disk data and it will be monitored for errors. Communication between the MC run control and individual USB threads will be realized using message queues. A scheme of the readout is presented in Fig. 6.

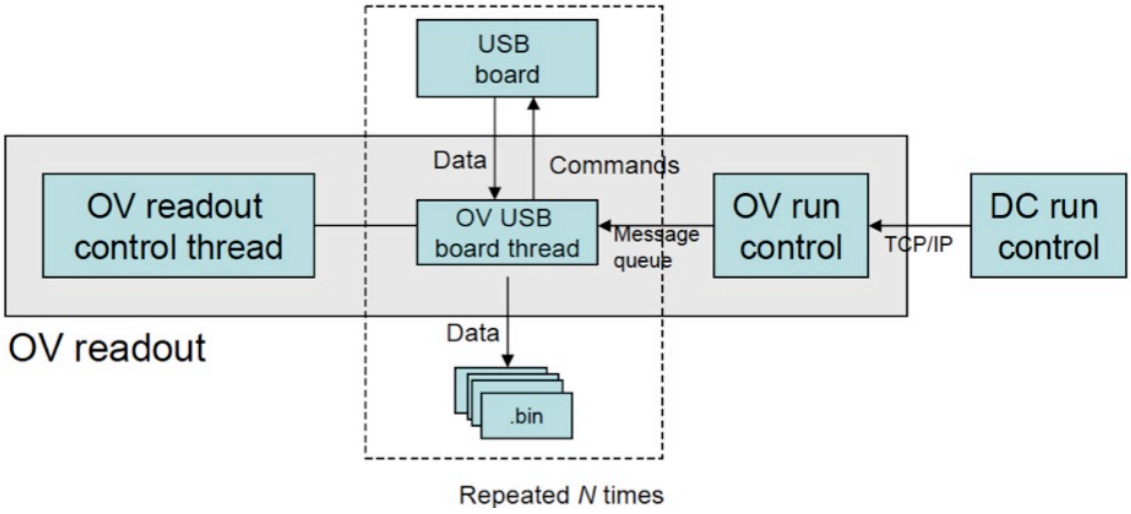

FIG. 6. Muon counter readout scheme

[1] P. Barrillon *et al.*, Web site: http://elec-in2p3.lal.in2p3.fr/micro/maroc/.
[2] F. Ardellier *et al.* [Double Chooz Collaboration], arXiv:hep-ex/0606025.