

Protodune Muon Tagger

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Outer Veto (OV)

System will be positioned in the front and back of the TPC

- identify muon present in beam alone
- tag this muon send trigger info to TPC

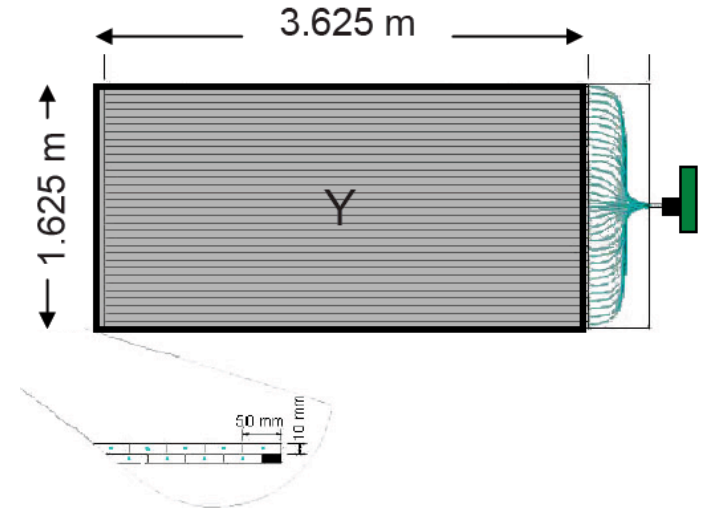
System will also have some panel on top of the TPC

- Muon veto, send trigger info to TPC

Trigger will be generated as an OR of the X and Y panels

Send to the TPC trigger board within 500 ns.

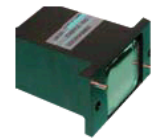
Hit info or ADC info in separate data stream.



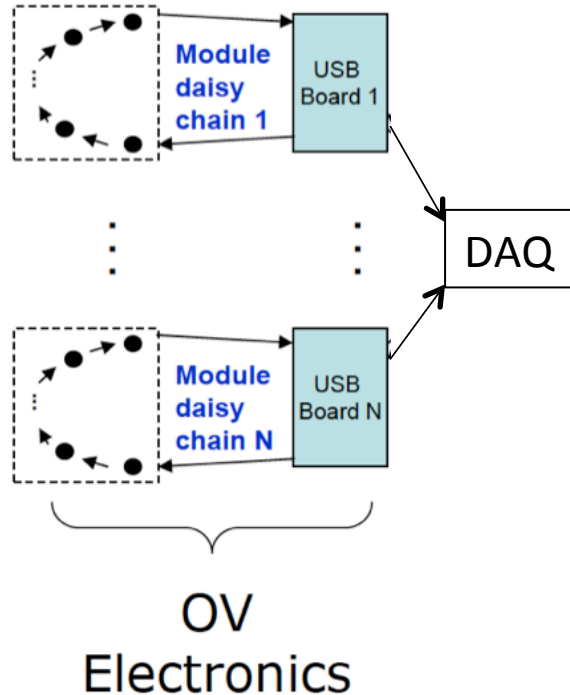
OV modules consist of two layers of 64 scintillator strips with WLS fibers connected to a multi-anode PMT

OV Readout Electronics

- Multi-anode PMT (Hamamatsu M64)
- Multi-anode readout chip (Maroc2)
- Multi-anode front-end readout board (custom-made at Columbia / Nevis labs)
- USB board (custom-made at Columbia / Nevis labs)
- Fan-out / trigger boxes (custom-made at Columbia / Nevis labs)



System overview and trigger signals

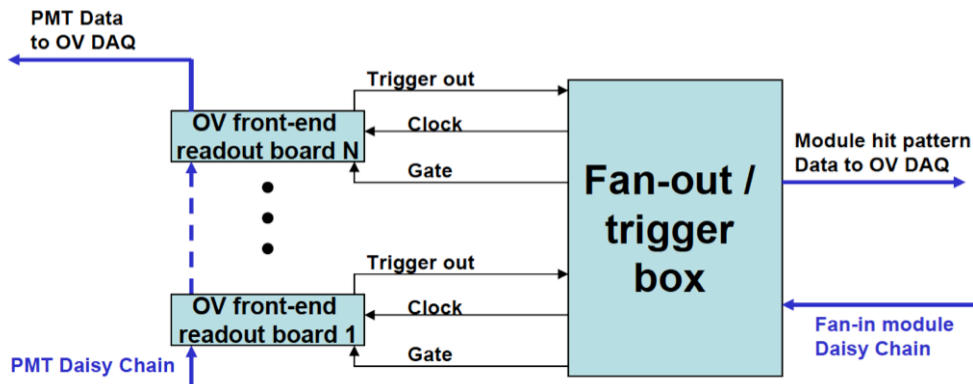


Each PMT board:

- Readout 64 channels - provide hits or ADC info
 - Hits processing require 120 ns
 - ADC processing require 32 μ s
- Board trigger does not know about other boards

Trigger board:

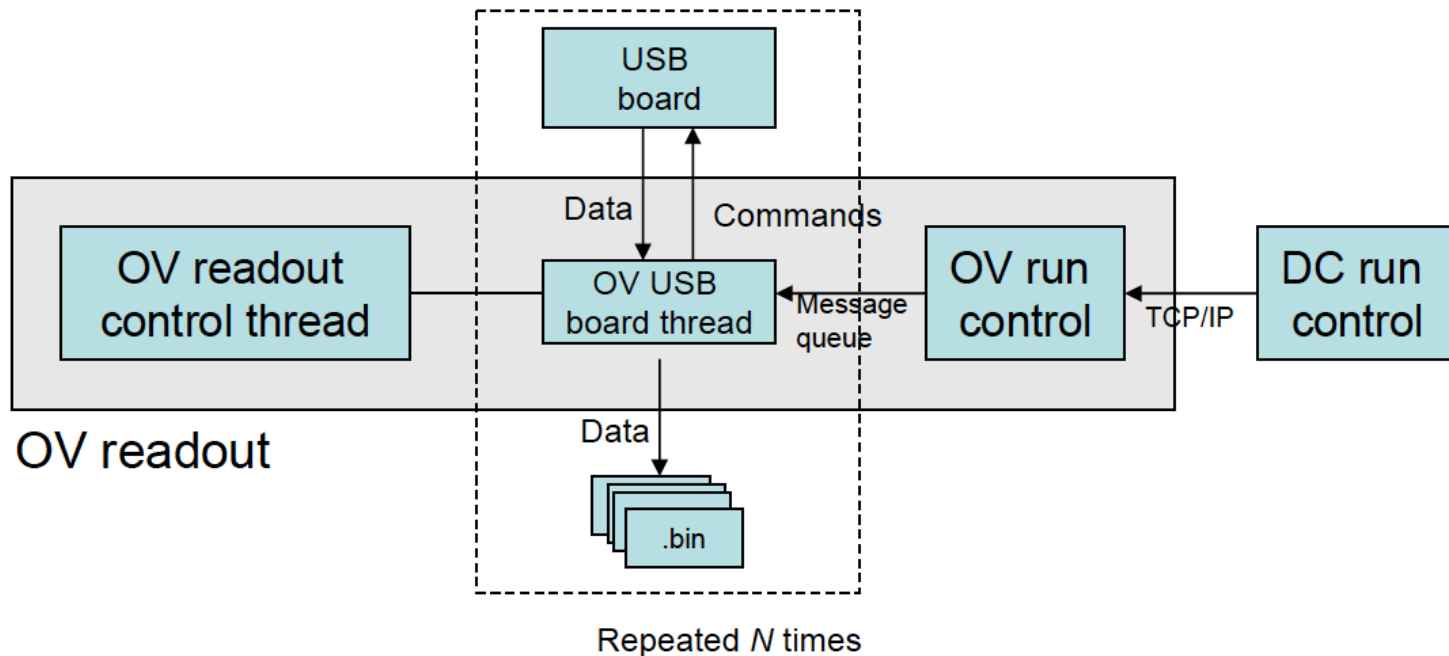
- Collect info from all PMT boards
- Provide hit info pattern (through DAQ)
- Form a trigger signal (based on single board info)
 - 2 trigger out available
 - Geometrical overlapping modules in < 500 ns
 - OR of all modules in < 500 ns



Data stream contains 32 bit timestamp can be used for data merging offline, only when a proper bit is asserted in the main data stream.

OV Readout

- Launches independent threads (C++) to manage each USB board
 - USB communication using libusb
- Separate OV run control process (perl) connects to DC run control via TCP/IP
 - OV run control sends internal commands using message queues
- Binary data written to disk independently for each USB data stream



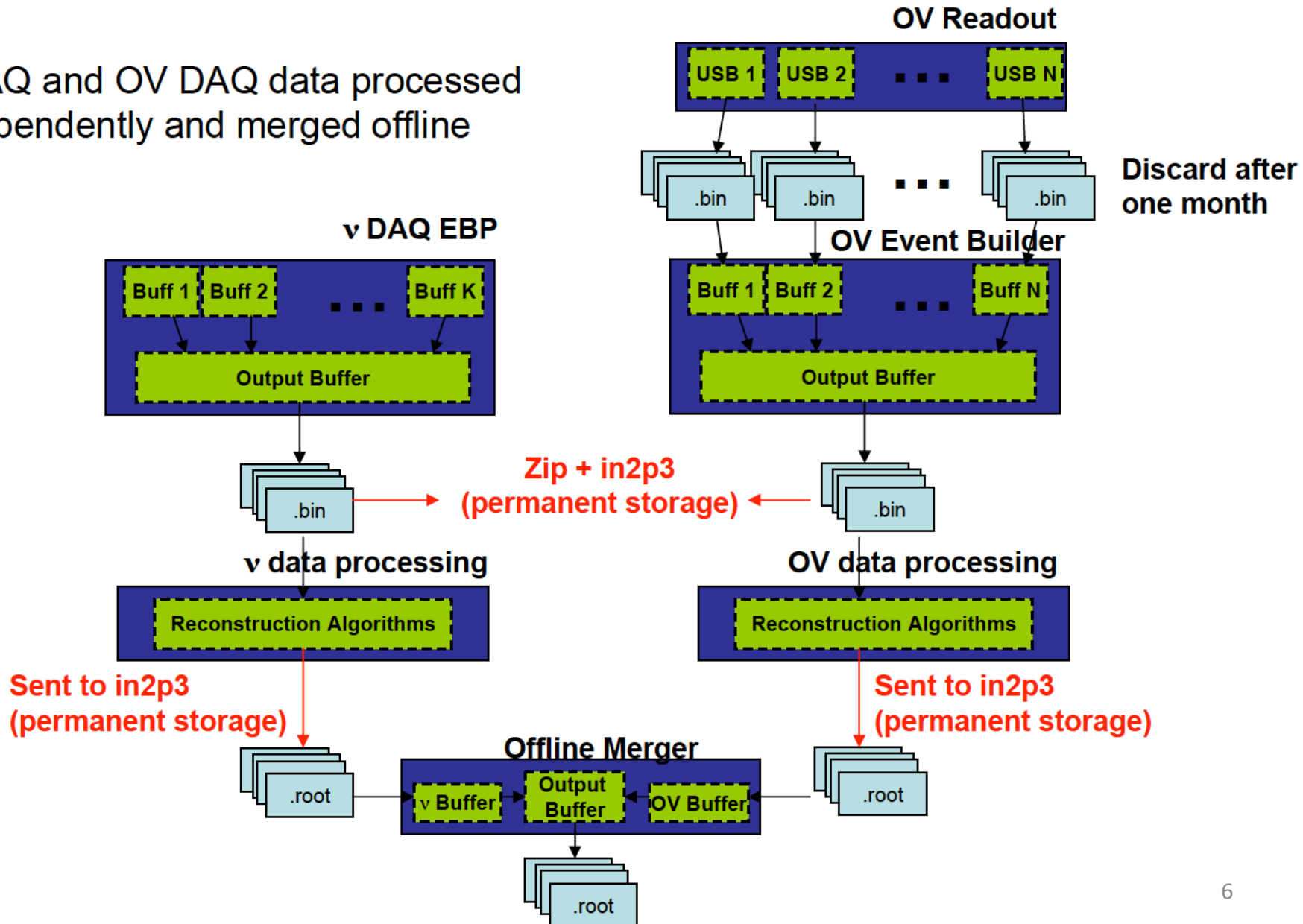
OV Event Builder

- OV Event Builder written in C++ and designed to:
 - **Read in raw data from OV DAQ**
 - Independent, unsorted data streams for each USB, consisting of data packets from individual OV modules
 - **Compute and subtract baselines**
 - **Apply offline thresholds**
 - Event rejected unless both hits in “ μ -like” double > 1.5 PE
 - **Time-order hits within individual USB data streams**
 - **Merge all USB data streams in time-order, grouping hits into OV events**
 - Hits separated by ≤ 3 clock cycles added to same event

Data Flow and Merging

Example

v DAQ and OV DAQ data processed independently and merged offline



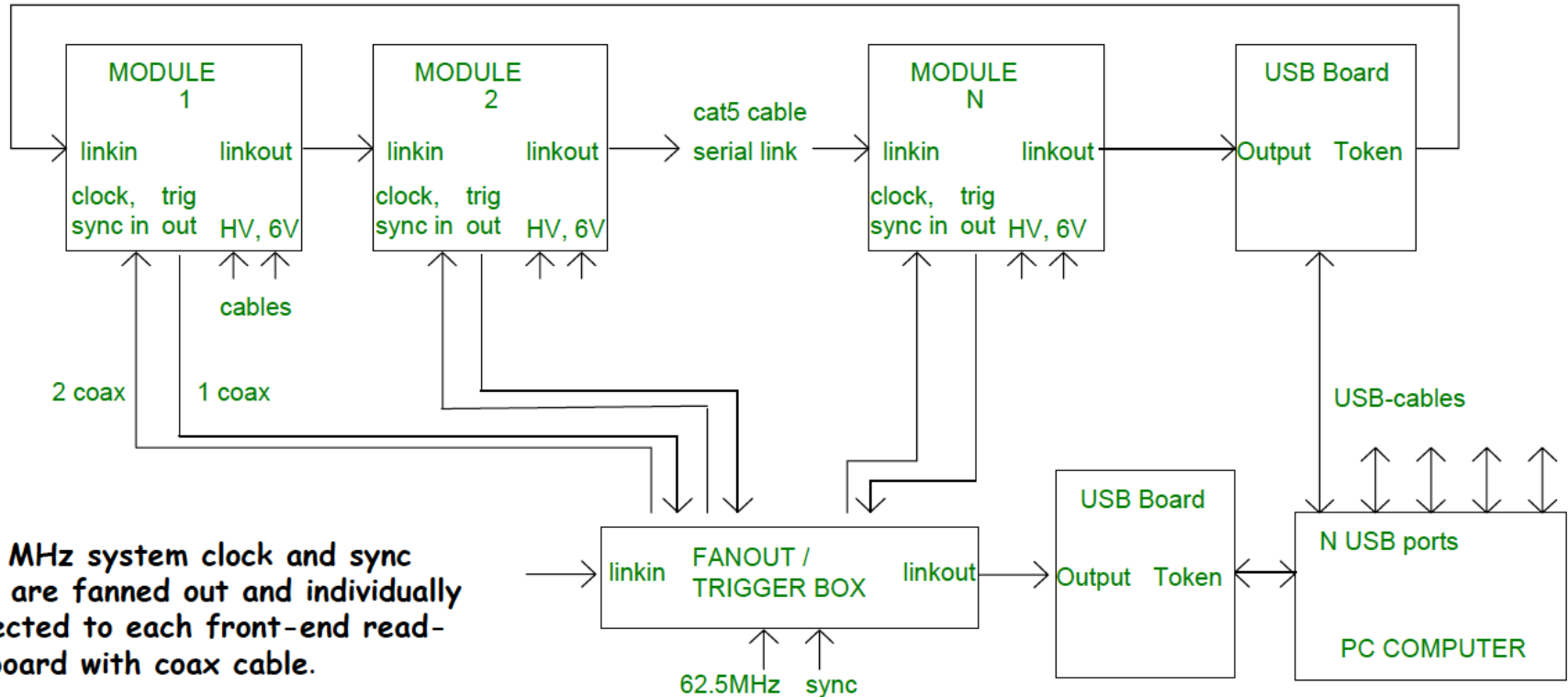
Backup

Specs

- MAPMT - 800-900V, 300-400 μ A
- PMT board - 6 V, 0.28A
- Trigger Board - 6 V, 1.0A

- USB board - 5V, decoupled from PC, 0.4A

OV Readout Scheme



OV modules common to a veto plane are linked together with Cat5e cable.

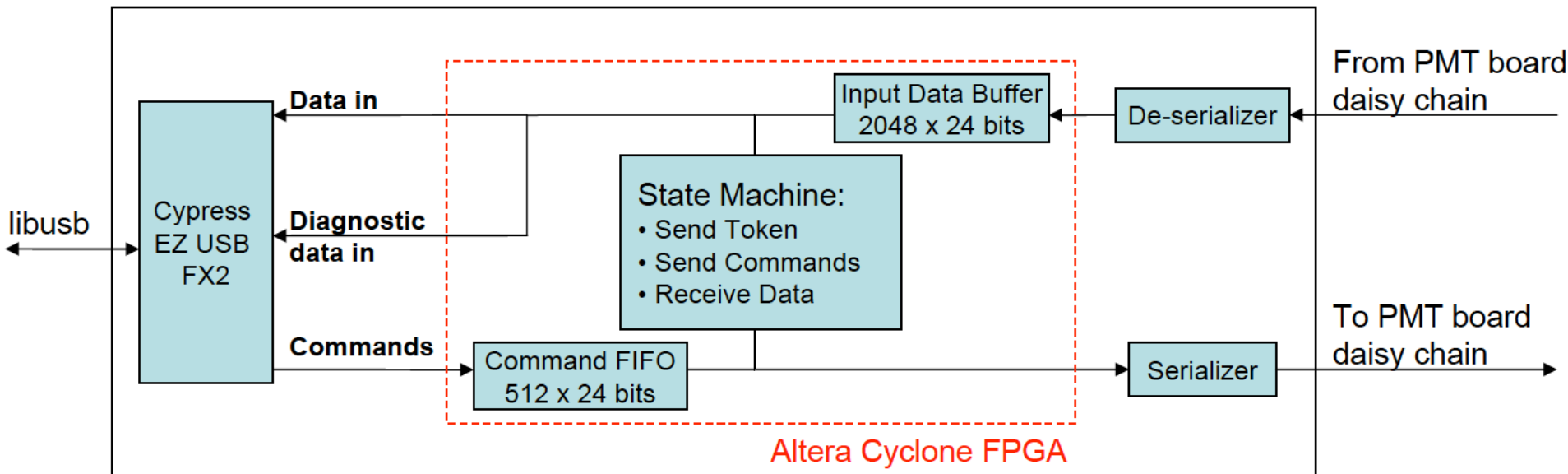
A token passing scheme is used to read out serial data to a USB hub-module:

- If OV module has no data, the token is passed forward.
- If OV module has data, it reads-out the next triggered event from the ADC FIFO, and then passes the token to next OV module.

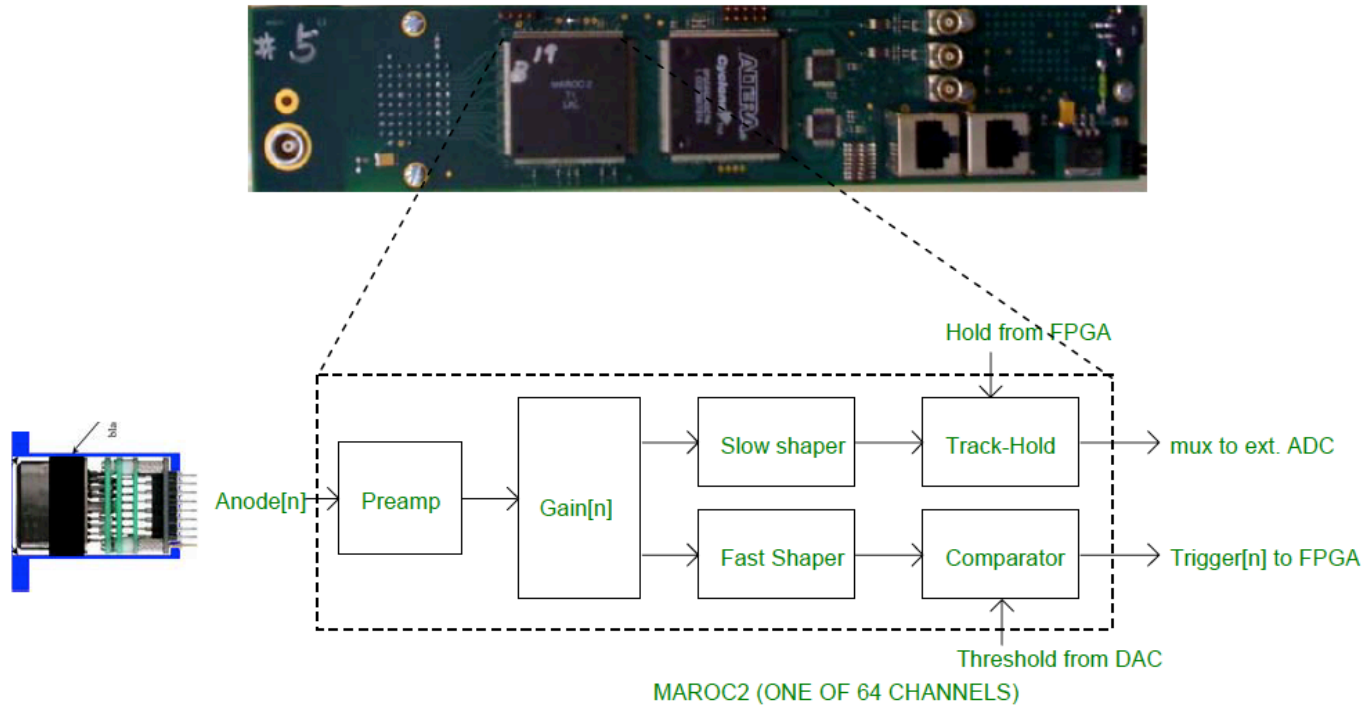
The USB board transfers the data packets to the PC and re-circulates token.

USB Board Architecture

- Cypress EZ USB FX2 micro-controller
- Three USB endpoints:
 - Data in
 - Diagnostic data in
 - Commands out
- Altera Cyclone FPGA for serial link I/O



OV Front-end Readout Board (I)



- Maroc2 architecture allows individual 6-bit gain correction for each channel
- Comparator input threshold from DAC common to all channels
- The outputs of the 64 comparators go to the FPGA to form a trigger
- Slow shaper provides trigger delay to track and hold

Performance of a full-scale test 40 boards

Expected data rate = 25 kHz (0.9Mb/s)

DAQ rate @ VT = 35.5kHz (1.2Mb/s);

All the operations on the system
were done remotely

Total acquisition time = 1000 h

LV on: = 1392 h

HV on: = 1290 h

Consecutive acquisition time (stress test) = 192 h
(typical DC run = 10h);

No board fail;
No PMT fail.

Data written to disk in total (1000h) ~ 3.1 Tb;

Data written to disk for the 192 h ~ 0.6 Tb

System is operating in France for
6 years now in the DC far and 2
years in the DC near.

DAQ performance (measured injecting pulse):
pulser stability ~ 5 %, DAQ stable.

LV power module failure.

1 daisy chain failure. Power
failure for one board.

Analysis of the 192 h run:

Data error - none

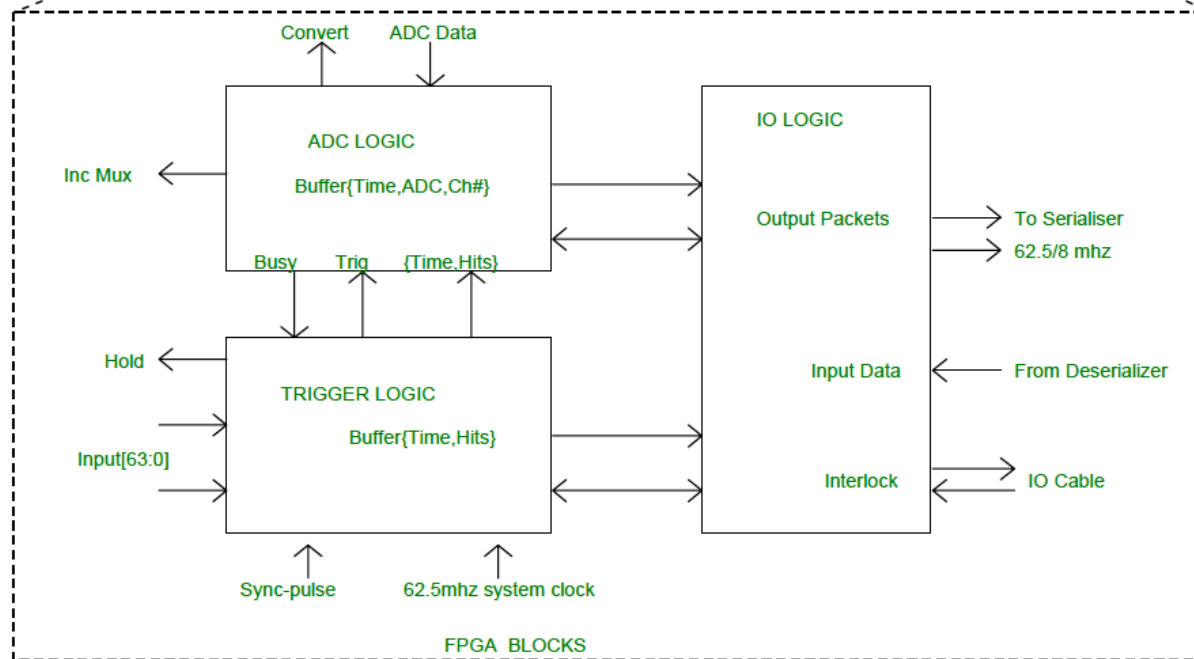
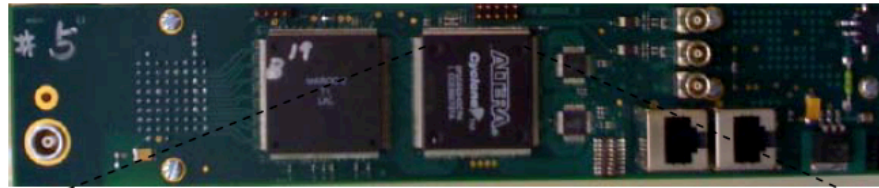
DAQ crash - none

Evt builder crash - none

Online monitor - none

Problems/warnings - none

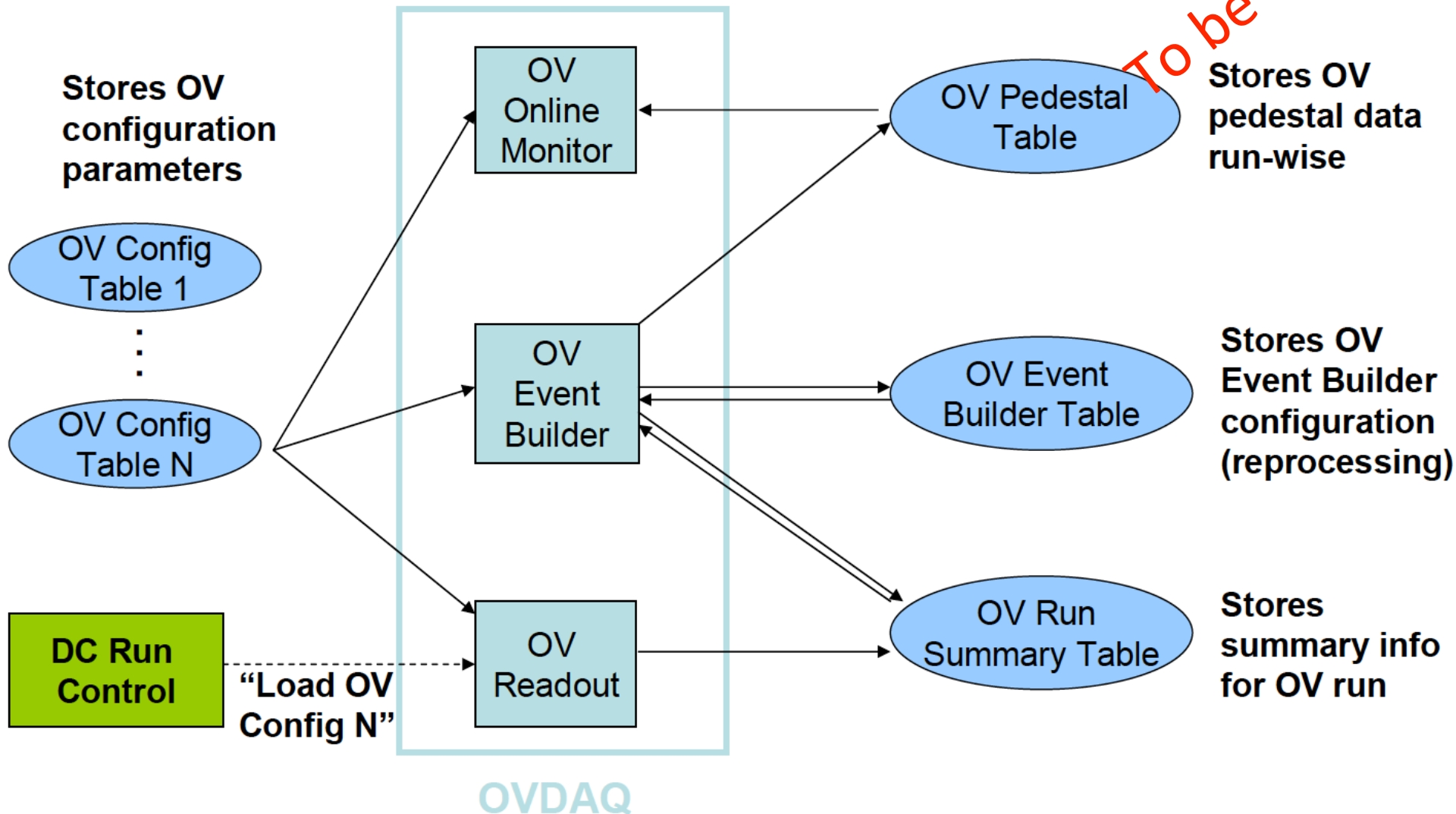
OV Front-end Readout Board (II)



- Trigger logic formed from Maroc2 comparator outputs generates hold signal
- ADC control logic reads out the track and hold data to an external 12-bit ADC
- ADC data and channel number output for each channel above threshold
- Output packets also include word count, memory address, and 32-bit clock counter

OV DAQ MySQL Dependencies

To be updated



OV Online Monitor To be updated

- Written in C++ (object-oriented design)
- Communicates with DC online monitor server via TCP/IP socket
 - Java-based DC online monitor GUI
- Designed to monitor:
 - Front-end readout board hit rates and mean ADC values
 - By channel, module, and USB (time history)
 - Trigger box hit rates
 - By front-end readout board and trigger box
 - Raw data quality and online data processing status
 - OV High Voltage
- Sends warnings/alarms (DC message server, syslog, emails)

