Light Readout Electronics - Design

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DUNE Review - Parallel session Photon and Slow control - CERN 24-25 April 2017

APC - Astroparticule et Cosmologie

Outline

Context

IN2P3 Collaboration

Joint effort between several in2p3 laboratories in France

Omega Microelectronics Design Center for Physics and Medical Imaging - ASIC development and testing

LAPP Particle and Nuclear Physics - PCB layout and routing

APC Cosmology and Astroparticle Physics - ASIC testing, PCB schematics

IPNL Nuclear Phycis - General support, advice and firmware

(Micro)electronics front end for PMTs

Goals

Go beyond ASIC functionality

Integrate an state of the art, latest generation ASIC completed with a few FPGA advanced features

- Advanced: dead timeless monitoring system
- Digital event counting (not an ASIC feature)
- Endless (x-bits) time stamping

Implement Digital Pulse Processing

Perform advanced DPP on the samples with FPGA fabric

- Sampling of analog signals
- Compute falling tail, windowing, etc.
- Event rejection, pile up handling, etc.

Steps

First prototype developed in 2015

- Using former ASIC generation (ParisROC)

Second version under current development

- Newest ASIC generation (CatiROC)
- Bug fix release

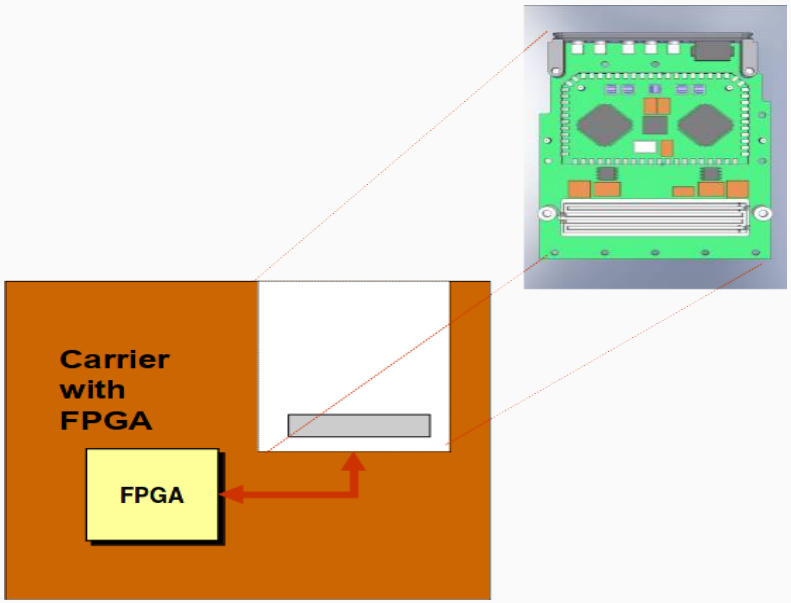
Production release 2018

- Double width AMC, 32 channels, ...

FMC Board

VITA Standard (VITA 57)

I/O mezzanine modules optimized to work with FPGA-based carrier board



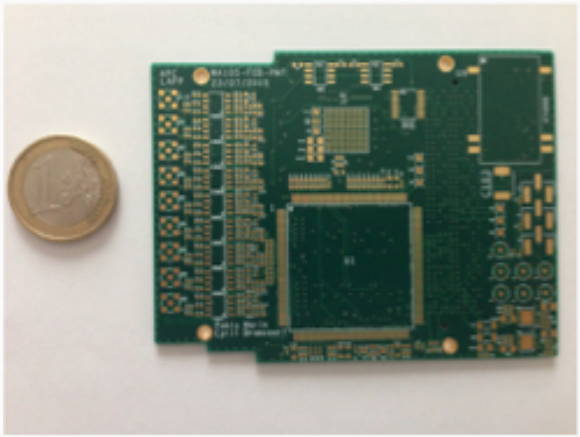
- Maximizes data throughput
- Minimizes latency
- Eliminates need for complex protocol logic on mezzanine
- Reduces FPGA design complexity

- Minimizes system overheads
- Single width: 69x76.5 mm
- Parallel I/O – single-ended or differential pairs
- HPC: 400 pins

First prototype of FMC board

16 Channels ASIC + ADC

Scale



Printed Circuit

Top view

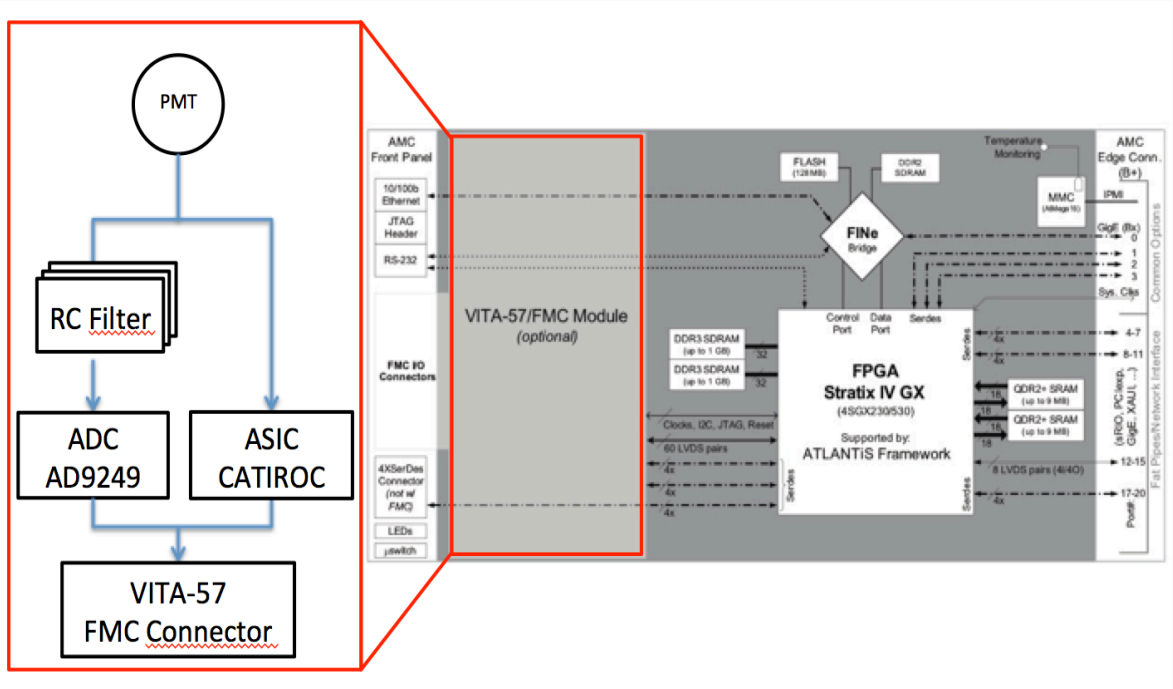
ParisROC ASIC + ADC

Bottom view

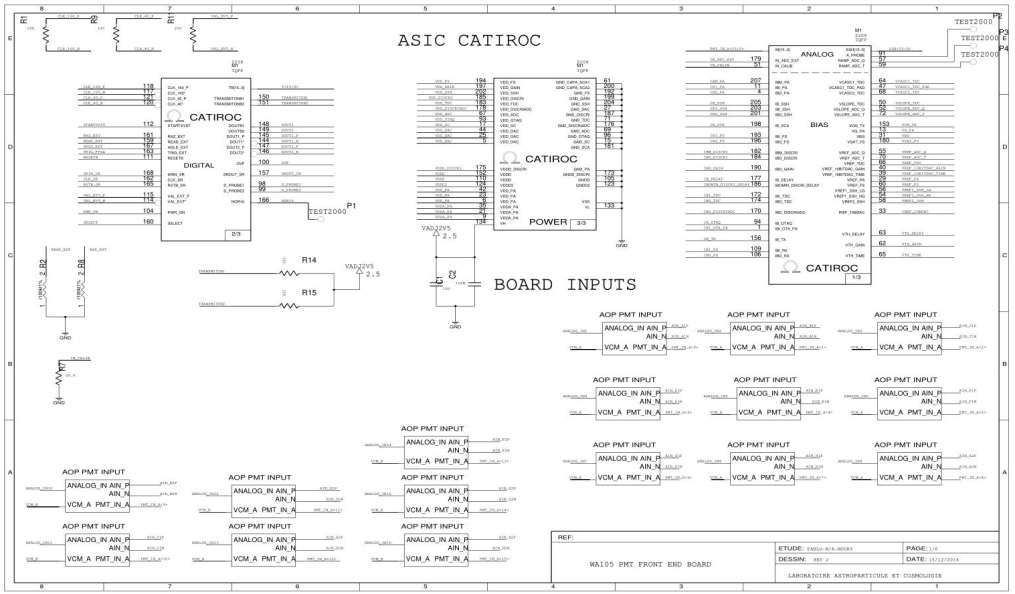
FMC connector

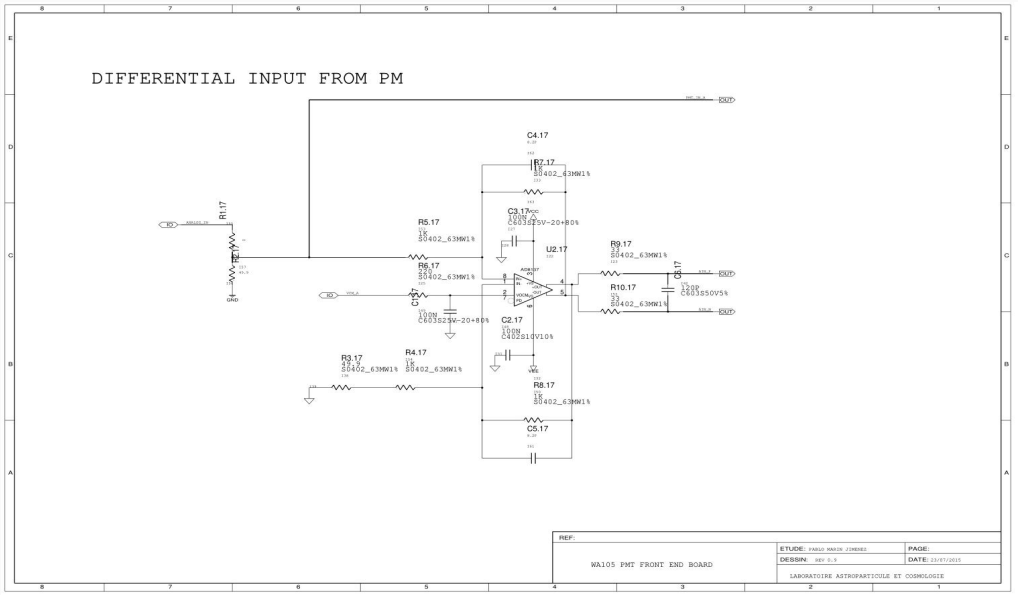
Current prototype - Block Diagram

- Splitting of analog inputs
- Anti aliasing filter
- Analog processing in ASIC
- Samples go to FPGA
- Readout of data from ASIC to FPGA
- Data is merged and processed in FPGA



Current prototype - Schematics





- Low pass filtering
- ADC9249, 65 MHz, 14 bits
- CatiROC ASIC - 16 ch.
- Power management
- VITA 57 FMC connector
- 1 ASIC Calibration signal
- 3 Spare signals

Ancillary signals

ASIC InCalib

Dedicated input

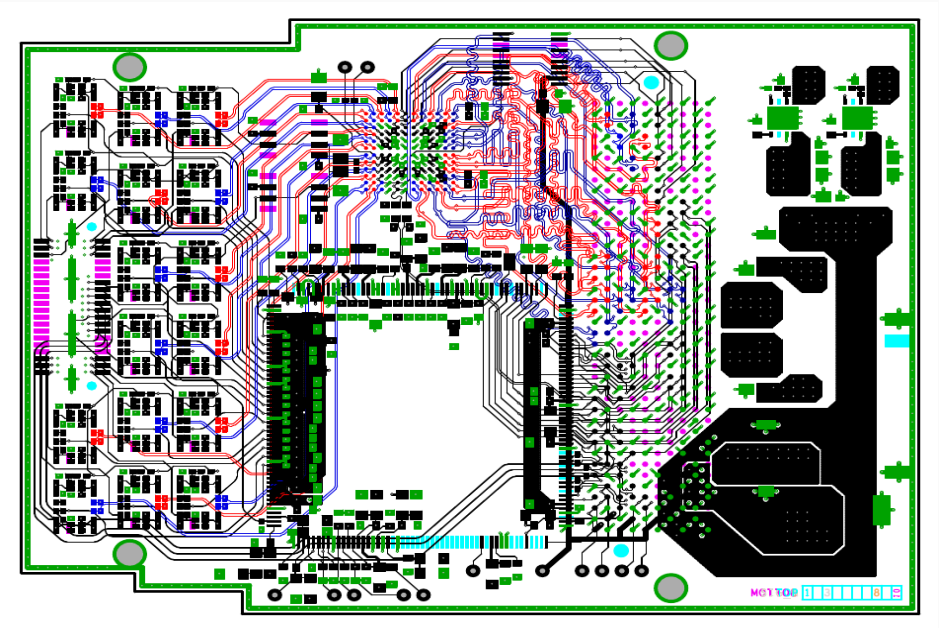
- Replaces all analog inputs
- Software controlled
- ASIC in-lab calibration

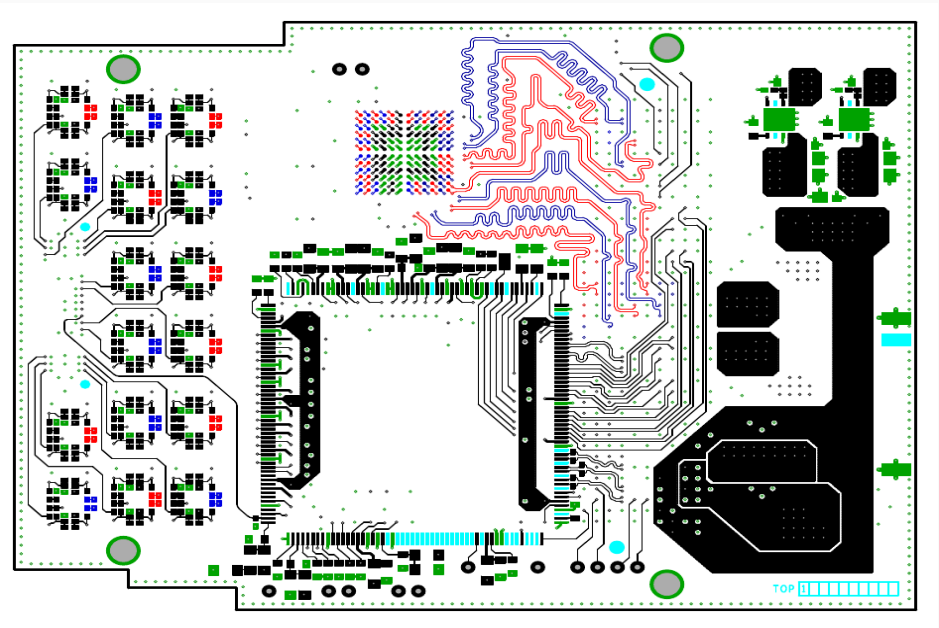
Spare x3

General purpose signals

- Handle positive/negative polarity signals
- -400 mV / 1.5 V
- Software selectable

Current prototype - Layout and routing



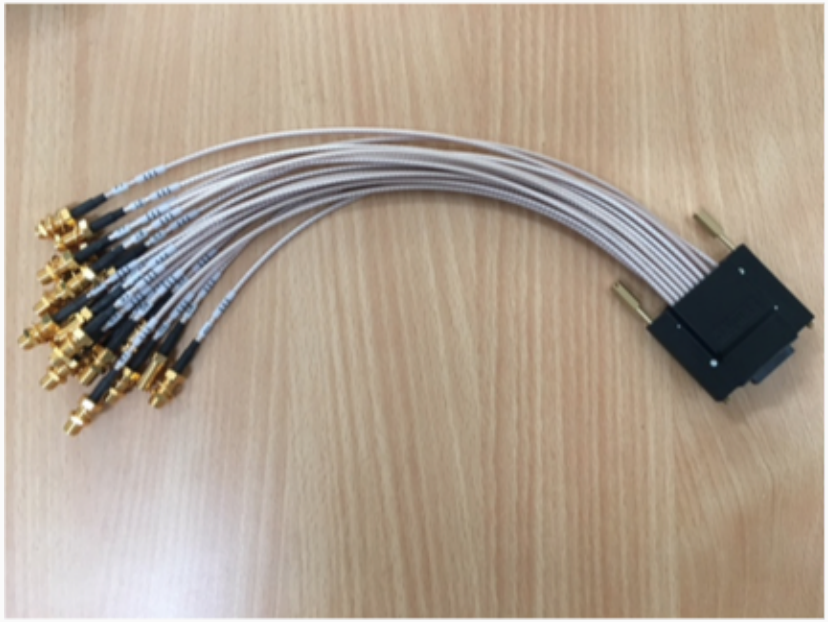


- Limiting constraints
- Analog / digital
- Reduced size
- Complex design
- Fast ADC signals
- Trace length matching
- Impedance matching
- 10 Layers

How to bring 20 signals in a reduced space

Plugged to RG58 cabling from splitter box through a male SMA connector

Bunch of 20 cables



30 cm. length

SMA standard

SMA female

Synchronization

All channels run synchronously, all events are time stamped

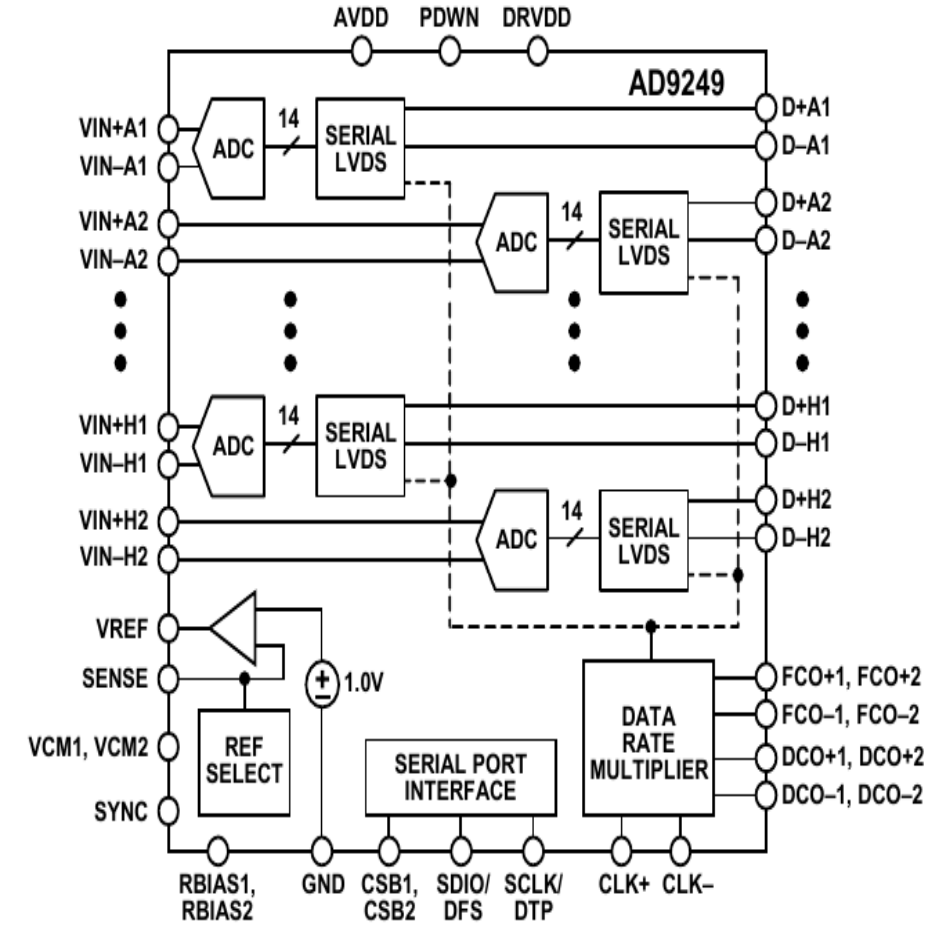
Integrated with the charge readout electronics via the common time base and the back-end receiving the data

16-Channels	Mezzanine peripheral is sync with AMC mother board
AMC Units	Each AMC mother board takes a clock through the uTCA backplane
Crate Sync	A dedicated MCH controller board acts as a sync receiver, distributing clocks to AMC cards
System sync	All system electronics are in sync using White Rabbit and dedicated receiver units

Trigerless operation or during beam time in an external trigger mode via white rabbit

ADC

AD9249 - Sampling ADC



- Two independent 8-channel blocks
- 16 data out lines
- Capture FCO and DCO available
- Fully differential
- Low voltage & low power
- Small footprint
- SPI Serial port control

AD9249 Features

65 MSPS / 650 MHz Bandwidth

Configurable sampling frequency - Anti aliasing filter necessary

16 channels - Serial LVDS

Data and frame outputs - Capture clock available

2 Vp-p - 14 bits - 75 dBFS SNR

DNL < 0.6 LSB; INL < 0.9 LSB

Memory map

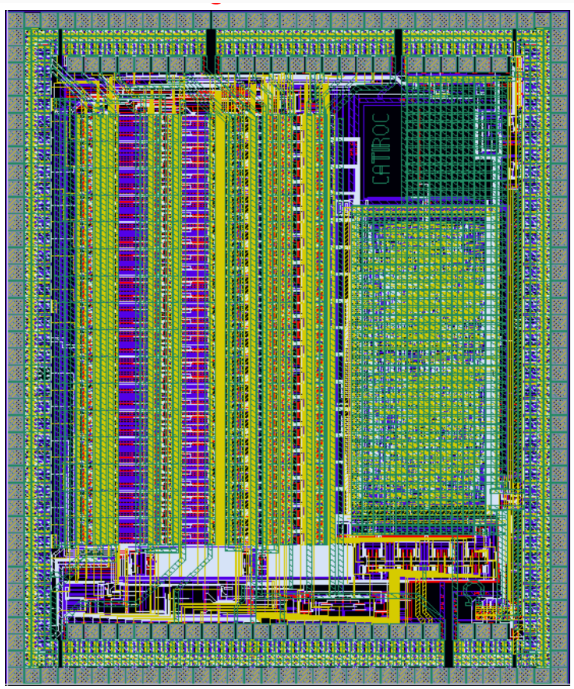
Write / read accessible - Fully configurable device

ASIC

CatiROC - AMS SiGe 0.35 um - 13.2 mm2

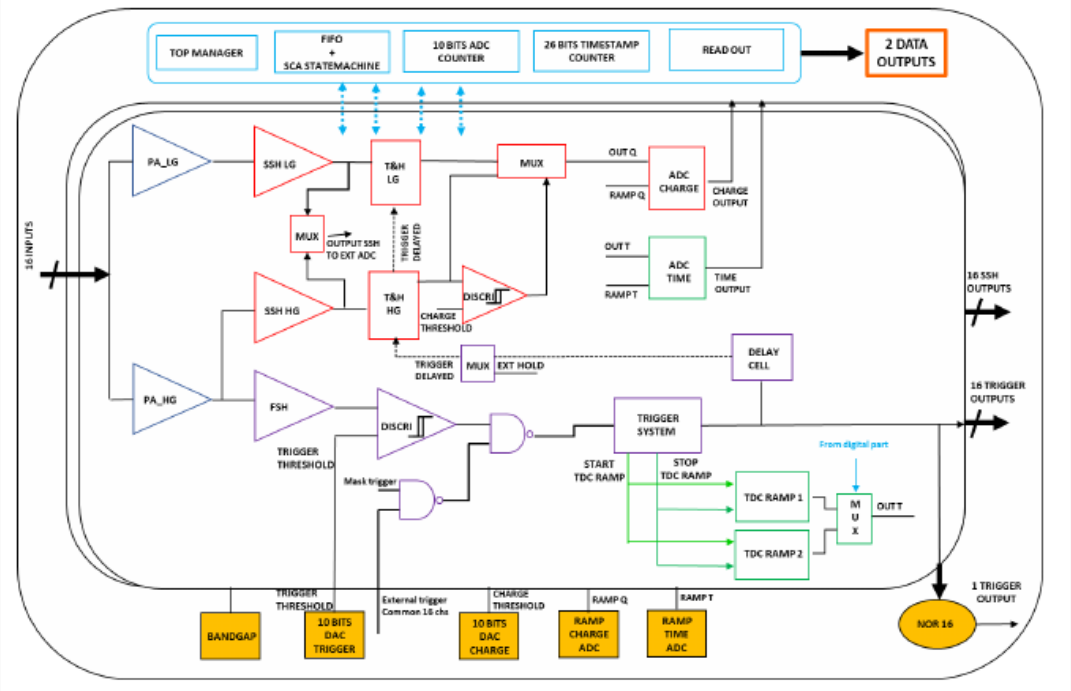
Detailed datasheet available at omega.in2p3.fr

Architecture



TQFP208 Package

Block Diagram



Fast/slow shapers

Two capacitors/channel

CatiROC features

Detector Read-Out	PMTs
Number of Channels	16
Signal Polarity	negative
Sensitivity	voltage
Timing	**Time stamp: 26 bits counter @40 MHz** **Fine time**: resolution < 100 ps (simulation) A TDC ramp for each channel
Charge Dynamic Range	160 fC up to 100pC
Trigger	Triggerless acquisition Noise= 5 fC; Minimum threshold= 25 fC (5σ)
Digital	**Conversion: 10 bits** ADC at **160 MHz** **Two Read out: 80 MHz** Read out frame: **50 bits** 2 frames of (29+21) bits 1st frame/8chs: Ch nb= 3; coarse time= 26 2nd frame/8chs: Gain used= 1; Charge converted= 10, Fine time converted= 10
Packaging & Dimension	TQFP 208 (28x28x1.4 mm) die : 3.3 mm x 4 mm
Power Consumption	30 mW/channel
Outputs	16 trigger outputs NOR16 16 slow shaper outputs Charge measurement over 10 bits Time measurement over 10 bits
Main Internal Programmable Features	Variable preamplifier gain Shaping time of the charge shaper (variable shaping and gain) Common trigger threshold adjustment Common gain threshold adjustment

Some specifications

311	Pw_Slow_lvds_receiv_PP	Force ON or Power pulsing mode (see table 5 in § 2.2.3)	
312	Sw_40MHz_lvds	switch off 40MHZ and 160MHz lvds receivers (0 = OFF, 1=ON)	1 (ON)
313	Sw_160MHz_lvds	switch off 160MHZ lvds receiver (0 = OFF, 1=ON)	1 (ON)
314	sel_clkDiv4	select ext. (0) or int. (1) 40MHz (int = 160MHz/4, ext : LVDS Receiver)	1 (internal)
315	sel_80M	Select readout clock (0= input clk, 1 = input clk/2) but always 80MHZ	1 (160MHz / 2)
316	Dis_ovfCpt	Disable buffer for overflow of Timestamp counter (0 = en, 1 = dis)	1 (disable)
317	sel ext Raz channel	0= internal Raz, 1= external Raz (for debugging)	0 (internal)
318	Not used		
319	sel ext Read	0= internal Read, 1= external Read (for debugging)	0 (internal)
320	EN_TacReadout	Enable readout of Tac data : 0= no Data, 1= data readOut	0 (no data)
321	EN_NOR16	Enable output buffer for NOR16 : 0= disable, 1= enable	1 (enable readout)
322	EN_transmit	Enable output buffers for transmit on : 0= dis., 1= enable	1 (enable readout)
323	EN_data_oc	Enable output buffers for data readout : 0= dis., 1= enable	1 (enable readout)
324	Dis_trigger	disable buffers for triggers : 0 = enable, 1 = disable	0 (enable triggers)
325	Pw_lvds_transmitter_EN	Enable LVDS transmitters for DATA output	10 (ON)
326	Pw_lvds_transmitter_PP	Force ON or Power pulsing mode (see table 5 in § 2.2.3)	
327	Sw_1mA_TX	Increase bias current in data transmitter (+1mA and + 2mA) 0 =OFF, 1= ON	11 (+1mA+2mA)
328	Sw_2mA_TX		

- I/O 1-bit shift register
- 328 bits to setup

CatiROC facts

16 channels readout chip for PMTs with fully independent charge and time measurements

16 negative inputs: each voltage input is sent to high/low noise amplifiers for small and large signals to ensure a good charge precision (30 fC)

Variable 8 bit gain / amplifier / channel

Charge: preamp followed by 2 variable slow shapers sent to analog memories to measure up to 50pC

Time: coarse + fine timing

10 bits Wilkinson ADC to convert charge and fine time @ 160 MHz

A fast shaper / channel followed by a discri for auto-trigger

Digital section handles the acq, conversion and readout, providing a 26 bits coarse time measurement (TS)

... but only one common 10 bit threshold

Summary

Collaboration

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Conclusions

- Work in progress ...
- Board schematics -> done
- End of routing by the end on April
- Board production during May
- ADC data capture firmware -> done
- ASIC control and data capture firmware -> done