Light Readout Electronics - Production / QA

Thomas Patzak - On behalf of the IN2P3 group

DUNE Review - Parallel session Photon and Slow control - CERN 24-25 April 2017

APC - Astroparticule et Cosmologie

Outline

Context

IN2P3 Collaboration

Joint effort between several in2p3 laboratories in France

Omega	Microelectronics Design Center for Physics and Medical Imaging - ASIC development and testing
LAPP	Particle and Nuclear Physics - PCB layout and routing
APC	Cosmology and Astroparticle Physics - ASIC testing, PCB schematics
IPNL	Nuclear Phycis - General support, advice and firmware

(Micro)electronics front end for PMTs

Goals

Go beyond ASIC functionality

Integrate an state of the art, latest generation ASIC completed with a few FPGA advanced features

- Advanced: dead timeless monitoring system
- Digital event counting (not an ASIC feature)
- Endless (x-bits) time stamping

Implement Digital Pulse Processing

Perform advanced DPP on the samples with FPGA fabric

- Sampling of analog signals
- Compute falling tail, windowing, etc.
- Event rejection, pile up handling, etc.

Steps

First prototype developed in 2015

- Using former ASIC generation (ParisROC)

Second version under current development

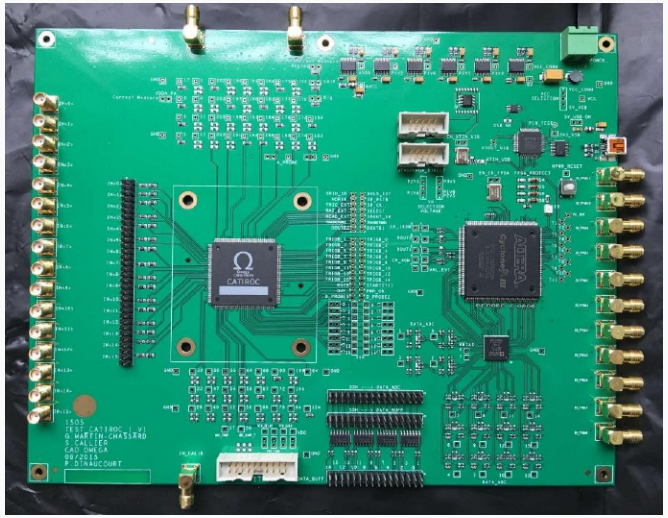
- Newest ASIC generation (CatiROC)
- Bug fix release

Production release 2018

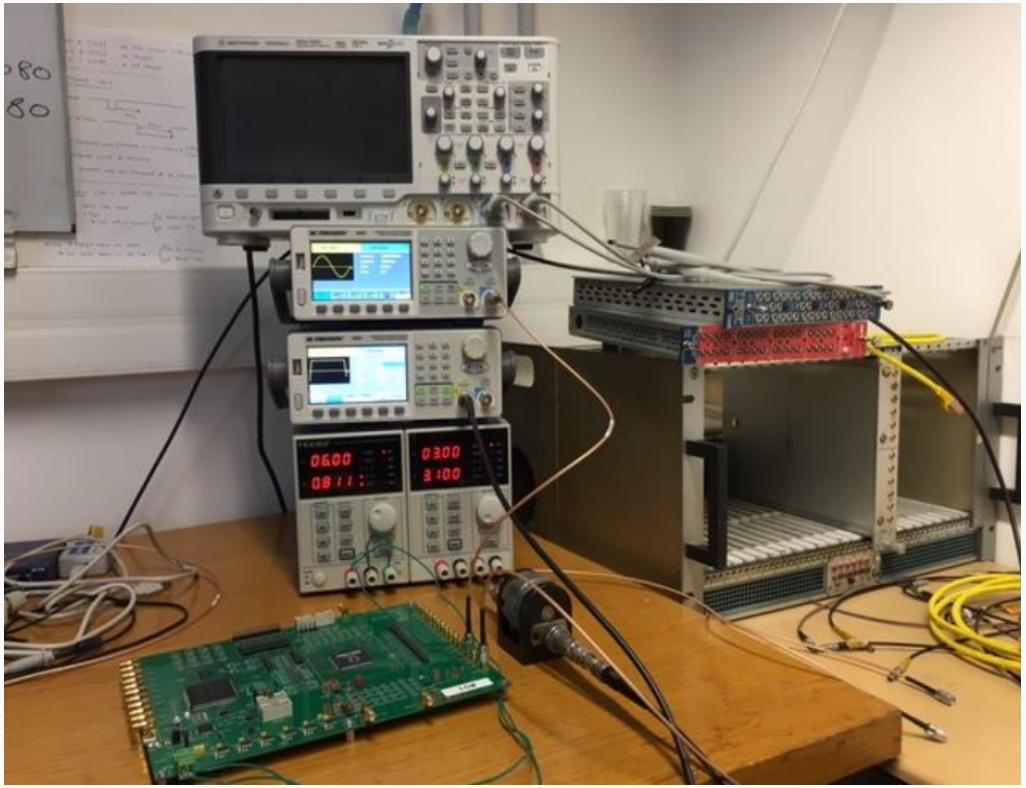
- Double width AMC, 32 channels, ...

ASIC Qualification

CatiROC Qualification - Testbench



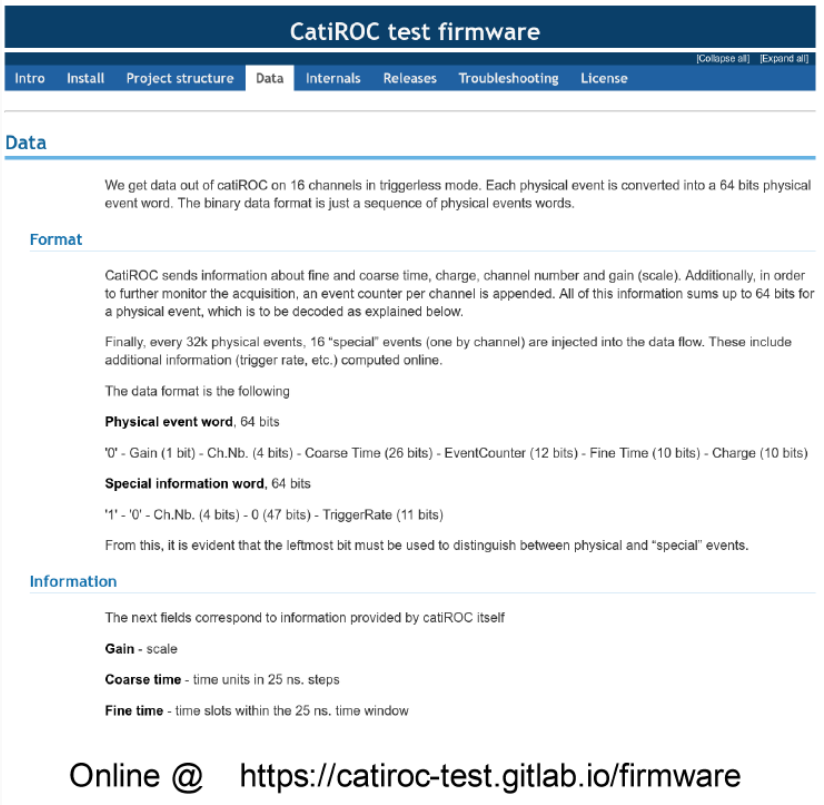
- USB2 communication
- Cyclone III FPGA
- Differential ADC
- All I/O accessible
- 16 channels ADC
- High bandwidth SMA



- Fanout board for timing, crosstalk, etc.
- Arbitrary Pulse Generator
- High gain (10^7) PMT
- Histogramming oscilloscope

CatiROC Qualification - Coding

Web site: fully documented / accessible - easy to share between teams



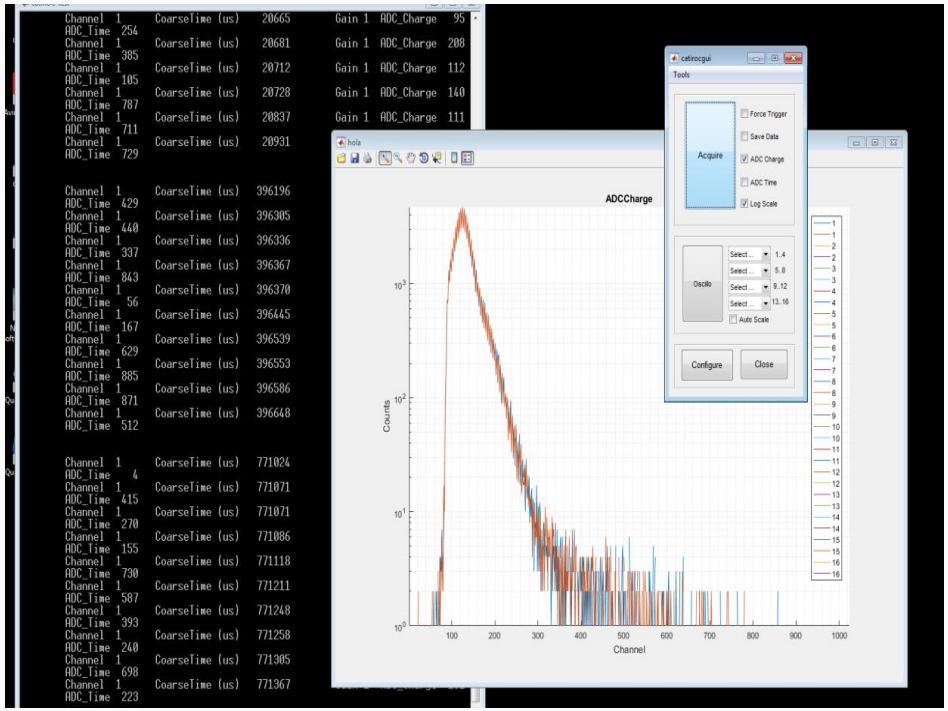
- all under git *version control system*
- *reproducible research* paradigm

- VHDL/C++/Matlab
- from scratch, full stack

CatiROC Qualification - Acquisition

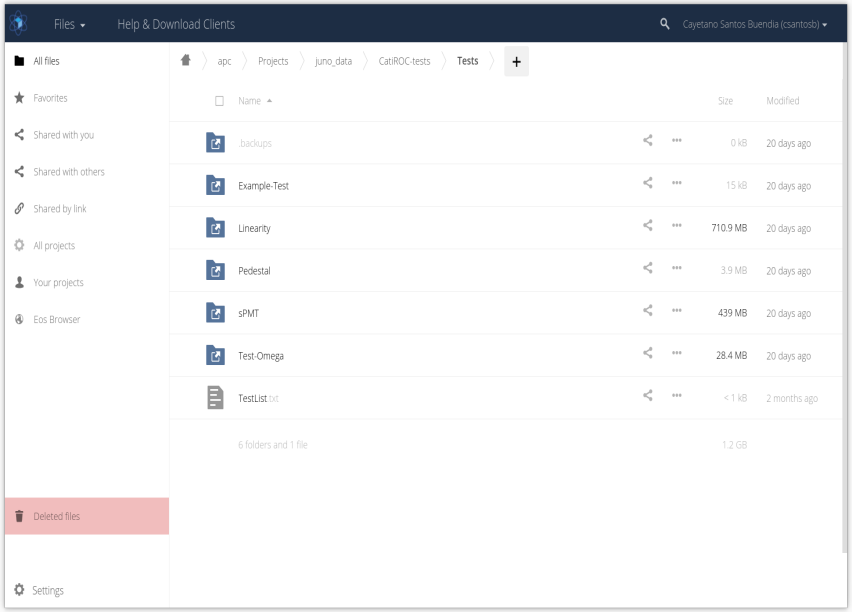
GUI user front end - cli planned

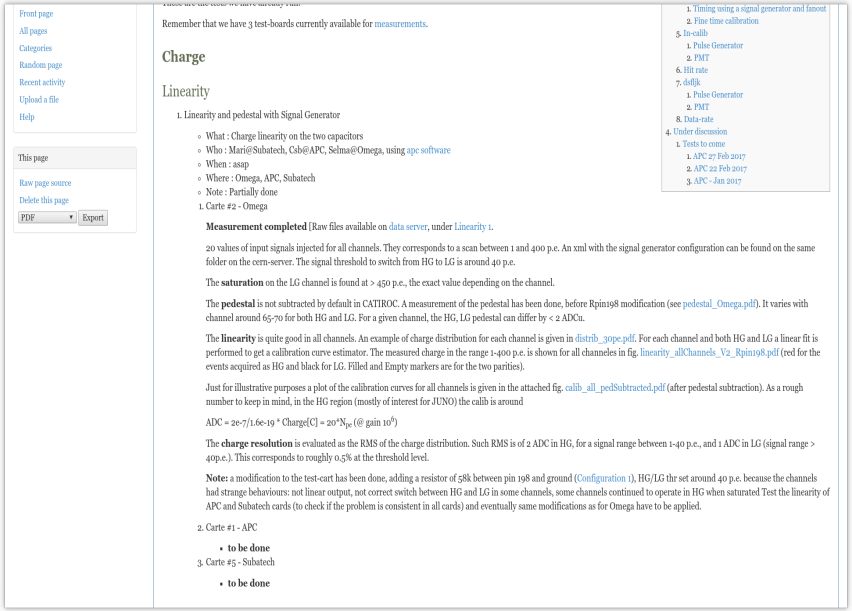
- Low level software in C++
- Gui / data processing in Matlab
- Windows / Linux
- Amplitude histogramming
- Timing histogramming
- Row data recording for offline analysis
- Fitting, etc.
- Extra embedded features
  - event count tagging
  - data rate monitoring
  - dead time monitoring
  - TOT measurement



CatiROC Qualification - Methodology

All data tests documented in shared spaces for traceability





- data saved online for reference
- shared data repository @ CERN
- read / write available to group

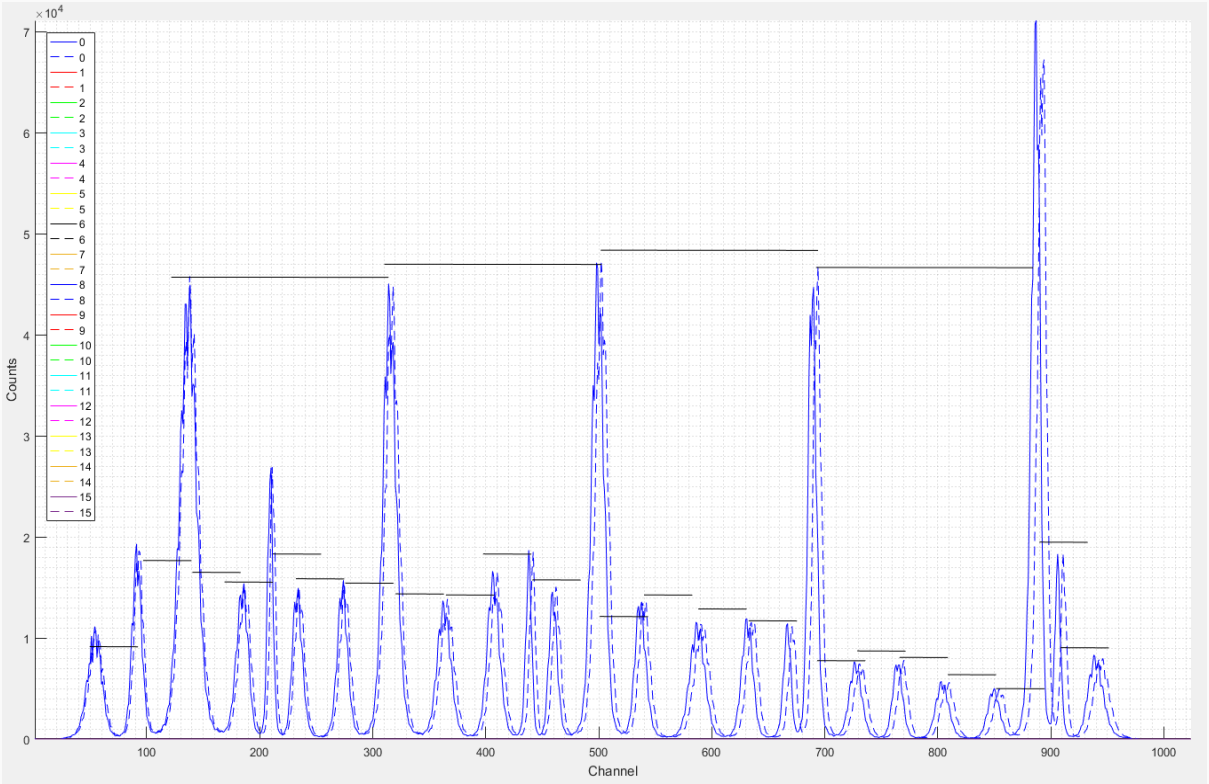
- sharing results and conclusions
- online wiki git repository
- data in tests explained

ASIC Validation

CatiROC Validation - Timing linearity

Fine time Integral non Linearity measurements

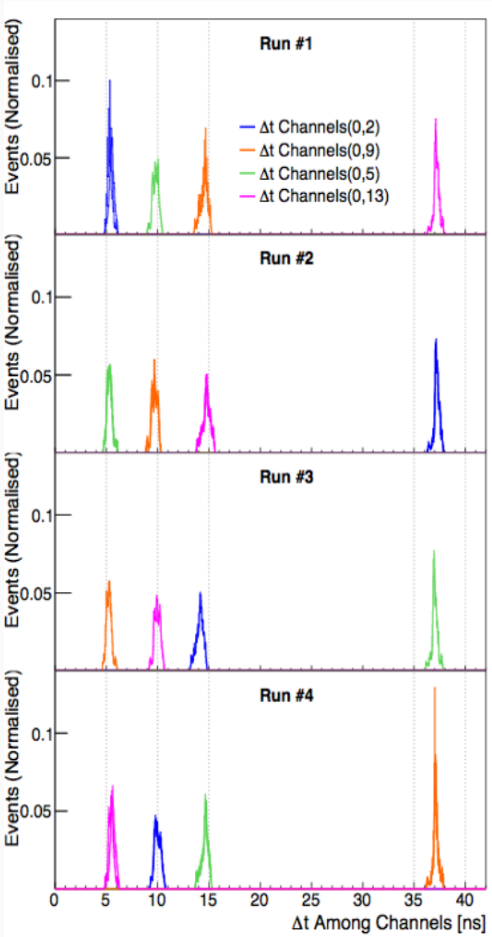
Systematic scan of the 25 ns. coarse time window



- Arbitrary signal generator
- In sync (10 MHz) with acquisition
- 1 ns. steps
- 25 ns. window / 10 bits / 1024 channels
- 98 ps. programmable digital delay line
- Configurable to perform systematic scans

CatiROC Validation - Timing ...

Validation of features for experiment requirements



For each event, compute Δt between two channels experiencing different delays

Δt mean value is set by cable length
Δt RMS is an estimate of time resolution

Time difference between channels is:
- ✓ insensitive to pulse generator jitter
- ✓ insensitive to systematics common to all channels (intra-channel correlation) ✗

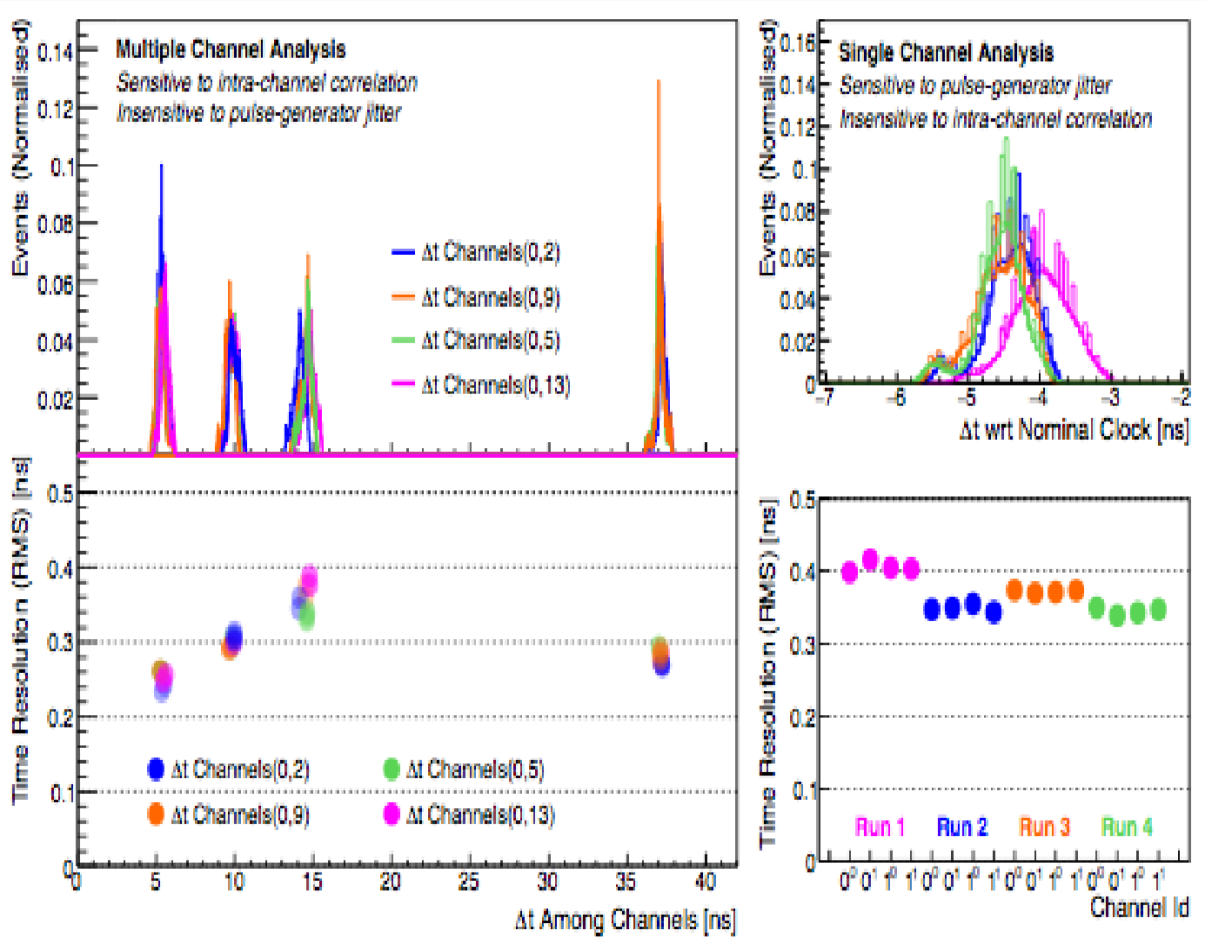
Assuming no correlation:
σ_T(single channel) = RMS /√2

Conservative estimation:
σ_T(single channel) ~ RMS

- Single rate digital pulse generator
- Signal is splitted to 4 channels
- Different cable lengths are used
- Raw data saving
- Computing time differences
- Cables are rotated: four data sets

CatiROC Validation - ... less than ~250 ps

Well below what is necessary

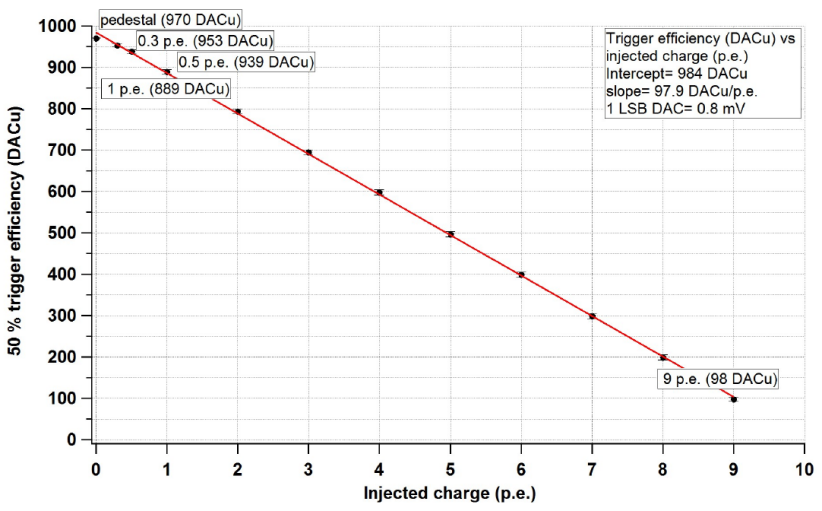


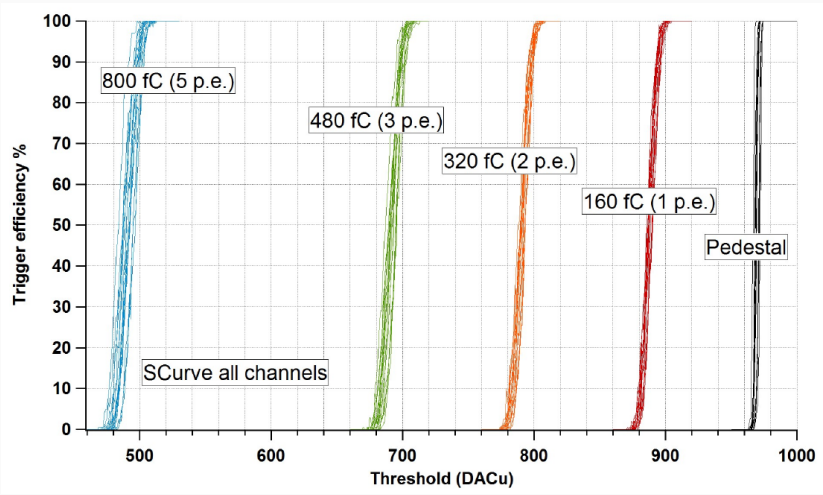
- Coherent between data sets
- Timing independent of channel
- Independent of capacitor in ch.
- Method takes into account all non linearities
- Single ch. timing worst due to p.g. jitter
- Less than ~400 ps ch. to ch.

CatiROC Validation - Trigger efficiency

Signal between 0 - 9 p.e.

DAC scan -> monitor discriminator output



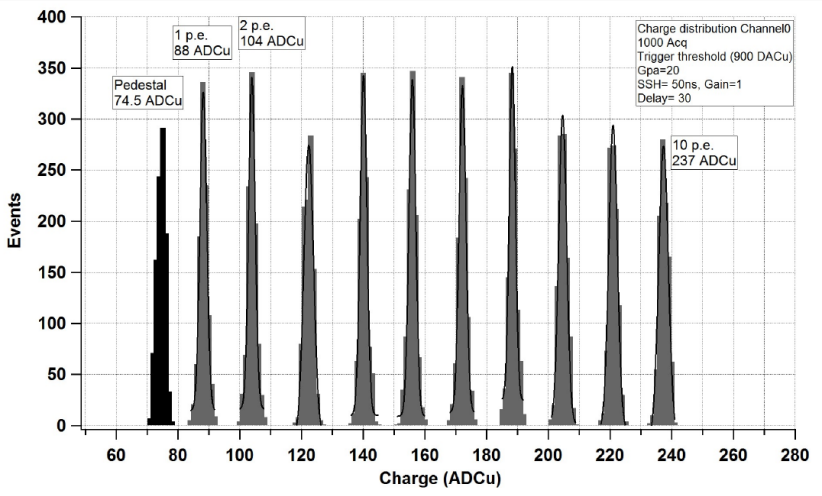


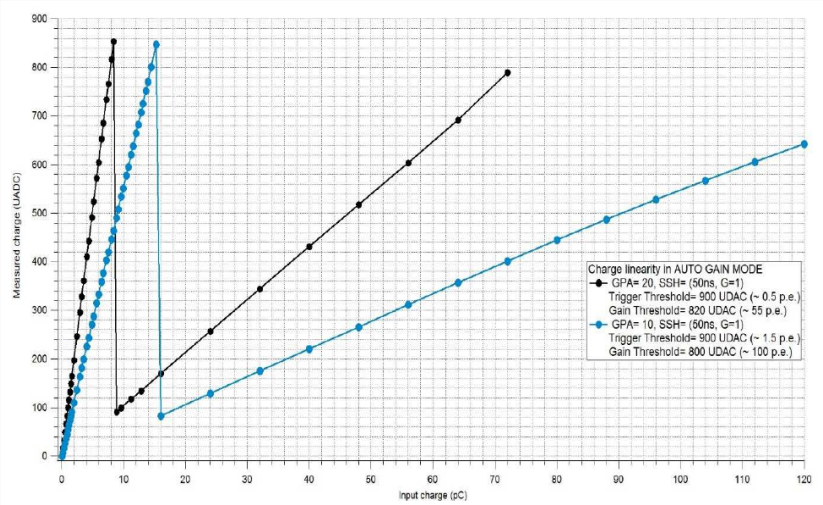
- 50% trigger efficiency
- Sensitivity of 100 DACu per p.e.
- Linearity better than 1% up to 9 p.e.
- Noise measurement 5 DACu

- Data show from all 16 channels
- Input charge from 1 to 5 p.e.
- Channel dispersion < 5 DACu
- 4 mV noise level

CatiROC Validation - Charge linearity

From 160 fC to 1.6 pC with 50 ns. shaping time





- Charge distribution from 1 to 10 p.e.
- Sensitivity 16 ADCu per p.e.
- RMS 1.2 ADCu (0.07 p.e.)
- Full chain SNR 13

- Two scales: low and high gain
- Charge discriminator 820 DACu ~ 1.8 V.
- HG LSB 0.0625 p.e. / LG LSB 0.5 p.e.
- Automatic range switch

Mezzanine production and testing

PCB fabrication and cabling

Produced by a well known, proven and experienced pcb expert company

- Industrial manufacture with high quality standards
- In depth fail testing
- Only COTS proven parts + in-lab tested CatiROC
- Mounting of components and optical checkout
- 10 layers board verification and qualification

Fully tested hardware product

PCB Systematic testing

Electrical and features testing

- On socket ASIC testing before mounting for reliability
- On pcb ASIC testing after mounting for performances
- In laboratory automated test bench for checkout scan
- Verification of noise level, bandwidth, temperature drift, etc.
- Validation of full setup under experiment conditions

Fully tested hardware/software product

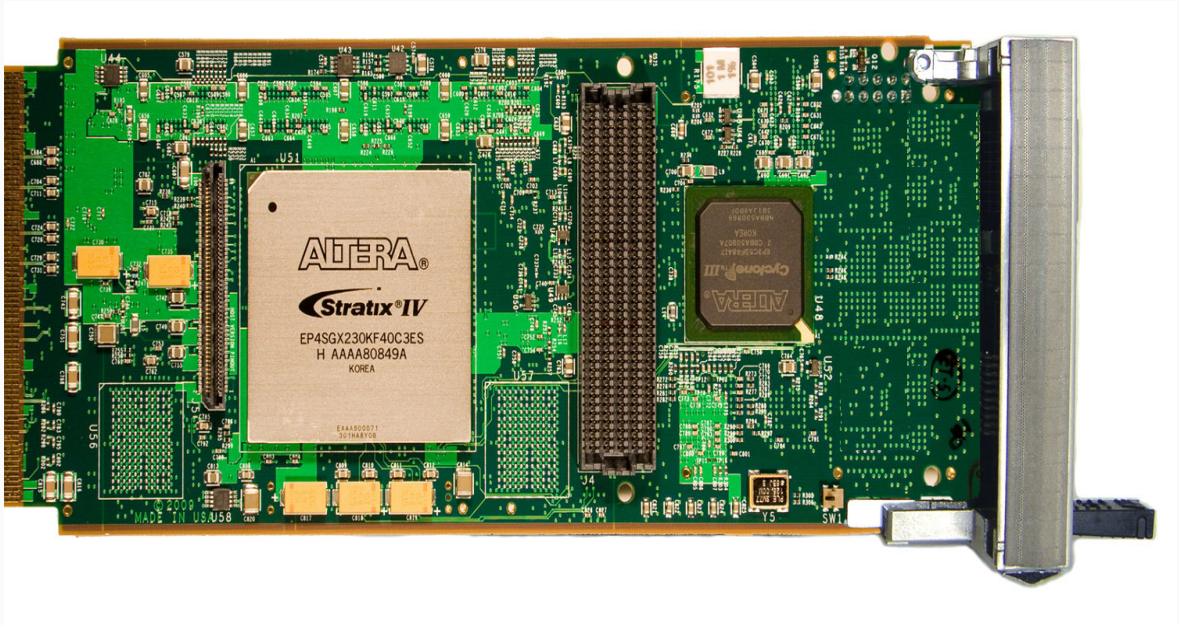
uTCA Support

Prototyping crate - Native C1

- Low cost, 1u 19’ rack-mounted MTCA Chassis
- 1 MCH - 6 AdvancedMC (AMC) - 1 Power module (PM) slots
- Maximum 80W per AMC slot

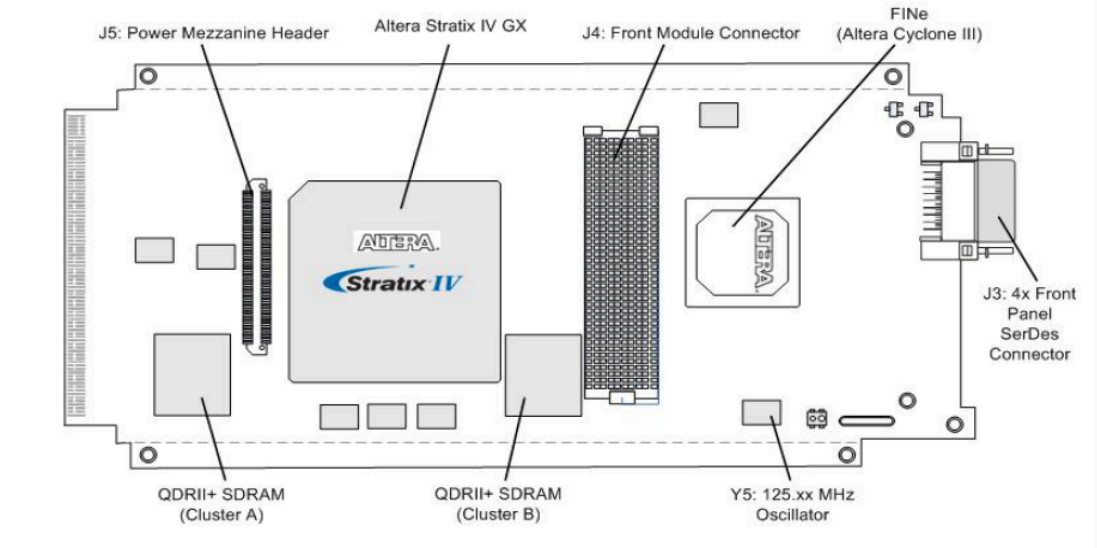
- 1 GbE routed to AMC Port 0 - kTCLKA, TCLKB, and FCLKA to each AMC
- Point-t-point SATA/SAS Port 2 & 3 - Fabrics D, E, F, G Port 4-7

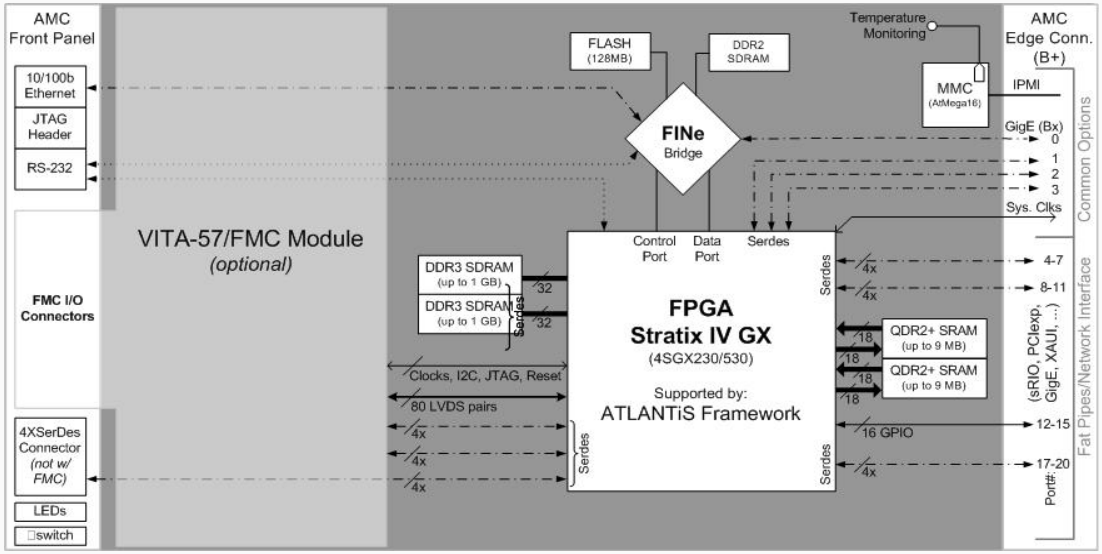
COTS mother board - S4 AMC



- Well established vendor - Bittware
- Commercial, well tested robust solution
- High performance computing platform
- COTS: Reduced risk of failure
- Robust form factor
- Stable operating temperature
- Strong power supply stability

COTS mother board - S4 AMC - Block Diagram



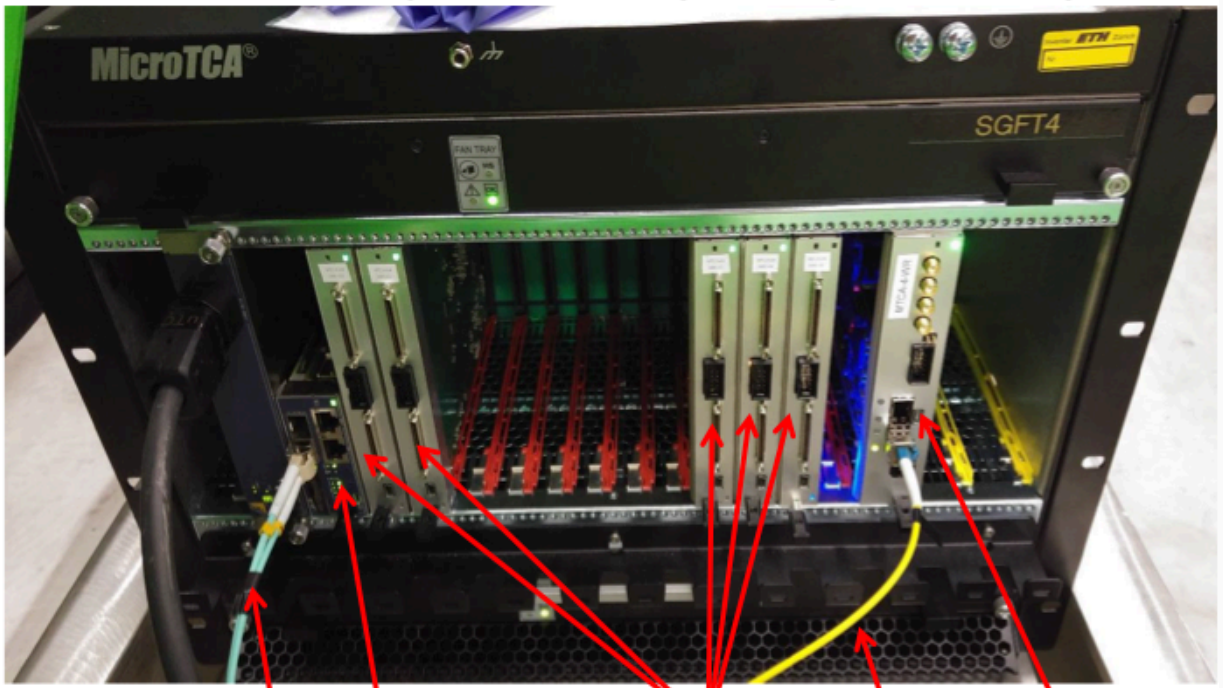


- Altera Stratix IV GX FPGA
- l BittWare's FINe™ Host/Control Bridge
- 10/100/1000 Ethernet, SerDes, LVDS, RS-232, and JTAG
- 2 GBytes of memory
- Fully connected to AMC (16 ports SerDes, 4 ports GPIO)
- l VITA 57 FMC site for I/O expansion
- l Six clocks

Production crate

To be used during the experiment

How a crates was looking like before VHDCI signals cabling to the warm flange



- 12 double width slots
- 2 MCH slots
- Dedicated hardware for synchronizing
- Developed by / image from IPNL

Summary

Collaboration

APC Paris - apc.univ-paris7.fr

- Alexis Noury <anoury.univ-paris7.fr>
- Cayetano Santos <cayetano.santos@apc.univ-paris7.fr>

LAPP Annecy - lapp.in2p3.fr

- Cyril Drancourt <cyril.drancourt@lapp.in2p3.fr>
- Alexandre Dalmaz <dalmaz@lapp.in2p3.fr>

Omega Palaiseau - omega.in2p3.fr

- Selma Conforti <conforti@omega.in2p3.fr>

Conclusions

- Work in progress ...
- Shared effort between projects and laboratories
- Test bench operational -> done
- ASIC fully characterized: good performances -> done [1]
- ASIC test results published
  - *Performance of CATIROC: ASIC for smart readout of large photomultiplier arrays*, S. Conforti at all, Topical Workshop on Electronics for Particle Physics (TWEPP2016) [2]
- Board production during May
- Board testing during June

[1] datasheet available at omega.in2p3.fr

[2] `http://dx.doi.org/10.1088/1748-0221/12/03/C03041`.