

# MSU Electronics for LArIAT

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# LArTPC electronics at MSU

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Excellent Electronics Engineering at MSU – improving signal/noise at each stage below

## Dan Edmunds

- Bo – Warm amplifiers 3planes, 96 channels – tracks immediately (wire to disk)
- Bo – Warm amplifiers 3planes, 144 channels – new feedthru, bias C/R in LAr
- ArgoNeuT – Warm amplifiers, grid + 2 planes, 480 channels – bias C/R in LAr
- Bo – COLD CMOS Hybrid amplifiers 3planes, 144 channels, Warm Receiver/Driver  
Next step would be ASIC ...

## Dan Edmunds & Dean Shooltz

LAPD – Reconfigured COLD CMOS (LongBo 2m drift) + 1 prototype 16 ch. BNL ASIC

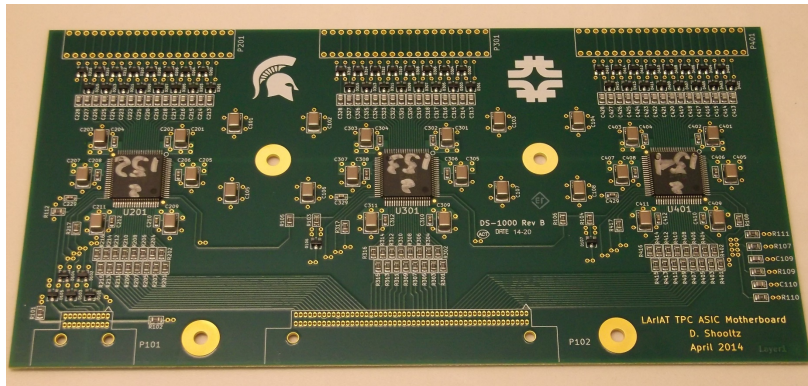
## Dean Shooltz

- LArIAT (ArgoNeuT TPC) Not feasible to reuse ArgoNeuT electronics (but cables OK)
- FNAL Neutrino Dept. arranged BNL FE ASIC (50 uBoone spares) for us
  - 10 Cold Mother Boards (CMB), 3 ASICs/CMB, circuit layout similar to uBoone
  - New feedthru – ASIC digital cont. + power + test pulse, ASIC analog out
  - New Warm Receiver Driver card + Digital control + test pulse driver
  - CAEN ADC – single ended input – D2S (differential to single ended) cards/crate
  - Runs 1 & 2, now Run 3 in progress, all 480 ch. electronics operational

# LArIAT Electronics

## Cold Motherboard (48 ch)

PC board connectors to wire planes



Power/Control\*

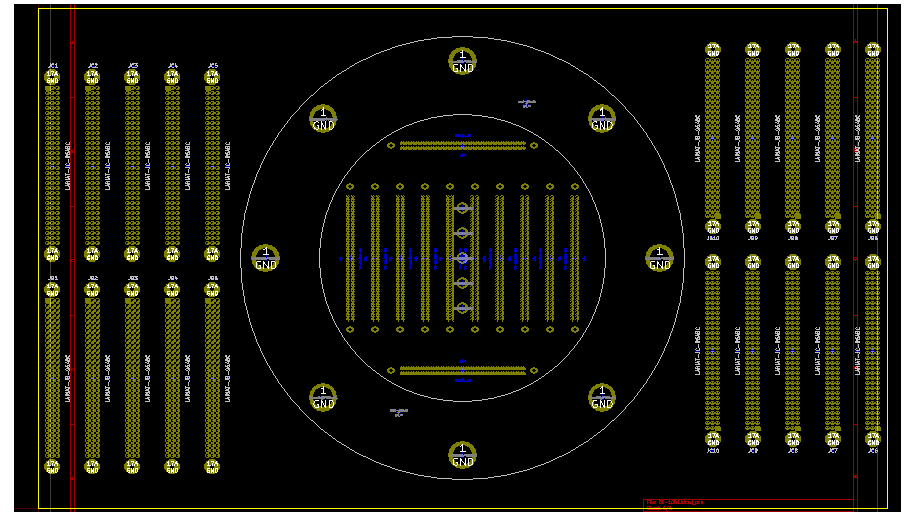
Analog Out



Digital/Test

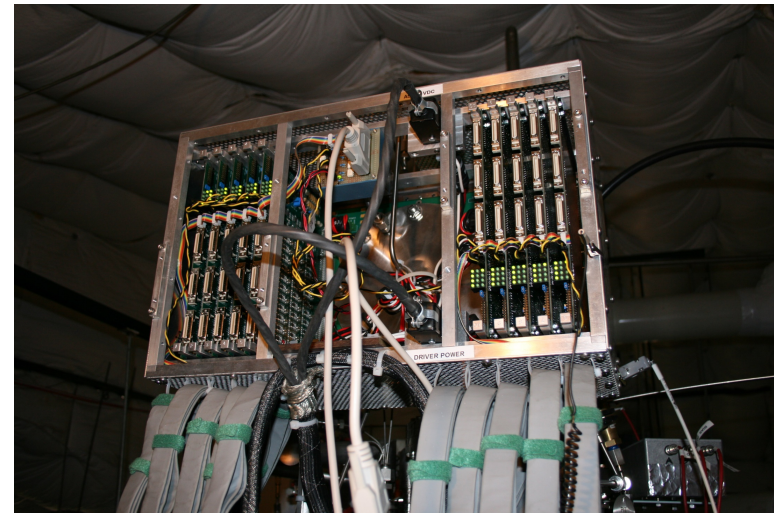
Feedthru

Digital/Test



Analog

Analog



# Performance & Issues

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## Run I

Light System – coherent noise leaks – Shielding improved (got it <10% of stochastic noise)  
WRD – cable driver chip (uBoone) w/low-pass filter had MHz oscillations, remove C  
Grid Plane – Induction plane shadows. No Q-capacitor (ArgoNeuT missed it – Why? S/N !)  
PMTs – neg. HV on photocathode near collection plane wires, so major signal distortions  
ASIC serial data corruption – lowered impedance & reload each spill, acoustic wire motion

## Run II

**Most REPAIRED (or mitigated) by Run II**

Beam Track Signal (~100 ADC counts = 50 mV) Very Low Noise (~1.4 counts = 0.7 mV)

Convert noise to electrons:

ASIC buffers off, we find 25mV/fC, 2us filter setting, yields 18 mV/fC

ASIC output -> CAEN ADC input = 0.91 (18mV/fC) = 16.4 mV/fC @ CAEN

0.7 mV: ENC = 270 electrons (reasonable for 0.5m wires +board capacitances)

Convert Beam track ionization to electrons: Basics (25 eV/ion, 2.2 MeV/cm, 1.4fC/mm)

Drift field 500V/cm, tracks have 68% free ionization, 0.95fC/mm

Expected Signal = 0.95fC/mm \* 4.6mm = 4.4fC , without attenuation

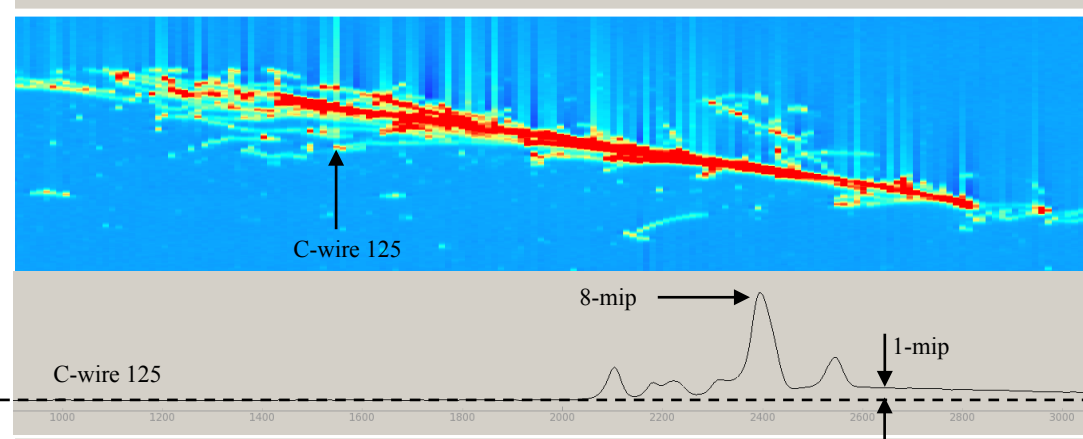
Beam tracks 50mV/16.4 mV/fC = 3fC (**0.5 ms electron lifetime?**)

Run III In progress – 5mm then 3mm pitch should see signal and noise.

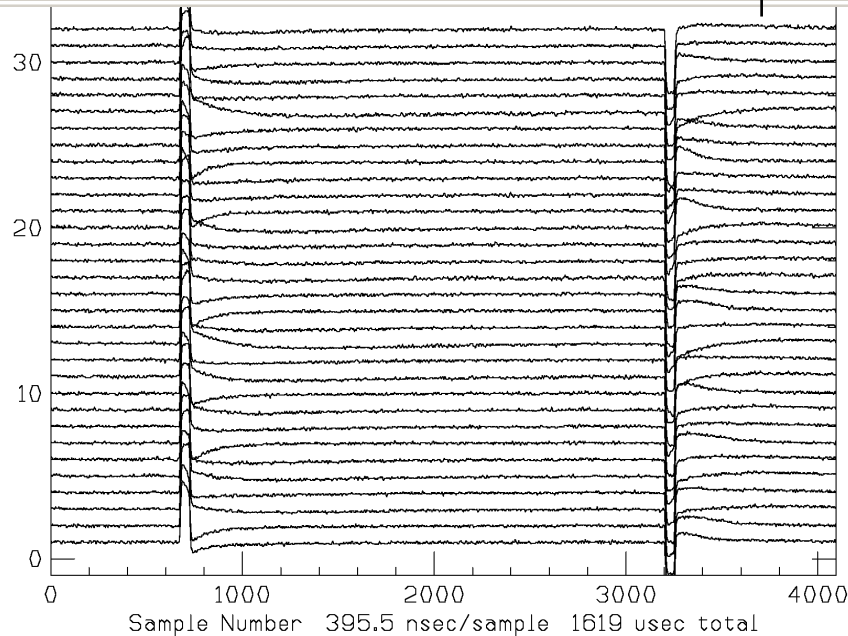
Due to excellent S/N, we found a major problem with **cold** FE ASIC chip.

# FE-ASIC - baseline restoration problem

What are these streaks? Same FE ASIC as uBoone *did not see it initially*, and 35-ton



MSU Bench tests **cold**  
Baseline problem has  
both signs and  
differs chip to chip!



BNL tracked this down  
and reports that  
increased transistor  
size in the ASIC pole-  
zero circuitry, has  
considerably reduced  
this baseline effect.

# MSU enabling cold ASIC/FEMB testing (DUNE/SBN)

## Cold Testing of 4 ASIC chips and/or full FEMBs

Avoid condensation at all costs (air carries dirt & contaminants).

Seal and purge with GN2

Slow (but not too slow) cool down to 77K to avoid thermal shock

Immerse in LN2 for full functionality testing

Remove from LN2 and slow (but not too slow) warm up while purging with GN2

### Dean Shooltz Implementation

MSU providing 2 (perhaps 4) stations to BNL this month for such testing.

- 1) LN2 Dewar (below) filled once per day ~ 1 liter/cycle .
- 2) Electronics package lowered into slot and sealed in Cryostat
- 3) Purge cryostat with Dewar boil-off, with heaters & fans
- 4) Boil off valve closed, Dewar heated & LN2 rises into cryostat
- 5) Valve maintains LN2 below electronics while fans cool it
- 6) LN2 level raised to cover electronics – cold testing now
- 7) Valve opens allowing LN2 to drain back to Dewar
- 8) Heaters and Fans raise temperature while GN2 purging

Cycle takes ~15 minutes.    up to 16ASIC/hour/station  
up to 4 FEMB/hour/station

Want one?

